Single, Double or Triple-Output Hot Plug Controller

The HIP1020 applies a linear voltage ramp to the gates of any combination of 3.3V, 5V, and 12V MOSFETs. The internal charge pump doubles a 12V bias or triples a 5V bias to deliver the high-side drive capability required when using more cost-effective N-Channel MOSFETs. The 5V/ms ramp rate is controlled internally and is the proper value to turn on most devices within the Device-Bay-specified di/dt limit. If a slower rate is required, the internally-determined ramp rate can be over ridden using an optional external capacitor.

When VCC = 12V, the charge pump ramps the voltage on HGATE from zero to 22V in about 4ms. This allows either a standard or a logic-level MOSFET to become fully enhanced when used as a high-side switch for 12V power control. The voltage on LGATE ramps from zero to 16V allowing the simultaneous control of 3.3V and/or 5V MOSFETs.

When VCC = 5V, the charge pump enters voltage-tripler mode. The voltage on HGATE ramps from zero to 12.5V in about 3ms while LGATE ramps to 12.0V. This mode is ideal for control of high-side MOSFET switches used in 3.3V and 5V power switching when 12V bias is not available.

Ordering Information

PART NUMBER	TEMP. RANGE (^{O}C)	PACKAGE	PKG. DWG. #
HIP1020CK-T	0 to 70	5 Ld SOT23 T + R	P5.064
HIP1020CKZ-T (See Note)	0 to 70	5 Ld SOT23 T + R (Pb-free)	P5.064

NOTE: Intersil Pb-free products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which is compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J Std-020B.

Typical Applications

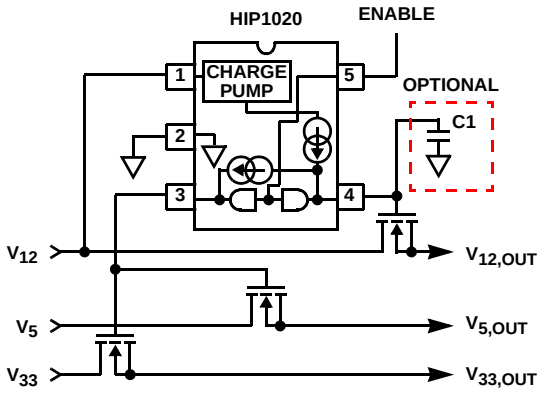


FIGURE 1A. DEVICE-BAY HOT PLUG CONTROLLER WITH VCC = 12V

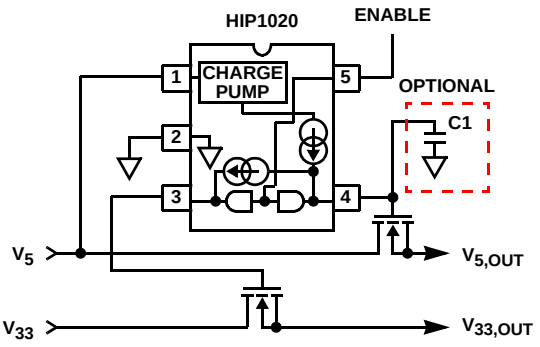


FIGURE 1B. DEVICE-BAY HOT PLUG CONTROLLER WITH VCC = 5V

Features

- Rise Time Controlled to Device-Bay Specifications
- No Additional Components Required
- Internal Charge Pump Drives N-Channel MOSFETs
- Drives any Combination of One, Two or Three Outputs
- Internally-Controlled Turn-On Ramp
  - Optional Capacitor Selects Slower Rates
- Prevents False Turn on During Hot Insertion
- Operates using 12V or 5V Bias
- Improves Device Bay Peripheral Size Cost and Complexity
  - Minimal Component Count
  - Tiny 5-Pin SOT23 Package
- Controls Standard and Logic-Level MOSFETs
- Compatible with TTL and 3.3V Logic Devices
- Shutdown Current . . . . . < 1µA
- Operating Current . . . . . .< 3mA

Applications

- Device Bay Peripherals
- Hot Plug Control
- Power Distribution Control

Pinout

HIP1020 (SOT23)
TOP VIEW



CAUTION: These devices are sensitive to electrostatic discharge; follow proper IC Handling Procedures.
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Pin Descriptions

PIN	SYMBOL	FUNCTION	DESCRIPTION
1	VCC	Bias Supply	Connect this pin to either a 12V or a 5V source. The HIP1020 detects the bias-voltage level at pin 1 and decides whether to operate as a voltage-doubler or a voltage-tripler. Consequently, it is not recommended to operate with bias voltages between 5V (±10%) and 12V (±10%). In the absence of an enable signal at pin 5, the current into pin 1 is less than 1µA. It is necessary for voltage to be present at pin 1 prior to applying an enable signal at pin 5.
2	GND	Ground	Connect to the negative rail of the supply that is connected to pin 1.
3	LGATE	Gate Driver for the 5V and/or 3.3V MOSFET(s)	When VCC = 12V, connect this pin to the gate(s) of the 5V and/or 3.3V MOSFETs. When VCC = 5V, connect this pin to the gate of a 3.3V MOSFET. Upon a rising edge on EN (pin 5), the voltage on this pin will ramp linearly to ~16V when VCC = 12V and ~12V when VCC = 5V. An internal dv/dt activated clamp shunts coupled noise to ground preventing unintended turn on at either output. The internal dv/dt-activated clamp also protects pin 5.
4	HGATE	12V or 5V MOSFET Gate Driver	When VCC = 12V, connect this pin to the gate of the 12V MOSFET. When VCC = 5V, connect this pin to the gate of the 5V MOSFET. Upon a rising edge on EN (pin 5), the voltage on this pin will ramp linearly to ~22V when VCC = 12V and ~13V when VCC = 5V.
5	EN	Enable	Connect a TTL or 3.3V logic signal to this pin to control the outputs at pins 3 and 4. A rising edge on pin 5 initiates the linear voltage ramps at pins 3 and 4. Be sure that the device driving EN does not enter a high-impedance state when enabling is not desired and that it's maximum rise time does not exceed 100µs.

Absolute Maximum Ratings

Supply Voltage, VCC 14.5V
HGATE Current 10mA
LGATE Current. 10mA
EN Voltage 7.0V

Operating Conditions

Supply Voltage, VCC . . . . . 5V ±10% or 12V ±10%
Temperature Range . . . . . 0^oC to 70^oC

Thermal Information

Thermal Resistance (Typical, Note 1) θ_{JA} ($^oC/W$)
SOT23/5L Package 240
Maximum Junction Temperature . . . . . 150^oC
Maximum Storage Temperature Range. . . . . -65^oC to 150^oC
Maximum Lead Temperature (Soldering 10s) . . . . . 300^oC

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
VCC SUPPLY CURRENT						
Operating Supply	$I_{CC,12}$	V_{EN} = 5V,V_{CC} = 12V	-	1.6	2.3	mA
Operating Supply	$I_{CC,5}$	V_{EN} = 5V, V_{CC} = 5V	-	0.77	1.1	mA
Shutdown Supply	I_{SHDN}	V_{EN} = 0V	-	-	1	µA
GATE CONTROL OUTPUTS						
HGATE dv/dt (No External Capacitor)	dv/dt	V_{CC} = 12V	2.5	5	8.5	V/ms
		V_{CC} = 5V	2.4	5	7.2	V/ms
LGATE dv/dt (No External Capacitor)	dv/dt	V_{CC} = 12V	2.5	5	8.5	V/ms
		V_{CC} = 5V	2.6	5	7.4	V/ms
HGATE Pull-Up Current	I_{HGATE}	V_{CC} = 12V, V_{HGATE} = 19V	7.6	13.4	18.5	µA
		V_{CC} = 5V, V_{HGATE} = 9.5V	7.6	12.3	18.5	µA
HGATE Output Voltage	V_{HGATE}	V_{CC} = 12V	20.7	21.8	22.8	V
		V_{CC} = 5V	11.6	12.5	13.4	V
LGATE Output Voltage	V_{LGATE}	V_{CC} = 12V	15.2	16.3	18.3	V
		V_{CC} = 5V	10.6	11.7	12.9	V
ENABLE						
Input Threshold Voltage	V_{EN}	V_{CC} = 12V	1	-	2.4	V
Enable Current	I_{EN}	V_{EN} = 5V	-	-	1	µA

Typical Performance Curves

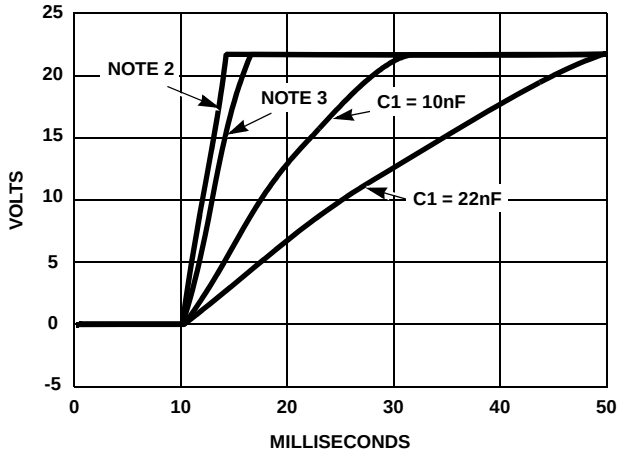


FIGURE 2. HGATE (PIN 4) TURNING ON WITH VCC = 12V

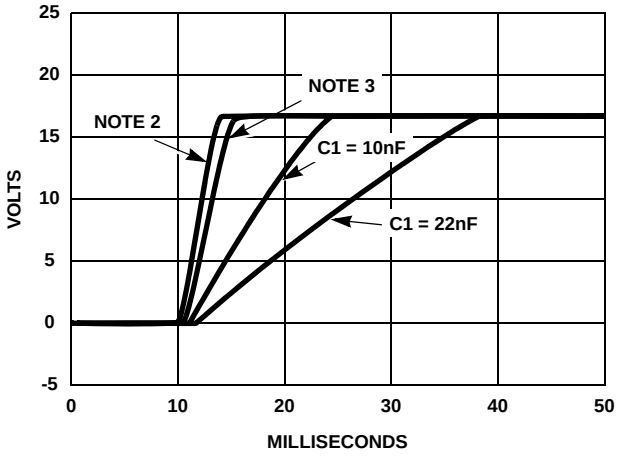


FIGURE 3. LGATE (PIN 3) TURNING ON WITH VCC = 12V

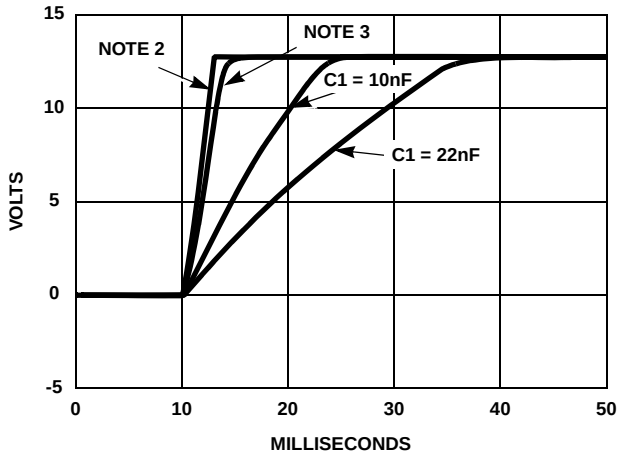


FIGURE 4. HGATE (PIN 4) TURNING ON WITH VCC = 5V

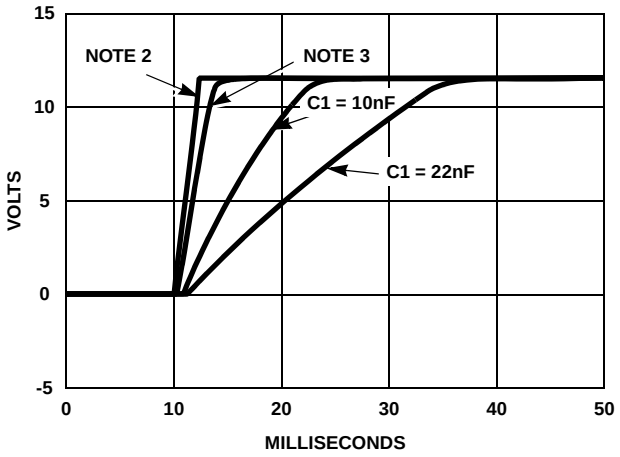


FIGURE 5. LGATE (PIN 3)TURNING ON WITH VCC = 5V

NOTES: Device is enabled at 10 milliseconds.

2. Pins 3 and 4 are unconnected.
3. Pins 3 and 4 are connected to the gates of “typical” high-performance N-Channel MOSFETs.

Application Information

The HIP1020 was designed specifically to address the requirements of Device Bay peripherals. The small package, low cost and integrated features make it the ideal component for high-side power control of all three Device-Bay rail voltages without using any additional components except for the switching MOSFETs themselves. The integrated charge pump supplies sufficient voltage to fully enhance the lower-cost N-Channel power MOSFETs, and the internally-controlled turn-on ramp provides soft switching for all types of loads.

Although the HIP1020 was developed with Device Bay in mind, it has the versatility to perform in any situation where low-cost load switching is required.

MOSFET Selection for Device Bay Peripherals

When selecting power MOSFETs for Device Bay (or any similar application), two major concerns are the voltage drop across the MOSFET and the thermal requirements imposed by the particular application. Voltage drop across the MOSFET is controlled by its on-state resistance, $r_{DS(ON)}$, and the peak current through the device, while the thermal requirements are determined by several factors including ambient temperature, amount of air flow if any, area of the copper mounting pad, the thermal characteristics of the MOSFET and its package, and the average current through the MOSFET.

TABLE 1. DEVICE-BAY MOSFET SELECTION GUIDE FOR PERIPHERAL-POWER CONTROL

INTERSIL PART NO.	MOUNTING-PAD AREA (IN^2)	PACKAGE		$r_{DS(ON)}$ (mΩ)	BUS (VOLTAGE)	MAXIMUM AVERAGE CURRENT	MAXIMUM PEAK CURRENT
HUF76105DK8	0.05	SO-8	Dual	63	12	≤3A (Note 4)	≤7A (Note 5)
				51	5	≤1A	≤2A
				48	3.3	≤1A	≤1.25A
HUF76113DK8	0.05	SO-8	Dual	43	12	≤3A (Note 4)	≤11A (Note 5)
or				40	5	≤2A	≤2.5A
HUF76113T3ST	0.08	SOT223	Single	37	3.3	≤1.5A	≤1.5A
HUF76131SK8	0.05	SO-8	Single	17	12	≤6A (Note 4)	≤25A (Note 5)
				16	5	≤5A (Note 4)	≤6A (Note 5)
				15	3.3	≤4A	≤4A
HUF76143S3S	0.31	TO-263	Single	7	3.3	≤9A (Note 4)	≤9A (Note 5)

NOTES:

4. Maximum-Average-Current level meets or exceeds the Device-Bay specified level for a 30s “peak”.
5. Maximum-Peak-Current level meets or exceeds the Device-Bay specified level for a 100μs “transient”.

The MOSFETs in Table 1 were selected based on the assumption that at most 2% the of the 5V or 3.3V-bus voltage could appear across the 5V or 3.3V MOSFET, and that at most 4% of the 12V-bus voltage could appear across the 12V MOSFET. The worst-case voltage drop occurs during a 100μs current transient given in the Maximum-Peak-Current column. Longer transients may not be tolerable by the MOSFET depending on its junction temperature prior to the transient.

In most cases, the given Mounting-Pad Area is required to achieve the Maximum-Average-Current rating. It assumes 1-oz. copper, zero air flow, and an ambient temperature not exceeding 50^oC. The Mounting-Pad Area is the approximate area of a rectangle encompassing the MOSFET package and its leads. The $r_{DS(ON)}$ numbers assume the device has reached thermal equillibrium at the Maximum-Average-Current. In some cases, the thermal capabilities as well as $r_{DS(ON)}$ can be improved by using larger pads, heavier copper, air flow, or lower ambient temperature.

Protection from Unwanted Turn On

A dv/dt-activated clamp circuit is internally connected to LGATE (pin 4), and is active when the chip is not powered. It is activated when the voltage on either LGATE or HGATE rises too quickly, and it immediately provides a low-impedance ground path for current from either gate pin.

The purpose of the dv/dt-activated clamp circuit is to prevent unwanted turn on of the power MOSFETs during a hot insertion event. When a Device-Bay peripheral is inserted into the bay, the power pins on the peripheral are brought into contact with the already-energized mating contacts in the bay. This results in a very fast-rising voltage edge on the drains of the power MOSFETs which can inject current through the gate-to-drain capacitance and briefly turn on the power MOSFET. The result is a momentary dip in the rail voltage which can effect the device’s operation as well as the operation of any other device already connected and potentially the host system itself. Without the dv/dt-activated clamp, a decoupling capacitor would be needed between each power MOSFET drain and ground using up valuable board space and adding unnecessary cost. The HIP1020 solves this problem by providing a path for capacitively-coupled current to reach ground.

Increasing the Rise Time

The HIP1020 has an internal-ramping charge pump that increases the voltage to the power MOSFETs in a predictable controlled manner allowing soft turn on of most types of loads. It is possible that some types of load would require slower turn on. This could arise when a load has a large capacitive component or for some other reason requires an extraordinarily high starting current. Without the external capacitor, C1 (see Figure 1), the ramp rate is about 5V/ms. A capacitor between HGATE and ground will slow the rise time of both gate voltages to a rate given by

$$C1 = \frac{I_{HGATE}}{\left(\frac{dv}{dt}\right)} \quad \text{(EQ.1)}$$

In Equation 1, C1 is the value of capacitor in Farads required to achieve a rise rate of dv/dt in V/s, and I_{HGATE} is current output of pin 4 given in Amperes as shown in the “Electrical Specifications” section of this data sheet. Figures 2 through 5 show gate voltage waveforms for selected values of C1.

Special Applications

The HIP1020 is well suited to work with N-Channel MOSFETs controlling voltages other than 12V, 5V, or 3.3V provided three basic constraints are observed. The first constraint is that the bias voltage for the HIP1020 is either 12V or 5V. Chip operation at voltages significantly below 5V is not possible, while a bias voltage very much above 12V can unnecessarily stress the part. Operation between 5V and 12V can “confuse” the chip as it tries to determine whether to operate as a voltage doubler or voltage tripler.

The final two constraints have to do with proper operation of the power MOSFETs. These constraints assume that a rail voltage, V_{RAIL}, is to be switched using an N-Channel power MOSFET having a gate-to-source breakdown voltage of V_{BR} and a threshold voltage of V_{TH}.

$$V_{TH} < V_{GATE} - V_{RAIL} \quad \text{(EQ.2)}$$

$$V_{BR} > V_{GATE} - V_{RAIL} \quad \text{(EQ.3)}$$

V_{GATE} can be either V_{HGATE} or V_{LGATE} depending on which pin is connected to the power MOSFET and will be selected based on which gate voltage is most appropriate for the application. The requirement in Equation 2 is necessary to assure that the power MOSFET is fully enhanced. V_{TH} should be the maximum data-sheet value needed to assure adequately low r_{DSON}. The requirement in Equation 3 assures that the power MOSFET is protected from breakdown of the gate oxide.

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