Integrated Device Technology, Inc.

PARALLEL BIDIRECTIONAL FIFO 512 x 18 & 1024 x 18

IDT72511
IDT72521

FEATURES:

- Two side-by-side FIFO memory arrays for bidirectional data transfers
- 512 x 18-Bit - 512 x 18-Bit (IDT72511)
- 1024 x 18-Bit - 1024 x 18-Bit (IDT72521)
- 18-bit data buses on Port A side and Port B side
- Can be configured for 18-to-18-bit or 36-to-36-bit communication
- Fast 35ns access time
- Fully programmable standard microprocessor interface
- Built-in bypass path for direct data transfer between two ports
- Two fixed flags, Empty and Full, for both the A-to-B and the B-to-A FIFO
- Two programmable flags, Almost-Empty and Almost-Full for each FIFO
- Programmable flag offset can be set to any depth in the FIFO
- Any of the eight flags can be assigned to four external flag pins
- Flexible reread/rewrite capabilities
- Six general-purpose programmable I/O pins
- Standard DMA control pins for data exchange with peripherals
- 68-pin PGA and PLCC packages

DESCRIPTION:

The IDT72511 and IDT72521 are highly integrated first-in, first-out memories that enhance processor-to-processor and processor-to-peripheral communications. IDT BiFIFOs integrate two side-by-side memory arrays for data transfers in two directions.

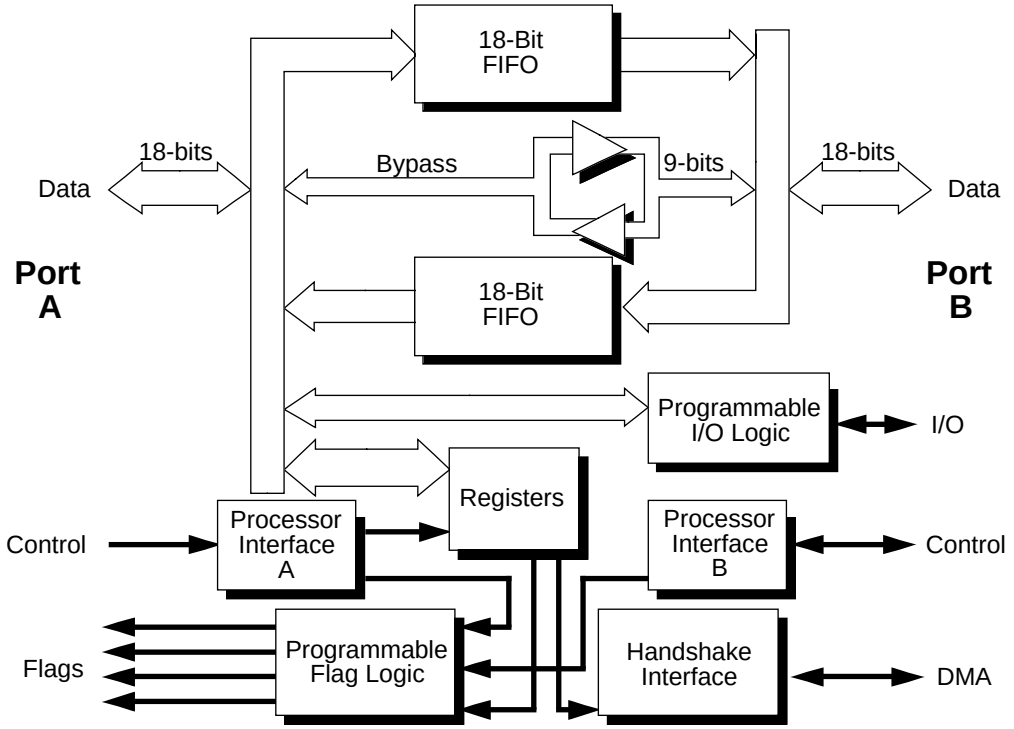
The BiFIFOs have two ports, A and B, that both have standard microprocessor interfaces. All BiFIFO operations are controlled from the 18-bit wide Port A. Port B is also 18 bits wide and can be connected to another processor or a peripheral controller. The BiFIFOs have a 9-bit bypass path that allows the device connected to Port A to pass messages directly to the Port B device.

Ten registers are accessible through Port A, a Command Register, a Status Register, and eight Configuration Registers.

The IDT BiFIFO has programmable flags. Each FIFO memory array has four internal flags, Empty, Almost-Empty, Almost-Full and Full, for a total of eight internal flags. The Almost-Empty and Almost-Full flag offsets can be set to any depth through the Configuration Registers. These eight internal flags can be assigned to any of four external flag pins (FLG_A-FLG_D) through one Configuration Register.

Port B has programmable I/O, reread/rewrite and DMA functions. Six programmable I/O pins are manipulated through

SIMPLIFIED BLOCK DIAGRAM



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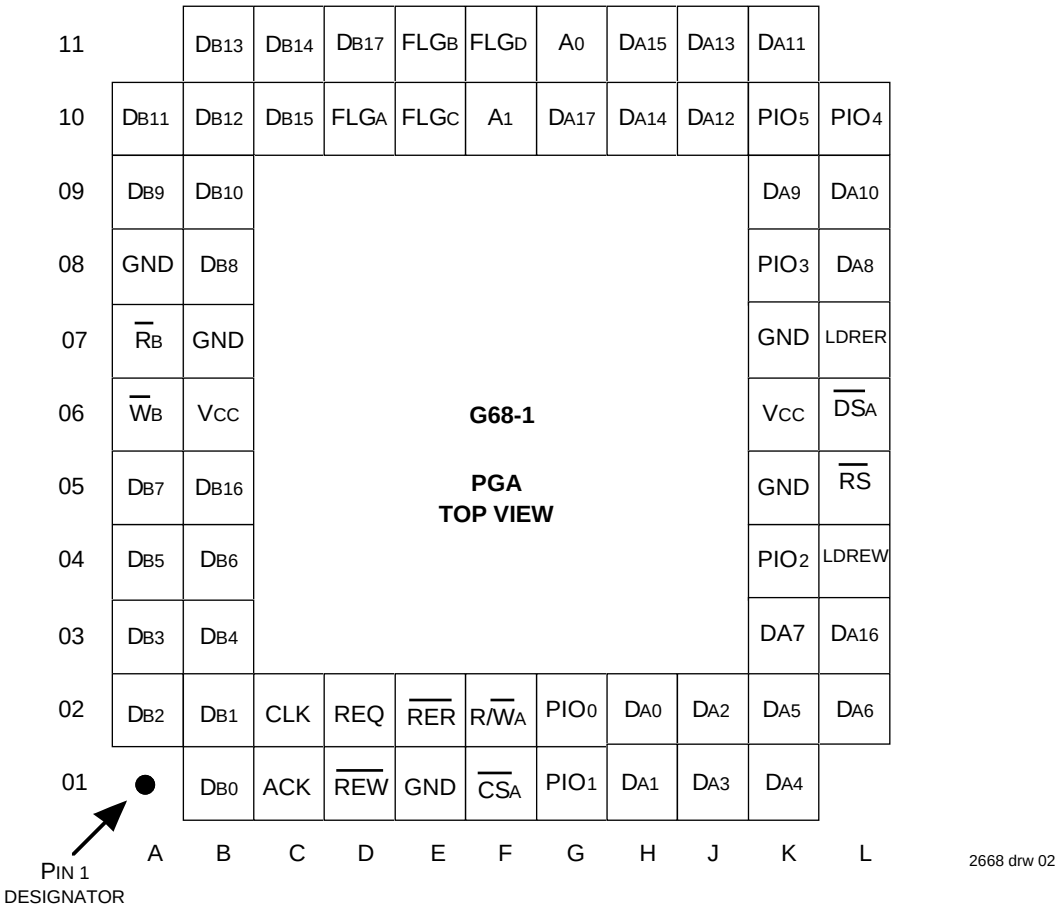
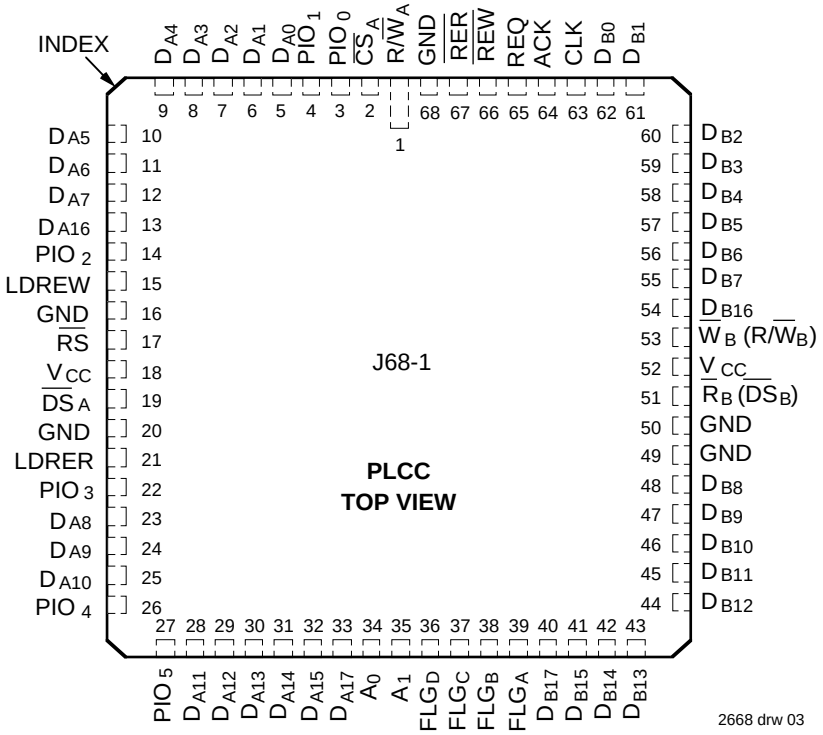
two Configuration Registers. The Reread and Rewrite controls will read or write Port B data blocks multiple times. The BiFIFO has three pins, REQ, ACK and CLK, to control DMA transfers from Port B devices.

PIN CONFIGURATIONS



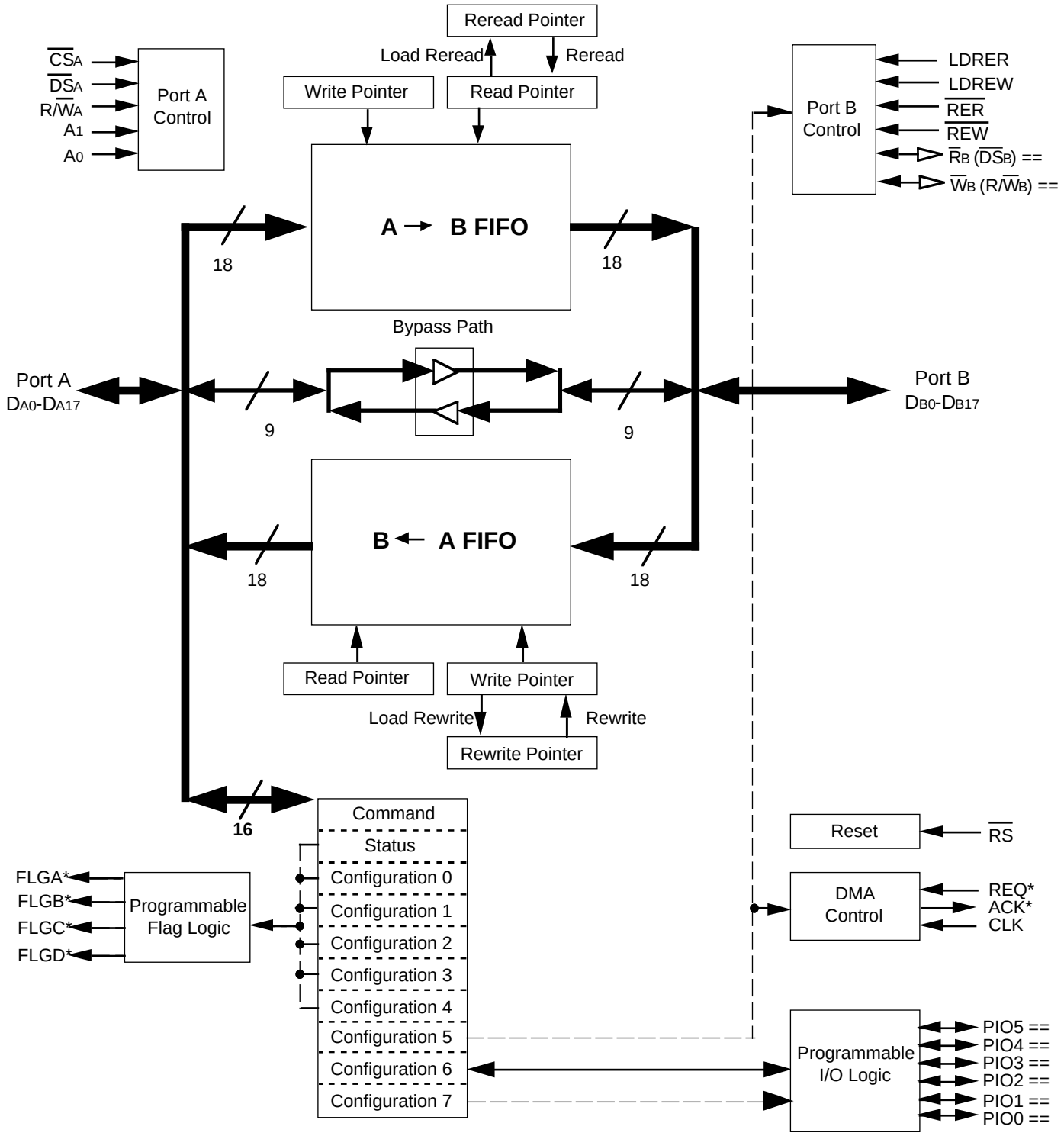


PIN DESCRIPTION

Symbol	Name	I/O	Description
D_{A0}-D_{A17}	Data A	I/O	Data inputs and outputs for the 18-bit Port A bus.
$\overline{CS}_A$	Chip Select A	I	Port A is accessed when Chip Select A is LOW.
$\overline{DS}_A$	Data Strobe A	I	Data is written into Port A on the rising edge of Data Strobe when Chip Select is LOW. Data is read out of Port A on the falling edge of Data Strobe when Chip Select is LOW.
R/$\overline{W}_A$	Read/Write A	I	This pin controls the read or write direction of Port A. When $\overline{CS}_A$ is LOW and R/$\overline{W}_A$ is HIGH, data is read from Port A on the falling edge of $\overline{DS}_A$. When $\overline{CS}_A$ is LOW and R/$\overline{W}_A$ is LOW, data is written into Port A on the rising edge of $\overline{DS}_A$.
A_0, A_1	Addresses	I	When Chip Select A is asserted, A_0, A_1, and Read/Write A are used to select one of six internal resources.
D_{B0}-D_{B17}	Data B	I/O	Data inputs and outputs for the 18-bit Port B bus.
$\overline{R}_B$ ($\overline{DS}_B$)	Read B	I or O	If Port B is programmed to processor mode, this pin functions as an input. If Port B is programmed to peripheral mode this pin functions as an output. This pin can function as part of an Intel-style interface ($\overline{R}_B$) or as part of a Motorola-style interface ($\overline{DS}_B$). As an Intel-style interface, data is read from Port B on a falling edge of $\overline{R}_B$. As a Motorola-style interface, data is read on the falling edge of $\overline{DS}_B$ or written on the rising edge of $\overline{DS}_B$ through Port B. The default is Intel-style processor mode. ($\overline{R}_B$ as an input).
$\overline{W}_B$ (R/$\overline{W}_B$)	Write B	I or O	If Port B is programmed to processor mode, this pin functions as an input. If Port B is programmed to peripheral mode this pin functions as an output. This pin can function as part of an Intel-style interface ($\overline{W}_B$) or as part of a Motorola-style interface (R/$\overline{W}_B$). As an Intel-style interface, data is written to Port B on a rising edge of $\overline{W}_B$. As a Motorola-style interface, data is read (R/$\overline{W}_B$ = HIGH) or written (R/$\overline{W}_B$ = LOW) to Port B in conjunction with a Data Strobe B falling or rising edge. The default is Intel-style processor mode ($\overline{W}_B$ as an input.)
$\overline{RER}$	Reread	I	Loads A→B FIFO Read Pointer with the value of the Reread Pointer when LOW.
$\overline{REW}$	Rewrite	I	Loads B→A FIFO Write Pointer with the value of the Rewrite Pointer when LOW.
LDRER	Load Reread	I	Loads the Reread Pointer with the value of the A→B FIFO Read Pointer when HIGH.
LDREW	Load Rewrite	I	Loads the Rewrite Pointer with the value of the B→A FIFO Write Pointer when HIGH.
REQ	Request	I	When Port B is programmed in peripheral mode, asserting this pin begins a data transfer. Request can be programmed either active HIGH or active LOW.
ACK	Acknowledge	O	When Port B is programmed in peripheral mode, Acknowledge is asserted in response to a Request signal. This confirms that a data transfer may begin. Acknowledge can be programmed either active HIGH or active LOW.
CLK	Clock	I	This pin is used to generate timing for ACK, $\overline{R}_B$, $\overline{W}_B$, $\overline{DS}_B$ and R/$\overline{W}_B$ when Port B is in the peripheral mode.
FLG_A-FLG_D	Flags	O	These four outputs pins can be assigned any one of the eight internal flags in the BiFIFO. Each of the two internal FIFOs (A→B and B→A) has four internal flags: Empty, Almost-Empty, Almost-Full and Full.
PIO_0-PIO_5	Program-mable Inputs/ Outputs	I/O	Six general purpose I/O pins. The input or output direction of each pin can be set independently.
$\overline{RS}$	Reset	I	A LOW on this pin will perform a reset of all BiFIFO functions.
V_{CC}	Power		There are two +5V power pins.
GND	Ground		There are five Ground pins at 0V.

2668 tbl 01

DETAILED BLOCK DIAGRAM



2668 drw 04

NOTES:

(*) Can be programmed either active high or active low in internal configuration registerers.

(==) Can be programmed through an internal configuration register to be either an input or an output.

FUNCTIONAL DESCRIPTION

IDT's BiFIFO family is versatile for both multiprocessor and peripheral applications. Data can be sent through both FIFO memories concurrently, thus freeing both processors from laborious direct memory access (DMA) protocols and frequent interrupts.

Two full 18-bit wide FIFOs are integrated into the IDT BiFIFO, making simultaneous data exchange possible. Each FIFO is monitored by separate internal read and write pointers, so communication is not only bidirectional, it is also totally independent in each direction. The processor connected to Port A of the BiFIFO can send or receive messages directly to the Port B device using the BiFIFO's 9-bit bypass path.

The BiFIFO can be used in different bus configurations: 18 bits to 18 bits and 36 bits to 36 bits. One BiFIFO can be used for the 18- to 18-bit configuration, and two BiFIFOs are required for 36- to 36-bit configuration. This configuration can be extended to wider bus widths (54- to 54-bits, 72- to 72-bits, …) by adding more BiFIFOs to the configuration.

The microprocessor or microcontroller connected to Port A controls all operations of the BiFIFO. Thus, all Port A interface pins are inputs driven by the controlling processor. Port B can be programmed to interface either with a second processor or a peripheral device. When Port B is programmed in processor interface mode, the Port B interface pins are inputs driven by the second processor. If a peripheral device is connected to the BiFIFO, Port B is programmed to peripheral interface mode and the interface pins are outputs.

18- to 18-bit Configurations

A single BiFIFO can be configured to connect an 18-bit processor to another 18-bit processor or an 18-bit peripheral. The upper BiFIFO shown in each of the Figures 1 and 2 can be used in 18- to 18-bit configurations for processor and peripheral interface modes respectively.

36- to 36-bit Configurations

In a 36- to 36-bit configuration, two BiFIFOs operate in parallel. Both BiFIFOs are programmed simultaneously, 18 data bits to each device. Figures 1 and 2 show multiple BiFIFOs configured for processor and peripheral interface modes respectively.

Processor Interface Mode

When a microprocessor or microcontroller is connected to Port B, all BiFIFOs in the configuration must be programmed to processor interface mode. In this mode, all Port B interface controls are inputs. Both REQ and CLK pins should be pulled LOW to ensure that the setup and hold time requirements for these pins are met during reset. Figure 1 shows the BiFIFO in processor interface mode.

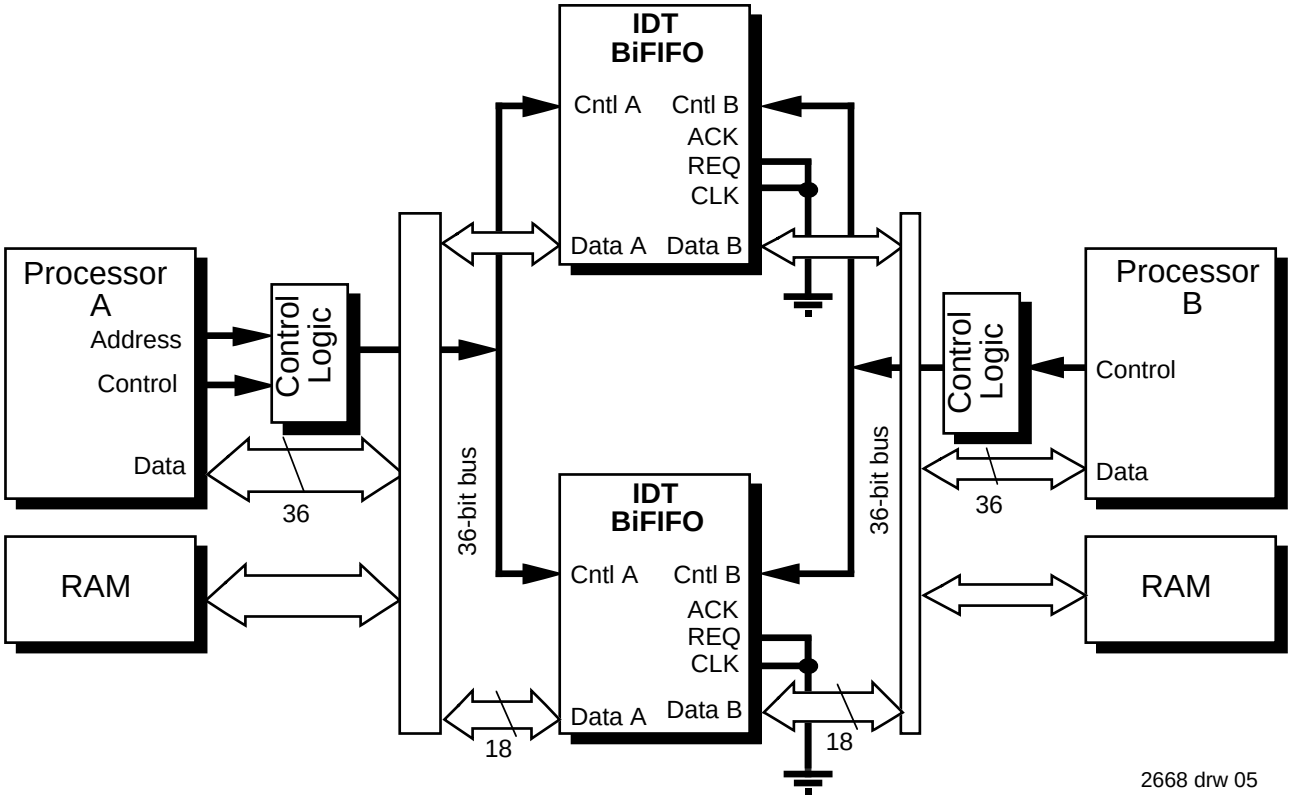


Figure 1. 36-Bit Processor to 36-Bit Processor Configuration

NOTE:

1. 36- to 36-bit processor interface configuration. Upper BiFIFO only is used in 18- to 18-bit configuration. Note that *Cntl A* refers to $\overline{CS}_A$, A_1, A_0, R/$\overline{W}_A$, and $\overline{DS}_A$; *Cntl B* refers to R/$\overline{W}_B$ and $\overline{DS}_B$ or $\overline{R}_B$ and $\overline{W}_B$.

Peripheral Interface Mode

If Port B is connected to a peripheral controller, all BiFIFOs in the configuration must be programmed in peripheral interface mode. In this mode, all the Port B interface pins are all outputs. To assure fixed high states for $\overline{R}_B$ and $\overline{W}_B$ before they are programmed into an output, these two pins should be pulled up to V_{CC} with 10K resistors. Of course, only one set of Port B interface pins should be used to control a single peripheral device, while the other interface pins are all ignored. Figure 2 shows a BiFIFO configuration connected to a peripheral.

Port A Interface

The BiFIFO is straightforward to use in microprocessor-based systems because each BiFIFO port has a standard microprocessor control set. Port A has access to six resources: the A→B FIFO, the B→A FIFO, the 9-bit direct data bus (bypass path), the configuration registers, status and command registers. The Port A Address and Read/Write pins determine the resource being accessed as shown in Table 1. Data Strobe is used to move data in and out of the BiFIFO.

When either of the internal FIFOs are accessed, 18 bits of data are transferred across Port A. Since the bypass path is only 9 bits wide, the least significant byte (D_{A0}-D_{A7}, D_{A16}) is used on Port A. All of the registers are 16 bits wide which means only the data bits (D_{A0}-D_{A15}) are passed by Port A.

Bypass Path

The bypass path acts as a bidirectional bus transceiver directly between Port A and Port B. The direct connection requires that the Port A interface pins are inputs and the Port B interface pins are outputs. The bypass path is 9 bits wide in an 18- to 18-bit configuration or 18 bits wide in a 36- to 36-bit configuration.

During bypass operations, the BiFIFOs must be programmed into peripheral interface mode. Bit 10 of Configuration Register 5 (see Table 10) is set to **1** for peripheral interface mode.

Command Register

Ten registers are accessible through Port A, a Command Register, a Status Register, and eight Configuration Registers.

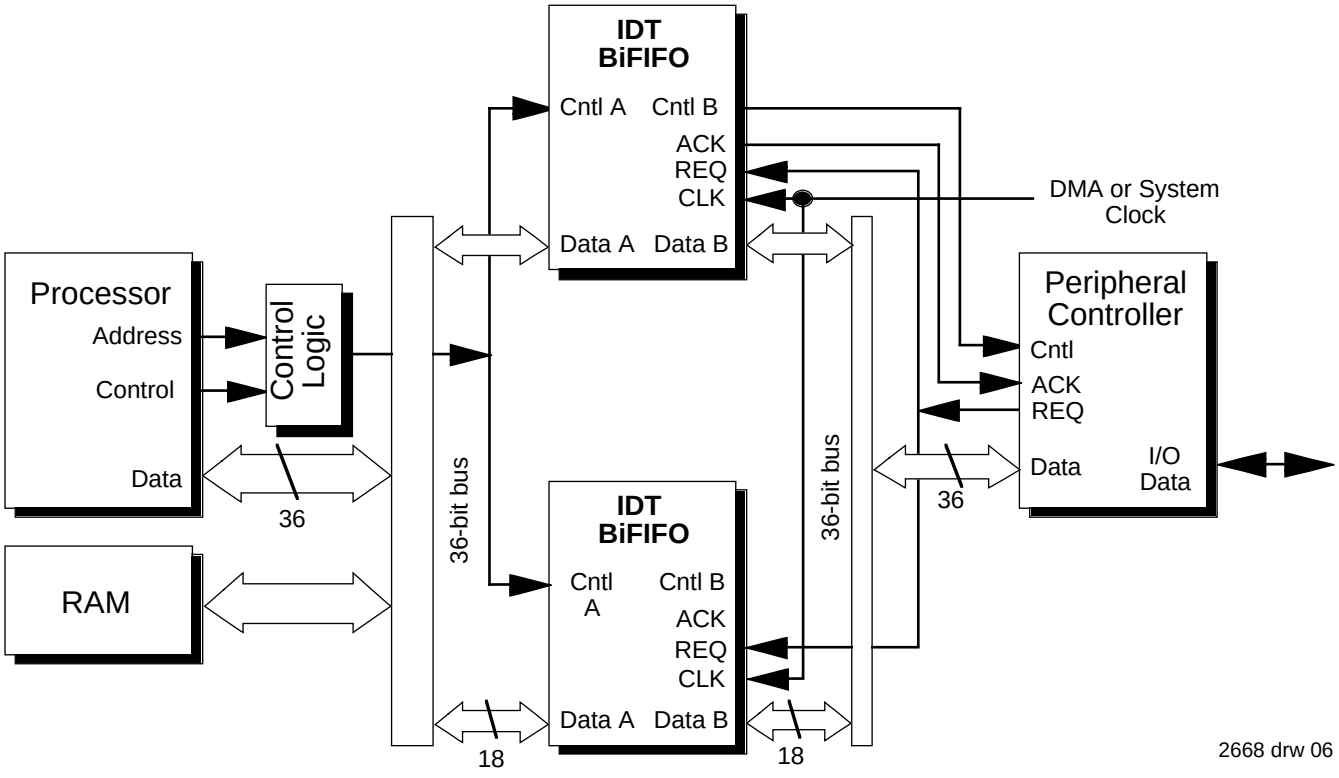


Figure 2. 36-Bit Processor to 36-Bit Peripheral Configuration

NOTE:

1. 36- to 36-bit peripheral interface configuration. Upper BiFIFO only is used in 18- to 18-bit configuration. Note that *Cntl A* refers to $\overline{CS}_A$, A_1, A_0, R/$\overline{W}_A$, and $\overline{DS}_A$; *Cntl B* refers to R/$\overline{W}_B$ and $\overline{DS}_B$ or $\overline{R}_B$ and $\overline{W}_B$.

The Command Register is written by setting $\overline{CS}_A$ = 0, A_1 = 1, A_0 = 1. Commands written into the BiFIFO have a 4-bit opcode (bit8 – bit 11) and a 3-bit operand (bit 0 – bit 2) as shown in Figure 3. The commands can be used to reset the BiFIFO, to select the Configuration Register, to perform intelligent reread/rewrite, to set the Port B DMA direction, to set the Status Register format, and to modify the Port B Read and Write Pointers. The command opcodes are shown in Table 2.

The reset command initializes different portions of the BiFIFO depending on the command operand. Table 3 shows the reset command operands.

The configuration Register address is set directly by the command operands shown in Table 4.

Intelligent reread/rewrite is performed by interchanging the Port B Read Pointer with the Reread Pointer or by interchanging the Port B Write Pointer with the Rewrite Pointer. No command operands are required to perform a reread/rewrite operation.

When Port B of the BiFIFO is in peripheral mode, the DMA direction is controlled by the Command Register. Table 5 shows the Port B read/write DMA direction operands.

Two commands are provided to increment the Port B Read and Write Pointers. No operands are required for these commands.

COMMAND FORMAT

15			12	11 – 8	7				3	2 – 0
X	X	X	X	Command Opcode	X	X	X	X	X	Command Operand

2668 tbl 02

Figure 3. Format for Commands Written into Port A

Reset

The IDT72511 and IDT72521 have a hardware reset pin ($\overline{RS}$) that resets all BiFIFO functions. A hardware reset requires the following four conditions: $\overline{R}_B$ and $\overline{W}_B$ must be HIGH, $\overline{RER}$ and $\overline{REW}$ must be HIGH, LDRER and LDREW must be LOW, and $\overline{DS}_A$ must be HIGH (Figure 9). After a hardware reset, the BiFIFO is in the following state: Configuration Registers 0-3 are **0000H**, Configuration Register 4 is set to **6420H**, and Configuration Registers 5, 6 and 7 are **0000H**. Additionally, all the pointers including the Reread and Rewrite Pointers are set to **0**, the DMA direction is set to B→A write, and the internal DMA request circuitry is cleared (set to its initial state).

A software reset command can reset A→B pointers and the B→A pointers to **0** independently or together. The internal request DMA circuitry can also be reset independently. A software Reset All command resets all the pointers, the DMA request circuitry, and sets all the Configuration Registers to their default condition. Note that a hardware reset is **NOT** the same as a software Reset All command. Table 6 shows the BiFIFO state after the different hardware and software resets

Status Register

The Status Register reports the state of the programmable flags and the DMA read/write direction. The Status Register is read by setting $\overline{CS}_A$ = 0, A_1 = 1, A_0 = 1 (see Table 1). See Table 7 for the Status Register format.

Configuration Registers

The eight Configuration Register formats are shown in

PORT A RESOURCE SELECTION

$\overline{CS}_A$	A_1	A_0	Read	Write
0	0	0	B→A FIFO	A→B FIFO
0	0	1	9-bit Bypass Path	9-bit Bypass Path
0	1	0	Configuration Registers	Configuration Registers
0	1	1	Status Register	Command Register
1	X	X	Disabled	Disabled

2668 tbl 03

Table 1. Accessing Port A Resources Using $\overline{CS}_A$, A_0 and A_1

COMMAND OPERATIONS

Command Opcode	Function
0000	Reset BiFIFO (see Table 3)
0001	Select Configuration Register (see Table 4)
0010	Load Reread Pointer with Read Pointer Value
0011	Load Rewrite Pointer with Write Pointer Value
0100	Load Read Pointer with Reread Pointer Value
0101	Load Write Pointer with Rewrite Pointer Value
0110	Set DMA Transfer Direction (see Table 5)
0111	Reserved
1000	Increment A→B FIFO Read Pointer (Port B)
1001	Increment B→A FIFO Write Pointer (Port B)
1010	Reserved
1011	Reserved

2668 tbl 05

Table 2. Functions Performed by Port A Commands

RESET COMMAND FUNCTIONS

Reset Operands	Function
000	No Operation
001	Reset B→A FIFO (Read, Write, and Rewrite Pointers = 0)
010	Reset A→B FIFO (Read, Write, and Reread Pointers = 0)
011	Reset B→A and A→B FIFO
100	Reset Internal DMA Request Circuitry
101	No Operation
110	No Operation
111	Reset All

2668 tbl 04

Table 3. Reset Command Functions

SELECT CONFIGURATION REGISTER/ COMMAND FUNCTIONS

Operands	Function
000	Select Configuration Register 0
001	Select Configuration Register 1
010	Select Configuration Register 2
011	Select Configuration Register 3
100	Select Configuration Register 4
101	Select Configuration Register 5
110	Select Configuration Register 6
111	Select Configuration Register 7

2668 tbl 06

Table 4. Select Configuration Register Functions.

DMA DIRECTION COMMAND FUNCTIONS

Operands	Function
XX0	Write B→A FIFO
XX1	Read A→B FIFO

2668 tbl 07

Table 5. Set DMA Direction Command Functions. Command Only Operates in Peripheral Interface Mode

STATE AFTER RESET

	Hardware Reset (*RS* asserted)	Software Reset				
		B→A(001)	A→B(010)	B→A and A→B(011)	Internal Request (100)	All(111)
Configuration Registers 0-3	0000H	—	—	—	—	0000H
Configuration Register 4	6420H	—	—	—	—	6420H
Configuration Register 5	0000H	—	—	—	—	0000H
Configuration Register 6-7	0000H	—	—	—	—	0000H
Status Register format	0	—	—	—	—	—
B→A Read, Write, Rewrite Pointers	0	0	—	0	—	0
A→B Read, Write, Reread Pointers	0	—	0	0	—	0
DMA direction	B→A write	—	—	—	—	—
DMA internal request	clear	—	—	—	clear	clear

2668 tbl 08

Table 6. The BiFIFO State After a Reset Command

Table 8. Configuration Registers 0-3 contain the programmable flag offsets for the Almost-Empty and Almost-Full flags. These offsets are set to **0** when a hardware reset or a software Reset All is applied. Note that Table 8 shows that Configuration Registers 0-3 are 10 bits wide to accommodate the 1024 locations in each FIFO memory of the IDT7252/520. Only 9 least significant bits are used for the 512 locations of the IDT7251/510; the most significant bit, bit 9, must be set to **0**.

Configuration Register 4 is used to assign the internal flags to the external flag pins (FLG_A-FLG_D). Each external flag pin is assigned an internal flag based on the four bit codes shown in Table 9. The default condition for Configuration Register 4 is **6420H** as shown in Table 6. The default flag assignments are: FLG_D is assigned B→A $\overline{Full}$, FLG_C is assigned B→A $\overline{Empty}$, FLG_B is assigned A→B $\overline{Full}$, FLG_A is assigned A→B $\overline{Empty}$.

Configuration Register 5 is a general control register. The format of Configuration Register 5 is shown in Table 10.

Bit 0 sets the Intel-style interface ($\overline{R}_B$, $\overline{W}_B$) or Motorola-style interface ($\overline{DS}_B$, R/$\overline{W}_B$) for Port B. Bits 2 and 3 redefine Full and Empty Flags for reread/rewrite data protection.

Bits 4-9 control the DMA interface and are only applicable in peripheral interface mode. In processor interface mode, these bits are don't care states. Bits 4 and 5 set the polarity of the DMA control pins REQ and ACK respectively. An internal clock controls all DMA operations. This internal clock is derived from the external clock (CLK). Bit 9 determines the internal clock frequency: the internal clock = CLK or the internal clock = CLK divided by 2. Bit 8 sets whether $\overline{R}_B$, $\overline{W}_B$, and $\overline{DS}_B$ are asserted for either one or two internal clocks. Bits 6 and 7 set the number of internal clocks between REQ assertion and ACK assertion. The timing can be from 2 to 5 cycles as shown in Figure 17.

Bit 10 controls Port B processor or peripheral interface mode. In processor mode, the Port B control pins ($\overline{R}_B$, $\overline{W}_B$, $\overline{DS}_B$, R/$\overline{W}_B$) are inputs and the DMA controls are ignored. In peripheral mode, the Port B control pins are outputs and the DMA controls are active.

Six PIO pins can be programmed as an input or output by the corresponding mask bits in Configuration Register 7. The format of Configuration Register 7 is shown in Figure 5. Each bit of the register set the I/O direction independently. A logic **1** indicates that the corresponding PIO pin is an output, while a logic **0** indicates that the PIO pin is an input. This I/O mask register can be read or written.

A programmed output PIO_i pin (i = 0, 1, . . . 5) displays the data latched in Bit i of Configuration Register 6. A programmed input PIO_i pin allows Port A bus to sample the data on D_{Ai} by reading Configuration Register 6.

STATUS REGISTER FORMAT

Bit	Signal
0	Reserved
1	Reserved
2	Reserved
3	DMA Direction
4	A→B Empty Flag
5	A→B Almost-Empty Flag
6	B→A Full Flag
7	B→A Almost-Full Flag
8	Reserved
9	Reserved
10	Reserved
11	Reserved
12	A→B Full Flag
13	A→B Almost-Full Flag
14	B→A Empty Flag
15	B→A Almost-Empty Flag

2668 tbl 09

Table 7. The Status Register Format

CONFIGURATION REGISTER FORMATS

	15					10	9	0
Config. Reg. 0	X	X	X	X	X	X	A→B FIFO Almost Empty Flag Offset	
Config. Reg. 1	X	X	X	X	X	X	A→B FIFO Almost Full Flag Offset	
Config. Reg. 2	X	X	X	X	X	X	B→A FIFO Almost Empty Flag Offset	
Config. Reg. 3	X	X	X	X	X	X	B→A FIFO Almost Full Flag Offset	

	15	12	11	8	7	4	3	0
Config. Reg. 4	Flag D Pin Assignment		Flag C Pin Assignment		Flag B Pin Assignment		Flag A Pin Assignment	

	15	0
Config. Reg. 5	General Control	
Config. Reg. 6	I/O Data	
Config. Reg. 7	I/O Direction Control	

2668 tbl 10

NOTE:

1. Bit 9 of Configuration Registers 0-3 must be set to 0 on the IDT72511.

Table 8. The BiFIFO Configuration Register Formats

Programmable Flags

The IDT BiFIFO has eight internal flags. Associated with each FIFO memory array are four internal flags, Empty, Almost-Empty, Almost-Full and Full, for the total of eight internal flags. The Almost-Empty and Almost-Full offsets can be set to any depth through the Configuration Registers 0-3 (see Table 8). The flags are asserted at the depths shown in Table 11. After a hardware reset or a software Reset All, the almost flag offsets are set to **0**. Even though the offsets are equivalent, the Empty and Almost-Empty flags have different timing which means that the flags are not coincident. Similarly, the Full and Almost-Full flags are not coincident after reset because of timing.

These eight internal flags can be assigned to any of four external flag pins (FLGA-FLGD) through Configuration Register 4 (see Table 9). For the specific flag timings, see Figures 20-23.

The current state of all eight flags is available in the Status Register.

EXTERNAL FLAG ASSIGNMENT CODES

Assignment Code	Internal Flag Assigned to Flag Pin
0000	A→B $\overline{\text{Empty}}$
0001	A→B $\overline{\text{Almost-Empty}}$
0010	A→B $\overline{\text{Full}}$
0011	A→B $\overline{\text{Almost-Full}}$
0100	B→A $\overline{\text{Empty}}$
0101	B→A $\overline{\text{Almost-Empty}}$
0110	B→A $\overline{\text{Full}}$
0111	B→A $\overline{\text{Almost-Full}}$
1000	A→B Empty
1001	A→B Almost-Empty
1010	A→B Full
1011	A→B Almost-Full
1100	B→A Empty
1101	B→A Almost-Empty
1110	B→A Full
1111	B→A Almost-Full

2668 tbl 11

Table 9. Configuration Register 4 Internal Flag Assignments to External Flag Pins

CONFIGURATION REGISTER 5 FORMAT

Bit	Function		
0	Select Port B Interface $\overline{R}_B$ and $\overline{W}_B$ or $\overline{DS}_B$ and R/$\overline{W}_B$	0	Pins are $\overline{R}_B$ and $\overline{W}_B$ (Intel-style interface)
		1	Pins are $\overline{DS}_B$ and R/$\overline{W}_B$ (Motorola-style interface)
1	Unused		
2	Full Flag Definition	0	Write pointer meets read pointer
		1	Write pointer meets reread pointer
3	Empty Flag Definition	0	Read pointer meets write pointer
		1	Read pointer meets rewrite pointer
4	REQ Pin Polarity	0	REQ pin active HIGH
		1	REQ pin active LOW
5	ACK Pin Polarity	0	ACK pin active LOW
		1	ACK pin active HIGH
7-6	REQ / ACK Timing	00	2 internal clocks between REQ assertion and ACK assertion
		01	3 internal clocks between REQ assertion and ACK assertion
		10	4 internal clocks between REQ assertion and ACK assertion
		11	5 internal clocks between REQ assertion and ACK assertion
8	Port B Read & Write Timing Control for Peripheral Mode	0	$\overline{R}_B$, $\overline{W}_B$, and $\overline{DS}_B$ are asserted for 1 internal clock
		1	$\overline{R}_B$, $\overline{W}_B$, and $\overline{DS}_B$ are asserted for 2 internal clocks
9	Internal Clock Frequency Control	0	Internal clock = CLK
		1	Internal clock = CLK divided by 2
10	Port B Interface Mode Control	0	Processor interface mode (Port B controls are inputs)
		1	Peripheral interface mode (Port B controls are outputs)
11	Unused		
12	Unused		
13	Unused		
14	Unused		
15	Unused		

2668 tbl 12

Table 10. BiFIFO Configuration Register 5 Format

CONFIGURATION REGISTER 6 FORMAT

15 6	5	4	3	2	1	0
Unused	PIO5	PIO4	PIO3	PIO2	PIO1	PIO0

2668 tbl 13

Figure 4. BiFIFO Configuration Register 6 Format for Programmable I/O Data

CONFIGURATION REGISTER 7 FORMAT

15 6	5	4	3	2	1	0
Unused	MIO5	MIO4	MIO3	MIO2	MIO1	MIO0

2668 tbl 14

Figure 5. BiFIFO Configuration Register 7 Format for Programmable I/O Direction Mask

Port B Interface

Port B has reread/rewrite and DMA functions. Port B can be configured to interface to either Intel-style ($\overline{R}_B$, $\overline{W}_B$) or Motorola-style ($\overline{DS}_B$, R/$\overline{W}_B$) devices in Configuration Register 5 (see Table 10). Port B can also be configured to talk to a processor or a peripheral device through Configuration Register 5. In processor interface mode, the Port B interface controls are inputs. In peripheral interface mode, the Port B interface controls are outputs. After a hardware reset or a software Reset All command, Port B defaults to an Intel-style processor interface; the controls are inputs.

DMA Control Interface

The BiFIFO has DMA control to simplify data transfers with peripherals. For the BiFIFO DMA controls (REQ, ACK and CLK) to operate, the BiFIFO must be in peripheral interface mode (Configuration Register 5, Table 10).

DMA timing is controlled by the external clock input, CLK. An internal clock is derived from this CLK signal to generate the $\overline{R}_B$, $\overline{W}_B$, $\overline{DS}_B$ and R/$\overline{W}_B$ output signals. The internal clock also determines the timing between REQ assertion and ACK assertion. Bit 9 of Configuration Register 5 determines whether the internal clock is the same as CLK or whether the internal clock is CLK divided by 2.

Bit 8 of Configuration Register 5 set whether $\overline{R}_B$, $\overline{W}_B$ and $\overline{DS}_B$ are asserted for 1 or 2 internal clocks. Bits 6 and 7 of Configuration Register 5 set the number of clocks between REQ assertion and ACK assertion. The clocks between REQ assertion and ACK assertion can be 2, 3, 4 or 5.

Bits 4 and 5 of Configuration Register 5 set the polarity of the REQ and ACK pins respectively.

A DMA transfer command sets the Port B read/write direction (see Table 5). The timing diagram for DMA transfers is shown in Figure 17. The basic DMA transfer starts with REQ assertion. After 2 to 5 internal clocks, ACK is asserted by the BiFIFO. ACK will not be asserted if a read is attempted on an empty A→B FIFO or if a write is attempted on a full B→A FIFO. If the BiFIFO is in Motorola-style interface mode, R/$\overline{W}_B$ is set at the same time that ACK is asserted. One internal clock later, $\overline{DS}_B$ is asserted. If the BiFIFO is in Intel-style interface mode, either $\overline{R}_B$ or $\overline{W}_B$ is asserted one internal clock after ACK assertion. These read/write controls stay asserted for 1 or 2 internal clocks, then ACK, $\overline{DS}_B$, $\overline{R}_B$ and $\overline{W}_B$ are made inactive. This completes the transfer of one 9-bit word.

On the next rising edge of CLK, REQ is sampled. If REQ is still asserted, another DMA transfer starts with the assertion of ACK. Data transfers will continue as long as REQ is asserted.

Intelligent Reread/Rewrite

Intelligent reread/rewrite is a method the BiFIFO uses to help assure data integrity. Port B of the BiFIFO has two extra pointers, the Reread Pointer and the Rewrite Pointer.The Reread Pointer is associated with the A->B FIFO Read Pointer, while the Rewrite Pointer is associated with the B->A FIFO Write Pointer. The Reread Pointer holds the start address of a data block in the A->B FIFO RAM, and the Read Pointer is the current address of the same FIFO RAM array. By loading the Read Pointer with the value held in the Reread Pointer (RER asserted), reads will start over at the beginning of the data block. In order to mark the beginning of a data block, the Reread Pointer should be loaded with the Read Pointer value (LDRER asserted) before the first read is performed on this data block. Figure 6 shows a Reread operation.

Similarly, the Rewrite Pointer holds the start address of a data block in the B->A FIFO RAM, while the Write Pointer is the current address within the RAM array. The operation of the REW and LDREW is identical to the RER and LDRER discussed above. Figure 7 shows a Rewrite operation.

For the reread data protection, Bit 2 of Configuration Register 5 can be set to 1 to prevent the data block from being overwritten. In this way, the assertion of A->B full flag will occur when the write pointer meets the reread pointer instead of the read pointer as in the normal definition. For the rewrite data protection, Bit 3 of Configuration Register 5 can be set to 1 to

INTERNAL FLAG TRUTH TABLE

Number of Words in FIFO					
From	To	Empty Flag	Almost-Empty Flag	Almost-Full Flag	Full Flag
0	0	Asserted	Asserted	Not Asserted	Not Asserted
1	n	Not Asserted	Asserted	Not Asserted	Not Asserted
n + 1	D – (m + 1)	Not Asserted	Not Asserted	Not Asserted	Not Asserted
D – m	D – 1	Not Asserted	Not Asserted	Asserted	Not Asserted
D	D	Not Asserted	Not Asserted	Asserted	Asserted

NOTE: 2668 tbl 15

1. BiFIFO flags must be assigned to external flag pins to be observed. D = FIFO depth (IDT72511 = 512, IDT72521 = 1024), n = Almost-Empty flag offset, m = Almost-Full flag offset.

Table 11. Internal Flag Truth Table

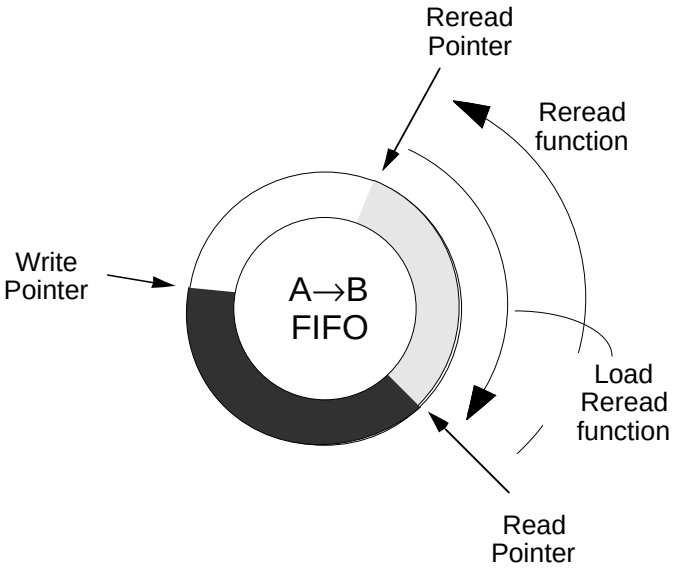
prevent the data block from being read. In this case the assertion of B->A empty flag will occur when the read pointer meets the rewrite pointer instead of the write pointer.

In conclusion, Bit 2 and 3 of Configuration Register 5 are used to redefine Full & Empty flags for data block partition. Although it can serve the purpose of data protection, the setting of these 2 bits is independent of the functions caused by RER/REW, or LDRER/LDREW assertions.

Programmable Input/Output

The BiFIFO has six programmable I/0 pins (PIO_0 - PIO_5) which are controlled by Port A through Configuration Registers 6 and 7. Data from the programmable I/O pins is mapped directly to the six least significant bits of Configuration Register 6. Figure 4 shows the format of Configuration Register 6. This data is read or written by Port A on the data pins (DA_0- DA_5). A programmed output PIO_i pin (i = 0, 1, . . . , 5) displays the data latched in Bit i of Configuration Register 6. A programmed input PIO_i pin allows Port A bus to sample its data on D_{Ai} by reading Configuration Register 6. The read and write timing for the programmable I/O pins is shown in Figure 19. The direction of each programmable I/O pin can be set independently by programming the mask in Configuration Register 7. Each P10 pin has a corresponding input/output direction mask bit in Configuration Register 7. Figure 5 shows the format of Configuration Register 7. Setting a mask bit to a logic 1 makes the corresponding I/O pin an output. Mask bits set to logic 0 force the corresponding I/O pin to an input.

REREAD OPERATIONS (1,2)

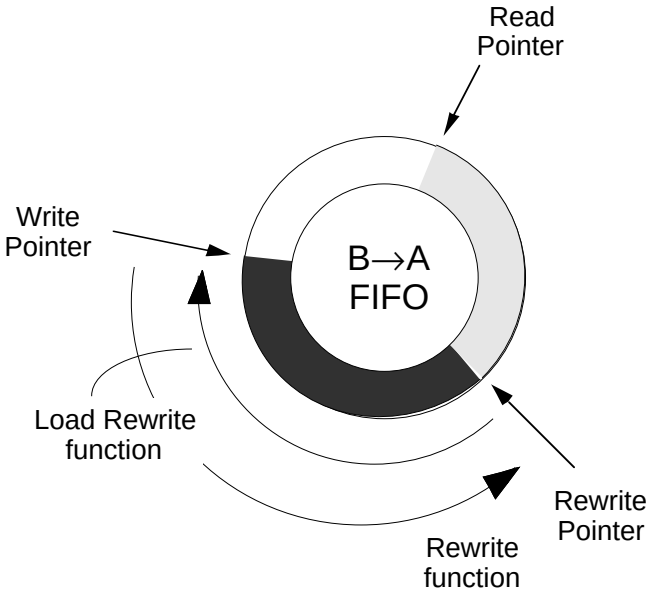


2668 drw 08

NOTES:
1. If bit 2 is set to 1,
   Empty flag asserted if Read = Write
   Full flag asserted if Reread + FIFO size = Write
2. If bit 2 is set to 0,
   Empty flag asserted if Read = Write
   Full flag asserted if Read + FIFO size = Write

Figure 6. BiFIFO Reread Operations

REWRITE OPERATIONS (3,4)



2668 drw 09

NOTES:
1. If bit 3 is set to 1,
   Empty flag asserted if Read = Rewrite
   Full flag asserted if Read + FIFO size = Write
2. If bit 3 is set to 0,
   Empty flag asserted if Read = Write
   Full flag asserted if Read + FIFO size = Write

Figure 7. BiFIFO Rewrite Operations

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Commercial	Military	Unit
V_{TERM}	Terminal Voltage With Respect To Ground	–0.5 to +7.0	–0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	–55 to +125	°C
T_{BIAS}	Temperature Under Bias	–55 to +125	–65 to +135	°C
T_{STG}	Storage Temperature	–55 to +125	–65 to +155	°C
I_{OUT}	DC Output Current	50	50	mA

NOTE: 2668 tbl 16

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CCM}	Military Supply Voltage	4.5	5.0	5.5	V
V_{CCC}	Commercial Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input HIGH Voltage Commercial	2.0	—	—	V
V_{IH}	Input HIGH Voltage Military	2.2	—	—	V
V_{IL}(1)	Input LOW Voltage Commercial and Military	—	—	0.8	V

NOTE: 2668 tbl 17

1. 1.5V undershoots are allowed for 10ns once per cycle.

DC ELECTRICAL CHARACTERISTICS

(Commercial: V_{CC} = 5V ± 10%, T_A = 0°C to +70°C; Military: V_{CC} = 5V ± 10%, T_A = –55°C to +125°C)

Symbol	Parameter	IDT72511L IDT72521L Commercial t_A = 25, 35, 50ns Min.	Typ.	Max.	IDT72521L Military t_A = 40, 50ns Min.	Typ.	Max.	Unit
I_{IL}(1)	Input Leakage Current (Any Input)	–1	—	1	–10	—	10	µA
I_{OL}(2)	Output Leakage Current	–10	—	10	–10	—	10	µA
V_{OH}	Output Logic "1" Voltage I_{OUT} = –1mA	2.4	—	—	2.4	—	—	V
V_{OL}	Output Logic "0" Voltage I_{OUT} = 4mA	—	—	0.4	—	—	0.4	V
I_{CC1}(3)(4)	Average VCC Power Supply Current	—	150	230	—	180	250	mA
I_{CC2}(3)	Average Standby Current ($\overline{R}_B$ = $\overline{W}_B$ = $\overline{DS}_A$ = V_{IH})	—	16	30	—	24	50	mA

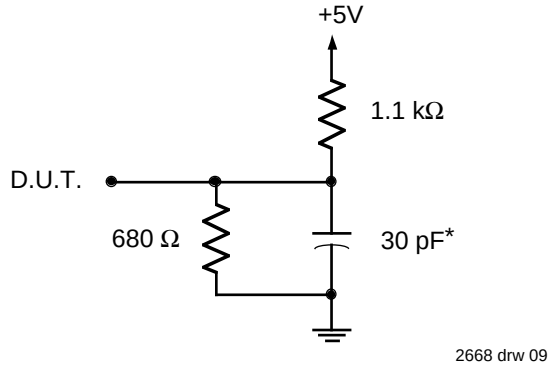
NOTES: 2668 tbl 18

1. Measurements with 0.4V ≤ V_{IN} ≤ V_{CC}, $\overline{DS}_A$ = $\overline{DS}_B$ ≥ V_{IH}
2. Measurements with 0.4V ≤ V_{OUT} ≤ V_{CC}, $\overline{DS}_A$ = $\overline{DS}_B$ ≥ V_{IH}
3. Measurements are made with outputs open.

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	3ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figure 8

2668 tbl 19



or equivalent circuit

Figure 8. Output Load
*Includes jig and scope capacitances

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter	Conditions	Max.	Unit
C_{IN}(2)	Input Capacitance	V_{IN} = 0V	8	pF
C_{OUT}(1,2)	Output Capacitance	V_{OUT} = 0V	12	pF

NOTES: 2668 tbl 20

1. With output deselected.
2. Characterized values, not currently tested.

AC ELECTRICAL CHARACTERISTICS

(Commercial: V_{CC} = 5V ± 10%, T_A = 0°C to + 70°C; Military: V_{CC} = 5V ± 10%, T_A = –55°C to + 125°C)

Symbol	Parameter	Commercial IDT72511L25 IDT72521L25 Min.	Commercial IDT72511L25 IDT72521L25 Max.	Commercial IDT72511L35 IDT72521L35 Min.	Commercial IDT72511L35 IDT72521L35 Max.	Military IDT72521L40 Min.	Military IDT72521L40 Max.	Com'l & Mil.(2) IDT72511L50 IDT72521L50 Min.	Com'l & Mil.(2) IDT72511L50 IDT72521L50 Max.	Unit	Timing Figure
RESET TIMING (Port A and Port B)											
t_{RSC}	Reset cycle time	35	—	45	—	50	—	65	—	ns	9
t_{RS}	Reset pulse width	25	—	35	—	40	—	50	—	ns	9
t_{RSS}	Reset set-up time	25	—	35	—	40	—	50	—	ns	9
t_{RSR}	Reset recovery time	10	—	10	—	10	—	15	—	ns	9
t_{RSF}	Reset to flag time	—	35	—	45	—	50	—	65	ns	9
PORT A TIMING											
t_{aA}	Port A access time	—	25	—	35	—	40	—	50	ns	12, 14, 15
t_{aLZ}	Read or write pulse LOW to data bus at Low-Z	5	—	5	—	5	—	5	—	ns	12, 15, 16
t_{aHZ}	Read or write pulse HIGH to data bus at High- Z	—	15	—	20	—	25	—	30	ns	12, 14, 15, 16
t_{aDV}	Data valid from read pulse HIGH	5	—	5	—	5	—	5	—	ns	12, 14, 16
t_{aRC}	Read cycle time	35	—	45	—	50	—	65	—	ns	12
t_{aRPW}	Read pulse width	25	—	35	—	40	—	50	—	ns	12, 14, 15
t_{aRR}	Read recovery time	10	—	10	—	10	—	15	—	ns	12
t_{aS}	$\overline{CS}_A$, A_0, A_1, $R/\overline{W}_A$ set-up time	5	—	5	—	5	—	5	—	ns	10, 12, 16
t_{aH}	$\overline{CS}_A$, A_0, A_1, $R/\overline{W}_A$ hold time	5	—	5	—	5	—	5	—	ns	10, 12
t_{aDS}	Data set-up time	15	—	18	—	20	—	30	—	ns	11, 12, 14, 15
t_{aDH}(1)	Data hold time	0	—	2	—	5	—	5	—	ns	11, 12, 14, 15
t_{aWC}	Write cycle time	35	—	45	—	50	—	65	—	ns	12
t_{aWPW}	Write pulse width	25	—	35	—	40	—	50	—	ns	11, 12, 14
t_{aWR}	Write recovery time	10	—	10	—	10	—	15	—	ns	12
t_{aWRCOM}	Write recovery time after a command	25	—	35	—	40	—	50	—	ns	11

2668 tbl 21

NOTE:

1. The minimum data hold time is 5ns (10ns for the 80ns speed grade) when writing to the Command or Configuration registers.
2. IDT72511 not available in military.

AC ELECTRICAL CHARACTERISTICS

(Commercial: V_{CC} = 5V ± 10%, T_A = 0°C to + 70°C; Military: V_{CC} = 5V ± 10%, T_A = –55°C to + 125°C)

		Commercial				Military		Com'l & Mil.(1)			
		IDT72511L25 IDT72521L25		IDT72511L35 IDT72521L35		IDT72521L40		IDT72511L50 IDT72521L50			Timing
Symbol	Parameter	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Unit	Figure
PORT B PROCESSOR INTERFACE TIMING											
tb_A	Port B access time	—	25	—	35	—	40	—	50	ns	13, 14, 15
tb_{LZ}	Read or write pulse LOW to data bus at Low-Z	5	—	5	—	5	—	5	—	ns	13, 14, 15
tb_{HZ}	Read or write pulse HIGH to data bus at High-Z	—	15	—	20	—	25	—	30	ns	14, 13, 15
tb_{DV}	Data valid from read pulse HIGH	5	—	5	—	5	—	5	—	ns	13, 14, 15, 16
tb_{RC}	Read cycle time	35	—	45	—	50	—	65	—	ns	13
tb_{RPW}	Read pulse width	25	—	35	—	40	—	50	—	ns	13
tb_{RR}	Read recovery time	10	—	10	—	10	—	15	—	ns	13
tb_S	$R/\overline{W}_B$ set-up time	5	—	5	—	5	—	5	—	ns	13
tb_H	$R/\overline{W}_B$ hold time	5	—	5	—	5	—	5	—	ns	13
tb_{DS}	Data set-up time	15	—	18	—	20	—	30	—	ns	13, 14, 15
tb_{DH}	Data hold time	0	—	2	—	5	—	5	—	ns	13, 14, 15
tb_{WC}	Write cycle time	35	—	45	—	50	—	65	—	ns	13
tb_{WPW}	Write pulse width	25	—	35	—	40	—	50	—	ns	13, 15
tb_{WR}	Write recovery time	10	—	10	—	10	—	15	—	ns	13
PORT B PERIPHERAL INTERFACE TIMING											
tb_A	Port B access time	—	25	—	40	—	45	—	55	ns	17
tb_{CKC}	Clock cycle time	15	—	20	—	20	—	25	—	ns	17
tb_{CKH}	Clock pulse HIGH time	6	—	6	—	8	—	10	—	ns	17
tb_{CKL}	Clock pulse LOW time	6	—	6	—	8	—	10	—	ns	17
tb_{REQS}	Request set-up time	5	—	5	—	5	—	10	—	ns	17
tb_{REQH}	Request hold time	5	—	5	—	5	—	5	—	ns	17
tb_{ACKL}	Delay from a rising clock edge to ACK switching	—	15	—	18	—	20	—	25	ns	17

NOTE:

1. IDT72511 not available in military.

2668 tbl 22

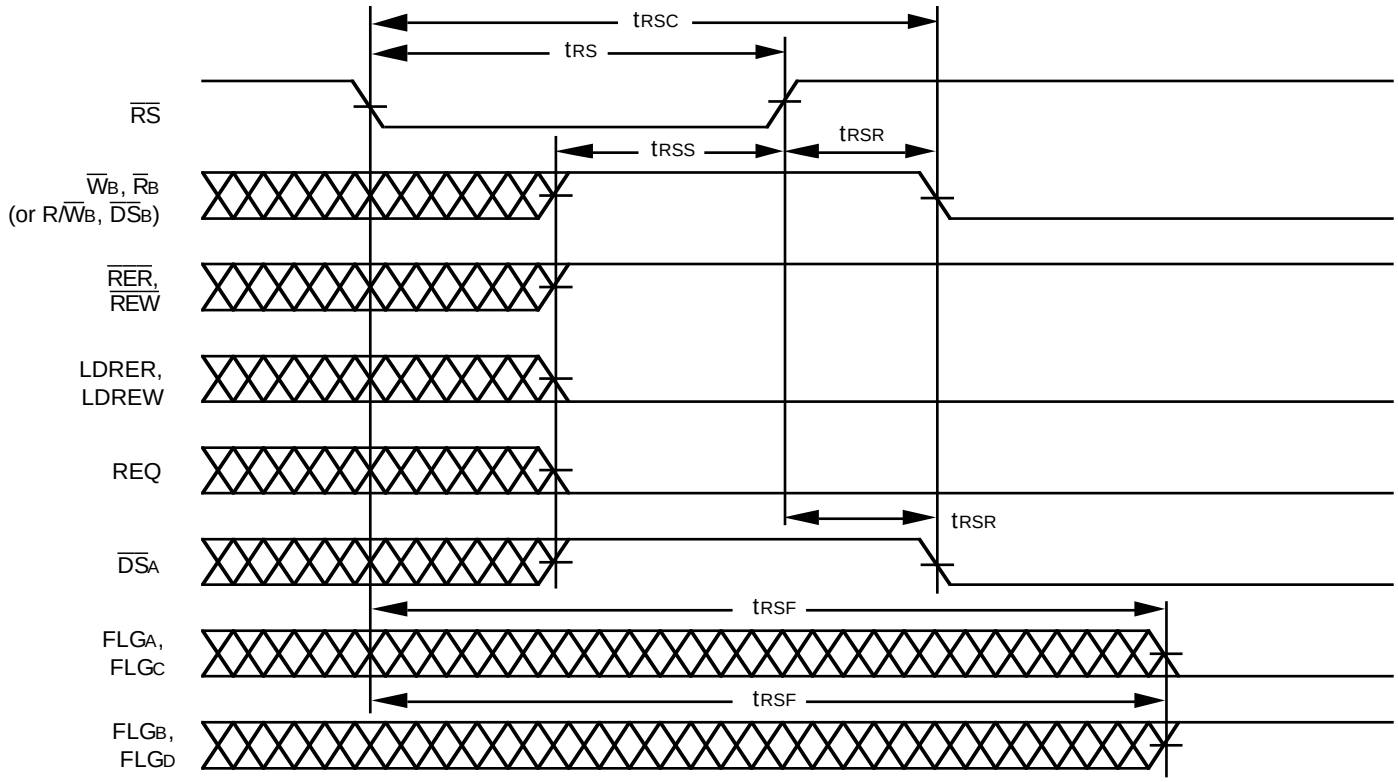
AC ELECTRICAL CHARACTERISTICS

(Commercial: V_{CC} = 5V ± 10%, T_A = 0°C to + 70°C; Military: V_{CC} = 5V ± 10%, T_A = –55°C to + 125°C)

		Commercial				Military		Com'l & Mil.(4)			
		IDT72511L25 IDT72521L25		IDT72511L35 IDT72521L35		IDT72521L40		IDT72511L50 IDT72521L50			Timing
Symbol	Parameter	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Unit	Figure
PORT B RETRANSMIT TIMING											
t_{bDSBH}	$\overline{RER}$, $\overline{REW}$, LDRER, LDREW set-up and recovery time	10	—	10	—	10	—	15	—	ns	9, 18
PROGRAMMABLE I/O TIMING											
t_{PIOA}	Programmable I/O access time	—	20	—	25	—	25	—	30	ns	19
t_{PIOS}	Programmable I/O set-up time	8	—	10	—	10	—	15	—	ns	19
t_{PIOH}	Programmable I/O hold time	8	—	10	—	10	—	15	—	ns	19
BYPASS TIMING											
t_{BYA}	Bypass access time	—	18	—	20	—	25	—	30	ns	16
t_{BYD}	Bypass delay	—	10	—	15	—	20	—	20	ns	16
t_{aBYDV}	Bypass data valid time from $\overline{DS}_A$	15	—	15	—	15	—	15	—	ns	16
t_{bBYDV} (3)	Bypass data valid time from $\overline{DS}_B$	3	—	3	—	3	—	3	—	ns	16
FLAG TIMING (1) (2)											
t_{REF}	Read clock edge to Empty Flag asserted	—	25	—	35	—	40	—	45	ns	14, 15, 20, 22
t_{WEF}	Write clock edge to Empty Flag not asserted	—	25	—	35	—	40	—	45	ns	14, 15, 20, 22
t_{RFF}	Read clock edge to Full Flag not asserted	—	25	—	35	—	40	—	45	ns	14, 15, 21, 23
t_{WFF}	Write clock edge to Full Flag asserted	—	25	—	35	—	40	—	45	ns	14, 15, 21, 23
t_{RAEF}	Read clock edge to Almost-Empty Flag asserted	—	40	—	50	—	55	—	60	ns	20, 22
t_{WAEF}	Write clock edge to Almost-Empty Flag not asserted	—	40	—	50	—	55	—	60	ns	20, 22
t_{RAFF}	Read clock edge to Almost-Full Flag not asserted	—	40	—	50	—	55	—	60	ns	21, 23
t_{WAFF}	Write clock edge to Almost-Full Flag asserted	—	40	—	50	—	55	—	60	ns	21, 23

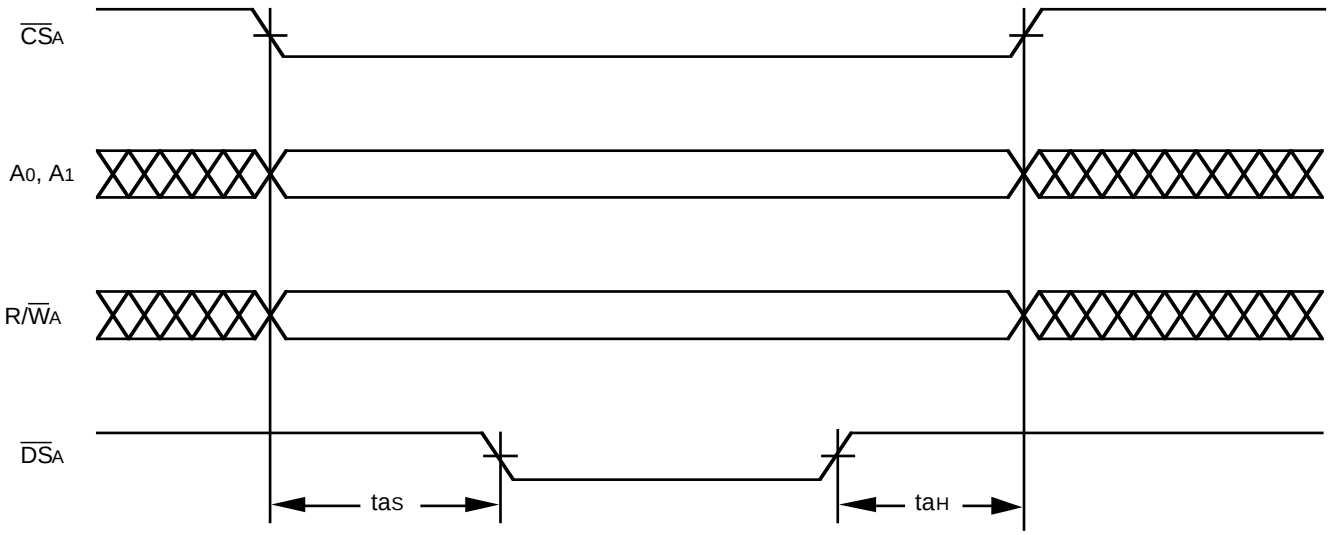
NOTES: 2668 tbl 23

1. Read and write are internal signals derived from $\overline{DS}_A$, $R/\overline{W}_A$, $\overline{DS}_B$, $\overline{R}/W_B$, $\overline{R}_B$, and $\overline{W}_B$.
2. Although the flags, Empty, Almost-Empty, Almost-Full, and Full Flags are internal flags, the timing given is for those assigned to external pins.
3. Values guaranteed by design, not currently tested.
4. IDT72511 not available in military.



2668 drw 10

Figure 9. Hardware Reset Timing



2668 drw 11

Figure 10. Basic Port A Control Signal Timing (Applies to All Port A Timing)

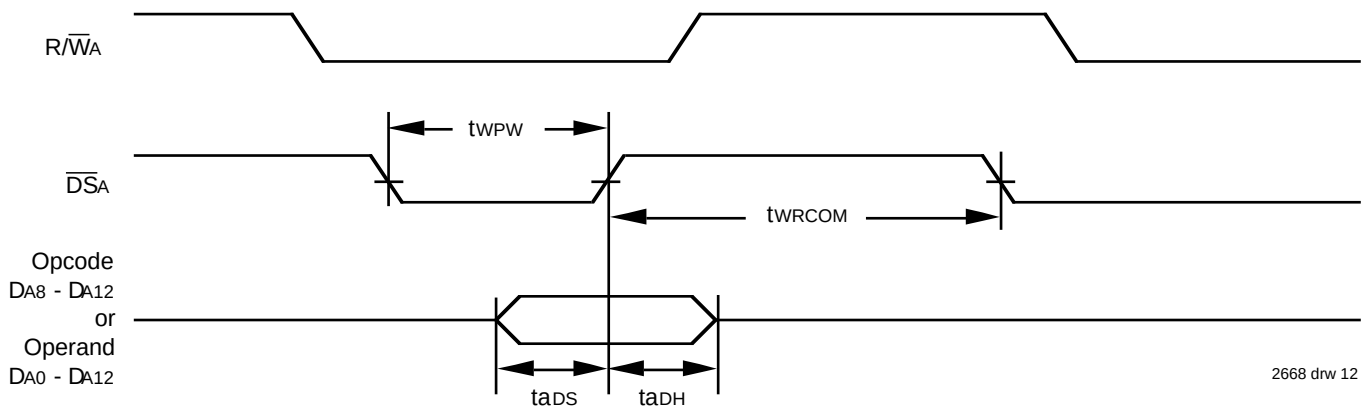
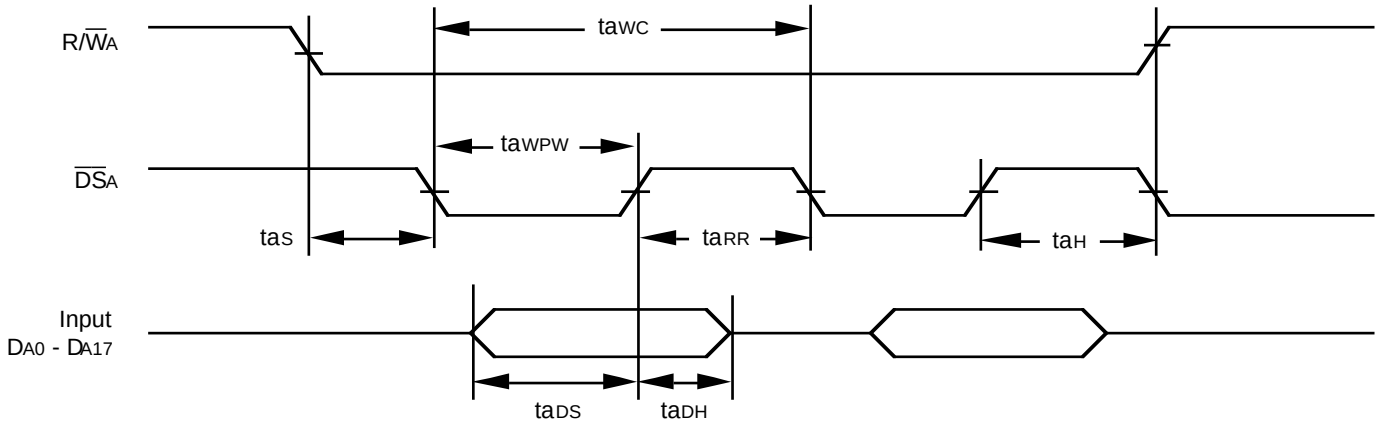


Figure 11. Port A Command Timing (write).

WRITE



READ

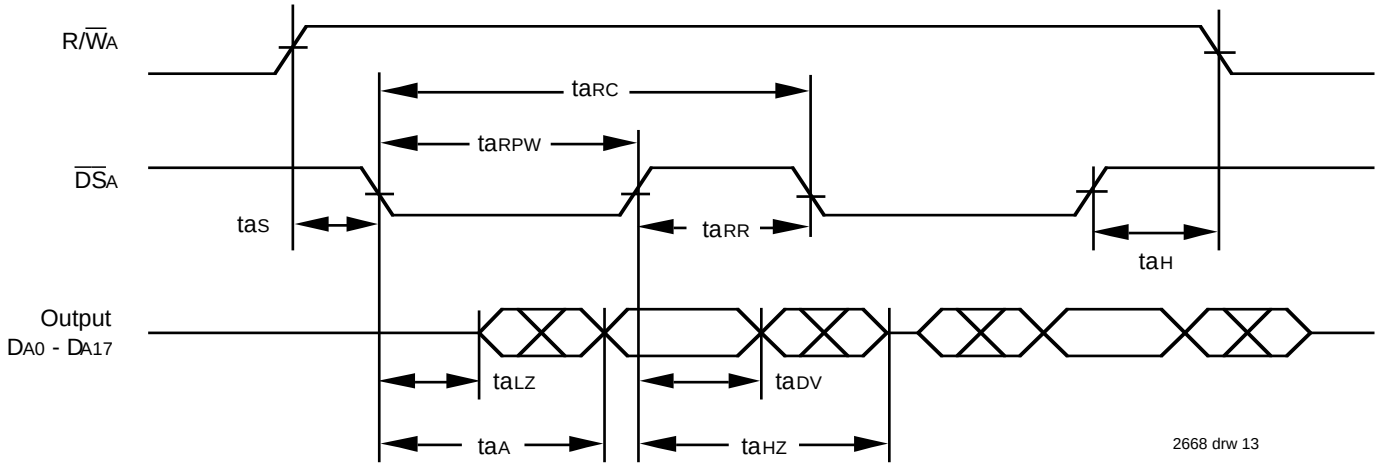
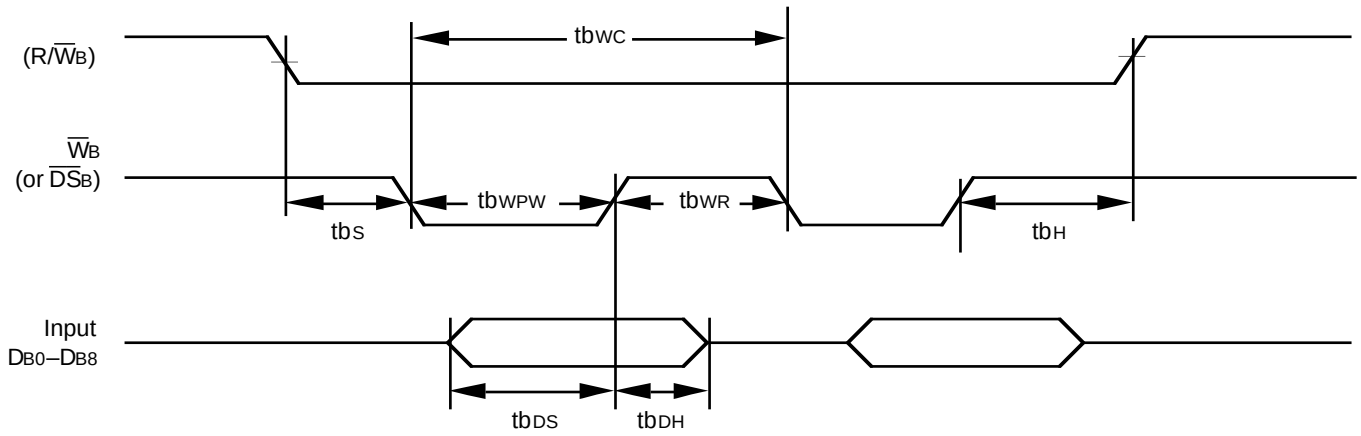


Figure 12. Read and Write Timing for Port A

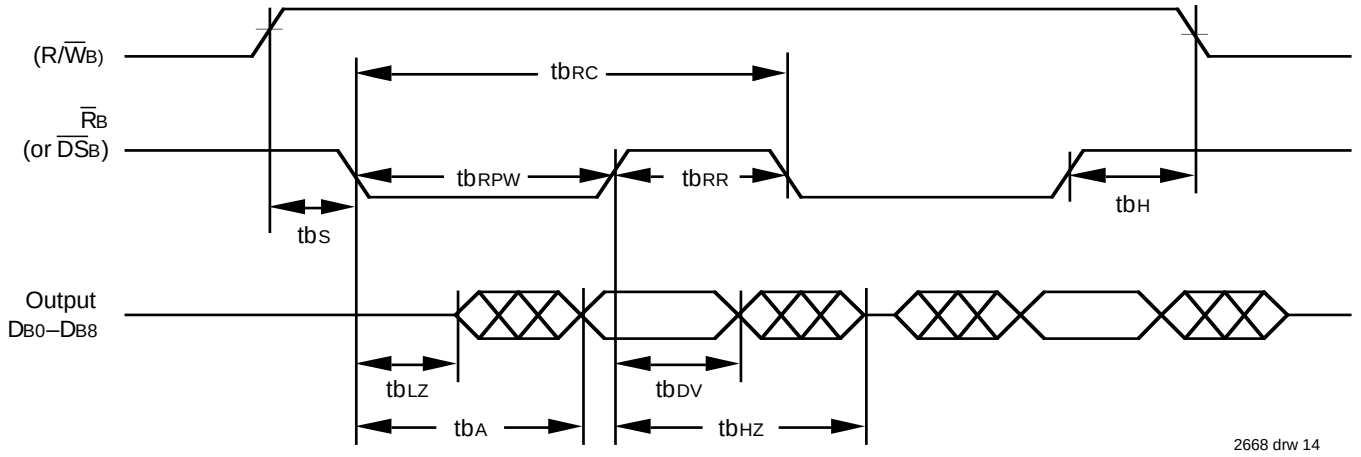
WRITE



NOTE:

1. $\overline{R}_B$ = 1

READ

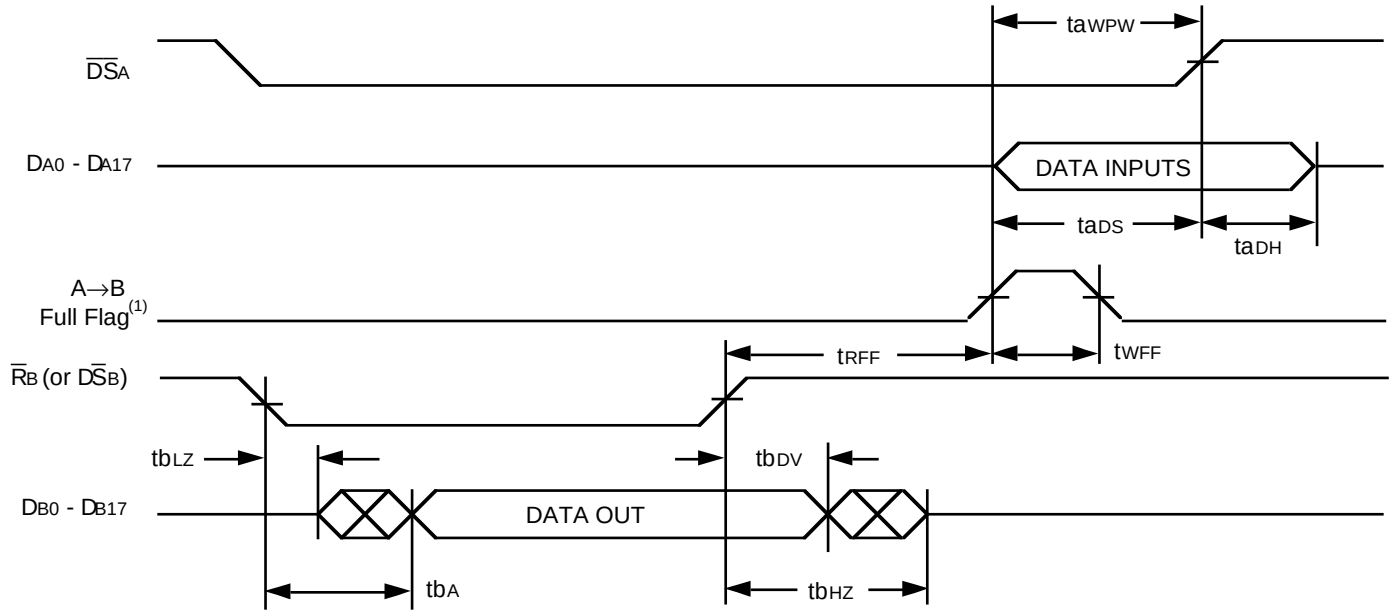


NOTE:

1. $\overline{W}_B$ = 1

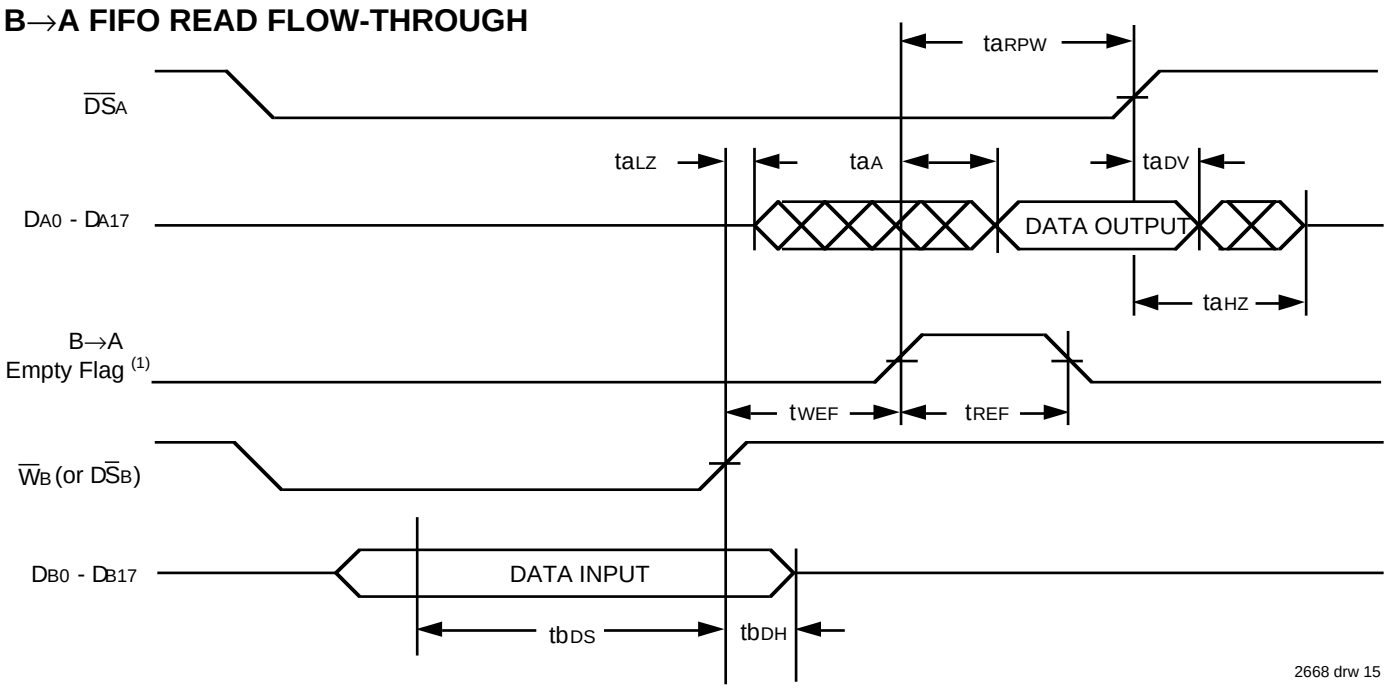
Figure 13. Port B Read and Write Timing, Processor Interface Mode Only

A→B FIFO WRITE FLOW-THROUGH



NOTES:
1. Assume the flag pin is programmed active LOW.
2. R/$\overline{W}$A = 0

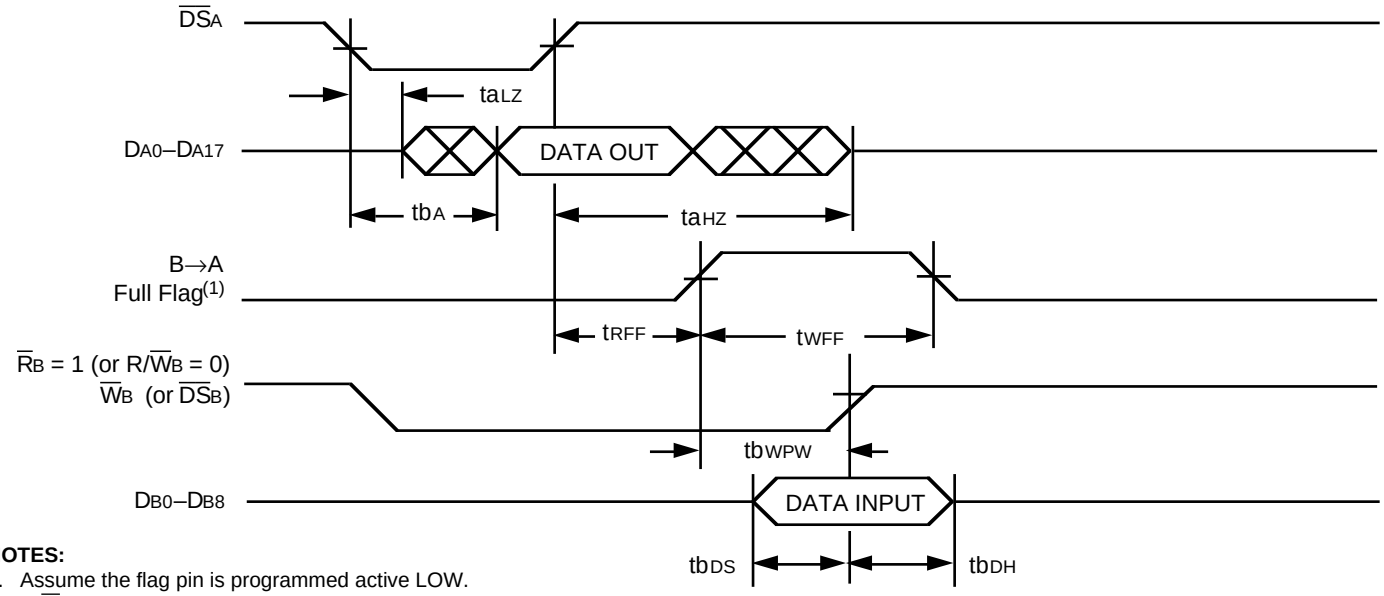
B→A FIFO READ FLOW-THROUGH



NOTES:
1. Assume the flag pin is programmed active LOW.
2. R/$\overline{W}$A = 1

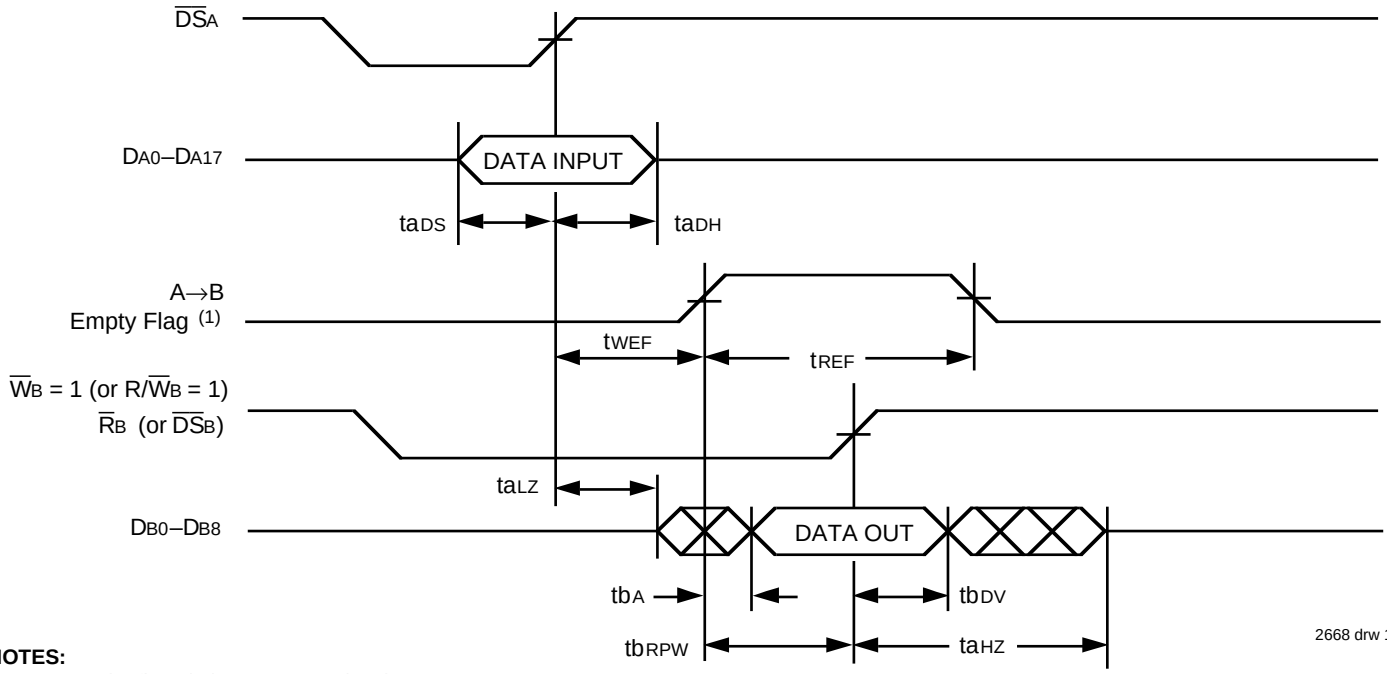
Figure 14. Port A Read and Write Flow-Through Timing, Processor Interface Mode Only

A→B FIFO WRITE FLOW-THROUGH



NOTES:
1. Assume the flag pin is programmed active LOW.
2. R/$\overline{W}$A = 1

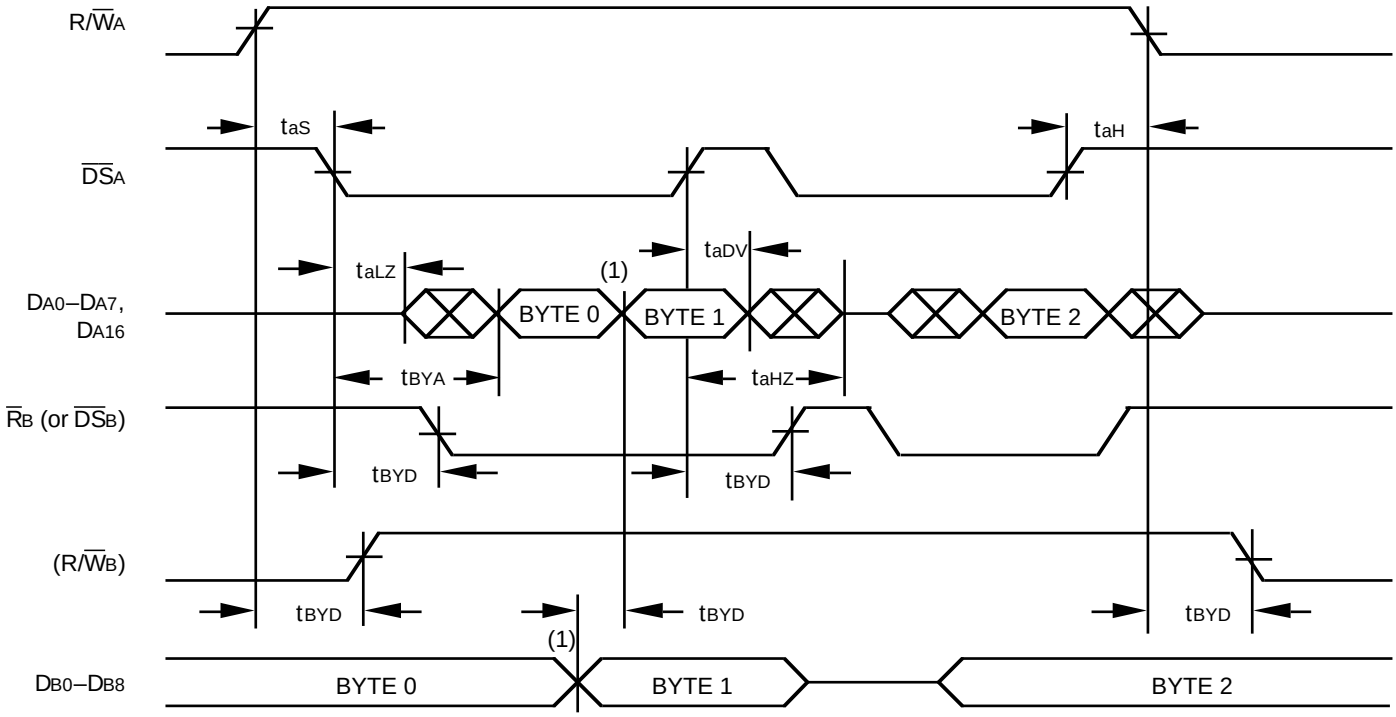
A→B FIFO READ FLOW-THROUGH



NOTES:
1. Assume the flag pin is programmed active LOW.
2. R/$\overline{W}$A = 0

Figure 15. Port B Read and Write Flow-Through Timing, Processor Interface Mode Only

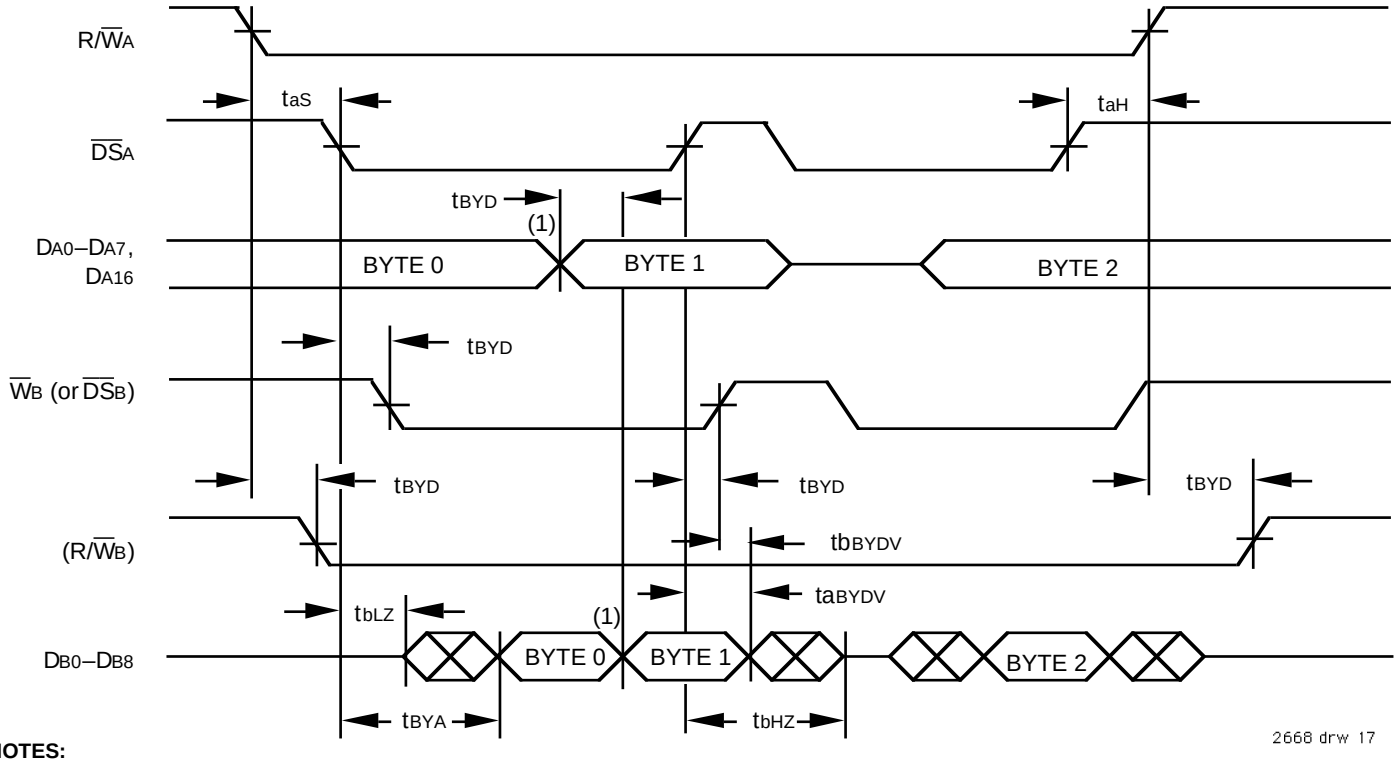
B→A READ BYPASS



NOTES:

1. Once the bypass mode starts, any data change on Port B bus (Byte 0→Byte 1) will be passed to Port A bus.
2. $\overline{W}$B = 1

A→B WRITE BYPASS

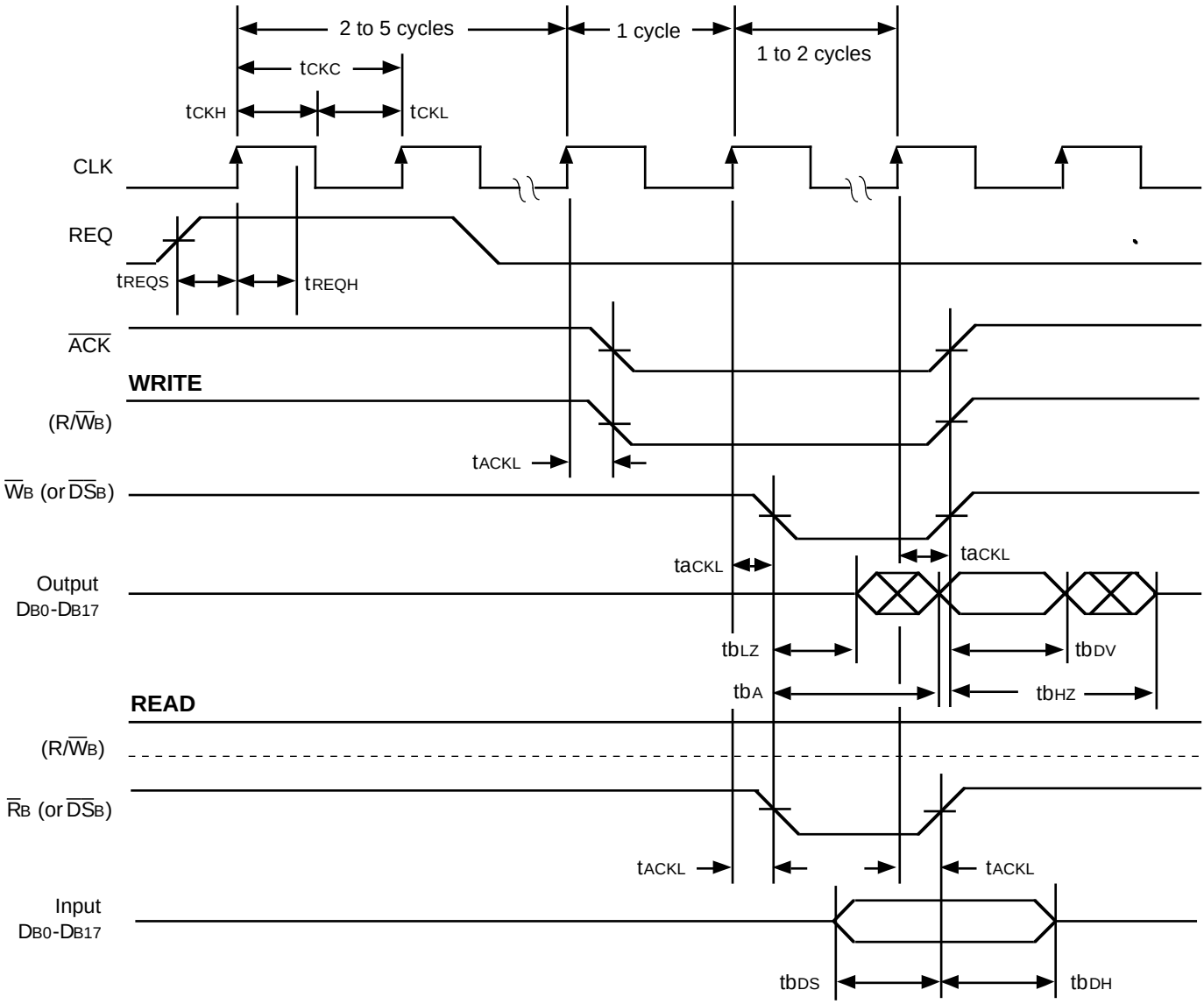


NOTES:

1. Once the bypass mode starts, any data change on Port A bus (Byte 0→Byte 1) will be passed to Port B bus.
2. $\overline{R}$B = 1

Figure 16. Bypass Path Timing, BiFIFO Must Be in Peripheral Interface Mode

SINGLE WORD DMA TRANSFER



BLOCK DMA TRANSFER

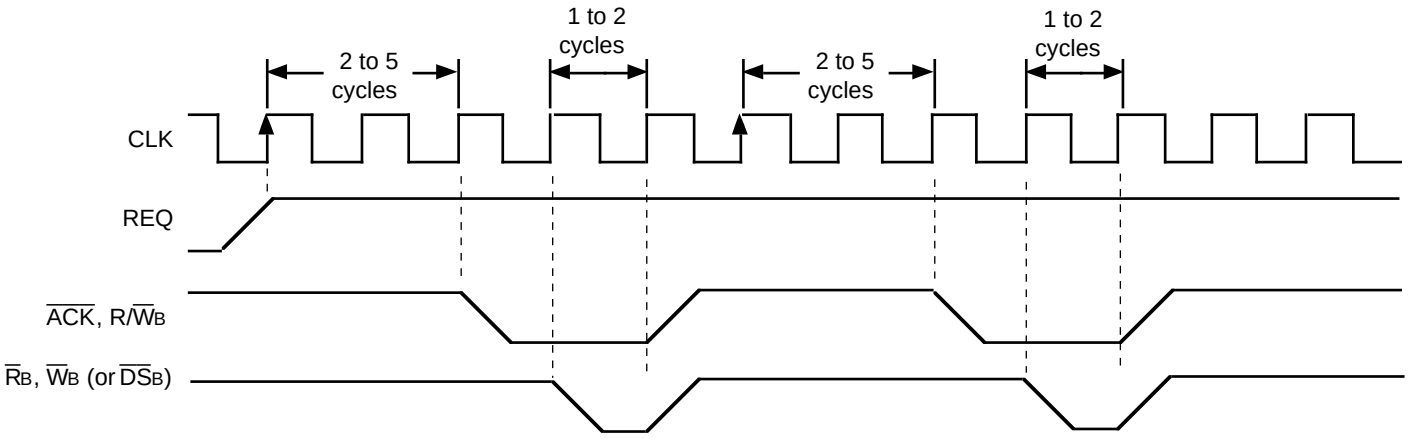


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Figure 17. Port B Read and Write DMA timing. Peripheral Interface Mode Only

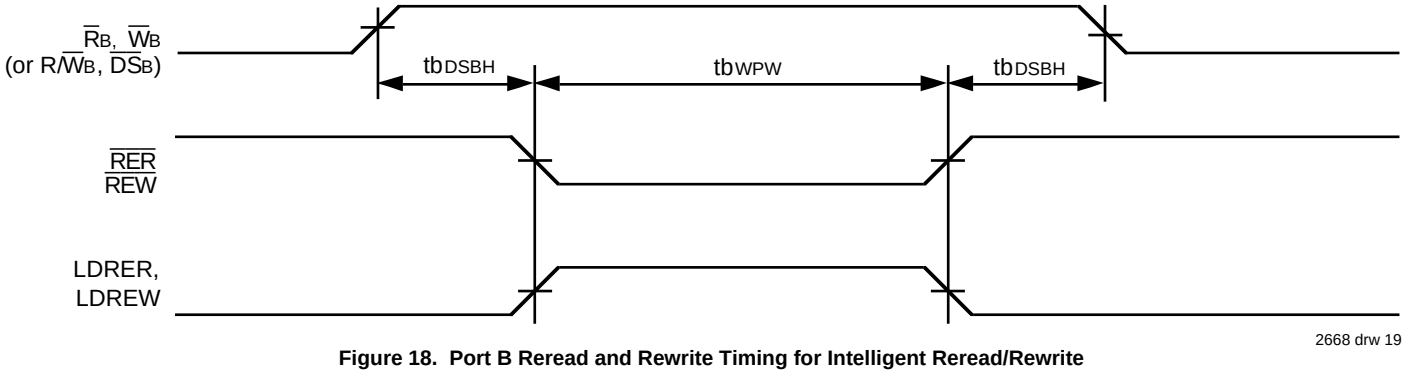
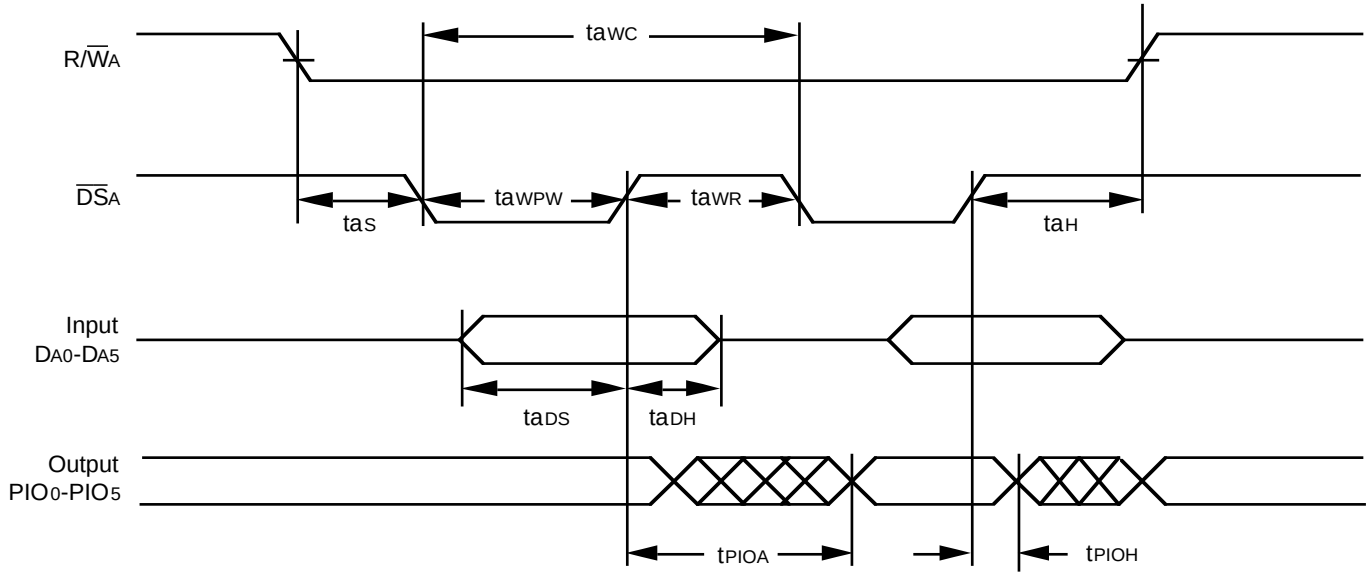


Figure 18. Port B Reread and Rewrite Timing for Intelligent Reread/Rewrite

Port A → PIO WRITE



PIO → Port A READ

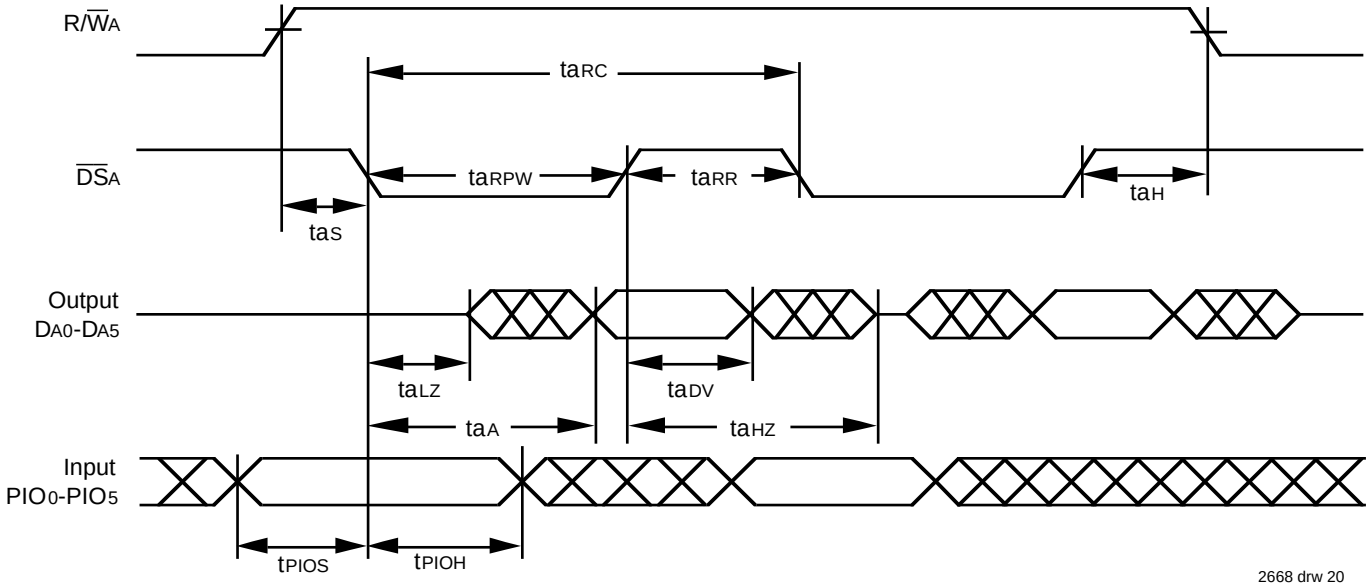
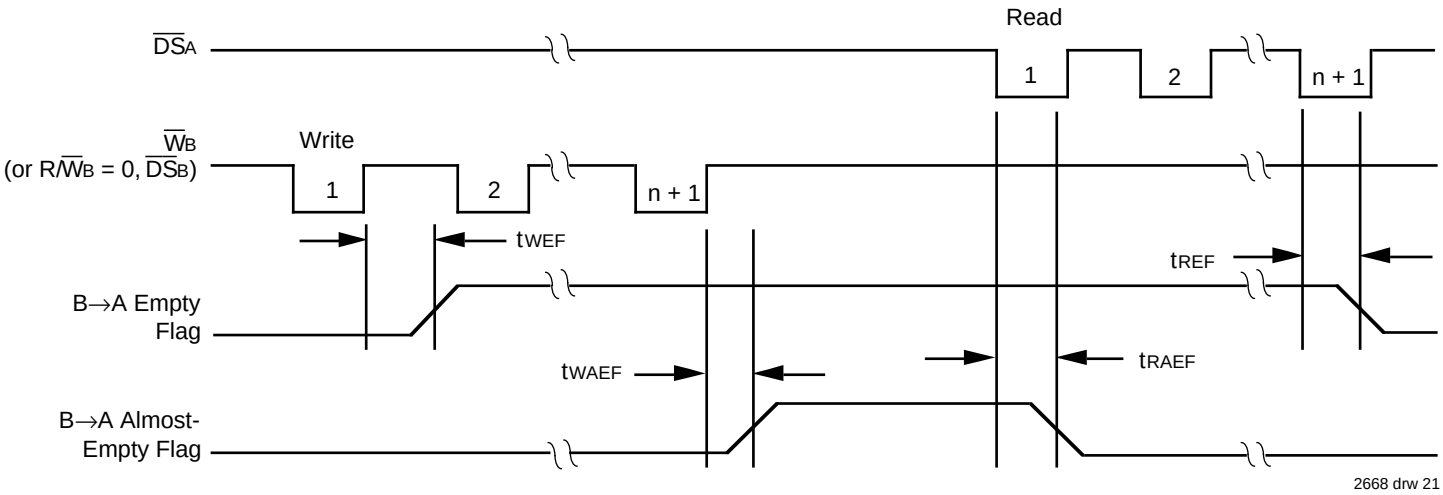
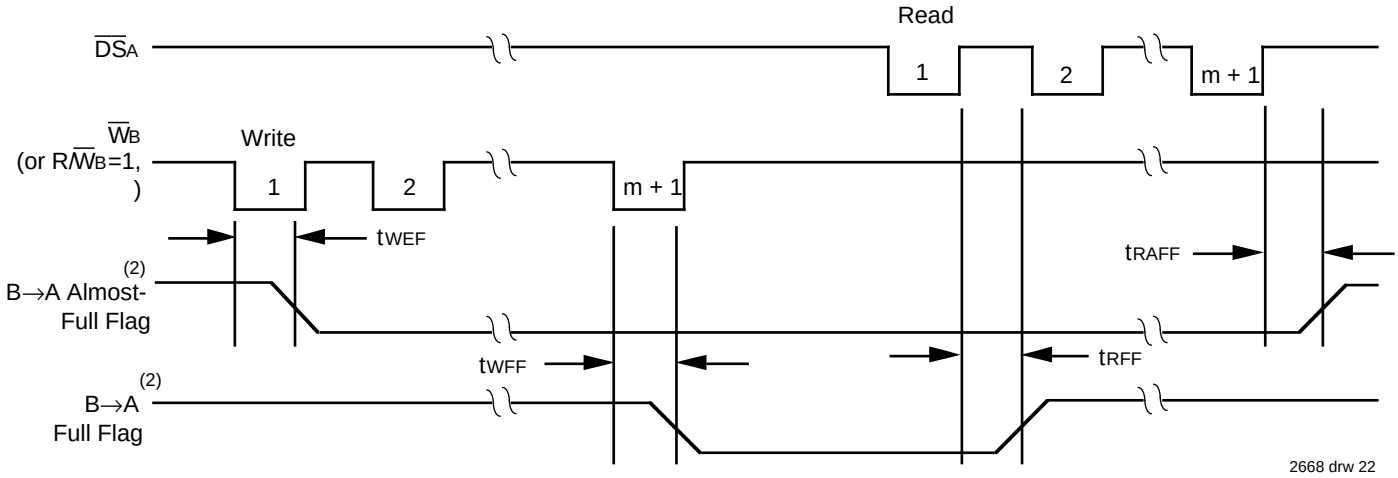


Figure 19. Programmable I/O Timing



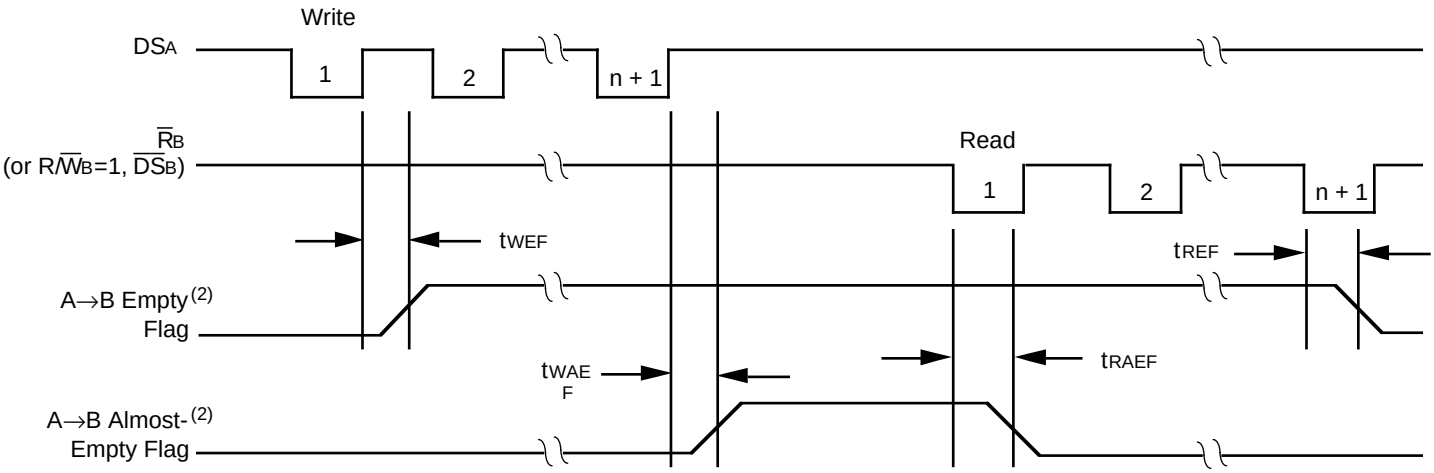
NOTES:
1. B→A FIFO is initially empty.
2. Assume the flag pins are programmed active LOW.
3. R/$\overline{W}$A = 1.

Figure 20. Empty and Almost-Empty Flag Timing for B→A FIFO, (n = programmed offset)



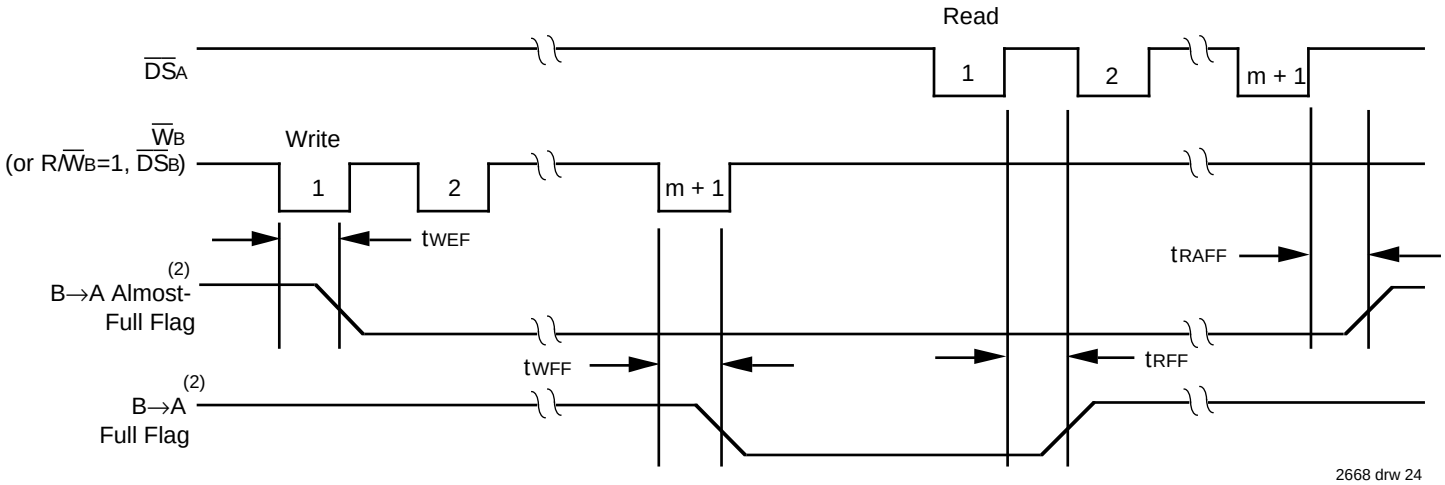
NOTES:
1. B→A FIFO initially contains D – (M + 1) data words. D = 512 for IDT72511; D = 1024 for IDT72521.
2. Assume the flag pins are programmed active LOW.
3. R/$\overline{W}$A = 1.

Figure 21. Full and Almost-Full Flag Timing for B→A FIFO, (m = programmed offset)



NOTES:
1. A→B FIFO is initially empty.
2. Assume the flag pins are programmed active LOW.
3. R/WA = 1.

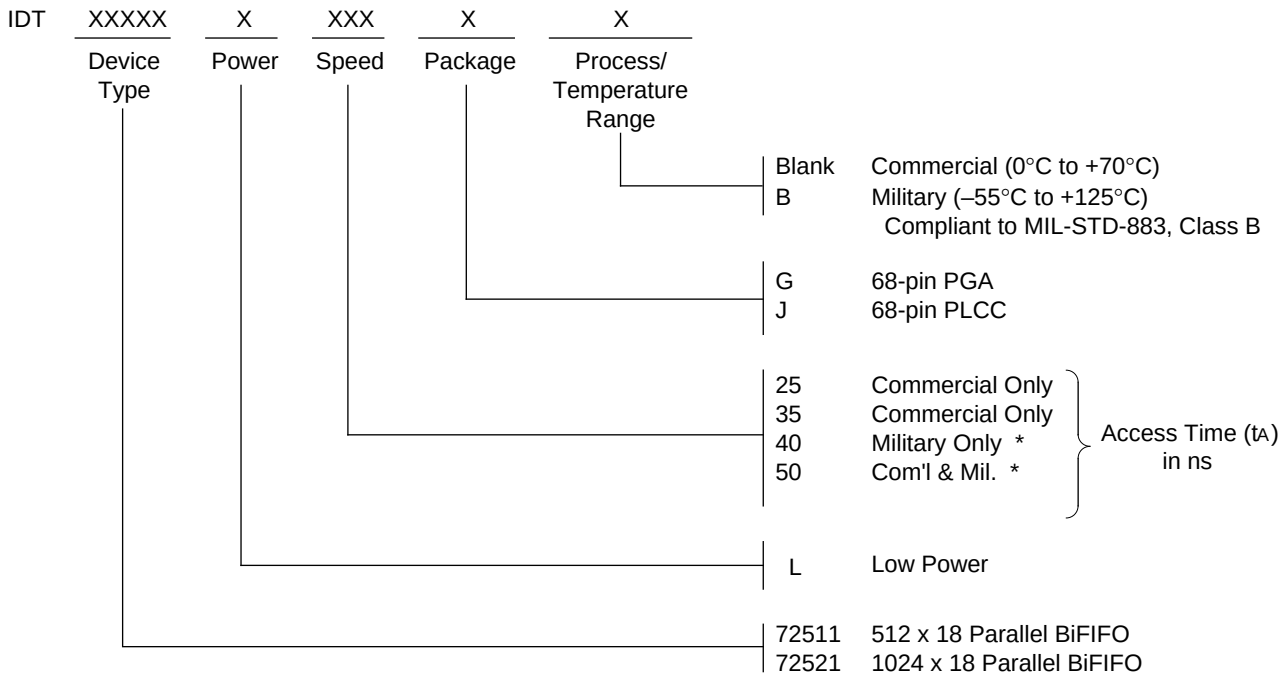
Figure 22. Empty and Almost-Empty Flag Timing for A→B FIFO, (n = programmed offset)



NOTES:
1. B→A FIFO initially contains D – (M + 1) data words. D = 512 for IDT72511; D = 1024 for IDT72521.
2. Assume the flag pins are programmed active LOW.
3. R/WA = 1.

Figure 23. Full and Almost-Full Flag Timing for A→B FIFO, (m = programmed offset)

ORDERING INFORMATION



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* 40 Military Only, IDT72521
* 50 Commercial and Military, IDT72511 available in commercial only

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