



# LIS302DL

## MEMS motion sensor 3-axis - $\pm 2g/\pm 8g$ smart digital output “piccolo” accelerometer

### Feature

- 2.16V to 3.6V supply voltage
- 1.8V compatible IOs
- <1mW power consumption
- $\pm 2g / \pm 8g$  dynamically selectable full-scale
- I<sup>2</sup>C/SPI digital output interface
- Programmable multiple interrupt generator
- Click and double click recognition
- Embedded high pass filter
- Embedded self test
- 10000g high shock survivability
- ECOPACK® RoHS and “Green” compliant (see [Section 9](#))

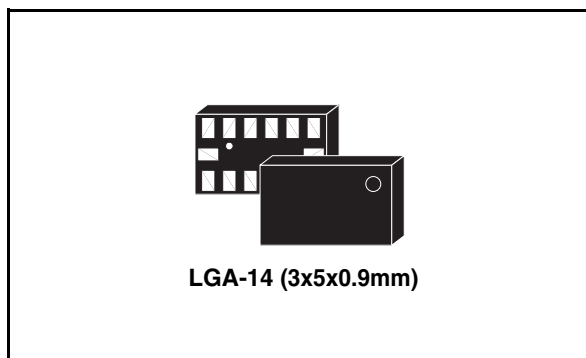
### Application

- Free-Fall detection
- Motion activated functions
- Gaming and virtual reality input devices
- Vibration monitoring and compensation

### Description

The LIS302DL is an ultra compact low-power three axes linear accelerometer. It includes a sensing element and an IC interface able to provide the measured acceleration to the external world through I<sup>2</sup>C/SPI serial interface.

The sensing element, capable of detecting the acceleration, is manufactured using a dedicated



process developed by ST to produce inertial sensors and actuators in silicon.

The IC interface is manufactured using a CMOS process that allows to design a dedicated circuit which is trimmed to better match the sensing element characteristics.

The LIS302DL has dynamically user selectable full scales of  $\pm 2g/\pm 8g$  and it is capable of measuring accelerations with an output data rate of 100Hz or 400Hz.

A self-test capability allows the user to check the functioning of the sensor in the final application.

The device may be configured to generate inertial wake-up/free-fall interrupt signals when a programmable acceleration threshold is crossed at least in one of the three axes. Thresholds and timing of interrupt generators are programmable by the end user on the fly.

The LIS302DL is available in plastic Thin Land Grid Array package (TLGA) and it is guaranteed to operate over an extended temperature range from -40°C to +85°C.

**Table 1. Device summary**

| Part number | Temp range, °C | Package | Packing                       |
|-------------|----------------|---------|-------------------------------|
| LIS302DL    | -40 to +85     | LGA     | Tray                          |
| LIS302DLTR  | -40 to +85     | LGA     | Tape and reel (5000 pcs/reel) |
| LIS302DLTR8 | -40 to +85     | LGA     | Tape and reel (8000 pcs/reel) |

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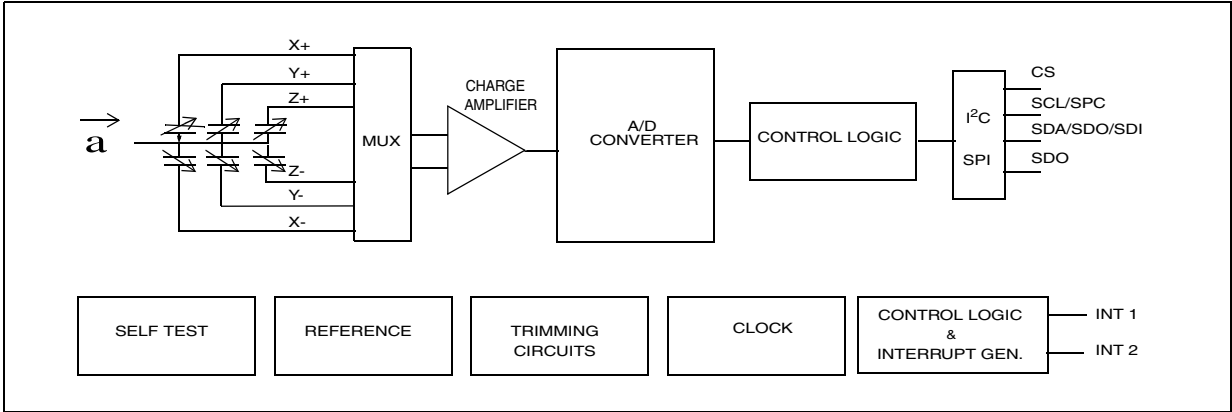
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# 1 Block diagram and pin description

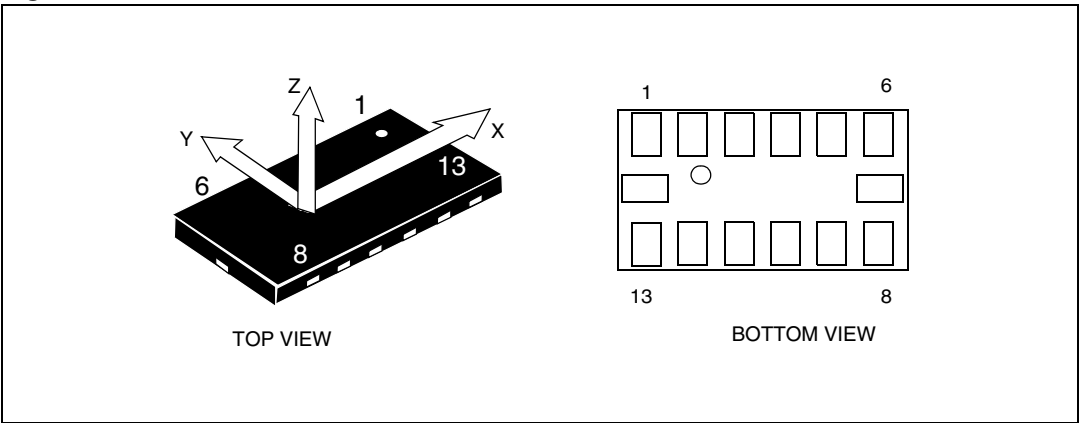
## 1.1 Block diagram

Figure 1. Block diagram



## 1.2 Pin description

Figure 2. Pin connection



**Table 2. Pin description**

| Pin# | Name              | Function                                                                                                       |
|------|-------------------|----------------------------------------------------------------------------------------------------------------|
| 1    | Vdd_IO            | Power supply for I/O pins                                                                                      |
| 2    | GND               | 0V supply                                                                                                      |
| 3    | Reserved          | Connect to Vdd                                                                                                 |
| 4    | GND               | 0V supply                                                                                                      |
| 5    | GND               | 0V supply                                                                                                      |
| 6    | Vdd               | Power supply                                                                                                   |
| 7    | CS                | SPI enable<br>I <sup>2</sup> C/SPI mode selection (1: I <sup>2</sup> C mode; 0: SPI enabled)                   |
| 8    | INT 1             | Inertial interrupt 1                                                                                           |
| 9    | INT 2             | Inertial interrupt 2                                                                                           |
| 10   | GND               | 0V supply                                                                                                      |
| 11   | Reserved          | Connect to Gnd                                                                                                 |
| 12   | SDO               | SPI Serial data output<br>I <sup>2</sup> C less significant bit of the device address                          |
| 13   | SDA<br>SDI<br>SDO | I <sup>2</sup> C Serial Data (SDA)<br>SPI Serial Data Input (SDI)<br>3-wire Interface Serial Data Output (SDO) |
| 14   | SCL<br>SPC        | I <sup>2</sup> C Serial Clock (SCL)<br>SPI Serial Port Clock (SPC)                                             |

## 2 Mechanical and electrical specifications

### 2.1 Mechanical characteristics

**Table 3. Mechanical characteristics<sup>(1) (2)</sup>**

| Symbol | Parameter                                               | Test conditions                                                | Min. | Typ. <sup>(3)</sup> | Max. | Unit     |
|--------|---------------------------------------------------------|----------------------------------------------------------------|------|---------------------|------|----------|
| FS     | Measurement range <sup>(4)</sup>                        | FS bit set to 0                                                | ±2.0 | ±2.3                |      | g        |
|        |                                                         | FS bit set to 1                                                | ±8.0 | ±9.2                |      |          |
| So     | Sensitivity                                             | FS bit set to 0                                                | 16.2 | 18                  | 19.8 | mg/digit |
|        |                                                         | FS bit set to 1                                                | 64.8 | 72                  | 79.2 |          |
| TCSO   | Sensitivity change vs temperature                       | FS bit set to 0                                                |      | ±0.01               |      | %/°C     |
| TyOff  | Typical zero-g level offset accuracy <sup>(5),(6)</sup> | FS bit set to 0                                                |      | ±40                 |      | mg       |
|        |                                                         | FS bit set to 1                                                |      | ±60                 |      | mg       |
| TCOff  | Zero-g level change vs temperature                      | Max delta from 25°C                                            |      | ±0.5                |      | mg/°C    |
| Vst    | Self test output change <sup>(7),(8),(9)</sup>          | FS bit set to 0<br>STP bit used<br>X axis<br>Vdd=2.16V to 3.6V | -16  |                     | -3   | LSb      |
|        |                                                         | FS bit set to 0<br>STP bit used<br>Y axis<br>Vdd=2.16V to 3.6V | 3    |                     | 16   | LSb      |
|        |                                                         | FS bit set to 0<br>STP bit used<br>Z axis<br>Vdd=2.16V to 3.6V | 3    |                     | 16   | LSb      |
| BW     | System bandwidth <sup>(10)</sup>                        |                                                                |      | ODR/2               |      | Hz       |
| Top    | Operating temperature range                             |                                                                | -40  |                     | +85  | °C       |
| Wh     | Product weight                                          |                                                                |      | 30                  |      | mgram    |

1. The product is factory calibrated at 2.5V. The device can be used from 2.16V to 3.6V
2. All the parameters are specified @ Vdd=2.5V, T = 25°C unless otherwise noted
3. Typical specifications are not guaranteed
4. Verified by wafer level test and measurement of initial offset and sensitivity
5. Typical zero-g level offset value after MSL3 preconditioning
6. Offset can be eliminated by enabling the built-in high pass filter
7. If STM bit is used values change in sign for all axes
8. Self Test output changes with the power supply. "Self test output change" is defined as  $\text{OUTPUT}[\text{LSb}]_{(\text{Self-test bit on ctrl\_reg1=1})} - \text{OUTPUT}[\text{LSb}]_{(\text{Self-test bit on ctrl\_reg1=0})}$ . 1LSb=4.6g/256 at 8bit representation, ±2.3g Full-Scale
9. Output data reach 99% of final value after 3/ODR when enabling Self-Test mode due to device filtering
10. ODR is output data rate. Refer to [Table 4](#) for specifications

## 2.2 Electrical characteristics

**Table 4. Electrical characteristics<sup>(1) (2)</sup>**

| Symbol | Parameter                              | Test conditions     | Min.       | Typ. <sup>(3)</sup> | Max.       | Unit |
|--------|----------------------------------------|---------------------|------------|---------------------|------------|------|
| Vdd    | Supply voltage                         |                     | 2.16       | 2.5                 | 3.6        | V    |
| Vdd_IO | I/O pins supply voltage <sup>(4)</sup> |                     | 1.71       |                     | Vdd+0.1    | V    |
| Idd    | Supply current                         | T = 25°C, ODR=100Hz |            | 0.3                 | 0.4        | mA   |
| IddPdn | Current consumption in power-down mode | T = 25°C            |            | 1                   | 5          | μA   |
| VIH    | Digital high level input voltage       |                     | 0.8*Vdd_IO |                     |            | V    |
| VIL    | Digital low level input voltage        |                     |            |                     | 0.2*Vdd_IO | V    |
| VOH    | High level output voltage              |                     | 0.9*Vdd_IO |                     |            | V    |
| VOL    | Low level output voltage               |                     |            |                     | 0.1*Vdd_IO | V    |
| ODR    | Output data rate                       | DR=0                |            | 100                 |            | Hz   |
|        |                                        | DR=1                |            | 400                 |            |      |
| BW     | System bandwidth <sup>(5)</sup>        |                     |            | ODR/2               |            | Hz   |
| Ton    | Turn-on time <sup>(6)</sup>            |                     |            | 3/ODR               |            | s    |
| Top    | Operating temperature range            |                     | -40        |                     | +85        | °C   |

1. The product is factory calibrated at 2.5V. The device can be used from 2.16V to 3.6V
2. All the parameters are specified @ Vdd=2.5V, T= 25°C unless otherwise noted
3. Typical specification are not guaranteed
4. It is possible to remove Vdd maintaining Vdd\_IO without blocking the communication busses, in this condition the measurement chain is powered off.
5. Filter cut-off frequency
6. Time to obtain valid data after exiting Power-Down mode

## 2.3 Communication interface characteristics

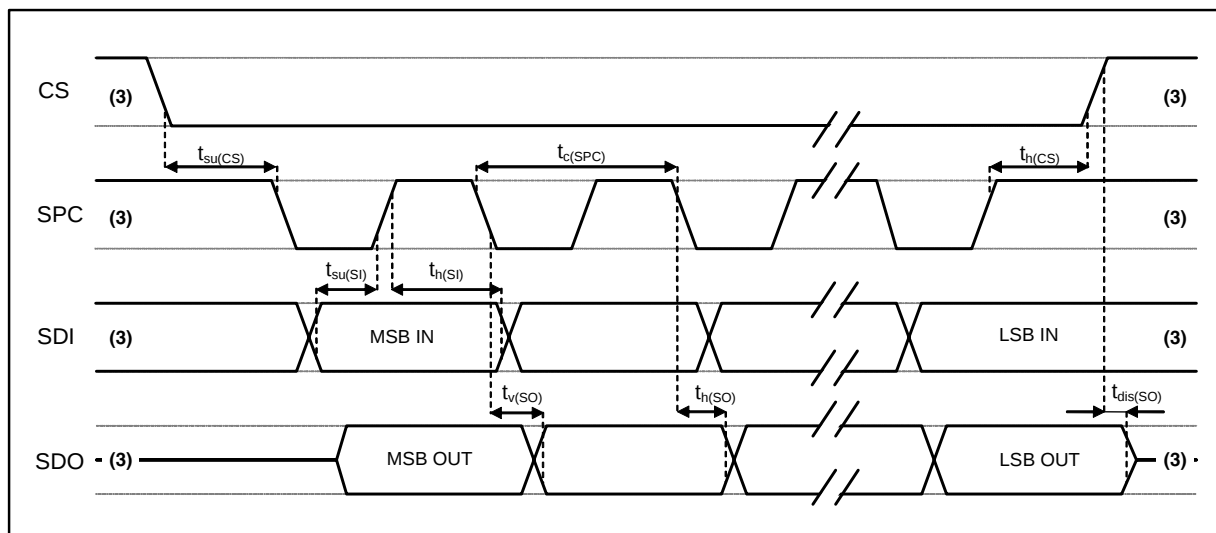
### 2.3.1 SPI - Serial Peripheral Interface

Subject to general operating conditions for Vdd and top.

**Table 5. SPI slave timing values**

| Symbol   | Parameter               | Value <sup>(1)</sup> |     | Unit |
|----------|-------------------------|----------------------|-----|------|
|          |                         | Min                  | Max |      |
| tc(SPC)  | SPI clock cycle         | 100                  |     | ns   |
| fc(SPC)  | SPI clock frequency     |                      | 10  | MHz  |
| tsu(CS)  | CS setup time           | 5                    |     | ns   |
| th(CS)   | CS hold time            | 8                    |     |      |
| tsu(SI)  | SDI input setup time    | 5                    |     |      |
| th(SI)   | SDI input hold time     | 15                   |     |      |
| tv(SO)   | SDO valid output time   |                      | 50  |      |
| th(SO)   | SDO output hold time    | 6                    |     |      |
| tdis(SO) | SDO output disable time |                      | 50  |      |

**Figure 3. SPI slave timing diagram <sup>(2)</sup>**



1. Values are guaranteed at 10MHz clock frequency for SPI with both 4 and 3 wires, based on characterization results, not tested in production
2. Measurement points are done at 0.2·Vdd\_IO and 0.8·Vdd\_IO, for both Input and Output port
3. When no communication is on-going, data on CS, SPC, SDI and SDO are driven by internal pull-up resistors

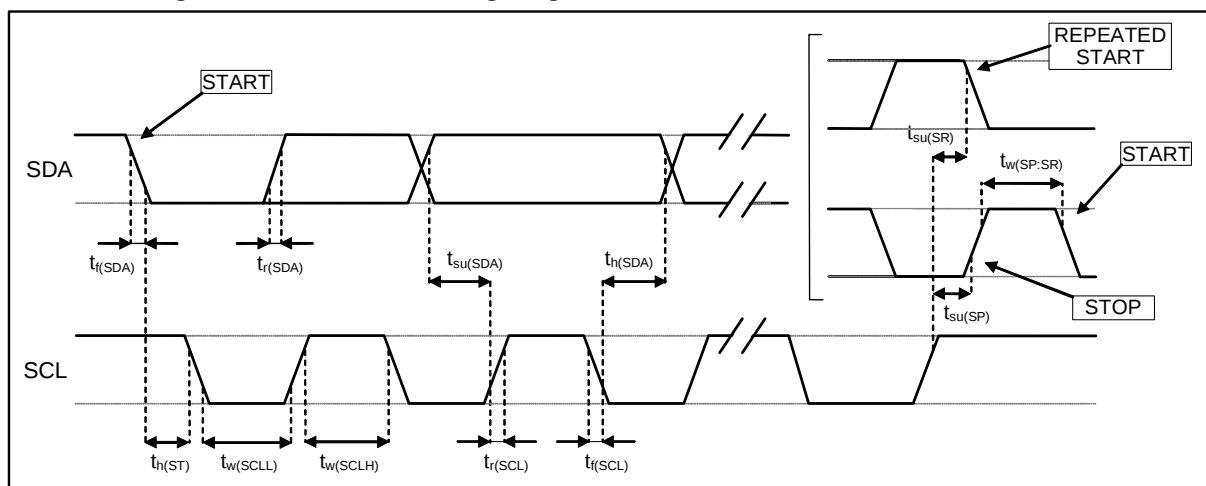
### 2.3.2 I<sup>2</sup>C - inter IC control interface

Subject to general operating conditions for Vdd and top.

**Table 6. I<sup>2</sup>C slave timing values**

| Symbol                                  | Parameter                                      | I <sup>2</sup> C Standard mode <sup>(1)</sup> |                     | I <sup>2</sup> C Fast mode <sup>(1)</sup> |                    | Unit |
|-----------------------------------------|------------------------------------------------|-----------------------------------------------|---------------------|-------------------------------------------|--------------------|------|
|                                         |                                                | Min                                           | Max                 | Min                                       | Max                |      |
| f <sub>(SCL)</sub>                      | SCL clock frequency                            | 0                                             | 100                 | 0                                         | 400                | KHz  |
| t <sub>w(SCLL)</sub>                    | SCL clock low time                             | 4.7                                           |                     | 1.3                                       |                    | μs   |
| t <sub>w(SCLH)</sub>                    | SCL clock high time                            | 4.0                                           |                     | 0.6                                       |                    |      |
| t <sub>su(SDA)</sub>                    | SDA setup time                                 | 250                                           |                     | 100                                       |                    | ns   |
| t <sub>h(SDA)</sub>                     | SDA data hold time                             | 0                                             | 3.45 <sup>(2)</sup> | 0                                         | 0.9 <sup>(2)</sup> | μs   |
| t <sub>r(SDA)</sub> t <sub>r(SCL)</sub> | SDA and SCL rise time                          |                                               | 1000                | 20 + 0.1C <sub>b</sub> <sup>(3)</sup>     | 300                | ns   |
| t <sub>f(SDA)</sub> t <sub>f(SCL)</sub> | SDA and SCL fall time                          |                                               | 300                 | 20 + 0.1C <sub>b</sub> <sup>(3)</sup>     | 300                |      |
| t <sub>h(ST)</sub>                      | START condition hold time                      | 4                                             |                     | 0.6                                       |                    | μs   |
| t <sub>su(SR)</sub>                     | Repeated START condition setup time            | 4.7                                           |                     | 0.6                                       |                    |      |
| t <sub>su(SP)</sub>                     | STOP condition setup time                      | 4                                             |                     | 0.6                                       |                    |      |
| t <sub>w(SP:SR)</sub>                   | Bus free time between STOP and START condition | 4.7                                           |                     | 1.3                                       |                    |      |

**Figure 4. I<sup>2</sup>C slave timing diagram <sup>(4)</sup>**



1. Data based on standard I<sup>2</sup>C protocol requirement, not tested in production
2. A device must internally provide an hold time of at least 300ns for the SDA signal (referred to VIHmin of the SCL signal) to bridge the undefined region of the falling edge of SCL
3. C<sub>b</sub> = total capacitance of one bus line, in pF
4. Measurement points are done at 0.2·Vdd\_IO and 0.8·Vdd\_IO, for both port

## 2.4 Absolute maximum ratings

Stresses above those listed as “absolute maximum ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device under these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

**Table 7. Absolute maximum ratings**

| Symbol             | Ratings                                                        | Maximum Value                   | Unit |
|--------------------|----------------------------------------------------------------|---------------------------------|------|
| V <sub>dd</sub>    | Supply voltage                                                 | -0.3 to 6                       | V    |
| V <sub>dd_IO</sub> | I/O pins supply voltage                                        | -0.3 to 6                       | V    |
| V <sub>in</sub>    | Input voltage on any control pin<br>(CS, SCL/SPC, SDA/SDI/SDO) | -0.3 to V <sub>dd_IO</sub> +0.3 | V    |
| A <sub>POW</sub>   | Acceleration (any axis, powered, V <sub>dd</sub> =2.5V)        | 3000g for 0.5 ms                |      |
|                    |                                                                | 10000g for 0.1 ms               |      |
| A <sub>UNP</sub>   | Acceleration (any axis, unpowered)                             | 3000g for 0.5 ms                |      |
|                    |                                                                | 10000g for 0.1 ms               |      |
| T <sub>OP</sub>    | Operating temperature range                                    | -40 to +85                      | °C   |
| T <sub>STG</sub>   | Storage temperature range                                      | -40 to +125                     | °C   |
| ESD                | Electrostatic discharge protection                             | 4 (HBM)                         | kV   |
|                    |                                                                | 1.5 (CDM)                       | kV   |
|                    |                                                                | 200 (MM)                        | V    |

*Note:* Supply voltage on any pin should never exceed 6.0V



This is a Mechanical Shock sensitive device, improper handling can cause permanent damages to the part



This is an ESD sensitive device, improper handling can cause permanent damages to the part

## 2.5 Terminology

### 2.5.1 Sensitivity

Sensitivity describes the gain of the sensor and can be determined e.g. by applying 1g acceleration to it. As the sensor can measure DC accelerations this can be done easily by pointing the axis of interest towards the center of the Earth, noting the output value, rotating the sensor by 180 degrees (point to the sky) and noting the output value again. By doing so,  $\pm 1g$  acceleration is applied to the sensor. Subtracting the larger output value from the smaller one and dividing the result by 2 leads to the actual sensitivity of the sensor. This value changes very little over temperature and also very little over time. The Sensitivity Tolerance describes the range of Sensitivities of a large population of sensor.

### 2.5.2 Zero-g level

Zero-g level Offset (Off) describes the deviation of an actual output signal from the ideal output signal if there is no acceleration present. A sensor in a steady state on a horizontal surface will measure 0g in X axis and 0g in Y axis whereas the Z axis will measure 1g. The output is ideally in the middle of the dynamic range of the sensor (content of OUT registers 00h, data expressed as 2's complement number). A deviation from ideal value in this case is called Zero-g offset. Offset is to some extent a result of stress to a precise MEMS sensor and therefore the offset can slightly change after mounting the sensor onto a printed circuit board or exposing it to extensive mechanical stress. Offset changes little over temperature, see "Zero-g level change vs. temperature". The Zero-g level of an individual sensor is stable over lifetime. The Zero-g level tolerance describes the range of Zero-g levels of a population of sensors.

### 2.5.3 Self test

Self Test allows to check the sensor functionality without moving it. The Self Test function is off when the self-test bit of CTRL\_REG1 (control register 1) is programmed to '0'. When the self-test bit of ctrl\_reg1 is programmed to '1' an actuation force is applied to the sensor, simulating a definite input acceleration. In this case the sensor outputs will exhibit a change in their DC levels which is related to the selected full scale through the device sensitivity. When Self Test is activated, the device output level is given by the algebraic sum of the signals produced by the acceleration acting on the sensor and by the electrostatic test-force. If the output signals change within the amplitude specified inside [Table 3](#), then the sensor is working properly and the parameters of the interface chip are within the defined specification.

### 2.5.4 Click and Double Click recognition

The Click and Double Click recognition functions help to create man-machine interface with little software overload. The device can be configured to output an interrupt signal on dedicated pin when tapped in any direction.

If the sensor is exposed to a single input stimulus it generates an interrupt request on inertial interrupt pin (INT1 and/or INT2). A more advanced feature allows to generate an interrupt request when a "double click" with programmable time between the two events enabling a "mouse button like" use.

This function can be fully programmed by the user in terms of expected amplitude and timing of the stimuli.

## 3 Functionality

The LIS302DL is a ultracompact, low-power, digital output 3-axis linear accelerometer packaged in a LGA package. The complete device includes a sensing element and an IC interface able to take the information from the sensing element and to provide a signal to the external world through an I<sup>2</sup>C/SPI serial interface.

### 3.1 Sensing element

A proprietary process is used to create a surface micro-machined accelerometer. The technology allows to carry out suspended silicon structures which are attached to the substrate in a few points called anchors and are free to move in the direction of the sensed acceleration. To be compatible with the traditional packaging techniques a cap is placed on top of the sensing element to avoid blocking the moving parts during the moulding phase of the plastic encapsulation.

When an acceleration is applied to the sensor the proof mass displaces from its nominal position, causing an imbalance in the capacitive half-bridge. This imbalance is measured using charge integration in response to a voltage pulse applied to the sense capacitor.

At steady state the nominal value of the capacitors are few pF and when an acceleration is applied the maximum variation of the capacitive load is in fF range.

### 3.2 IC interface

The complete measurement chain is composed by a low-noise capacitive amplifier which converts into an analog voltage the capacitive unbalancing of the MEMS sensor and by analog-to-digital converters.

The acceleration data may be accessed through an I<sup>2</sup>C/SPI interface thus making the device particularly suitable for direct interfacing with a microcontroller.

The LIS302DL features a Data-Ready signal (RDY) which indicates when a new set of measured acceleration data is available thus simplifying data synchronization in the digital system that uses the device.

The LIS302DL may also be configured to generate an inertial Wake-Up and Free-Fall interrupt signal accordingly to a programmed acceleration event along the enabled axes. Both Free-Fall and Wake-Up can be available simultaneously on two different pins.

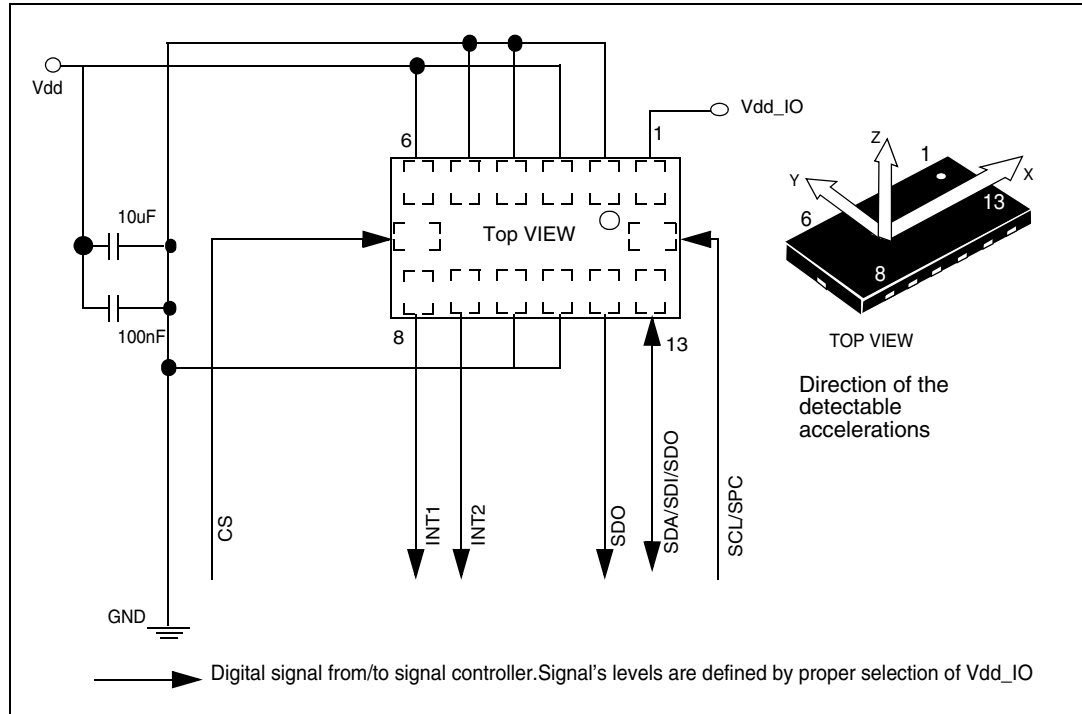
### 3.3 Factory calibration

The IC interface is factory calibrated for sensitivity (So) and Zero-g level (Off).

The trimming values are stored inside the device by a non volatile memory. Any time the device is turned on, the trimming parameters are downloaded into the registers to be used during the normal operation. This allows the user to use the device without further calibration.

## 4 Application hints

**Figure 5. LIS302DL electrical connection**



The device core is supplied through Vdd line while the I/O pads are supplied through Vdd\_IO line. Power supply decoupling capacitors (100 nF ceramic, 10 µF Al) should be placed as near as possible to the pin 6 of the device (common design practice).

All the voltage and ground supplies must be present at the same time to have proper behavior of the IC (refer to [Figure 5](#)). It is possible to remove Vdd maintaining Vdd\_IO without blocking the communication busses, in this condition the measurement chain is powered off.

The functionality of the device and the measured acceleration data is selectable and accessible through the I<sup>2</sup>C/SPI interface. When using the I<sup>2</sup>C, CS must be tied high.

The functions, the threshold the timing of the two interrupt pins (INT 1 and INT 2) can be completely programmed by the user through the I<sup>2</sup>C/SPI interface.

### 4.1 Soldering information

The LGA package is compliant with the ECOPACK, RoHS and “Green” standard. It is qualified for soldering heat resistance according to JEDEC J-STD-020C.

Leave “Pin#1 indicator” unconnected during soldering.

Land pattern and soldering recommendation are available at [www.st.com/mems](http://www.st.com/mems)

## 5 Digital interfaces

The registers embedded inside the LIS302DL may be accessed through both the I<sup>2</sup>C and SPI serial interfaces. The latter may be SW configured to operate either in 3-wire or 4-wire interface mode.

The serial interfaces are mapped onto the same pads. To select/exploit the I<sup>2</sup>C interface, CS line must be tied high (i.e connected to Vdd\_IO).

**Table 8. Serial interface pin description**

| Pin name    | PIN description                                                                                                |
|-------------|----------------------------------------------------------------------------------------------------------------|
| CS          | SPI enable<br>I <sup>2</sup> C/SPI mode selection (1: I <sup>2</sup> C mode; 0: SPI enabled)                   |
| SCL/SPC     | I <sup>2</sup> C Serial Clock (SCL)<br>SPI Serial Port Clock (SPC)                                             |
| SDA/SDI/SDO | I <sup>2</sup> C Serial Data (SDA)<br>SPI Serial Data Input (SDI)<br>3-wire Interface Serial Data Output (SDO) |
| SDO         | SPI Serial Data Output (SDO)                                                                                   |

### 5.1 I<sup>2</sup>C serial interface

The LIS302DL I<sup>2</sup>C is a bus slave. The I<sup>2</sup>C is employed to write the data into the registers whose content can also be read back.

The relevant I<sup>2</sup>C terminology is given in the table below.

**Table 9. Serial interface pin description**

| Term        | Description                                                                              |
|-------------|------------------------------------------------------------------------------------------|
| Transmitter | The device which sends data to the bus                                                   |
| Receiver    | The device which receives data from the bus                                              |
| Master      | The device which initiates a transfer, generates clock signals and terminates a transfer |
| Slave       | The device addressed by the master                                                       |

There are two signals associated with the I<sup>2</sup>C bus: the Serial Clock Line (SCL) and the Serial DATA line (SDA). The latter is a bidirectional line used for sending and receiving the data to/from the interface. Both the lines are connected to Vdd\_IO through a pull-up resistor embedded inside the LIS302DL. When the bus is free both the lines are high.

The I<sup>2</sup>C interface is compliant with Fast Mode (400 kHz) I<sup>2</sup>C standards as well as the normal mode.

### 5.1.1 I<sup>2</sup>C operation

The transaction on the bus is started through a START (ST) signal. A START condition is defined as a HIGH to LOW transition on the data line while the SCL line is held HIGH. After this has been transmitted by the Master, the bus is considered busy. The next byte of data transmitted after the start condition contains the address of the slave in the first 7 bits and the eighth bit tells whether the Master is receiving data from the slave or transmitting data to the slave. When an address is sent, each device in the system compares the first seven bits after a start condition with its address. If they match, the device considers itself addressed by the master.

The Slave Address (SAD) associated to the LIS302DL is 001110xb. **SDO** pad can be used to modify less significant bit of the device address. If SDO pad is connected to voltage supply LSb is '1' (address 0011101b) else if SDO pad is connected to ground LSb value is '0' (address 0011100b). This solution permits to connect and address two different accelerometer to the same I<sup>2</sup>C lines.

Data transfer with acknowledge is mandatory. The transmitter must release the SDA line during the acknowledge pulse. The receiver must then pull the data line LOW so that it remains stable low during the HIGH period of the acknowledge clock pulse. A receiver which has been addressed is obliged to generate an acknowledge after each byte of data has been received.

The I<sup>2</sup>C embedded inside the LIS302DL behaves like a slave device and the following protocol must be adhered to. After the start condition (ST) a slave address is sent, once a slave acknowledge (SAK) has been returned, a 8-bit sub-address will be transmitted: the 7 LSb represent the actual register address while the MSB enables address auto increment. If the MSb of the SUB field is 1, the SUB (register address) will be automatically incremented to allow multiple data read/write.

The slave address is completed with a Read/Write bit. If the bit was '1' (Read), a repeated START (SR) condition will have to be issued after the two sub-address bytes; if the bit is '0' (Write) the Master will transmit to the slave with direction unchanged. [Table 10](#) explain how the SAD+read/write bit pattern is composed, listing all the possible configurations.

**Table 10. SAD+read/write patterns**

| Command | SAD[6:1] | SAD[0] = SDO | R/W | SAD+R/W        |
|---------|----------|--------------|-----|----------------|
| Read    | 001110   | 0            | 1   | 00111001 (39h) |
| Write   | 001110   | 0            | 0   | 00111000 (38h) |
| Read    | 001110   | 1            | 1   | 00111011 (3Bh) |
| Write   | 001110   | 1            | 0   | 00111010 (3Ah) |

**Table 11. Transfer when master is writing one byte to slave**

|        |    |         |     |     |     |      |     |    |
|--------|----|---------|-----|-----|-----|------|-----|----|
| Master | ST | SAD + W |     | SUB |     | DATA |     | SP |
| Slave  |    |         | SAK |     | SAK |      | SAK |    |

**Table 12. Transfer when Master is writing multiple bytes to slave**

|        |    |         |     |     |     |      |     |      |     |    |
|--------|----|---------|-----|-----|-----|------|-----|------|-----|----|
| Master | ST | SAD + W |     | SUB |     | DATA |     | DATA |     | SP |
| Slave  |    |         | SAK |     | SAK |      | SAK |      | SAK |    |

**Table 13. Transfer when master is receiving (reading) one byte of data from slave**

|        |    |         |     |     |     |    |         |     |      |      |    |
|--------|----|---------|-----|-----|-----|----|---------|-----|------|------|----|
| Master | ST | SAD + W |     | SUB |     | SR | SAD + R |     |      | NMAK | SP |
| Slave  |    |         | SAK |     | SAK |    |         | SAK | DATA |      |    |

**Table 14. Transfer when master is receiving (reading)**

|        |    |         |     |     |     |    |         |     |      |     |
|--------|----|---------|-----|-----|-----|----|---------|-----|------|-----|
| Master | ST | SAD + W |     | SUB |     | SR | SAD + R |     |      | MAK |
| Slave  |    |         | SAK |     | SAK |    |         | SAK | DATA |     |

**Table 15. Multiple bytes of data from slave**

|        |      |     |      |      |    |
|--------|------|-----|------|------|----|
| Master |      | MAK |      | NMAK | SP |
| Slave  | DATA |     | DATA |      |    |

Data are transmitted in byte format (DATA). Each data transfer contains 8 bits. The number of bytes transferred per transfer is unlimited. Data is transferred with the most significant bit (MSb) first. If a receiver can't receive another complete byte of data until it has performed some other function, it can hold the clock line, SCL LOW to force the transmitter into a wait state. Data transfer only continues when the receiver is ready for another byte and releases the data line. If a slave receiver doesn't acknowledge the slave address (i.e. it is not able to receive because it is performing some real time function) the data line must be left HIGH by the slave. The Master can then abort the transfer. A LOW to HIGH transition on the SDA line while the SCL line is HIGH is defined as a STOP condition. Each data transfer must be terminated by the generation of a STOP (SP) condition.

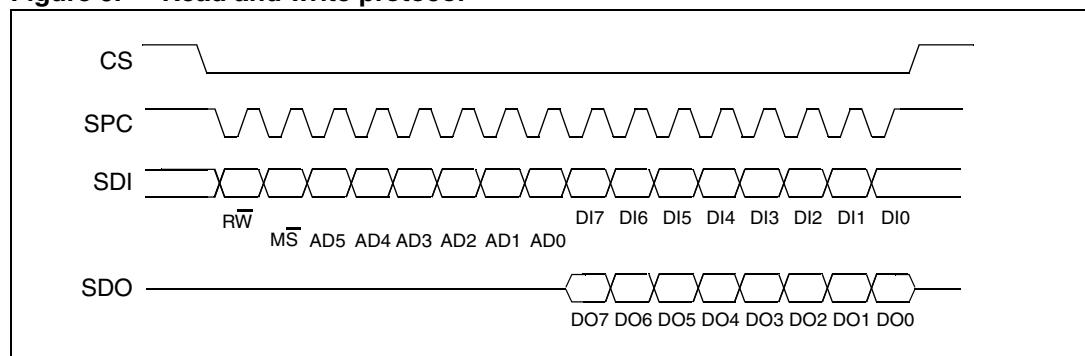
In order to read multiple bytes, it is necessary to assert the most significant bit of the sub-address field. In other words, SUB(7) must be equal to 1 while SUB(6-0) represents the address of first register to read.

In the presented communication format MAK is Master Acknowledge and NMAK is No Master Acknowledge.

## 5.2 SPI bus interface

The LIS302DL SPI is a bus slave. The SPI allows to write and read the registers of the device.

The Serial Interface interacts with the outside world with 4 wires: **CS**, **SPC**, **SDI** and **SDO**.

**Figure 6. Read and write protocol**

**CS** is the serial port enable and it is controlled by the SPI master. It goes low at the start of the transmission and goes back high at the end. **SPC** is the Serial Port Clock and it is controlled by the SPI master. It is stopped high when **CS** is high (no transmission). **SDI** and **SDO** are respectively the Serial Port Data Input and Output. Those lines are driven at the falling edge of **SPC** and should be captured at the rising edge of **SPC**.

Both the Read Register and Write Register commands are completed in 16 clock pulses or in multiple of 8 in case of multiple byte read/write. Bit duration is the time between two falling edges of **SPC**. The first bit (bit 0) starts at the first falling edge of **SPC** after the falling edge of **CS** while the last bit (bit 15, bit 23, ...) starts at the last falling edge of **SPC** just before the rising edge of **CS**.

**bit 0:**  $\overline{RW}$  bit. When 0, the data DI(7:0) is written into the device. When 1, the data DO(7:0) from the device is read. In latter case, the chip will drive **SDO** at the start of bit 8.

**bit 1:**  $\overline{MS}$  bit. When 0, the address will remain unchanged in multiple read/write commands. When 1, the address will be auto incremented in multiple read/write commands.

**bit 2-7:** address AD(5:0). This is the address field of the indexed register.

**bit 8-15:** data DI(7:0) (write mode). This is the data that will be written into the device (MSb first).

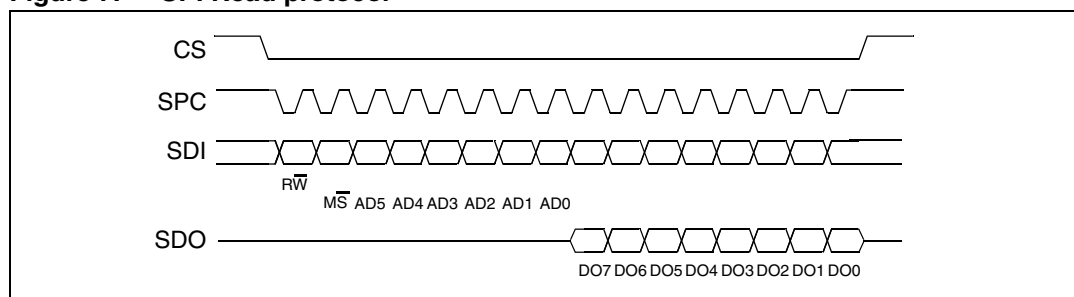
**bit 8-15:** data DO(7:0) (read mode). This is the data that will be read from the device (MSb first).

In multiple read/write commands further blocks of 8 clock periods will be added. When  $\overline{MS}$  bit is 0 the address used to read/write data remains the same for every block. When  $\overline{MS}$  bit is 1 the address used to read/write data is incremented at every block.

The function and the behavior of **SDI** and **SDO** remain unchanged.

### 5.2.1 SPI Read

Figure 7. SPI Read protocol



The SPI Read command is performed with 16 clock pulses. Multiple byte read command is performed adding blocks of 8 clock pulses at the previous one.

**bit 0:** READ bit. The value is 1.

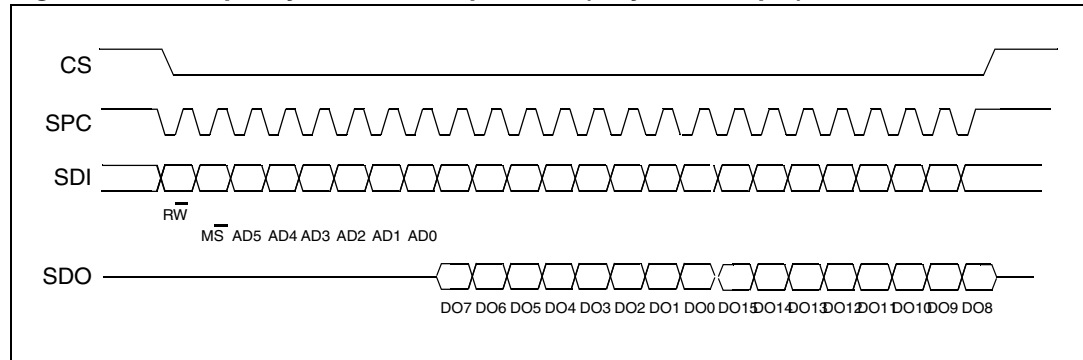
**bit 1:**  $\overline{MS}$  bit. When 0 do not increment address, when 1 increment address in multiple reading.

**bit 2-7:** address AD(5:0). This is the address field of the indexed register.

**bit 8-15:** data DO(7:0) (read mode). This is the data that will be read from the device (MSb first).

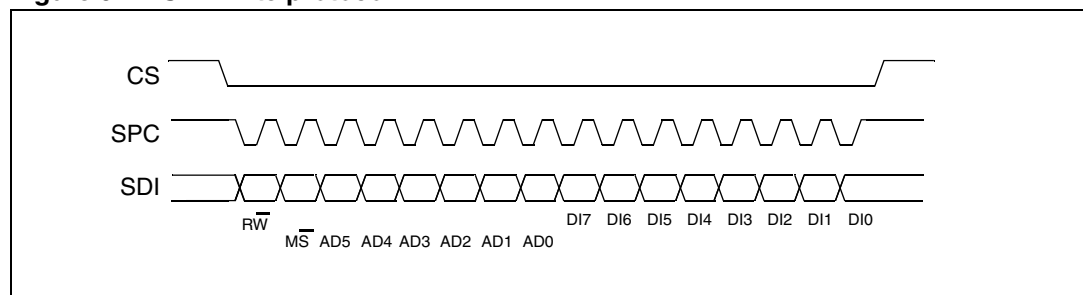
**bit 16-...** : data DO(...-8). Further data in multiple byte reading.

**Figure 8. Multiple bytes SPI Read protocol (2 bytes example)**



## 5.2.2 SPI Write

**Figure 9. SPI Write protocol**



The SPI Write command is performed with 16 clock pulses. Multiple byte write command is performed adding blocks of 8 clock pulses at the previous one.

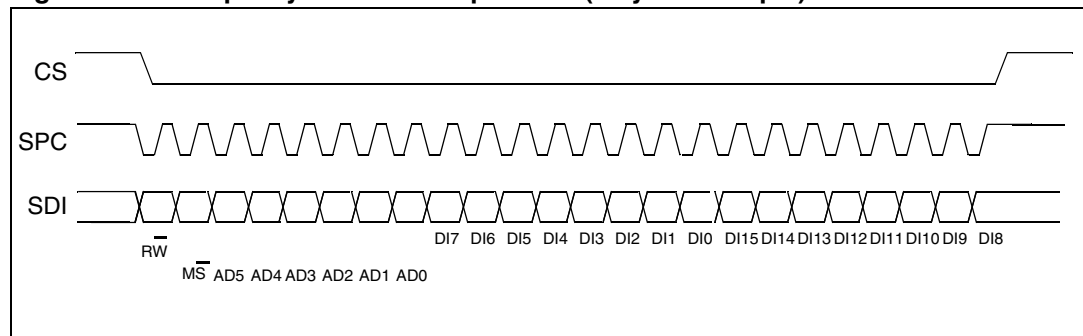
**bit 0:** WRITE bit. The value is 0.

**bit 1:**  $\overline{MS}$  bit. When 0 do not increment address, when 1 increment address in multiple writing.

**bit 2-7:** address AD(5:0). This is the address field of the indexed register.

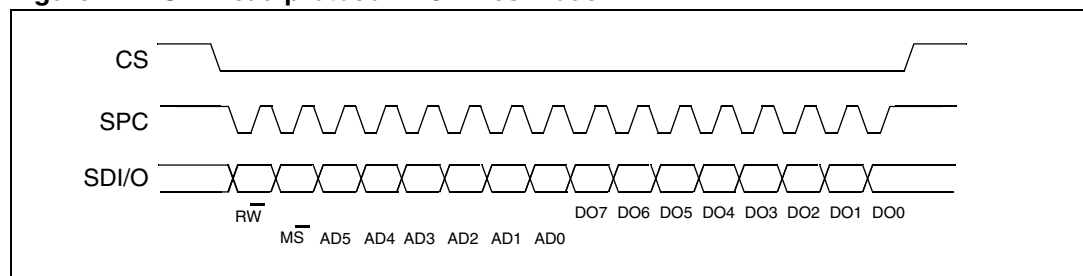
**bit 8-15:** data DI(7:0) (write mode). This is the data that will be written inside the device (MSb first).

**bit 16-...** : data DI(...-8). Further data in multiple byte writing.

**Figure 10. Multiple bytes SPI Write protocol (2 bytes example)**

### 5.2.3 SPI Read in 3-wires mode

3-wires mode is entered by setting to 1 bit SIM (SPI Serial Interface Mode selection) in CTRL\_REG2.

**Figure 11. SPI Read protocol in 3-wires mode**

The SPI Read command is performed with 16 clock pulses:

**bit 0:** READ bit. The value is 1.

**bit 1:**  $\overline{MS}$  bit. When 0 do not increment address, when 1 increment address in multiple reading.

**bit 2-7:** address AD(5:0). This is the address field of the indexed register.

**bit 8-15:** data DO(7:0) (read mode). This is the data that will be read from the device (MSb first).

Multiple read command is also available in 3-wires mode.

## 6 Register mapping

The table given below provides a listing of the 8 bit registers embedded in the device and the related address:

**Table 16. Register address map**

| Name                     | Type | Register address |          | Default  | Comment        |
|--------------------------|------|------------------|----------|----------|----------------|
|                          |      | Hex              | Binary   |          |                |
| Reserved (do not modify) |      | 00-0E            |          |          | Reserved       |
| Who_Am_I                 | r    | 0F               | 000 1111 | 00111011 | Dummy register |
| Reserved (do not modify) |      | 10-1F            |          |          | Reserved       |
| Ctrl_Reg1                | rw   | 20               | 010 0000 | 00000111 |                |
| Ctrl_Reg2                | rw   | 21               | 010 0001 | 00000000 |                |
| Ctrl_Reg3                | rw   | 22               | 010 0010 | 00000000 |                |
| HP_filter_reset          | r    | 23               | 010 0011 | dummy    | Dummy register |
| Reserved (do not modify) |      | 24-26            |          |          | Reserved       |
| Status_Reg               | r    | 27               | 010 0111 | 00000000 |                |
| --                       | r    | 28               | 010 1000 |          | Not used       |
| OutX                     | r    | 29               | 010 1001 | output   |                |
| --                       | r    | 2A               | 010 1010 |          | Not used       |
| OutY                     | r    | 2B               | 010 1011 | output   |                |
| --                       | r    | 2C               | 010 1100 |          | Not used       |
| OutZ                     | r    | 2D               | 010 1101 | output   |                |
| Reserved (do not modify) |      | 2E-2F            |          |          | Reserved       |
| FF_WU_CFG_1              | rw   | 30               | 011 0000 | 00000000 |                |
| FF_WU_SRC_1(ack1)        | r    | 31               | 011 0001 | 00000000 |                |
| FF_WU_THS_1              | rw   | 32               | 011 0010 | 00000000 |                |
| FF_WU_DURATION_1         | rw   | 33               | 011 0011 | 00000000 |                |
| FF_WU_CFG_2              | rw   | 34               | 011 0100 | 00000000 |                |
| FF_WU_SRC_2 (ack2)       | r    | 35               | 011 0101 | 00000000 |                |
| FF_WU_THS_2              | rw   | 36               | 011 0110 | 00000000 |                |
| FF_WU_DURATION_2         | rw   | 37               | 011 0111 | 00000000 |                |
| CLICK_CFG                | rw   | 38               | 011 1000 | 00000000 |                |
| CLICK_SRC (ack)          | r    | 39               | 011 1001 | 00000000 |                |
| --                       |      | 3A               |          |          | Not used       |
| CLICK_THSY_X             | rw   | 3B               | 011 1011 | 00000000 |                |
| CLICK_THSZ               | rw   | 3C               | 011 1100 | 00000000 |                |

**Table 16. Register address map (continued)**

| Name            | Type | Register address |          | Default  | Comment |
|-----------------|------|------------------|----------|----------|---------|
|                 |      | Hex              | Binary   |          |         |
| CLICK_timelimit | rw   | 3D               | 011 1101 | 00000000 |         |
| CLICK_latency   | rw   | 3E               | 011 1110 | 00000000 |         |
| CLICK_window    | rw   | 3F               | 011 1111 | 00000000 |         |

Registers marked as Reserved must not be changed. The writing to those registers may cause permanent damages to the device.

The content of the registers that are loaded at boot should not be changed. They contain the factory calibration values. Their content is automatically restored when the device is powered-up.

## 7 Register description

The device contains a set of registers which are used to control its behavior and to retrieve acceleration data. The registers address, made of 7 bits, is used to identify them and to write the data through serial interface.

### 7.1 WHO\_AM\_I (0Fh)

**Table 17. Register**

|   |   |   |   |   |   |   |   |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 1 | 1 | 1 | 0 | 1 | 1 |
|---|---|---|---|---|---|---|---|

Device identification register. This register contains the device identifier that for LIS302DL is set to 3Bh.

### 7.2 CTRL\_REG1 (20h)

**Table 18. Register**

|    |    |    |     |     |     |     |     |
|----|----|----|-----|-----|-----|-----|-----|
| DR | PD | FS | STP | STM | Zen | Yen | Xen |
|----|----|----|-----|-----|-----|-----|-----|

**Table 19. Register description**

|          |                                                                                                           |
|----------|-----------------------------------------------------------------------------------------------------------|
| DR       | Data rate selection. Default value: 0<br>(0: 100 Hz output data rate; 1: 400 Hz output data rate)         |
| PD       | Power Down Control. Default value: 0<br>(0: power down mode; 1: active mode)                              |
| FS       | Full Scale selection. Default value: 0<br>(refer to <a href="#">Table 3</a> for typical full scale value) |
| STP, STM | Self Test Enable. Default value: 0<br>(0: normal mode; 1: self test P, M enabled)                         |
| Zen      | Z axis enable. Default value: 1<br>(0: Z axis disabled; 1: Z axis enabled)                                |
| Yen      | Y axis enable. Default value: 1<br>(0: Y axis disabled; 1: Y axis enabled)                                |
| Xen      | X axis enable. Default value: 1<br>(0: X axis disabled; 1: X axis enabled)                                |

**DR** bit allows to select the data rate at which acceleration samples are produced. The default value is 0 which corresponds to a data-rate of 100Hz. By changing the content of DR to "1" the selected data-rate will be set equal to 400Hz.

**PD** bit allows to turn on the turn the device out of power-down mode. The device is in power-down mode when PD= "0" (default value after boot). The device is in normal mode when PD is set to 1.

**STP, STM** bit is used to activate the self test function. When the bit is set to one, an output change will occur to the device outputs (refer to [Table 3](#) and [4](#) for specification) thus allowing to check the functionality of the whole measurement chain.

**Zen** bit enables the generation of Data Ready signal for Z-axis measurement channel when set to 1. The default value is 1.

**Yen** bit enables the generation of Data Ready signal for Y-axis measurement channel when set to 1. The default value is 1.

**Xen** bit enables the generation of Data Ready signal for X-axis measurement channel when set to 1. The default value is 1.

## 7.3 CTRL\_REG2 (21h)

**Table 20. Register**

|     |      |    |     |               |               |           |           |
|-----|------|----|-----|---------------|---------------|-----------|-----------|
| SIM | BOOT | -- | FDS | HP_FF_W<br>U2 | HP_FF_W<br>U1 | HP_coeff2 | HP_coeff1 |
|-----|------|----|-----|---------------|---------------|-----------|-----------|

**Table 21. Register description**

|                        |                                                                                                                                  |
|------------------------|----------------------------------------------------------------------------------------------------------------------------------|
| SIM                    | SPI Serial Interface Mode selection. Default value: 0<br>(0: 4-wire interface; 1: 3-wire interface)                              |
| BOOT                   | Reboot memory content. Default value: 0<br>(0: normal mode; 1: reboot memory content)                                            |
| FDS                    | Filtered Data Selection. Default value: 0<br>(0: internal filter bypassed; 1: data from internal filter sent to output register) |
| HP_FF_WU2              | High Pass filter enabled for FreeFall/WakeUp # 2. Default value: 0<br>(0: filter bypassed; 1: filter enabled)                    |
| HPFF_WU1               | High Pass filter enabled for Free-Fall/Wake-Up #1. Default value: 0<br>(0: filter bypassed; 1: filter enabled)                   |
| HP_coeff2<br>HP_coeff1 | High pass filter cut-off frequency configuration. Default value: 00<br>(See table below)                                         |

**SIM** bit selects the SPI Serial Interface Mode. When SIM is '0' (default value) the 4-wire interface mode is selected. The data coming from the device are sent to SDO pad. In 3-wire interface mode output data are sent to SDA\_SDI pad.

**BOOT** bit is used to refresh the content of internal registers stored in the flash memory block. At the device power up the content of the flash memory block is transferred to the internal registers related to trimming functions to permit a good behavior of the device itself. If for any reason the content of trimming registers was changed it is sufficient to use this bit to restore correct values. When BOOT bit is set to '1' the content of internal flash is copied inside corresponding internal registers and it is used to calibrate the device. These values are factory trimmed and they are different for every accelerometer. They permit a good behavior of the device and normally they have not to be changed. At the end of the boot process the BOOT bit is set again to '0'.

**FDS** bit enables (FDS=1) or bypass (FDS=0) the high pass filter in the signal chain of the sensor

**HP\_coeff[2:1]**. These bits are used to configure high-pass filter cut-off frequency ft.

**Table 22. High pass filter cut-off frequency configuration.**

| HP_coeff2,1 | ft (Hz)<br>(DR=100 Hz) | ft (Hz)<br>(DR=400 Hz) |
|-------------|------------------------|------------------------|
| 00          | 2                      | 8                      |
| 01          | 1                      | 4                      |
| 10          | 0.5                    | 2                      |
| 11          | 0.25                   | 1                      |

## 7.4 CTRL\_REG3 [Interrupt CTRL register] (22h)

**Table 23. Register**

| IHL | PP_OD | I2CFG2 | I2CFG1 | I2CFG0 | I1CFG2 | I1CFG1 | I1CFG0 |
|-----|-------|--------|--------|--------|--------|--------|--------|
|-----|-------|--------|--------|--------|--------|--------|--------|

**Table 24. Register description**

|                            |                                                                                                    |
|----------------------------|----------------------------------------------------------------------------------------------------|
| IHL                        | Interrupt active high, low. Default value 0.<br>(0: active high; 1: active low)                    |
| PP_OD                      | Push-pull/Open Drain selection on interrupt pad. Default value 0.<br>(0: push-pull; 1: open drain) |
| I2CFG2<br>I2CFG1<br>I2CFG0 | Data Signal on Int2 pad control bits. Default value 000.<br>(see table below)                      |
| I1CFG2<br>I1CFG1<br>I1CFG0 | Data Signal on Int1 pad control bits. Default value 000.<br>(see table below)                      |

**Table 25. Truth table**

| I1(2)_CFG2 | I1(2)_CFG1 | I1(2)_CFG0 | Int1(2) Pad        |
|------------|------------|------------|--------------------|
| 0          | 0          | 0          | GND                |
| 0          | 0          | 1          | FF_WU_1            |
| 0          | 1          | 0          | FF_WU_2            |
| 0          | 1          | 1          | FF_WU_1 or FF_WU_2 |
| 1          | 0          | 0          | Data ready         |
| 1          | 1          | 1          | Click interrupt    |

## 7.5 HP\_FILTER\_RESET (23h)

Dummy register. Reading at this address zeroes instantaneously the content of the internal high pass-filter. If the high pass filter is enabled all three axes are instantaneously set to 0g. This allows to overcome the settling time of the high pass filter.

## 7.6 STATUS\_REG (27h)

**Table 26. Register**

|       |     |     |     |       |     |     |     |
|-------|-----|-----|-----|-------|-----|-----|-----|
| ZXYOR | ZOR | YOR | XOR | ZYXDA | ZDA | YDA | XDA |
|-------|-----|-----|-----|-------|-----|-----|-----|

**Table 27. Register description**

|       |                                                                                                                                                     |
|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------|
| ZXYOR | X, Y and Z axis data overrun. Default value: 0<br>(0: no overrun has occurred;<br>1: new data has over written the previous one before it was read) |
| ZOR   | Z axis data overrun. Default value: 0<br>(0: no overrun has occurred;<br>1: a new data for the Z-axis has overwritten the previous one)             |
| YOR   | Y axis data overrun. Default value: 0<br>(0: no overrun has occurred;<br>1: a new data for the Y-axis has overwritten the previous one)             |
| XOR   | X axis data overrun. Default value: 0<br>(0: no overrun has occurred;<br>1: a new data for the X-axis has overwritten the previous one)             |
| ZYXDA | X, Y and Z axis new data available. Default value: 0<br>(0: a new set of data is not yet available; 1: a new set of data is available)              |
| ZDA   | Z axis new data available. Default value: 0<br>(0: a new data for the Z-axis is not yet available;<br>1: a new data for the Z-axis is available)    |
| YDA   | Y axis new data available. Default value: 0<br>(0: a new data for the Y-axis is not yet available;<br>1: a new data for the Y-axis is available)    |
| XDA   | X axis new data available. Default value: 0<br>(0: a new data for the X-axis is not yet available;<br>1: a new data for the X-axis is available)    |

## 7.7 OUT\_X (29h)

**Table 28. Register**

|     |     |     |     |     |     |     |     |
|-----|-----|-----|-----|-----|-----|-----|-----|
| XD7 | XD6 | XD5 | XD4 | XD3 | XD2 | XD1 | XD0 |
|-----|-----|-----|-----|-----|-----|-----|-----|

X axis output data.

## 7.8 OUT\_Y (2Bh)

**Table 29. Register description**

|     |     |     |     |     |     |     |     |
|-----|-----|-----|-----|-----|-----|-----|-----|
| YD7 | YD6 | YD5 | YD4 | YD3 | YD2 | YD1 | YD0 |
|-----|-----|-----|-----|-----|-----|-----|-----|

Y axis output data.

## 7.9 OUT\_Z (2Dh)

**Table 30. Register**

| ZD7 | ZD6 | ZD5 | ZD4 | ZD3 | ZD2 | ZD1 | ZD0 |
|-----|-----|-----|-----|-----|-----|-----|-----|
|-----|-----|-----|-----|-----|-----|-----|-----|

Z axis output data.

## 7.10 FF\_WU\_CFG\_1 (30h)

**Table 31. Register**

| AOI | LIR | ZHIE | ZLIE | YHIE | YLIE | XHIE | XLIE |
|-----|-----|------|------|------|------|------|------|
|-----|-----|------|------|------|------|------|------|

**Table 32. Register description**

|      |                                                                                                                                                                                            |
|------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| AOI  | And/or combination of Interrupt events. Default value: 0<br>(0: OR combination of interrupt events; 1: AND combination of interrupt events)                                                |
| LIR  | Latch Interrupt request into FF_WU_SRC reg with the FF_WU_SRC reg cleared by reading FF_WU_SRC_1 reg. Default value: 0<br>(0: interrupt request not latched; 1: interrupt request latched) |
| ZHIE | Enable interrupt generation on Z high event. Default value: 0<br>(0: disable interrupt request;<br>1: enable interrupt request on measured accel. value higher than preset threshold)      |
| ZLIE | Enable interrupt generation on Z low event. Default value: 0<br>(0: disable interrupt request;<br>1: enable interrupt request on measured accel. value lower than preset threshold)        |
| YHIE | Enable interrupt generation on Y high event. Default value: 0<br>(0: disable interrupt request;<br>1: enable interrupt request on measured accel. value higher than preset threshold)      |
| YLIE | Enable interrupt generation on Y low event. Default value: 0<br>(0: disable interrupt request;<br>1: enable interrupt request on measured accel. value lower than preset threshold)        |
| XHIE | Enable interrupt generation on X high event. Default value: 0<br>(0: disable interrupt request;<br>1: enable interrupt request on measured accel. value higher than preset threshold)      |
| XLIE | Enable interrupt generation on X low event. Default value: 0<br>(0: disable interrupt request;<br>1: enable interrupt request on measured accel. value lower than preset threshold)        |

## 7.11 FF\_WU\_SRC\_1 (31h)

**Table 33. Register**

|   |    |    |    |    |    |    |    |
|---|----|----|----|----|----|----|----|
| X | IA | ZH | ZL | YH | YL | XH | XL |
|---|----|----|----|----|----|----|----|

**Table 34. Register description**

|    |                                                                                                                          |
|----|--------------------------------------------------------------------------------------------------------------------------|
| IA | Interrupt active. Default value: 0<br>(0: no interrupt has been generated; 1: one ore more interrupt has been generated) |
| ZH | Z high. Default value: 0<br>(0: no interrupt, 1: ZH event has occurred)                                                  |
| ZL | Z low. Default value: 0<br>(0: no interrupt; 1: ZL event has occurred)                                                   |
| YH | Y high. Default value: 0<br>(0: no interrupt, 1: YH event has occurred)                                                  |
| YL | Y low. Default value: 0<br>(0: no interrupt, 1: YL event has occurred)                                                   |
| XH | X high. Default value: 0<br>(0: no interrupt, 1: XH event has occurred)                                                  |
| XL | X low. Default value: 0<br>(0: no interrupt, 1: XL event has occurred)                                                   |

Free-fall and wake-up source register. Read only register.

Reading at this address clears FF\_WU\_SRC\_1 register and the FF, WU 1 interrupt and allows the refreshment of data in the FF\_WU\_SRC\_1 register if the latched option was chosen.

## 7.12 FF\_WU\_THS\_1 (32h)

**Table 35. Register**

|      |      |      |      |      |      |      |      |
|------|------|------|------|------|------|------|------|
| DCRM | THS6 | THS5 | THS4 | THS3 | THS2 | THS1 | THS0 |
|------|------|------|------|------|------|------|------|

**Table 36. Register description**

|            |                                                                                             |
|------------|---------------------------------------------------------------------------------------------|
| DCRM       | Resetting mode selection. Default value: 0<br>(0: counter resetted; 1: counter decremented) |
| THS6, THS0 | Free-fall / wake-up Threshold: default value: 000 0000                                      |

Most significant bit (DCRM) is used to select the resetting mode of the duration counter. If DCRM=0 counter is resetted when the interrupt is no more active else if DCRM=1 duration counter is decremented.

## 7.13 FF\_WU\_DURATION\_1 (33h)

**Table 37. Register**

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|----|----|----|----|----|----|----|----|
|----|----|----|----|----|----|----|----|

**Table 38. Register description**

| D7-D0 | Duration value. Default value: 0000 0000 |
|-------|------------------------------------------|
|-------|------------------------------------------|

Duration register for Free-Fall/Wake-Up interrupt 1. Duration step and maximum value depend on the ODR chosen. Step 2.5 msec, from 0 to 637.5 msec if ODR=400Hz, else step 10 msec, from 0 to 2.55 sec when ODR=100Hz. The counter used to implement duration function is blocked when LIR=1 in configuration register and the interrupt event is verified

## 7.14 FF\_WU\_CFG\_2 (34h)

**Table 39. Register**

| AOI | LIR | ZHIE | ZLIE | YHIE | YLIE | XHIE | XLIE |
|-----|-----|------|------|------|------|------|------|
|-----|-----|------|------|------|------|------|------|

**Table 40. Register description**

|      |                                                                                                                                                                                            |
|------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| AOI  | And/or combination of Interrupt events. Default value: 0<br>(0: OR combination of interrupt events; 1: AND combination of interrupt events)                                                |
| LIR  | Latch interrupt request into FF_WU_SRC reg with the FF_WU_SRC reg cleared by reading FF_WU_SRC_2 reg. Default value: 0<br>(0: interrupt request not latched; 1: interrupt request latched) |
| ZHIE | Enable interrupt generation on Z high event. Default value: 0<br>(0: disable interrupt request;<br>1: enable interrupt request on measured accel. value higher than preset threshold)      |
| ZLIE | Enable interrupt generation on Z low event. Default value: 0<br>(0: disable interrupt request;<br>1: enable interrupt request on measured accel. value lower than preset threshold)        |
| YHIE | Enable interrupt generation on Y high event. Default value: 0<br>(0: disable interrupt request;<br>1: enable interrupt request on measured accel. value higher than preset threshold)      |
| YLIE | Enable interrupt generation on Y low event. Default value: 0<br>(0: disable interrupt request;<br>1: enable interrupt request on measured accel. value lower than preset threshold)        |
| XHIE | Enable interrupt generation on X high event. Default value: 0<br>(0: disable interrupt request;<br>1: enable interrupt request on measured accel. value higher than preset threshold)      |
| XLIE | Enable interrupt generation on X low event. Default value: 0<br>(0: disable interrupt request;<br>1: enable interrupt request on measured accel. value lower than preset threshold)        |

## 7.15 FF\_WU\_SRC\_2 (35h)

**Table 41. Register**

| X | IA | ZH | ZL | YH | YL | XH | XL |
|---|----|----|----|----|----|----|----|
|---|----|----|----|----|----|----|----|

**Table 42. Register description**

|    |                                                                                                                                  |
|----|----------------------------------------------------------------------------------------------------------------------------------|
| IA | Interrupt active. Default value: 0<br>(0: no interrupt has been generated;<br>1: one or more interrupt event has been generated) |
| ZH | Z high. Default value: 0<br>(0: no interrupt; 1: ZH event has occurred)                                                          |
| ZL | Z low. Default value: 0<br>(0: no interrupt; 1: ZL event has occurred)                                                           |
| YH | Y high. Default value: 0<br>(0: no interrupt; 1: YH event has occurred)                                                          |
| YL | Y low. Default value: 0<br>(0: no interrupt; 1: YL event has occurred)                                                           |
| XH | X high. Default value: 0<br>(0: no interrupt; 1: XH event has occurred)                                                          |
| XL | X low. Default value: 0<br>(0: no interrupt; 1: XL event has occurred)                                                           |

Free-fall and wake-up source register. Read only register.

Reading at this address clears FF\_WU\_SRC\_2 register and the FF, WU 2 interrupt and allows the refreshment of data in the FF\_WU\_SRC\_2 register if the latched option was chosen.

## 7.16 FF\_WU\_THS\_2 (36h)

**Table 43. Register**

| DCRM | THS6 | THS5 | THS4 | THS3 | THS2 | THS1 | THS0 |
|------|------|------|------|------|------|------|------|
|------|------|------|------|------|------|------|------|

**Table 44. Register description**

|            |                                                                                             |
|------------|---------------------------------------------------------------------------------------------|
| DCRM       | Resetting mode selection. Default value: 0<br>(0: counter resetted; 1: counter decremented) |
| THS6, THS0 | Free-fall / wake-up Threshold. Default value: 000 0000                                      |

Most significant bit (DCRM) is used to select the resetting mode of the duration counter. If DCRM=0 counter is resetted when the interrupt is no more active else if DCRM=1 duration counter is decremented.

## 7.17 FF\_WU\_DURATION\_2 (37h)

**Table 45. Register**

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|----|----|----|----|----|----|----|----|
|----|----|----|----|----|----|----|----|

**Table 46. Register description**

|       |                                          |
|-------|------------------------------------------|
| D7-D0 | Duration value. Default value: 0000 0000 |
|-------|------------------------------------------|

Duration register for Free-Fall/Wake-Up interrupt 2. Duration step and maximum value depend on the ODR chosen. Step 2.5 msec, from 0 to 637.5 msec if ODR=400Hz, else step 10 msec, from 0 to 2.55 sec when ODR=100Hz. The counter used to implement duration function is blocked when LIR=1 in configuration register and the interrupt event is verified.

## 7.18 CLICK\_CFG (38h)

**Table 47. Register**

|   |     |          |          |          |          |          |          |
|---|-----|----------|----------|----------|----------|----------|----------|
| - | LIR | Double_Z | Single_Z | Double_Y | Single_Y | Double_X | Single_X |
|---|-----|----------|----------|----------|----------|----------|----------|

**Table 48. Register description**

|          |                                                                                                                                                                                         |
|----------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| LIR      | Latch interrupt request into CLICK_SRC reg with the CLICK_SRC reg refreshed by reading CLICK_SRC reg. Default value: 0 (0: interrupt request not latched; 1: interrupt request latched) |
| Double_Z | Enable interrupt generation on double click event on Z axis. Default value: 0 (0: disable interrupt request; 1: enable interrupt request)                                               |
| Single_Z | Enable interrupt generation on single click event on Z axis. Default value: 0 (0: disable interrupt request; 1: enable interrupt request)                                               |
| Double_Y | Enable interrupt generation on double click event on Y axis. Default value: 0 (0: disable interrupt request; 1: enable interrupt request)                                               |
| Single_Y | Enable interrupt generation on single click event on Y axis. Default value: 0 (0: disable interrupt request; 1: enable interrupt request)                                               |
| Double_X | Enable interrupt generation on double click event on X axis. Default value: 0 (0: disable interrupt request; 1: enable interrupt request)                                               |
| Single_X | Enable interrupt generation on single click event on X axis. Default value: 0 (0: disable interrupt request; 1: enable interrupt request)                                               |

**Table 49. Truth table**

| Double_Z / Y / X | Single_Z / Y / X | Click output     |
|------------------|------------------|------------------|
| 0                | 0                | 0                |
| 0                | 1                | Single           |
| 1                | 0                | Double           |
| 1                | 1                | Single or double |

## 7.19 CLICK\_SRC (39h)

**Table 50. Register**

|   |    |          |          |          |          |          |          |
|---|----|----------|----------|----------|----------|----------|----------|
| X | IA | Double_Z | Single_Z | Double_Y | Single_Y | Double_X | Single_X |
|---|----|----------|----------|----------|----------|----------|----------|

**Table 51. Register description**

|          |                                                                                                                                  |
|----------|----------------------------------------------------------------------------------------------------------------------------------|
| IA       | Interrupt active. Default value: 0<br>(0: no interrupt has been generated;<br>1: one or more interrupt event has been generated) |
| Double_Z | Double click on Z axis event. Default value: 0<br>(0: no interrupt; 1: Double Z event has occurred)                              |
| Single_Z | Single click on Z axis event. Default value: 0<br>(0: no interrupt; 1: Single Z event has occurred)                              |
| Double_Y | Double click on Y axis event. Default value: 0<br>(0: no interrupt; 1: Double Y event has occurred)                              |
| Single_Y | Single click on Y axis event. Default value: 0<br>(0: no interrupt; 1: Single Y event has occurred)                              |
| Double_X | Double click on X axis event. Default value: 0<br>(0: no interrupt; 1: Double X event has occurred)                              |
| Single_X | Single click on X axis event. Default value: 0<br>(0: no interrupt; 1: Single X event has occurred)                              |

## 7.20 CLICK\_THSY\_X (3Bh)

**Table 52. Register**

|       |       |       |       |       |       |       |       |
|-------|-------|-------|-------|-------|-------|-------|-------|
| THSy3 | THSy2 | THSy1 | THSy0 | THSx3 | THSx2 | THSx1 | THSx0 |
|-------|-------|-------|-------|-------|-------|-------|-------|

**Table 53. Register description**

|             |                                                |
|-------------|------------------------------------------------|
| THSy3-THSy0 | Click threshold on Y axis. Default value: 0000 |
| THSx3-THSx0 | Click threshold on X axis. Default value: 0000 |

From 0.5g(0001) to 7.5g(1111) with step of 0.5g.

## 7.21 CLICK\_THSZ (3Ch)

**Table 54. Register**

|   |   |   |   |       |       |       |       |
|---|---|---|---|-------|-------|-------|-------|
| X | X | X | X | THSz3 | THSz2 | THSz1 | THSz0 |
|---|---|---|---|-------|-------|-------|-------|

**Table 55. Register description**

|             |                                                |
|-------------|------------------------------------------------|
| THSz3-THSz0 | Click Threshold on Z axis. Default value: 0000 |
|-------------|------------------------------------------------|

From 0.5g(0001) to 7.5g(1111) with step of 0.5g.

## 7.22 CLICK\_TimeLimit (3Dh)

**Table 56. Register**

|      |      |      |      |      |      |      |      |
|------|------|------|------|------|------|------|------|
| Dur7 | Dur6 | Dur5 | Dur4 | Dur3 | Dur2 | Dur1 | Dur0 |
|------|------|------|------|------|------|------|------|

From 0 to 127.5msec with step of 0.5 msec,

## 7.23 CLICK\_Latency (3Eh)

**Table 57. Register**

| Lat7 | Lat6 | Lat5 | Lat4 | Lat3 | Lat2 | Lat1 | Lat0 |
|------|------|------|------|------|------|------|------|
|------|------|------|------|------|------|------|------|

From 0 to 255 msec with step of 1 msec.

## 7.24 CLICK\_Window (3Fh)

**Table 58. Register**

| Win7 | Win6 | Win5 | Win4 | Win3 | Win2 | Win1 | Win0 |
|------|------|------|------|------|------|------|------|
|------|------|------|------|------|------|------|------|

From 0 to 255 msec with step of 1 msec.

# 8 Typical performance characteristics

## 8.1 Mechanical characteristics at 25°C

Figure 12. X axis 0-g level at 2.5V

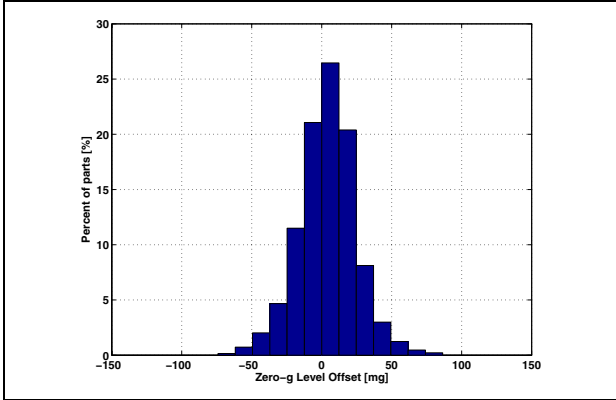


Figure 13. X axis sensitivity at 2.5V

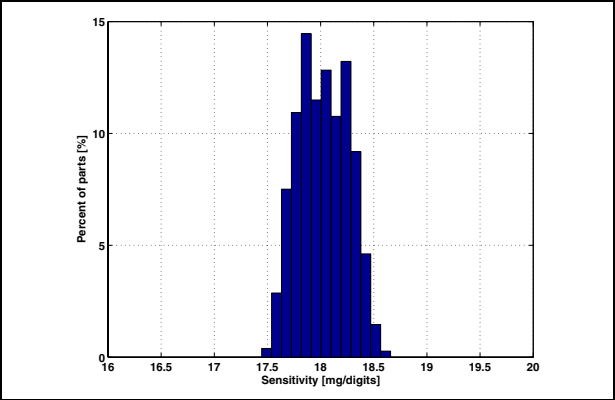


Figure 14. Y axis 0-g level at 2.5V

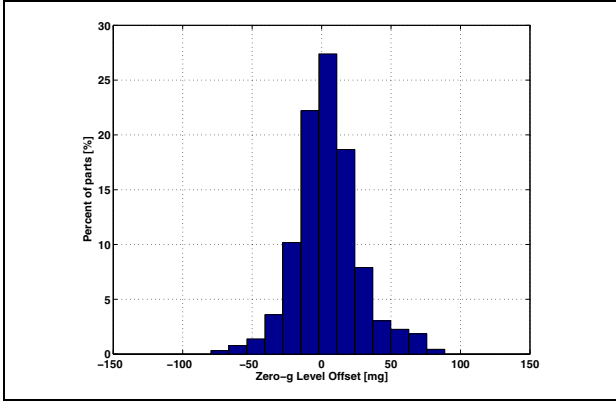


Figure 15. Y axis sensitivity at 2.5V

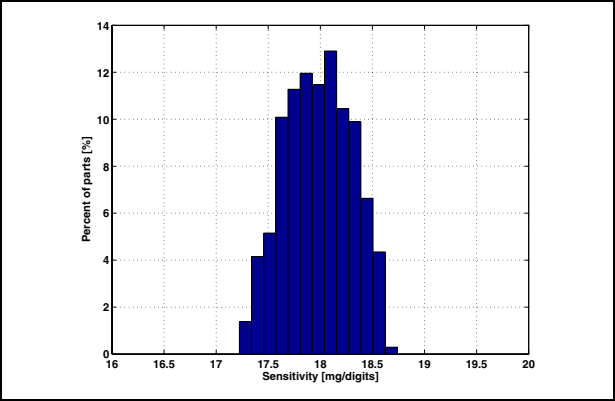


Figure 16. Z axis 0-g level at 2.5V

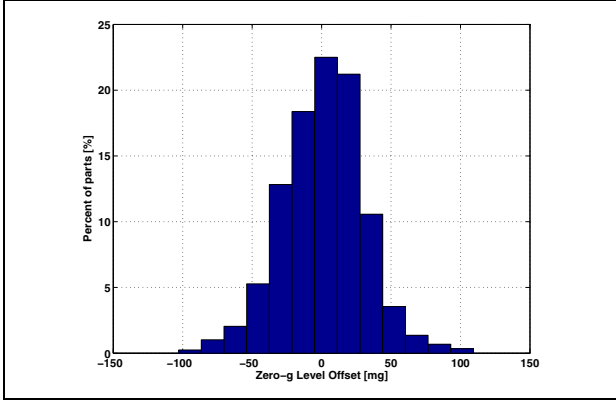
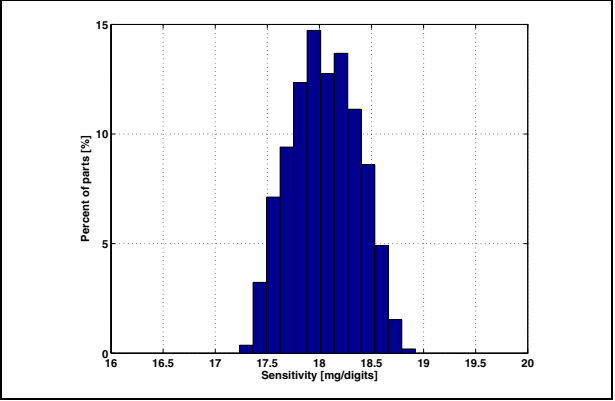


Figure 17. Z axis sensitivity at 2.5V



8.2 Mechanical characteristics derived from measurement in the -40°C to +85°C temperature range

Figure 18. X axis 0-g level change vs temperature at 2.5V

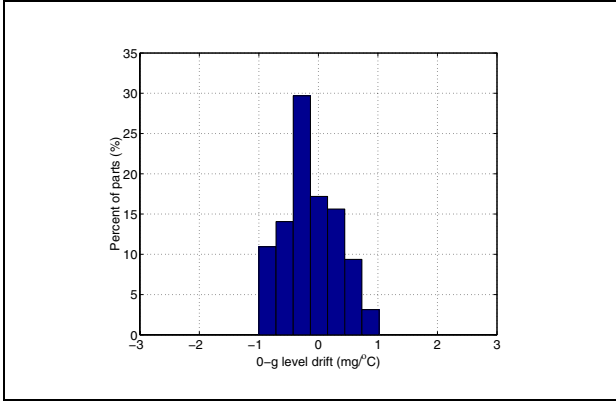


Figure 19. X axis Sensitivity change vs temperature at 2.5V

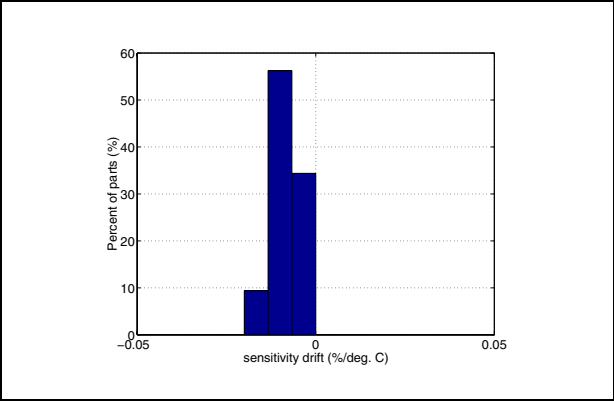


Figure 20. Y axis 0-g level change vs temperature at 2.5V

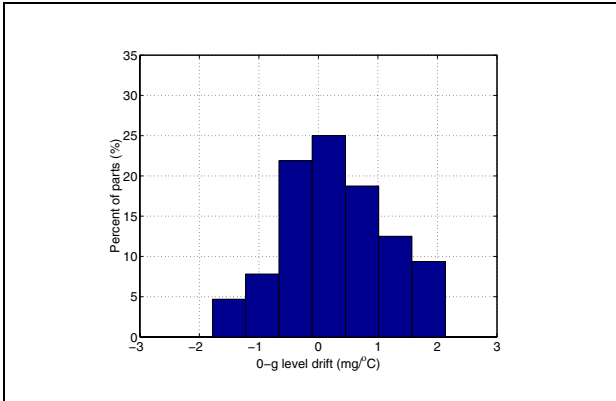


Figure 21. Y axis sensitivity change Vs temperature at 2.5V

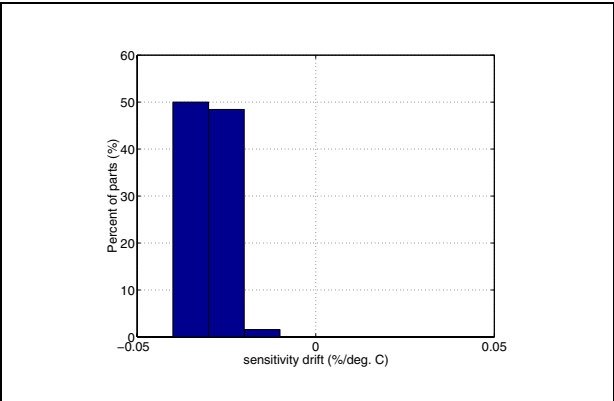


Figure 22. Z axis 0-g level change vs temperature at 2.5V

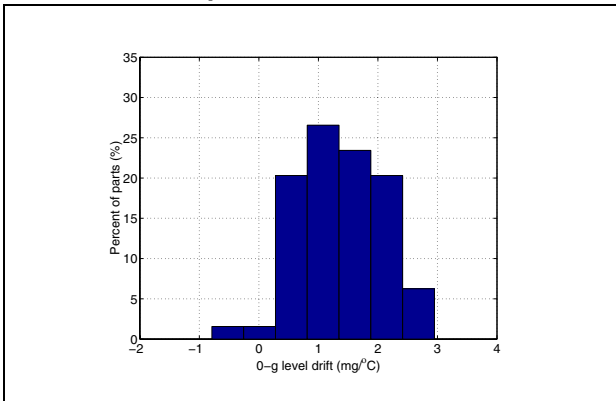
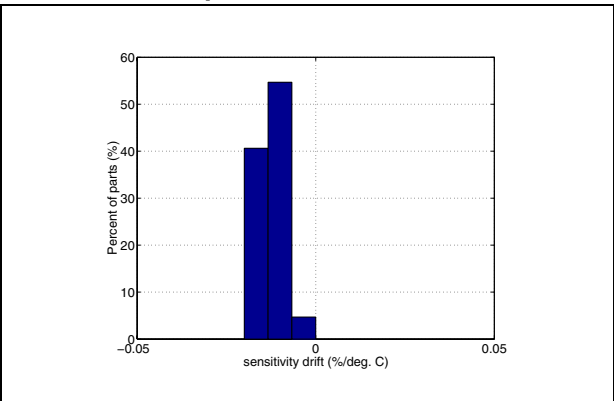


Figure 23. Z axis sensitivity change vs temperature at 2.5V



### 8.3 Electro-mechanical characteristics at 25°C

Figure 24. Current consumption in normal mode at 2.5V

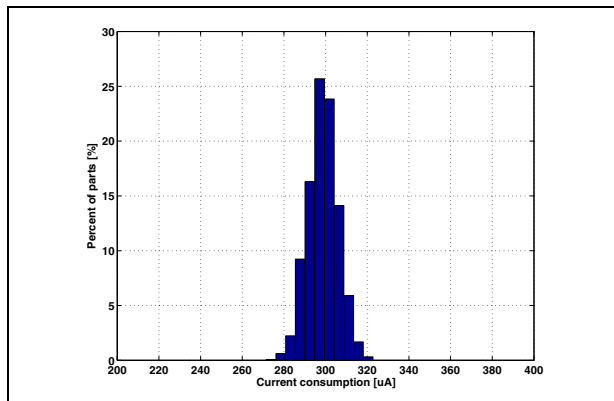
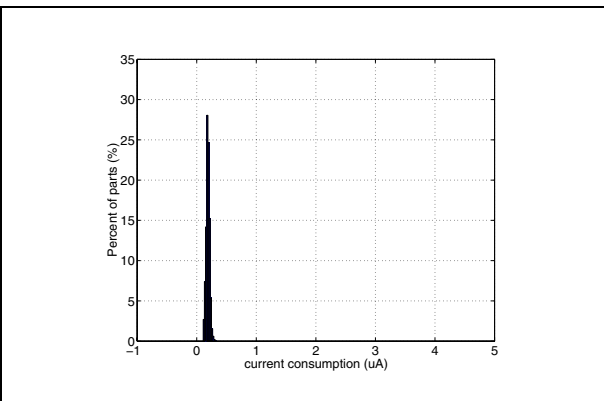


Figure 25. Current consumption in power down mode at 2.5V

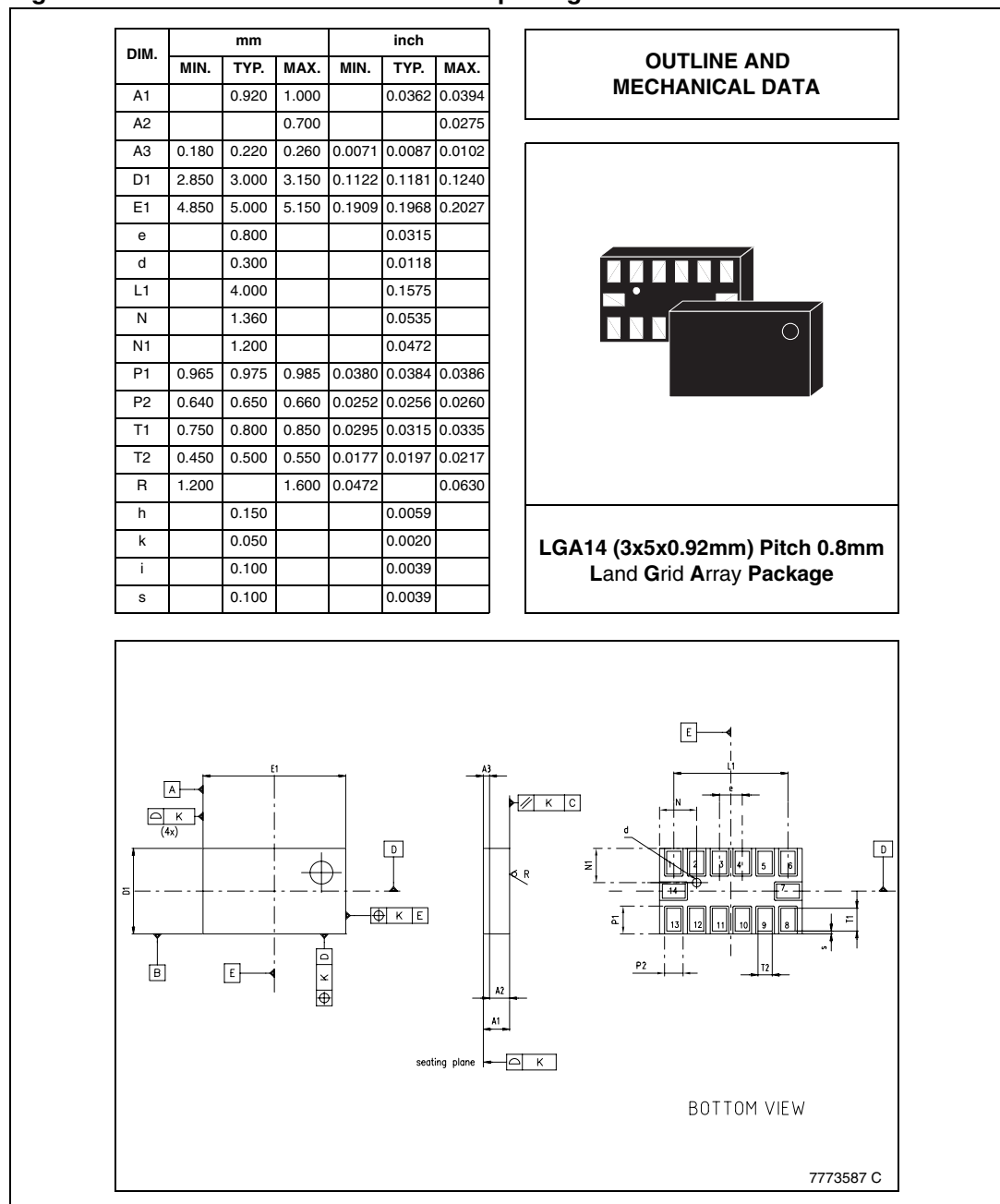


## 9 Package information

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect. The category of second Level Interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark.

ECOPACK specifications are available at: [www.st.com](http://www.st.com).

**Figure 26. LGA 14: Mechanical data and package dimensions**



## 10 Revision history

**Table 59. Document revision history**

| Date        | Revision | Changes                                                                                     |
|-------------|----------|---------------------------------------------------------------------------------------------|
| 3-Oct-2006  | 1        | Initial release.                                                                            |
| 6-Feb-2007  | 2        | Added functions and registers information and typical performance characteristics           |
| 25-Oct-2007 | 3        | Added interfaces timing characteristics and global datasheet review to improved readability |

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