Single-Phase Energy Measurement IC with 8052 MCU, RTC, and LCD Driver

ADE7518

GENERAL FEATURES

- Wide supply voltage operation: 2.4 V to 3.7 V
- Internal bipolar switch between regulated and battery inputs
- Ultralow power operation with power saving modes
  - Full operation: 4 mA to 1.6 mA (PLL clock dependent)
  - Battery mode: 3.2 mA to 400 µA (PLL clock dependent)
  - Sleep mode
    - Real-time clock (RTC) mode: 1.5 µA
    - RTC and LCD mode: 27 µA
- Reference: 1.2 V ± 0.1% (10 ppm/°C drift)
- 64-lead RoHS package option
  - Low profile quad flat package (LQFP)
- Operating temperature range: −40°C to +85°C

ENERGY MEASUREMENT FEATURES

- Proprietary analog-to-digital converters (ADCs) and digital signal processing (DSP) provide high accuracy active (WATT), reactive (VAR), and apparent energy (VA) measurement
  - Less than 0.1% error on active energy over a dynamic range of 1000 to 1 @ 25°C
  - Less than 0.5% error on reactive energy over a dynamic range of 1000 to 1 @ 25°C
  - Less than 0.5% error on root mean square (rms) measurements over a dynamic range of 500 to 1 for current (I_{rms}) and 100 to 1 for voltage (V_{rms}) @ 25°C
  - Supports IEC 62053-21, IEC 62053-22, IEC 62053-23, EN 50470-3 Class A, Class B, and Class C, and ANSI C12-16
- Differential input with programmable gain amplifiers (PGAs) supports shunts and current transformers
- High frequency outputs proportional to I_{rms}, active, reactive, or apparent power (AP)

MICROPROCESSOR FEATURES

- 8052-based core
  - Single-cycle 4 MIPS 8052 core
  - 8052-compatible instruction set
  - 32.768 kHz external crystal with on-chip PLL
  - Two external interrupt sources
  - External reset pin
- Low power battery mode
  - Wake-up from I/O, alarm, and universal asynchronous receiver/transmitter (UART)
  - LCD driver operation
- Real-time clock
  - Counter for seconds, minutes, and hours
  - Automatic battery switchover for RTC backup
  - Operation down to 2.4 V
  - Ultralow battery supply current: 1.5 µA
  - Selectable output frequency: 1 Hz to 16.384 kHz
  - Embedded digital crystal frequency compensation for calibration and temperature variation: 2 ppm resolution
- Integrated LCD driver
  - 108-segment driver
  - 2×, 3×, or 4× multiplexing
  - LCD voltages generated with external resistors
- On-chip peripherals
  - UART, SPI or I^2C, and watchdog timer
- Power supply management with user-selectable levels
- Memory: 16 kB flash memory, 512 bytes RAM
- Development tools
  - Single-pin emulation
  - IDE-based assembly and C-source debugging

Rev. 0
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REVISION HISTORY

1/09—Revision 0: Initial Version

GENERAL DESCRIPTION

The ADE7518[1] integrates the Analog Devices, Inc., energy (ADE) metering IC analog front end and fixed function DSP solution with an enhanced 8052 MCU core, an RTC, an LCD driver, and all the peripherals to make an electronic energy meter with an LCD display in a single part.

The ADE measurement core includes active, reactive, and apparent energy calculations, as well as voltage and current rms measurements. This information is ready to use for energy billing by using built-in energy scalars. Many power line supervisory features, such as SAG, peak, and zero crossing, are included in the energy measurement DSP to simplify energy meter design.

The microprocessor functionality includes a single-cycle 8052 core, a real-time clock with a power supply backup pin, a UART, and an SPI or I²C® interface. The ready-to-use information from the ADE core reduces the program memory size requirement, making it easy to integrate complicated design into 16 kB of flash memory.

The ADE7518 also includes a 108-segment LCD driver. This driver generates waveforms capable of driving LCDs up to 3.3 V.

FUNCTIONAL BLOCK DIAGRAM

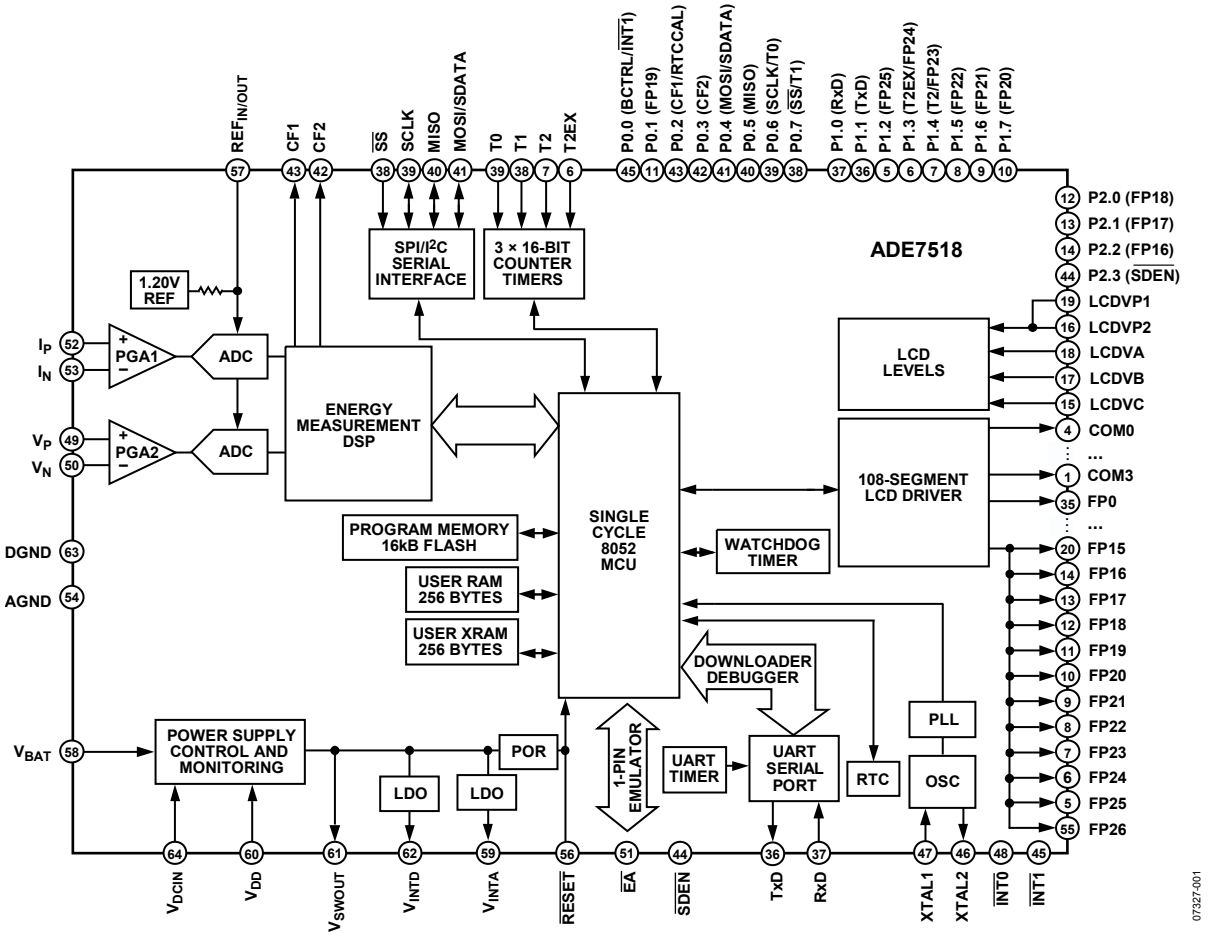


Figure 1.

[1] Patents pending.

SPECIFICATIONS

V_{DD} = 3.3 V ± 5%, AGND = DGND = 0 V, on-chip reference XTAL = 32.768 kHz, T_{MIN} to T_{MAX} = −40°C to +85°C, unless otherwise noted.

ENERGY METERING

Table 1.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
MEASUREMENT ACCURACY[1]					
Phase Error Between Channels					
PF = 0.8 Capacitive		±0.05		Degrees	37° phase lead
PF = 0.5 Inductive		±0.05		Degrees	60° phase lag
Active Energy Measurement Error[2]		0.1		% of reading	Over a dynamic range of 1000 to 1 @ 25°C
AC Power Supply Rejection[2]					V_{DD} = 3.3 V + 100 mV rms/120 Hz
Output Frequency Variation		0.01		%	$I_P = V_P$ = ±100 mV rms
DC Power Supply Rejection[2]					V_{DD} = 3.3 V ± 117 mV dc
Output Frequency Variation		0.01		%	
Active Energy Measurement Bandwidth[1]		8		kHz	
Reactive Energy Measurement Error[2]		0.5		% of reading	Over a dynamic range of 1000 to 1 @ 25°C
V_{rms} Measurement Error[2]		0.5		% of reading	Over a dynamic range of 100 to 1 @ 25°C
V_{rms} Measurement Bandwidth[1]		3.9		kHz	
I_{rms} Measurement Error[2]		0.5		% of reading	Over a dynamic range of 500 to 1 @ 25°C
I_{rms} Measurement Bandwidth[1]		3.9		kHz	
ANALOG INPUTS					
Maximum Signal Levels			±400	mV peak	$V_P - V_N$ differential input
			±400	mV peak	$I_P - I_N$ differential input
Input Impedance (DC)		770		kΩ	
ADC Offset Error[2]		±10		mV	PGA1 = PGA2 = 1
		±1		mV	PGA1 = 16
Gain Error[2]					
Current Channel	−3		+ 3	%	I_P = 0.4 V dc or I_P = 0.4 dc
Voltage Channel	−3		+ 3	%	Voltage channel = 0.4 V dc
Gain Error Match		±0.2		%	
CF1 AND CF2 PULSE OUTPUT					
Maximum Output Frequency		13.5		kHz	$V_P - V_N$ = 400 mV peak, $I_P - I_N$ = 250 mV, PGA1 = 2 sine wave
Duty Cycle		50		%	If CF1 or CF2 frequency, >5.55 Hz
Active High Pulse Width		90		ms	If CF1 or CF2 frequency, <5.55 Hz

[1] These specifications are not production tested but are guaranteed by design and/or characterization data on production release.
[2] See the Terminology section for definition.

ANALOG PERIPHERALS

Table 2.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
POWER-ON RESET (POR)					
V_{DD} POR					
Detection Threshold	2.5		2.95	V	
POR Active Timeout Period		33		ms	
V_{SWOUT} POR					
Detection Threshold	1.8		2.2	V	
POR Active Timeout Period		20		ms	
V_{INTD} POR					
Detection Threshold	2.03		2.22	V	
POR Active Timeout Period		16		ms	
V_{INTA} POR					
Detection Threshold	2.05		2.15	V	
POR Active Timeout Period		120		ms	
BATTERY SWITCHOVER					
Voltage Operating Range (V_{SWOUT})	2.4		3.7	V	
V_{DD} to V_{BAT} Switching					
Switching Threshold (V_{DD})	2.5		2.95	V	
Switching Delay		10		ns	When V_{DD} to V_{BAT} switch activated by V_{DD}
		30		ms	When V_{DD} to V_{BAT} switch activated by V_{DCIN}
V_{BAT} to V_{DD} Switching					
Switching Threshold (V_{DD})	2.5		2.95	V	
Switching Delay		30		ms	Based on V_{DD} > 2.75 V
V_{SWOUT} To V_{BAT} Leakage Current		10		nA	V_{BAT} = 0 V, V_{SWOUT} = 3.43 V, T_A = 25°C
LCD, RESISTOR LADDER ACTIVE					
Leakage Current			±20	nA	1/2 and 1/3 bias modes, no load
V1 Segment Line Voltage	LCDVA – 0.1		LCDVA	V	Current on segment line = −2 µA
V2 Segment Line Voltage	LCDVB – 0.1		LCDVB	V	Current on segment line = −2 µA
V3 Segment Line Voltage	LCDVC – 0.1		LCDVC	V	Current on segment line = −2 µA
ON-CHIP REFERENCE					
Reference Error			±0.9	mV	T_A = 25°C
Power Supply Rejection		80		dB	
Temperature Coefficient		10	50	ppm/°C	

DIGITAL INTERFACE

Table 3.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
LOGIC INPUTS					
All Inputs Except XTAL1, XTAL2, BCTRL, $\overline{\text{INT0}}$, $\overline{\text{INT1}}$, $\overline{\text{RESET}}$					
Input High Voltage, V_{INH}	2.0			V	
Input Low Voltage, V_{INL}			0.4	V	
BCTRL, $\overline{\text{INT0}}$, $\overline{\text{INT1}}$, $\overline{\text{RESET}}$					
Input High Voltage, V_{INH}	1.3			V	
Input Low Voltage, V_{INL}			0.4	V	
Input Currents					
$\overline{\text{RESET}}$			100	nA	$\overline{\text{RESET}} = V_{SWOUT} = 3.3$ V
Port 0, Port 1, Port 2			±100	nA	Internal pull-up disabled, input = 0 V or V_{SWOUT}
		−3.75	−8.5	µA	Internal pull-up enabled, input = 0 V, $V_{SWOUT} = 3.3$ V
Input Capacitance		10		pF	All digital inputs
FLASH MEMORY					
Endurance[1]	10,000			Cycles	
Data Retention[2]	20			Years	$T_J = 85°C$
CRYSTAL OSCILLATOR					
Crystal Equivalent Series Resistance	30		50	kΩ	
Crystal Frequency	32	32.768	33.5	kHz	
XTAL1 Input Capacitance		12		pF	
XTAL2 Output Capacitance		12		pF	
MCU CLOCK RATE (f_{CORE})		4.096		MHz	Crystal = 32.768 kHz and CD[2:0] = 0b000
		32		kHz	Crystal = 32.768 kHz and CD[2:0] = 0b111
LOGIC OUTPUTS					
Output High Voltage, V_{OH}	2.4			V	$V_{DD} = 3.3$ V ± 5%
I_{SOURCE}			80	µA	
Output Low Voltage, V_{OL}[3]			0.4	V	$V_{DD} = 3.3$ V ± 5%
I_{SINK}			2	mA	
START-UP TIME[4]					
PSM0 Power-On Time		448		ms	V_{DD} at 2.75 V to PSM0 code execution
From Power Saving Mode 1 (PSM1)					
PSM1 → PSM0		130		ms	V_{DD} at 2.75 V to PSM0 code execution
From Power Saving Mode 2 (PSM2)					
PSM2 → PSM1		48		ms	Wake-up event to PSM1 code execution
PSM2 → PSM0		186		ms	V_{DD} at 2.75 V to PSM0 code execution
POWER SUPPLY INPUTS					
V_{DD}	3.13	3.3	3.46	V	
V_{BAT}	2.4	3.3	3.7	V	
INTERNAL POWER SUPPLY SWITCH (V_{SWOUT})					
V_{BAT} to V_{SWOUT} On Resistance			22	Ω	$V_{BAT} = 2.4$ V
V_{DD} to V_{SWOUT} On Resistance			10.2	Ω	$V_{DD} = 3.13$ V
$V_{BAT} \longleftrightarrow V_{DD}$ Switching Open Time		40		ns	
BCTRL State Change and Switch Delay		18		µs	
V_{SWOUT} Output Current Drive		1	6	mA	
POWER SUPPLY OUTPUTS					
V_{INTA}	2.25		2.75	V	
V_{INTD}	2.3		2.70	V	
V_{INTA} Power Supply Rejection		60		dB	
V_{INTD} Power Supply Rejection		50		dB	

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
POWER SUPPLY CURRENTS					
Current in Normal Mode (PSM0)		4	5.3	mA	f_{CORE} = 4.096 MHz, LCD and meter active
		2.1		mA	f_{CORE} = 1.024 MHz, LCD and meter active
		1.6		mA	f_{CORE} = 32.768 kHz, LCD and meter active
		3.2	4.25	mA	f_{CORE} = 4.096 MHz, meter DSP active, metering ADC powered down
		3	3.9	mA	f_{CORE} = 4.096 MHz, metering ADC and DSP powered down
Current in PSM1		3.2	5.05	mA	f_{CORE} = 4.096 MHz, LCD active, V_{BAT} = 3.7 V
		880		µA	f_{CORE} = 1.024 MHz, LCD active
Current in PSM2		38		µA	LCD active at 3.3 V + RTC (real-time clock)
		1.5		µA	RTC only, T_A = 25°C, V_{BAT} = 3.3 V
POWER SUPPLY CURRENTS					
Current in Normal Mode (PSM0)		4	5.3	mA	f_{CORE} = 4.096 MHz, LCD and meter active

[1] Endurance is qualified as per JEDEC Standard 22 Method A117 and measured at −40°C, +25°C, +85°C, and +125°C.
[2] Retention lifetime equivalent at junction temperature (T_J) = 85°C as per JEDEC Standard 22 Method A117. Retention lifetime derates with junction temperature.
[3] Test performed with all the I/Os set to a low output level.
[4] Delay between power supply valid and execution of first instruction by 8052 core.

TIMING SPECIFICATIONS

AC inputs during testing were driven at V_{SWOUT} − 0.5 V for Logic 1 and 0.45 V for Logic 0. Timing measurements were made at V_{IH} minimum for Logic 1 and V_{IL} maximum for Logic 0, as shown in Figure 2.

For timing purposes, a port pin is no longer floating when a 100 mV change from load voltage occurs. A port pin begins to float when a 100 mV change from the loaded V_{OH}/V_{OL} level occurs, as shown in Figure 2.

For Table 4 to Table 9, C_{LOAD} = 80 pF for all outputs, V_{DD} = 2.7 V to 3.6 V, and all specifications T_{MIN} to T_{MAX}, unless otherwise noted.

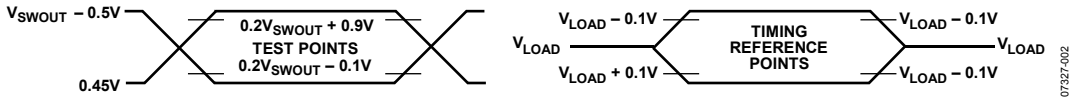


Figure 2. Timing Waveform Characteristics

Table 4. Clock Input (External Clock Driven XTAL1) Parameters

		32.768 kHz External Crystal			
Parameter	**Description**	**Min**	**Typ**	**Max**	**Unit**
t_{CK}	XTAL1 period		30.52		µs
t_{CKL}	XTAL1 width low		6.26		µs
t_{CKH}	XTAL1 width high		6.26		µs
t_{CKR}	XTAL1 rise time		9		ns
t_{CKF}	XTAL1 fall time		9		ns
$1/t_{CORE}$	Core clock frequency[1]	0.032768	1.024	4.096	MHz

[1] The ADE7518 internal PLL locks onto a multiple (512 times) of the 32.768 kHz external crystal frequency to provide a stable 4.096 MHz internal clock for the system. The core can operate at this frequency or at a binary submultiple defined by the CD[2:0] bits, selected via the POWCON SFR (see Table 24).

Table 5. I²C-Compatible Interface Timing Parameters (400 kHz)

Parameter	**Description**	**Typ**	**Unit**
t_{BUF}	Bus-free time between stop condition and start condition	1.3	µs
t_L	SCLK low pulse width	1.36	µs
t_H	SCLK high pulse width	1.14	µs
t_{SHD}	Start condition hold time	251.35	µs
t_{DSU}	Data setup time	740	ns
t_{DHD}	Data hold time	400	ns
t_{RSU}	Setup time for repeated start	12.5	ns
t_{PSU}	Stop condition setup time	400	ns
t_R	Rise time of both SCLK and SDATA	200	ns
t_F	Fall time of both SCLK and SDATA	300	ns
t_{SUP}[1]	Pulse width of spike suppressed	50	ns

[1] Input filtering on both the SCLK and SDATA inputs suppresses noise spikes of less than 50 ns.

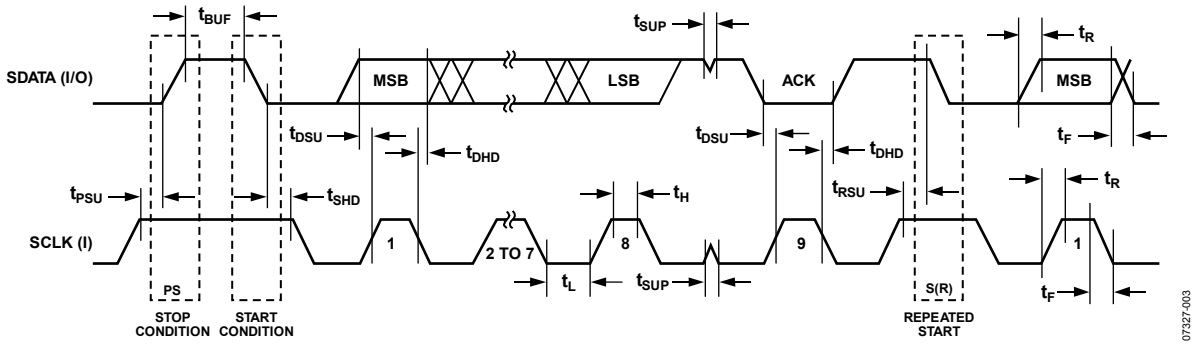


Figure 3. I²C-Compatible Interface Timing

Table 6. SPI Master Mode Timing (SPICPHA = 1) Parameters

Parameter	Description	Min	Typ	Max	Unit
t_{SL}	SCLK low pulse width	$2^{SPIR} \times t_{CORE}$[1]			ns
t_{SH}	SCLK high pulse width	$2^{SPIR} \times t_{CORE}$[1]			ns
t_{DAV}	Data output valid after SCLK edge			$3 \times t_{CORE}$[1]	ns
t_{DSU}	Data input setup time before SCLK edge	0			ns
t_{DHD}	Data input hold time after SCLK edge	t_{CORE}[1]			ns
t_{DF}	Data output fall time		19		ns
t_{DR}	Data output rise time		19		ns
t_{SR}	SCLK rise time		19		ns
t_{SF}	SCLK fall time		19		ns

[1] t_{CORE} depends on the clock divider or CD[2:0] bits of the POWCON SFR (see Table 24); $t_{CORE} = 2^{CD}/4.096$ MHz.

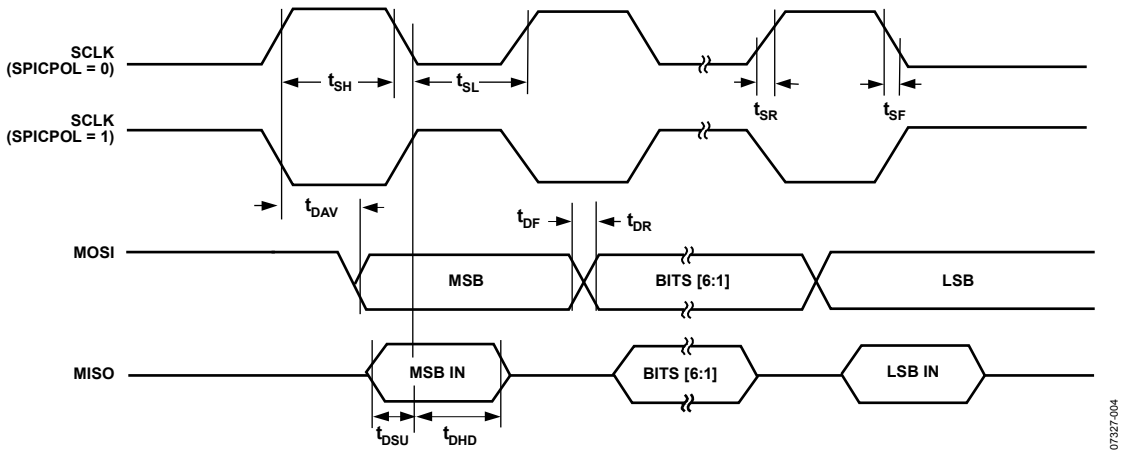


Figure 4. SPI Master Mode Timing (SPICPHA = 1)

Table 7. SPI Master Mode Timing (SPICPHA = 0) Parameters

Parameter	Description	Min	Typ	Max	Unit
t_{SL}	SCLK low pulse width	$2^{SPIR} \times t_{CORE}$[1]	$(SPIR + 1) \times t_{CORE}$[1]		ns
t_{SH}	SCLK high pulse width	$2^{SPIR} \times t_{CORE}$[1]	$(SPIR + 1) \times t_{CORE}$[1]		ns
t_{DAV}	Data output valid after SCLK edge			$3 \times t_{CORE}$[1]	ns
t_{DOSU}	Data output setup before SCLK edge			75	ns
t_{DSU}	Data input setup time before SCLK edge	0			ns
t_{DHD}	Data input hold time after SCLK edge	t_{CORE}[1]			ns
t_{DF}	Data output fall time		19		ns
t_{DR}	Data output rise time		19		ns
t_{SR}	SCLK rise time		19		ns
t_{SF}	SCLK fall time		19		ns

[1] t_{CORE} depends on the clock divider or CD[2:0] bits of the POWCON SFR (see Table 24); $t_{CORE} = 2^{CD}/4.096$ MHz.

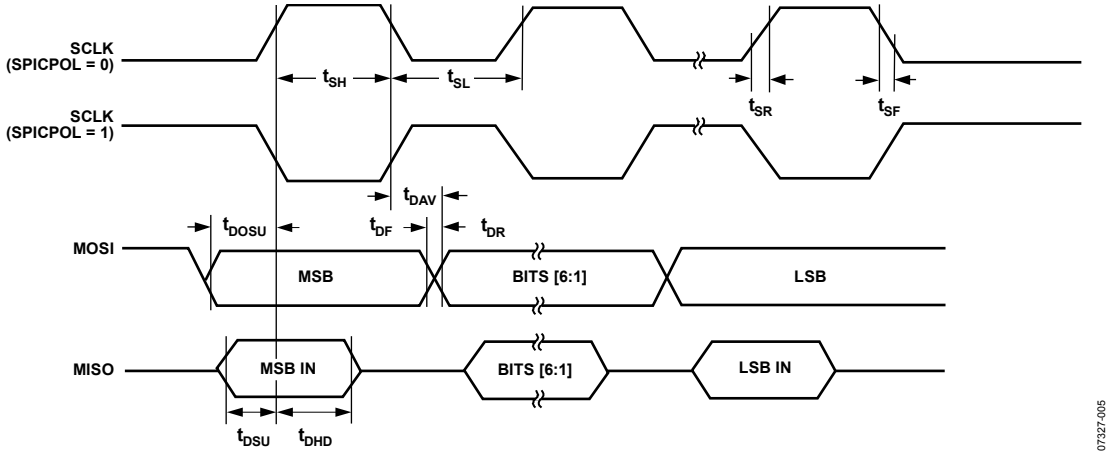


Figure 5. SPI Master Mode Timing (SPICPHA = 0)

Table 8. SPI Slave Mode Timing (SPICPHA = 1) Parameters

Parameter	Description	Min	Typ	Max	Unit
t_{SS}	$\overline{SS}$ to SCLK edge	145			ns
t_{SL}	SCLK low pulse width	$6 \times t_{CORE}$[1]			ns
t_{SH}	SCLK high pulse width	$6 \times t_{CORE}$[1]			ns
t_{DAV}	Data output valid after SCLK edge			25	ns
t_{DSU}	Data input setup time before SCLK edge	0			ns
t_{DHD}	Data input hold time after SCLK edge	$2 \times t_{CORE}$[1] + 0.5			µs
t_{DF}	Data output fall time		19		ns
t_{DR}	Data output rise time		19		ns
t_{SR}	SCLK rise time		19		ns
t_{SF}	SCLK fall time		19		ns
t_{SFS}	$\overline{SS}$ high after SCLK edge	0			ns

[1] t_{CORE} depends on the clock divider or CD[2:0] bits of the POWCON SFR (see Table 24); $t_{CORE} = 2^{CD}/4.096$ MHz.

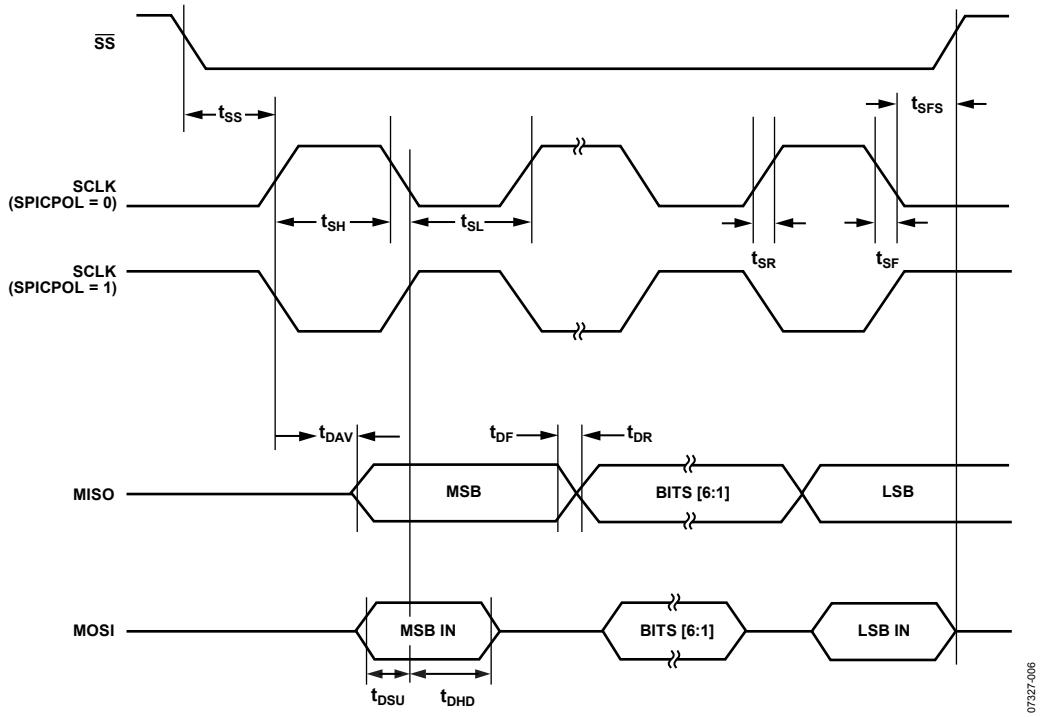


Figure 6. SPI Slave Mode Timing (SPICPHA = 1)

Table 9. SPI Slave Mode Timing (SPICPHA = 0) Parameters

Parameter	Description	Min	Typ	Max	Unit
t_{SS}	$\overline{SS}$ to SCLK edge	145			ns
t_{SL}	SCLK low pulse width	$6 \times t_{CORE}$[1]			ns
t_{SH}	SCLK high pulse width	$6 \times t_{CORE}$[1]			ns
t_{DAV}	Data output valid after SCLK edge			25	ns
t_{DSU}	Data input setup time before SCLK edge	0			ns
t_{DHD}	Data input hold time after SCLK edge	$2 \times t_{CORE}$[1] + 0.5			µs
t_{DF}	Data output fall time		19		ns
t_{DR}	Data output rise time		19		ns
t_{SR}	SCLK rise time		19		ns
t_{SF}	SCLK fall time		19		ns
t_{DOSS}	Data output valid after $\overline{SS}$ edge	0			ns
t_{SFS}	$\overline{SS}$ high after SCLK edge	0			ns

[1] t_{CORE} depends on the clock divider or CD[2:0] bits of the POWCON SFR (see Table 24); $t_{CORE} = 2^{CD}/4.096$ MHz.

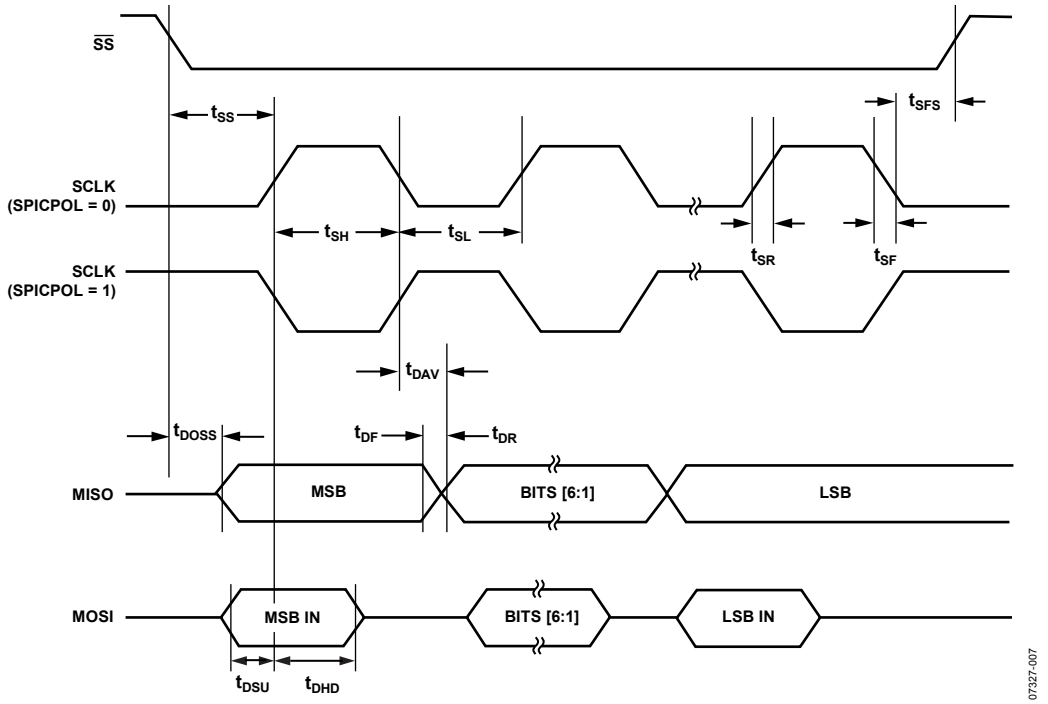


Figure 7. SPI Slave Mode Timing (SPICPHA = 0)

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 10.

Parameter	Rating
V_{DD} to DGND	−0.3 V to +3.7 V
V_{BAT} to DGND	−0.3 V to +3.7 V
V_{DCIN} to DGND	−0.3 V to V_{SWOUT} + 0.3 V
Input LCD Voltage to AGND, LCDVA, LCDVB, LCDVC[1]	−0.3 V to V_{SWOUT} + 0.3 V
Analog Input Voltage to AGND, V_P, V_N, I_P, and I_N	−2 V to +2 V
Digital Input Voltage to DGND	−0.3 V to V_{SWOUT} + 0.3 V
Digital Output Voltage to DGND	−0.3 V to V_{SWOUT} + 0.3 V
Operating Temperature Range (Industrial)	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
64-Lead LQFP, Power Dissipation	1 W
Lead Temperature	
Soldering	300°C
Time	30 sec

[1] When used with external resistor divider.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL RESISTANCE

θ_{JA} is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages.

Table 11. Thermal Resistance

Package Type	θ_{JA}	θ_{JC}	Unit
64-Lead LQFP	60	20.5	°C/W

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

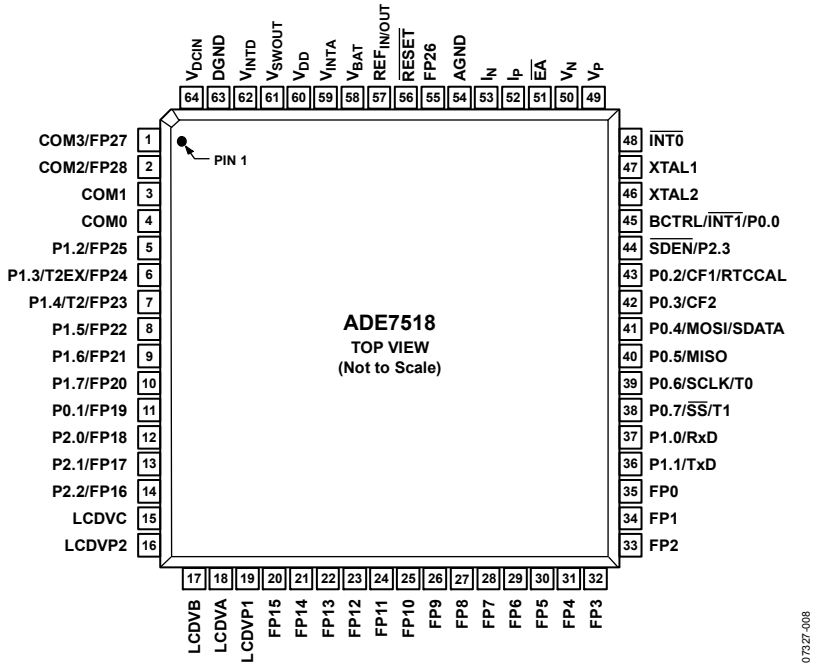


Figure 8. Pin Configuration

Table 12. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	COM3/FP27	Common Output 3 or LCD Segment Output 27. COM3 is used for LCD backplane.
2	COM2/FP28	Common Output 2 or LCD Segment Output 28. COM2 is used for LCD backplane.
3	COM1	Common Output 1. COM1 is used for LCD backplane.
4	COM0	Common Output 0. COM0 is used for LCD backplane.
5	P1.2/FP25	General-Purpose Digital I/O Port 1.2 or LCD Segment Output 25.
6	P1.3/T2EX/FP24	General-Purpose Digital I/O Port 1.3, Timer 2 Control Input, or LCD Segment Output 24.
7	P1.4/T2/FP23	General-Purpose Digital I/O Port 1.4, Timer 2 Input, or LCD Segment Output 23.
8	P1.5/FP22	General-Purpose Digital I/O Port 1.5 or LCD Segment Output 22.
9	P1.6/FP21	General-Purpose Digital I/O Port 1.6 or LCD Segment Output 21.
10	P1.7/FP20	General-Purpose Digital I/O Port 1.7 or LCD Segment Output 20.
11	P0.1/FP19	General-Purpose Digital I/O Port 0.1 or LCD Segment Output 19.
12	P2.0/FP18	General-Purpose Digital I/O Port 2.0 or LCD Segment Output 18.
13	P2.1/FP17	General-Purpose Digital I/O Port 2.1 or LCD Segment Output 17.
14	P2.2/FP16	General-Purpose Digital I/O Port 2.2 or LCD Segment Output 16.
15	LCDVC	This pin is internally connected to V_{DD}. A resistor should be connected between LCDVC and LCDVB to generate the top two voltages for the LCD waveforms (see the LCD Driver section).
16	LCDVP2	This pin is internally connected to LCDVP1 (see the LCD Driver section).
17	LCDVB	This pin is an input voltage for the LCD driver. A resistor should be connected between LCDVB and LCDVC to generate an intermediate voltage for the LCD driver. In 1/3 bias LCD mode, another resistor must be connected between LCDVB and LCDVA to generate another intermediate voltage. In 1/2 bias LCD mode, LCDVB and LCDVA are internally connected (see the LCD Driver section).
18	LCDVA	This pin is an input voltage for the LCD driver. A resistor should be connected between LCDVA and LCDVP1 to generate an intermediate voltage for the LCD driver. In 1/3 bias LCD mode, another resistor must be connected between LCDVB and LCDVA to generate another intermediate voltage. In 1/2 bias LCD mode, LCDVB and LCDVA are internally connected (see the LCD Driver section).
19	LCDVP1	This pin is an input voltage for the LCD driver. A resistor should be connected between LCDVA and LCDVP1 to generate an intermediate voltage for the LCD driver. Another resistor must be connected between LCDVP1 and DGND to generate another intermediate voltage (see the LCD Driver section).
35 to 20	FP0 to F15	LCD Segment Output 0 to LCD Segment Output 15.
36	P1.1/TxD	General-Purpose Digital I/O Port 1.1 or Transmitter Data Output (Asynchronous).

Pin No.	Mnemonic	Description
37	P1.0/RxD	General-Purpose Digital I/O Port 1.0 or Receiver Data Input (Asynchronous).
38	P0.7/$\overline{SS}$/T1	General-Purpose Digital I/O Port 0.7, Slave Select When SPI is in Slave Mode, or Timer 1 Input.
39	P0.6/SCLK/T0	General-Purpose Digital I/O Port 0.6, Clock Output for I^2C or SPI Port, or Timer 0 Input.
40	P0.5/MISO	General-Purpose Digital I/O Port 0.5 or Data Input for SPI Port.
41	P0.4/MOSI/SDATA	General-Purpose Digital I/O Port 0.4, Data Output for SPI Port, or I^2C-Compatible Data Line.
42	P0.3/CF2	General-Purpose Digital I/O Port 0.3 or Calibration Frequency Logic Output 2. The CF2 logic output gives instantaneous active, reactive, I_{rms}, or apparent power information.
43	P0.2/CF1/RTCCAL	General-Purpose Digital I/O Port 0.2, Calibration Frequency Logic Output 1, or RTC Calibration Frequency Logic Output. The CF1 logic output gives instantaneous active, reactive, I_{rms}, or apparent power information. The RTCCAL logic output gives access to the calibrated RTC output.
44	$\overline{SDEN}$/P2.3	Serial Download Mode Enable or Digital Output Port P2.3. This pin is used to enable serial download mode through a resistor when pulled low on power-up or reset. On reset, this pin momentarily becomes an input and the status of the pin is sampled. If there is no pull-down resistor in place, the pin momentarily goes high and then user code is executed. If the pin is pulled down on reset, the embedded serial download/debug kernel executes, and this pin remains low during the internal program execution. After reset, this pin can be used as a digital output port pin (P2.3).
45	BCTRL/$\overline{INT1}$/P0.0	Digital Input for Battery Control, External Interrupt Input 1, or General-Purpose Digital I/O Port 0.0. This logic input connects V_{DD} or V_{BAT} to V_{SWOUT} internally when set to logic high or logic low, respectively. When left open, the connection between V_{DD} and V_{SWOUT} or between V_{BAT} and V_{SWOUT} is selected internally.
46	XTAL2	A crystal can be connected across this pin and XTAL1 (see the XTAL1 pin description) to provide a clock source for the ADE7518. The XTAL2 pin can drive one CMOS load when an external clock is supplied at XTAL1 or by the gate oscillator circuit. An internal 6 pF capacitor is connected to this pin.
47	XTAL1	An external clock can be provided at this logic input. Alternatively, a parallel resonant AT crystal can be connected across XTAL1 and XTAL2 to provide a clock source for the ADE7518. The clock frequency for specified operation is 32.768 kHz. An internal 6 pF capacitor is connected to this pin.
48	$\overline{INT0}$	External Interrupt Input 0.
49, 50	V_P, V_N	Analog Inputs for Voltage Channel. These inputs are fully differential voltage inputs with a maximum differential level of ±400 mV for specified operation. This channel also has an internal PGA.
51	$\overline{EA}$	This pin is used as an input for emulation. When held high, this input enables the device to fetch code from internal program memory locations. The ADE7518 does not support external code memory. This pin should not be left floating.
52, 53	I_P, I_N	Analog Inputs for Current Channel. These inputs are fully differential voltage inputs with a maximum differential level of ±400 mV for specified operation. This channel also has an internal PGA.
54	AGND	This pin provides the ground reference for the analog circuitry.
55	FP26	LCD Segment Output 26.
56	$\overline{RESET}$	Reset Input, Active Low.
57	$REF_{IN/OUT}$	This pin provides access to the on-chip voltage reference. The on-chip reference has a nominal value of 1.2 V ± 0.1% and a typical temperature coefficient of 50 ppm/°C maximum. This pin should be decoupled with a 1 µF capacitor in parallel with a ceramic 100 nF capacitor.
58	V_{BAT}	Power Supply Input from the Battery with a 2.4 V to 2.7 V Range. This pin is connected internally to V_{DD} when the battery is selected as the power supply for the ADE7518.
59	V_{INTA}	This pin provides access to the on-chip 2.5 V analog LDO. No external active circuitry should be connected to this pin. This pin should be decoupled with a 10 µF capacitor in parallel with a ceramic 100 nF capacitor.
60	V_{DD}	3.3 V Power Supply Input from the Regulator. This pin is connected internally to V_{DD} when the regulator is selected as the power supply for the ADE7518. This pin should be decoupled with a 10 µF capacitor in parallel with a ceramic 100 nF capacitor.
61	V_{SWOUT}	3.3 V Power Supply Output. This pin provides the supply voltage for the LDOs and internal circuitry of the ADE7518. This pin should be decoupled with a 10 µF capacitor in parallel with a ceramic 100 nF capacitor.
62	V_{INTD}	This pin provides access to the on-chip 2.5 V digital LDO. No external active circuitry should be connected to this pin. This pin should be decoupled with a 10 µF capacitor in parallel with a ceramic 100 nF capacitor.
63	DGND	This pin provides the ground reference for the digital circuitry.
64	V_{DCIN}	Analog Input for DC Voltage Monitoring. The maximum input voltage on this pin is V_{SWOUT} with respect to AGND. This pin is used to monitor the preregulated dc voltage.

TYPICAL PERFORMANCE CHARACTERISTICS

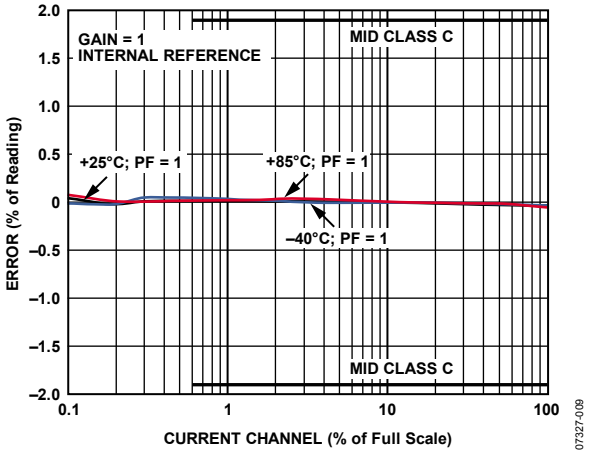


Figure 9. Active Energy Error as a Percentage of Reading (Gain = 1) over Temperature with Internal Reference

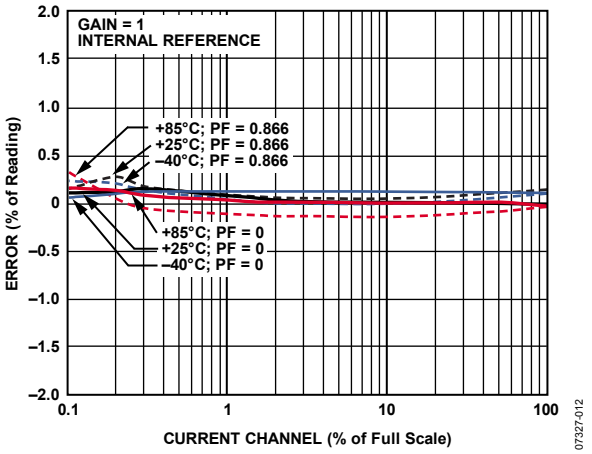


Figure 12. Reactive Energy Error as a Percentage of Reading (Gain = 1) over Power Factor with Internal Reference

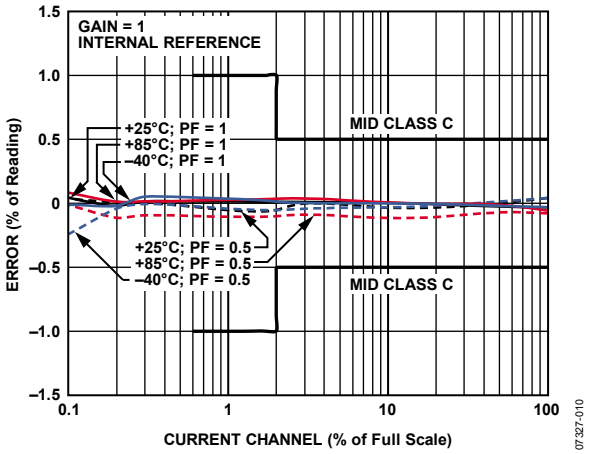


Figure 10. Active Energy Error as a Percentage of Reading (Gain = 1) over Power Factor with Internal Reference

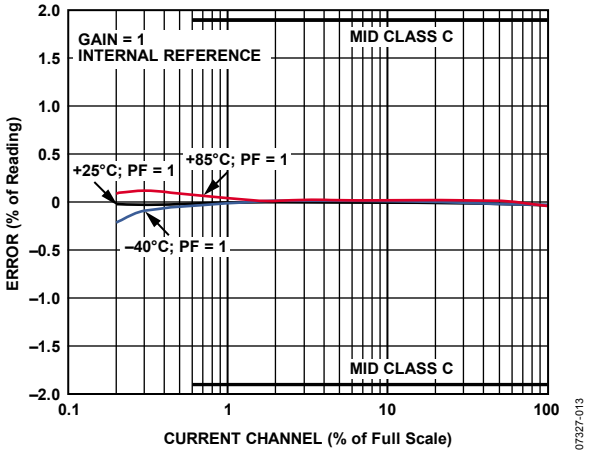


Figure 13. Current RMS Error as a Percentage of Reading (Gain = 1) over Temperature with Internal Reference

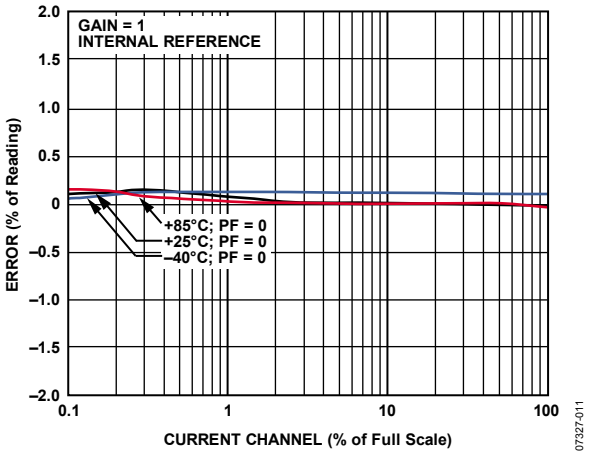


Figure 11. Reactive Energy Error as a Percentage of Reading (Gain = 1) over Temperature with Internal Reference

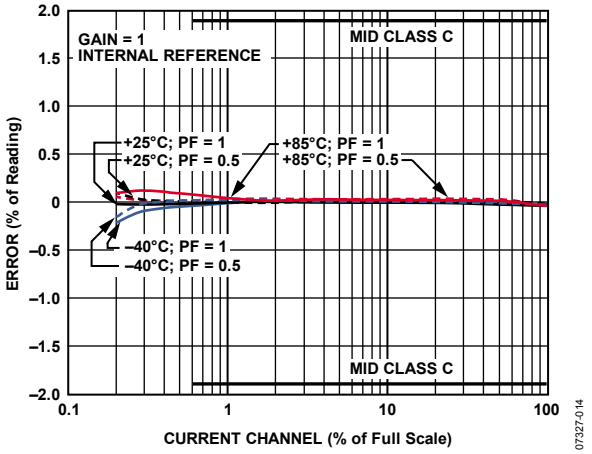


Figure 14. Current RMS Error as a Percentage of Reading (Gain = 1) over Power Factor with Internal Reference

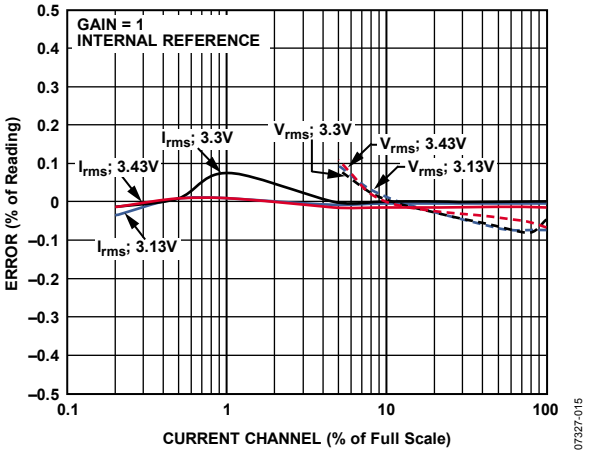


Figure 15. Voltage and Current RMS Error as a Percentage of Reading (Gain = 1) over Power Supply with Internal Reference

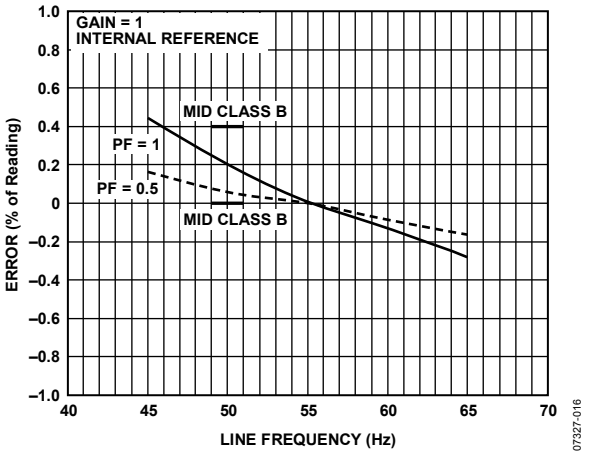


Figure 16. Active Energy Error as a Percentage of Reading (Gain = 1) over Frequency with Internal Reference

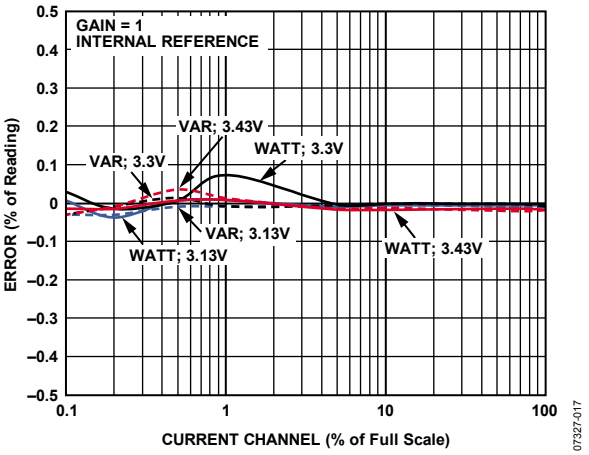


Figure 17. Active and Reactive Energy Error as a Percentage of Reading (Gain = 1) over Power Supply with Internal Reference

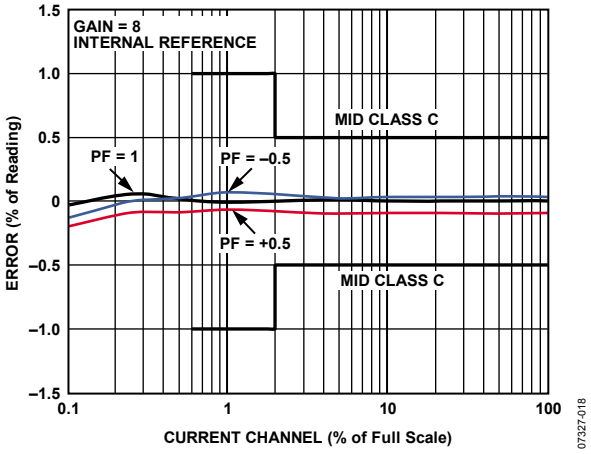


Figure 18. Active Energy Error as a Percentage of Reading (Gain = 8) over Power Factor with Internal Reference

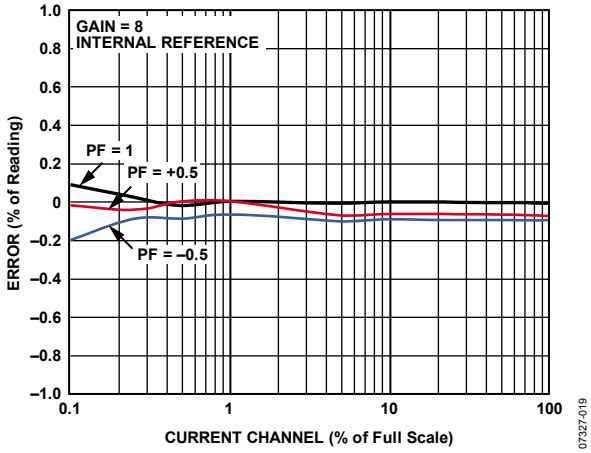


Figure 19. Reactive Energy Error as a Percentage of Reading (Gain = 8) over Power Factor with Internal Reference

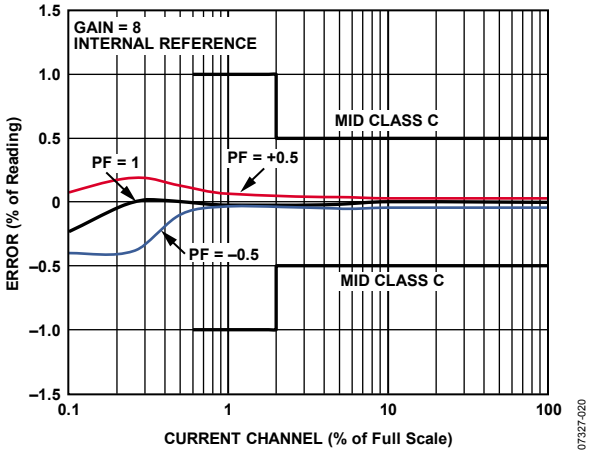


Figure 20. Current RMS Error as a Percentage of Reading (Gain = 8) over Power Factor with Internal Reference

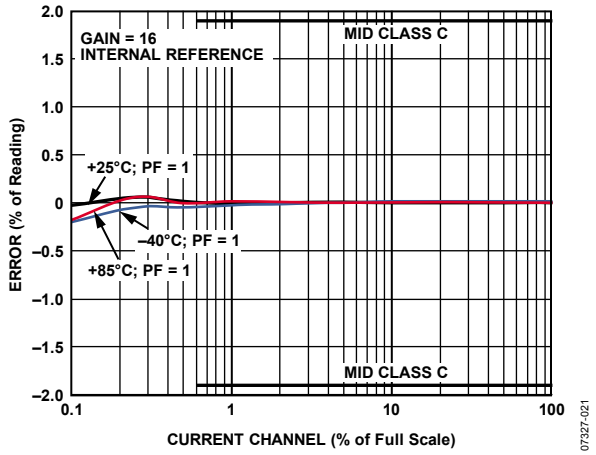


Figure 21. Active Energy Error as a Percentage of Reading (Gain = 16) over Temperature with Internal Reference

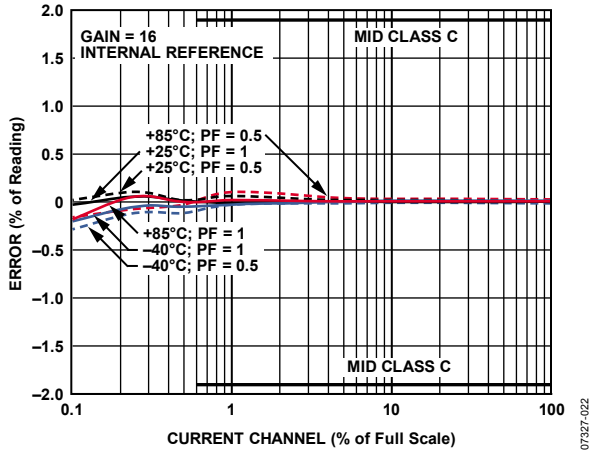


Figure 22. Active Energy Error as a Percentage of Reading (Gain = 16) over Power Factor with Internal Reference

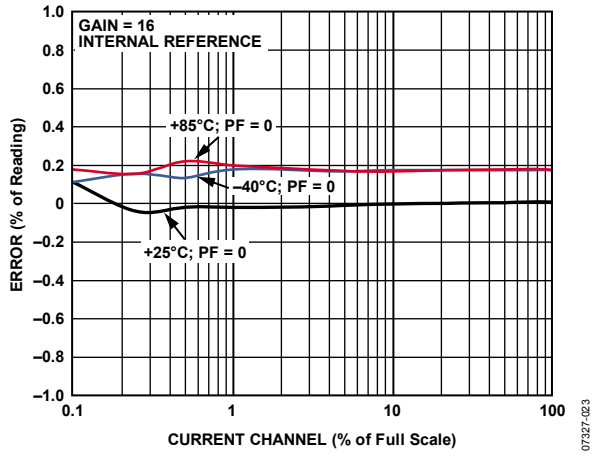


Figure 23. Reactive Energy Error as a Percentage of Reading (Gain = 16) over Temperature with Internal Reference

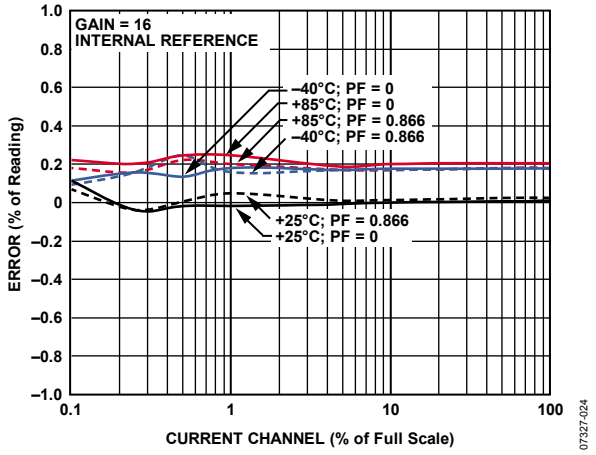


Figure 24. Reactive Energy Error as a Percentage of Reading (Gain = 16) over Power Factor with Internal Reference

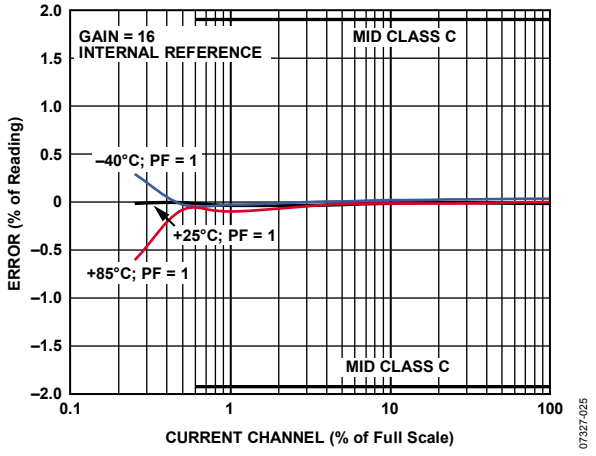


Figure 25. Current RMS Error as a Percentage of Reading (Gain = 16) over Temperature with Internal Reference

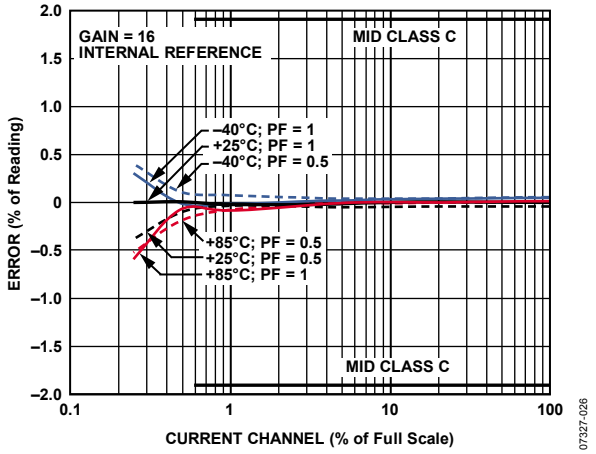


Figure 26. Current RMS Error as a Percentage of Reading (Gain = 16) over Power Factor with Internal Reference

TERMINOLOGY

Measurement Error
The error associated with the energy measurement made by the ADE7518 is defined by the following formula:

$$Percentage\ Error = \left(\frac{Energy\ Register - True\ Energy}{True\ Energy} \right) \times 100\%$$

Phase Error Between Channels
The digital integrator and the high-pass filter (HPF) in the current channel have a nonideal phase response. To offset this phase response and equalize the phase response between channels, two phase correction networks are placed in the current channel: one for the digital integrator and the other for the HPF. The phase correction networks correct the phase response of the corresponding component and ensure a phase match between current channel and voltage channel to within ±0.1° over a range of 45 Hz to 65 Hz with the digital integrator off. With the digital integrator on, the phase is corrected to within ±0.4° over a range of 45 Hz to 65 Hz.

Power Supply Rejection (PSR)
PSR quantifies the ADE7518 measurement error as a percentage of reading when the power supplies are varied. For the ac PSR measurement, a reading at nominal supplies (3.3 V) is taken. A second reading is obtained with the same input signal levels when an ac (100 mV rms/120 Hz) signal is introduced onto the supplies. Any error introduced by this ac signal is expressed as a percentage of reading (see the Measurement Error definition).

For the dc PSR measurement, a reading at nominal supplies (3.3 V) is taken. A second reading is obtained with the same input signal levels when the supplies are varied ±5%. Any error introduced is again expressed as a percentage of the reading.

ADC Offset Error
ADC offset error is the dc offset associated with the analog inputs to the ADCs. It means that, with the analog inputs connected to AGND, the ADCs still see a dc analog input signal. The magnitude of the offset depends on the gain and input range selection (see the Typical Performance Characteristics section). However, when HPF1 is switched on, the offset is removed from the current channel, and the power calculation is not affected by this offset. The offsets can be removed by performing an offset calibration (see the Analog Inputs section).

Gain Error
Gain error is the difference between the measured ADC output code (minus the offset) and the ideal output code (see the Current Channel ADC section and the Voltage Channel ADC section). It is measured for each of the gain settings on the current channel (1, 2, 4, 8, and 16). The difference is expressed as a percentage of the ideal code.

SFR MAPPING

Table 13.

Mnemonic	Address	Details
INTPR	0xFF	Table 15
SCRATCH4	0xFE	Table 23
SCRATCH3	0xFD	Table 22
SCRATCH2	0xFC	Table 21
SCRATCH1	0xFB	Table 20
IPSMF	0xF8	Table 16
TEMPCAL	0xF7	Table 116
RTCCOMP	0xF6	Table 115
BATPR	0xF5	Table 17
PERIPH	0xF4	Table 18
B	0xF0	Table 45
LCDSEGE2	0xED	Table 77
IPSME	0xEC	Table 19
SPISTAT	0xEA	Table 131
SPI2CSTAT	0xEA	Table 135
SPIMOD2	0xE9	Table 130
I2CADR	0xE9	Table 134
SPIMOD1	0xE8	Table 129
I2CMOD	0xE8	Table 133
WAV2H	0xE7	Table 29
WAV2M	0xE6	Table 29
WAV2L	0xE5	Table 29
WAV1H	0xE4	Table 29
WAV1M	0xE3	Table 29
WAV1L	0xE2	Table 29
ACC	0xE0	Table 45
MIRQSTH	0xDE	Table 39
MIRQSTM	0xDD	Table 38
MIRQSTL	0xDC	Table 37
MIRQENH	0xDB	Table 42
MIRQENM	0xDA	Table 41
MIRQENL	0xD9	Table 40
IRMSH	0xD6	Table 29
IRMSM	0xD5	Table 29
IRMSL	0xD4	Table 29
VRMSH	0xD3	Table 29
VRMSM	0xD2	Table 29
VRMSL	0xD1	Table 29
PSW	0xD0	Table 46
TH2	0xCD	Table 99
TL2	0xCC	Table 100
RCAP2H	0xCB	Table 101
RCAP2L	0xCA	Table 102
T2CON	0xC8	Table 94
EADRH	0xC7	Table 89
EADRL	0xC6	Table 88
POWCON	0xC5	Table 24
KYREG	0xC1	Table 105
WDCON	0xC0	Table 65
PROTR	0xBF	Table 87
PROTB1	0xBE	Table 86
PROTB0	0xBD	Table 85
EDATA	0xBC	Table 84
PROTKY	0xBB	Table 83
FLSHKY	0xBA	Table 82
ECON	0xB9	Table 81
IP	0xB8	Table 59
PINMAP2	0xB4	Table 140
PINMAP1	0xB3	Table 139
PINMAP0	0xB2	Table 138
LCDCONY	0xB1	Table 70
CFG	0xAF	Table 52
LCDDAT	0xAE	Table 76
LCDPTR	0xAC	Table 75
IEIP2	0xA9	Table 60
IE	0xA8	Table 58
DPCON	0xA7	Table 56
INTVAL	0xA6	Table 114
HOUR	0xA5	Table 113
MIN	0xA4	Table 112
SEC	0xA3	Table 111
HTHSEC	0xA2	Table 110
TIMECON	0xA1	Table 109
P2	0xA0	Table 143
EPCFG	0x9F	Table 137
SBAUDT	0x9E	Table 123
SBAUDF	0x9D	Table 124
LCDCONX	0x9C	Table 69
SPI2CRx	0x9B	Table 128
SPI2CTx	0x9A	Table 127
SBUF	0x99	Table 122
SCON	0x98	Table 121
LCDSEGE	0x97	Table 74
LCDCLK	0x96	Table 71
LCDCON	0x95	Table 68
MDATH	0x94	Table 29
MDATM	0x93	Table 29
MDATL	0x92	Table 29
MADDPT	0x91	Table 29
P1	0x90	Table 142
TH1	0x8D	Table 97
TH0	0x8C	Table 95
TL1	0x8B	Table 98
TL0	0x8A	Table 96
TMOD	0x89	Table 92
TCON	0x88	Table 93
PCON	0x87	Table 47
DPH	0x83	Table 49
DPL	0x82	Table 48
SP	0x81	Table 51
P0	0x80	Table 141

POWER MANAGEMENT

The ADE7518 has elaborate power management circuitry that manages the regular power supply to battery switchover and power supply failures. The power management functionalities can be accessed directly through the 8052 SFRs (see Table 14).

Table 14. Power Management SFRs

SFR Address	R/W	Mnemonic	Description
0xEC	R/W	IPSME	Power Management Interrupt Enable. See Table 19.
0xF5	R/W	BATPR	Battery Switchover Configuration. See Table 17.
0xF8	R/W	IPSMF	Power Management Interrupt Flag. See Table 16.
0xFF	R/W	INTPR	Interrupt Pins Configuration. See Table 15.
0xF4	R/W	PERIPH	Peripheral Configuration SFR. See Table 18.
0xC5	R/W	POWCON	Power Control. See Table 24.
0xFB	R/W	SCRATCH1	Scratch Pad 1. See Table 20.
0xFC	R/W	SCRATCH2	Scratch Pad 2. See Table 21.
0xFD	R/W	SCRATCH3	Scratch Pad 3. See Table 22.
0xFE	R/W	SCRATCH4	Scratch Pad 4. See Table 23.

POWER MANAGEMENT REGISTER DETAILS

Table 15. Interrupt Pins Configuration SFR (INTPR, 0xFF)

Bit	Mnemonic	Default	Description	
7	RTCCAL	0	Controls the RTC calibration output. When this bit is set, the RTC calibration frequency selected by FSEL[1:0] is output on the P0.2/CF1/RTCCAL pin.	
6 to 5	FSEL[1:0]	00	Sets the RTC calibration output frequency and calibration window.	
			FSEL[1:0]	**Result (Calibration Window, Frequency)**
			00	30.5 sec, 1 Hz
			01	30.5 sec, 512 Hz
			10	0.244 sec, 500 Hz
			11	0.244 sec, 16.384 kHz
4	Reserved	N/A		
3 to 1	INT1PRG[2:0]	000	Controls the function of $\overline{\text{INT1}}$.	
			INT1PRG[2:0]	**Result**
			x00	GPIO enabled
			x01	BCTRL enabled
			01x	$\overline{\text{INT1}}$ input disabled
			11x	$\overline{\text{INT1}}$ input enabled
0	INT0PRG	0	Controls the function of $\overline{\text{INT0}}$.	
			INT0PRG	**Result**
			0	$\overline{\text{INT0}}$ input disabled
			1	$\overline{\text{INT0}}$ input enabled

Writing to the Interrupt Pins Configuration SFR (INTPR, 0xFF)

To protect the RTC from runaway code, a key must be written to the Key SFR (KYREG, 0xC1) to obtain write access to INTPR. KYREG (see Table 105) should be set to 0xEA to unlock this SFR and then reset to zero after a timekeeping register is written to. The RTC registers can be written using the following 8052 assembly code:

```
MOV    KYREG, #0EAh
MOV    INTPR, #080h
```

Table 16. Power Management Interrupt Flag SFR (IPSMF, 0xF8)

Bit	Address	Mnemonic	Default	Description
7	0xFF	FPSR	0	Power Supply Restored Interrupt Flag. Set when the V_{DD} power supply has been restored. This occurs when the source of V_{SWOUT} changes from V_{BAT} to V_{DD}.
6	0xFE	FPSM	0	PSM Interrupt Flag. Set when an enabled PSM interrupt condition occurs.
5	0xFD	FSAG	0	Voltage SAG Interrupt Flag. Set when an ADE energy measurement SAG condition occurs.
4	0xFC	Reserved	0	This bit must be kept cleared for proper operation.
3	0xFB	Reserved	0	This bit must be kept cleared for proper operation.
2	0xFA	Reserved	0	This bit must be kept cleared for proper operation.
1	0xF9	FBSO	0	Battery Switchover Interrupt Flag. Set when V_{SWOUT} switches from V_{DD} to $V_{BAT.}$
0	0xF8	FVDCIN	0	V_{DCIN} Monitor Interrupt Flag. Set when V_{DCIN} falls below 1.2 V.

Table 17. Battery Switchover Configuration SFR (BATPR, 0xF5)

Bit	Mnemonic	Default	Description	
7 to 2	Reserved	0	These bits must be kept to 0 for proper operation.	
1 to 0	BATPRG[1:0]	00	Control Bits for Battery Switchover.	
			BATPRG[1:0]	**Result**
			00	Battery switchover enabled on low V_{DD}
			01	Battery switchover enabled on low V_{DD} and low V_{DCIN}
			1x	Battery switchover disabled

Table 18. Peripheral Configuration SFR (PERIPH, 0xF4)

Bit	Mnemonic	Default	Description	
7	RXFLAG	0	If set, indicates that an Rx edge event triggered wake-up from PSM2.	
6	VSWSOURCE	1	Indicates the power supply that is internally connected to V_{SWOUT} (0 $V_{SWOUT} = V_{BAT}$, 1 $V_{SWOUT} = V_{DD}$).	
5	VDD_OK	1	If set, indicates that the V_{DD} power supply is ready for operation.	
4	PLL_FLT	0	If set, indicates that a PLL fault occurred where the PLL lost lock. Set the PLL_FTL_ACK bit (see Table 107) in the Start ADC Measurement SFR (ADCGO, 0xD8) to acknowledge the fault and clear the PLL_FLT bit.	
3	Reserved	0	This bit should be kept to 0.	
2	Reserved	0	This bit should be kept to 0.	
1 to 0	RXPROG[1:0]	00	Controls the function of the P1.0/RxD pin.	
			RXPROG[1:0]	**Result**
			00	GPIO
			01	RxD with wake-up disabled
			11	RxD with wake-up enabled

Table 19. Power Management Interrupt Enable SFR (IPSME, 0xEC)

Bit	Mnemonic	Default	Description
7	EPSR	0	Enables a PSM interrupt when the power supply restored flag (FPSR) is set.
6	Reserved	0	Reserved.
5	ESAG	0	Enables a PSM interrupt when the voltage SAG flag (FSAG) is set.
4 to 2	Reserved	0	These bits must be kept cleared for proper operation.
1	EBSO	0	Enables a PSM interrupt when the battery switchover flag (FBSO) is set.
0	EVDCIN	0	Enables a PSM interrupt when the V_{DCIN} monitor flag (FVDCIN) is set.

Table 20. Scratch Pad 1 SFR (SCRATCH1, 0xFB)

Bit	Mnemonic	Default	Description
7 to 0	SCRATCH1	0	Value can be written/read in this register. This value is maintained in all the power saving modes.

Table 21. Scratch Pad 2 SFR (SCRATCH2, 0xFC)

Bit	Mnemonic	Default	Description
7 to 0	SCRATCH2	0	Value can be written/read in this register. This value is maintained in all the power saving modes.

Table 22. Scratch Pad 3 SFR (SCRATCH3, 0xFD)

Bit	Mnemonic	Default	Description
7 to 0	SCRATCH3	0	Value can be written/read in this register. This value is maintained in all the power saving modes.

Table 23. Scratch Pad 4 SFR (SCRATCH4, 0xFE)

Bit	Mnemonic	Default	Description
7 to 0	SCRATCH4	0	Value can be written/read in this register. This value is maintained in all the power saving modes.

Clearing the Scratch Pad Registers (SCRATCH1, 0xFB to SCRATCH4, 0xFE)

Note that these scratch pad registers are only cleared when the part loses V_{DD} and V_{BAT}. They are not cleared by software, watchdog, or PLL reset and, therefore, need to be set correctly in these situations.

Table 24. Power Control SFR (POWCON, 0xC5)

Bit	Mnemonic	Default	Description	
7	Reserved	1	Reserved.	
6	METER_OFF	0	Set this bit to turn off the modulators and energy metering DSP circuitry to reduce power if metering functions are not needed in PSM0.	
5	Reserved	0	This bit should be kept at 0 for proper operation.	
4	COREOFF	0	Set this bit to shut down the core and enter PSM2 if in PSM1 operating mode.	
3	Reserved	0	Reserved.	
2 to 0	CD[2:0]	010	Controls the core clock frequency, f_{CORE}. f_{CORE} = 4.096 MHz/2^{CD}.	
			CD[2:0]	**Result (f_{CORE} in MHz)**
			000	4.096
			001	2.048
			010	1.024
			011	0.512
			100	0.256
			101	0.128
			110	0.064
			111	0.032

Writing to the Power Control SFR (POWCON, 0xC5)

Writing data to the POWCON SFR involves writing 0xA7 into the Key SFR (KYREG, 0xC1), which is described in Table 105, followed by a write to the POWCON SFR. For example,

```
MOV KYREG,#0A7h     ;Write KYREG to 0xA7 to get write access to the POWCON SFR
MOV POWCON,#10h     ;Shutdown the core
```

POWER SUPPLY ARCHITECTURE

The ADE7518 has two power supply inputs, V_{DD} and V_{BAT}, and requires only a single 3.3 V power supply at V_{DD} for full operation. A battery backup, or secondary power supply, with a maximum of 3.7 V, can be connected to the V_{BAT} input. Internally, the ADE7518 connects V_{DD} or V_{BAT} to V_{SWOUT}, which is used to derive power for the ADE7518 circuitry. The V_{SWOUT} output pin reflects the voltage at the internal power supply (V_{SWOUT}) and has a maximum output current of 6 mA. This pin can also be used to power a limited number of peripheral components. The 2.5 V analog supply (V_{INTA}) and the 2.5 V supply for the core logic (V_{INTD}) are derived by on-chip linear regulators from V_{SWOUT}. Figure 27 shows the power supply architecture of ADE7518.

The ADE7518 provides automatic battery switchover between V_{DD} and V_{BAT} based on the voltage level detected at V_{DD} or V_{DCIN}. Additionally, the BCTRL input can be used to trigger a battery switchover. The conditions for switching V_{SWOUT} from V_{DD} to V_{BAT} and back to V_{DD} are described in the Battery Switchover section. V_{DCIN} is an input pin that can be connected to a 0 V to 3.3 V dc signal. This input is intended for power supply supervisory purposes and does not provide power to the ADE7518 circuitry (see the Battery Switchover section).

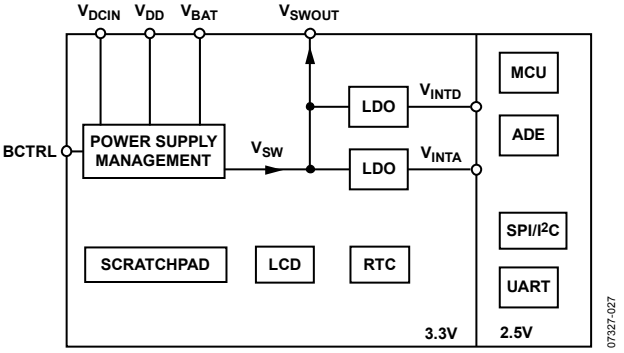


Figure 27. Power Supply Architecture

BATTERY SWITCHOVER

The ADE7518 monitors V_{DD}, V_{BAT}, and V_{DCIN}. Automatic battery switchover from V_{DD} to V_{BAT} can be configured based on the status of the V_{DD}, V_{DCIN}, or BCTRL pin. Battery switchover is enabled by default. Setting Bit 1 in the Battery Switchover Configuration SFR (BATPR, 0xF5) disables battery switchover so that V_{DD} is always connected to V_{SWOUT} (see Table 17). The source of V_{SWOUT} is indicated by Bit 6 in the Peripheral Configuration SFR (PERIPH, 0xF4), which is described in Table 18. Bit 6 is set when V_{SWOUT} is connected to V_{DD} and cleared when V_{SWOUT} is connected to V_{BAT}.

The battery switchover functionality provided by the ADE7518 allows a seamless transition from V_{DD} to V_{BAT}. An automatic battery switchover option ensures a stable power supply to the ADE7518, as long as the external battery voltage is above 2.75 V. It allows continuous code execution even while the internal power supply is switching from V_{DD} to V_{BAT} and back. Note that the energy metering ADCs are not available when V_{BAT} is being used for V_{SWOUT}.

Power supply management (PSM) interrupts can be enabled to indicate when battery switchover occurs and when the V_{DD} power supply is restored (see the Power Supply Management (PSM) Interrupt section).

V_{DD} to V_{BAT}

The following three events switch the internal power supply (V_{SWOUT}) from V_{DD} to V_{BAT}:

- V_{DCIN} < 1.2 V. When V_{DCIN} falls below 1.2 V, V_{SWOUT} switches from V_{DD} to V_{BAT}. This event is enabled when the BATPRG[1:0] bits in the Battery Switchover Configuration SFR (BATPR, 0xF5) = 0b01. Setting these bits disables switchover based on V_{DCIN}. Battery switchover on low V_{DCIN} is disabled by default.
- V_{DD} < 2.75 V. When V_{DD} falls below 2.75 V, V_{SWOUT} switches from V_{DD} to V_{BAT}. This event is enabled when BATPRG[1:0] in the BATPR SRF are cleared.
- Falling edge on BCTRL. When the battery control pin, BCTRL, goes low, V_{SWOUT} switches from V_{DD} to V_{BAT}. This external switchover signal can trigger a switchover to V_{BAT} at any time. Setting the bits INT1PRG[2:0] to 0bx01 in the Interrupt Pins Configuration SFR (INTPR, 0xFF) enables the battery control pin (see Table 15).

Switching from V_{BAT} to V_{DD}

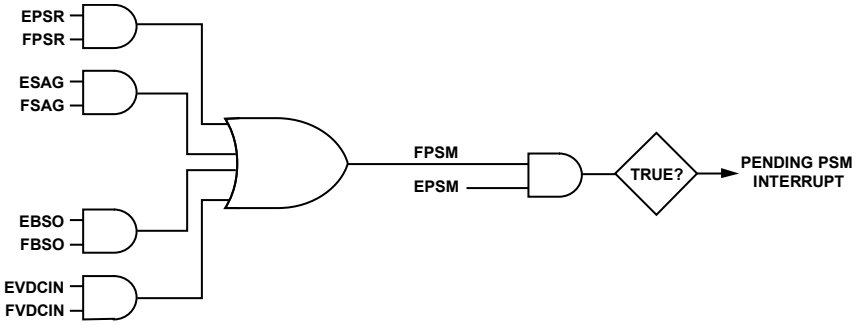
To switch V_{SWOUT} from V_{BAT} to V_{DD}, all of the following events that are enabled to force battery switchover must be false:

- V_{DCIN} < 1.2 V and V_{DD} < 2.75 V enabled. If the low V_{DCIN} condition is enabled, V_{SWOUT} switches to V_{DD} after V_{DCIN} remains above 1.2 V and V_{DD} remains above 2.75 V.
- V_{DD} < 2.75 V enabled. V_{SWOUT} switches back to V_{DD} after V_{DD} remains above 2.75 V.
- BCTRL enabled. V_{SWOUT} switches back to V_{DD} after BCTRL is high, and the first or second bullet point is satisfied.

POWER SUPPLY MANAGEMENT (PSM) INTERRUPT

The power supply management (PSM) interrupt alerts the 8052 core of power supply events. The PSM interrupt is disabled by default. Setting the EPSM bit in the Interrupt Enable and Priority 2 SFR (IEIP2, 0xA9) enables the PSM interrupt (see Table 60).

The Power Management Interrupt Enable SFR (IPSME, 0xEC) controls the events that result in a PSM interrupt (see Table 19). Figure 28 is a diagram illustrating how the PSM interrupt vector is shared among the PSM interrupt sources. The PSM interrupt flags are latched and must be cleared by writing to the IPSMF flag register (see Table 16).



IPSME ADDR. 0xEC	EPSR	RESERVED	ESAG	RESERVED	RESERVED	RESERVED	EBSO	EVDCIN
IPSMF ADDR. 0xF8	FPSR	FPSM	FSAG	RESERVED	RESERVED	RESERVED	FBSO	FVDCIN
IEIP2 ADDR. 0xA9	RESERVED	PTI	RESERVED	PSI	EADE	ETI	EPSM	ESI

NOT INVOLVED IN PSM INTERRUPT SIGNAL CHAIN

07327-028

Figure 28. PSM Interrupt Sources

Battery Switchover and Power Supply Restored PSM Interrupt

The ADE7518 can be configured to generate a PSM interrupt when the source of V_{SWOUT} changes from V_{DD} to V_{BAT}, indicating battery switchover. Setting the EBSO bit in the Power Management Interrupt Enable SFR (IPSME, 0xEC) enables this event to generate a PSM interrupt (see Table 19).

The ADE7518 can also be configured to generate an interrupt when the source of V_{SWOUT} changes from V_{BAT} to V_{DD}, indicating that the V_{DD} power supply has been restored. Setting the EPSR bit in the Power Management Interrupt Enable SFR (IPSME, 0xEC) enables this event to generate a PSM interrupt.

The flags in the IPSMF SFR for these interrupts, FBSO and FPSR, are set regardless of whether the respective enable bits have been set. The battery switchover and power supply restore event flags, FBSO and FPSR, are latched. These events must be cleared by writing 0 to these bits. Bit 6 in the Peripheral Configuration SFR (PERIPH, 0xF4), VSWSOURCE, tracks the source of V_{SWOUT}. The bit is set when V_{SWOUT} is connected to V_{DD} and cleared when V_{SWOUT} is connected to V_{BAT}.

V_{DCIN} Monitor PSM Interrupt

The V_{DCIN} voltage is monitored by a comparator. The FVDCIN bit in the Power Management Interrupt Flag SFR (IPSMF, 0xF8) is set when the V_{DCIN} input level is lower than 1.2 V. Setting the EVDCIN bit in the IPSME SFR enables this event to generate a PSM interrupt. This event, which is associated with the SAG monitoring, can be used to detect a power supply (V_{DD}) being compromised and to trigger further actions prior to deciding a switch of V_{DD} to V_{BAT}.

SAG Monitor PSM Interrupt

The ADE7518 energy measurement DSP monitors the ac voltage input at the V_P and V_N input pins. The SAGLVL register is used to set the threshold for a line voltage SAG event. The FSAG bit in the Power Management Interrupt Flag SFR (IPSMF, 0xF8) is set if the line voltage stays below the level set in the SAGLVL register for the number of line cycles set in the SAGCYC register. See the Line Voltage SAG Detection section for more information. Setting the ESAG bit in the Power Management Interrupt Enable SFR (IPSME, 0xEC) enables this event to generate a PSM interrupt.

USING THE POWER SUPPLY FEATURES

In an energy meter application, the 3.3 V power supply (V_{DD}) is typically generated from the ac line voltage and regulated to 3.3 V by a voltage regulator IC. The preregulated dc voltage, typically 5 V to 12 V, can be connected to V_{DCIN} through a resistor divider. A 3.6 V battery can be connected to V_{BAT}. Figure 29 shows how the ADE7518 power supply inputs are set up in this application.

Figure 30 shows the sequence of events that occurs if the main power supply generated by the PSU starts to fail in the power meter application shown in Figure 29. The SAG detection can provide the earliest warning of a potential problem on V_{DD}.

When a SAG event occurs, user code can be configured to back up data and prepare for battery switchover if desired. The relative spacing of these interrupts depends on the design of the power supply.

Figure 31 shows the sequence of events that occurs if the main power supply starts to fail in the power meter application shown in Figure 29, with battery switchover on low V_{DCIN} or low V_{DD} enabled.

Finally, the transition between V_{DD} and V_{BAT} and the different power supply modes (see the Operating Modes section) are represented in Figure 32 and Figure 33.

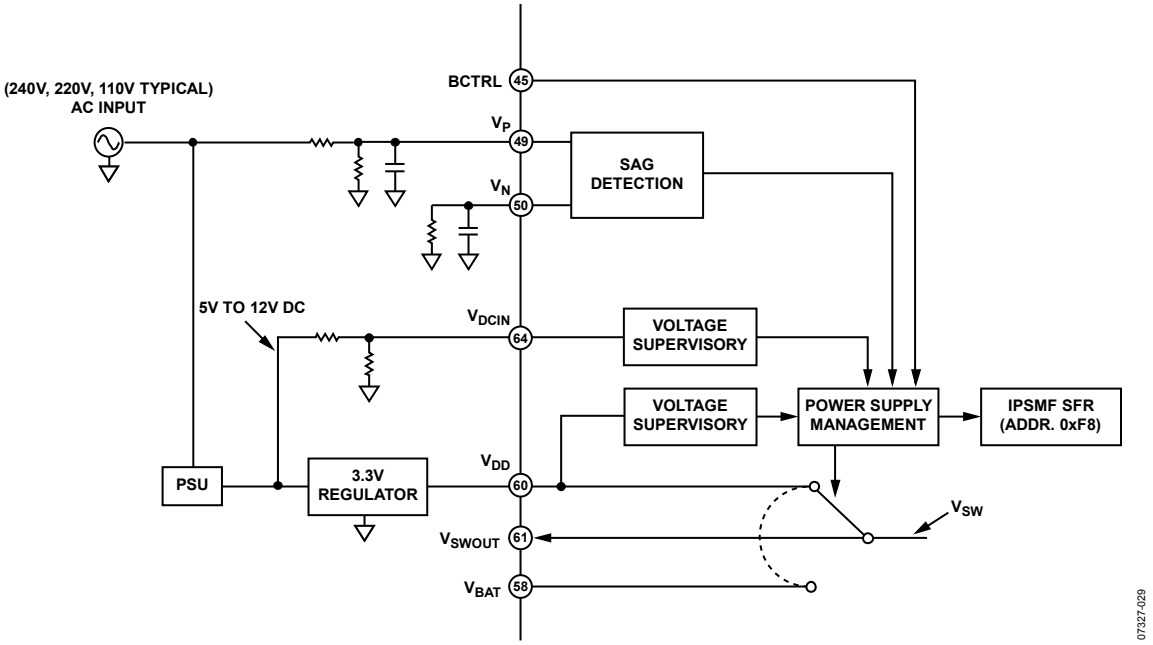


Figure 29. Power Supply Management for Energy Meter Application

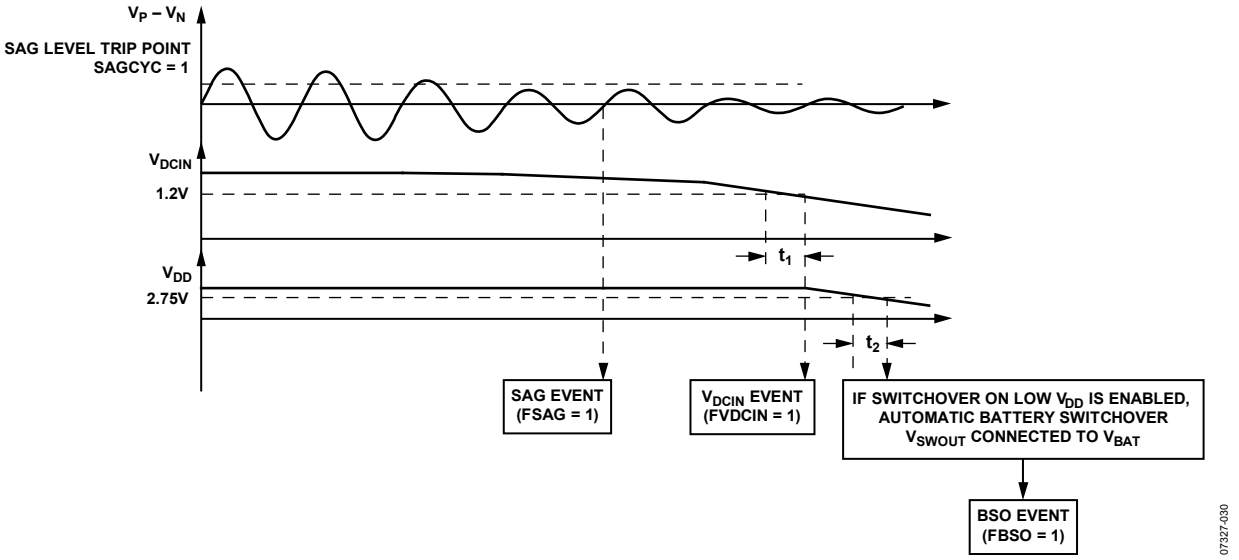


Figure 30. Power Supply Management Interrupts and Battery Switchover with Only V_{DD} Enabled for Battery Switchover

Table 25. Power Supply Event Timing Operating Modes

Parameter	Time	Description
t_1	10 ns min	Time between when V_{DCIN} falls below 1.2 V and when FVDCIN is raised.
t_2	10 ns min	Time between when V_{DD} falls below 2.75 V and when battery switchover occurs.
t_3	30 ms typ	Time between when V_{DCIN} falls below 1.2 V and when battery switchover occurs if V_{DCIN} is enabled to cause battery switchover.
t_4	130 ms typ	Time between when power supply restore conditions are met (V_{DCIN} above 1.2 V and V_{DD} above 2.75 V if BATPR[1:0] = 0b01 or V_{DD} above 2.75 V if BATPR[1:0] = 0b00) and when V_{SWOUT} switches to V_{DD}.

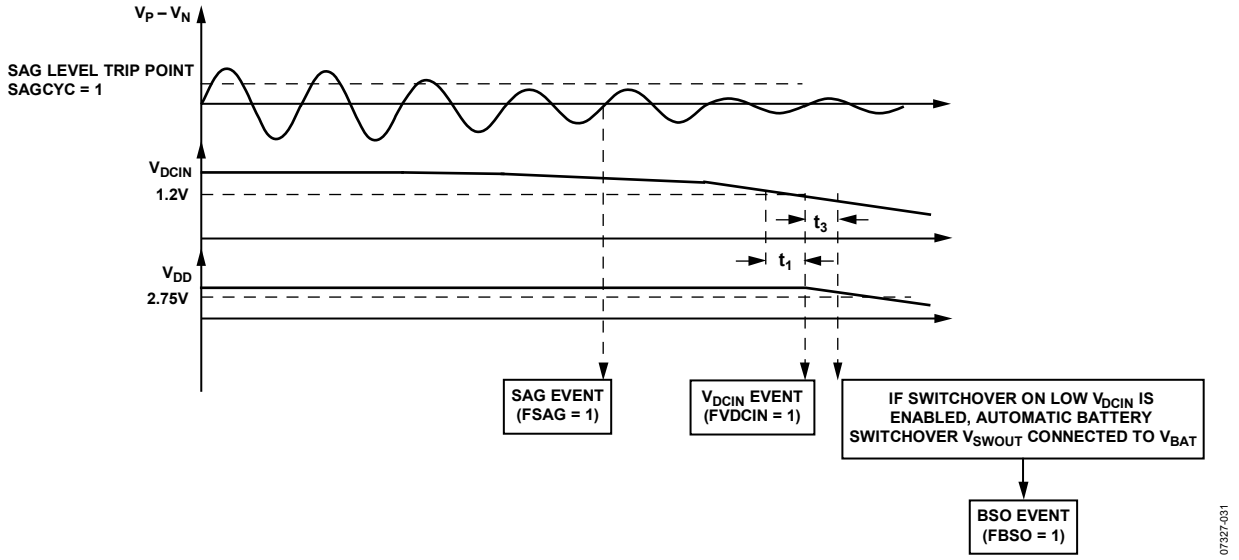


Figure 31. Power Supply Management Interrupts and Battery Switchover with V_{DD} or V_{DCIN} Enabled for Battery Switchover

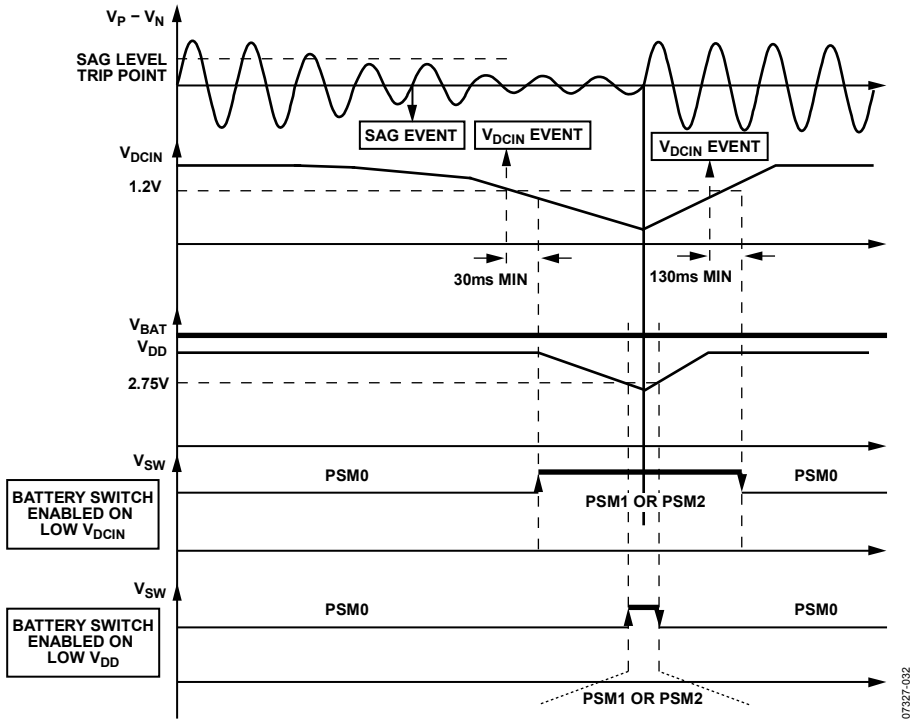


Figure 32. Power Supply Management Transitions Between Modes

OPERATING MODES

PSM0 (NORMAL MODE)

In PSM0, normal operating mode, V_{SWOUT} is connected to V_{DD}. All of the analog circuitry and digital circuitry powered by V_{INTD} and V_{INTA} are enabled by default. In normal mode, the default clock frequency, f_{CORE}, established during a power-on reset or software reset, is 1.024 MHz.

PSM1 (BATTERY MODE)

In PSM1, battery mode, V_{SWOUT} is connected to V_{BAT}. In this operating mode, the 8052 core and all of the digital circuitry are enabled by default. The analog circuitry for the ADE energy metering DSP powered by V_{INTA} is disabled. This analog circuitry automatically restarts, and the switch to the V_{DD} power supply occurs when the V_{DD} supply is above 2.75 V and the PWRDN bit in the MODE1 register (0x0B) is cleared (see Table 31). The default f_{CORE} for PSM1, established during a power-on reset or software reset, is 1.024 MHz.

PSM2 (SLEEP MODE)

PSM2 is a low power consumption sleep mode for use in battery operation. In this mode, V_{SWOUT} is connected to V_{BAT}. All of the 2.5 V digital and analog circuitry powered through V_{INTA} and V_{INTD} are disabled, including the MCU core, resulting in the following:

- The RAM in the MCU is no longer valid.
- The program counter for the 8052, also held in volatile memory, becomes invalid when the 2.5 V supply is shut down. Therefore, the program does not resume from where it left off but always starts from the power-on reset vector when the ADE7518 exits PSM2.

The 3.3 V peripherals (RTC, and LCD) are active in PSM2. They can be enabled or disabled to reduce power consumption and are configured for PSM2 operation when the MCU core is active (see Table 27 for more information about the individual peripherals and their PSM2 configuration). The ADE7518 remains in PSM2 until an event occurs to wake them up.

In PSM2, the ADE7518 provides four scratch pad RAM SFRs that are maintained during this mode. These SFRs can be used to save data from PSM0 or PSM1 when entering PSM2 (see Table 20 to Table 23).

In PSM2, the ADE7518 maintains some SFRs (see Table 26). The SFRs that are not listed in this table should be restored when the part enters PSM0 or PSM1 from PSM2.

Table 26. SFRs Maintained in PSM2

I/O Configuration	Power Supply Management	RTC Peripherals	LCD Peripherals
Interrupt Pins Configuration SFR (INTPR, 0xFF), see Table 15	Battery Switchover Configuration SFR (BATPR, 0xF5), see Table 17	RTC Nominal Compensation SFR (RTCCOMP, 0xF6), see Table 115	LCD Segment Enable 2 SFR (LCDSEGE2, 0xED), see Table 77
Peripheral Configuration SFR (PERIPH, 0xF4), see Table 18		RTC Temperature Compensation SFR (TEMPCAL, 0xF7), see Table 116	LCD Configuration Y SFR (LCDCONY, 0xB1), see Table 70
Port 0 Weak Pull-Up Enable SFR (PINMAP0, 0xB2), see Table 138		RTC Configuration SFR (TIMECON, 0xA1), see Table 109	LCD Configuration X SFR (LCDCONX, 0x9C), see Table 69
Port 1 Weak Pull-Up Enable SFR (PINMAP1, 0xB3), see Table 139		Hundredths of a Second Counter SFR (HTHSEC, 0xA2), see Table 110	LCD Configuration SFR (LCDCON, 0x95), see Table 68
Port 2 Weak Pull-Up Enable SFR (PINMAP2, 0xB4), see Table 140		Seconds Counter SFR (SEC, 0xA3), see Table 111	LCD Clock SFR (LCDCLK, 0x96), see Table 71
Scratch Pad 1 SFR (SCRATCH1, 0xFB), see Table 20		Minutes Counter SFR (MIN, 0xA4), see Table 112	LCD Segment Enable SFR (LCDSEGE, 0x97), see Table 74
Scratch Pad 2 SFR (SCRATCH2, 0xFC), see Table 21		Hours Counter SFR (HOUR, 0xA5), see Table 113	LCD Pointer SFR (LCDPTR, 0xAC), see Table 75
Scratch Pad 3 SFR (SCRATCH3, 0xFD), see Table 22		Alarm Interval SFR (INTVAL, 0xA6), see Table 114	LCD Data SFR (LCDDAT, 0xAE), see Table 76
Scratch Pad 4 SFR (SCRATCH4, 0xFE), see Table 23			

3.3 V PERIPHERALS AND WAKE-UP EVENTS

Some of the 3.3 V peripherals are capable of waking the ADE7518 from PSM2. The events that can cause the ADE7518 to wake up from PSM2 are listed in the Wake-Up Event column in Table 27. The interrupt flag associated with these events must be cleared prior to executing instructions that put the ADE7518 in PSM2 mode after wake-up.

Table 27. 3.3 V Peripherals and Wake-Up Events

3.3 V Peripheral	Wake-Up Event	Wake-Up Enable Bits	Flag	Interrupt Vector	Comments
Power Supply Management	PSR	Nonmaskable	PSR	IPSM	The ADE7518 wakes up if the power supply is restored (if V_{SWOUT} switches to be connected to V_{DD}). The VSWSOURCE flag, Bit 6 of the Peripheral Configuration SFR (PERIPH, 0xF4), is set to indicate that V_{SWOUT} is connected to V_{DD}.
RTC	Midnight	Nonmaskable	Midnight	IRTC	The ADE7518 wakes up at midnight every day to update its calendars. The RTC interrupt needs to be serviced and acknowledged prior to entering PSM2 mode.
	Alarm	Maskable	Alarm	IRTC	An alarm can be set to wake the ADE7518 after the desired amount of time. The RTC alarm is enabled by setting the ALARM bit in the RTC Configuration SFR (TIMECON, 0xA1). The RTC interrupt needs to be serviced and acknowledged prior to entering PSM2 mode.
I/O Ports[1]	$\overline{\text{INT0}}$	INT0PRG = 1		IE0	The edge of the interrupt is selected by Bit IT0 in the TCON register. The IE0 flag bit in the TCON register is not affected. The Interrupt 0 interrupt needs to be serviced and acknowledged prior to entering PSM2 mode.
	$\overline{\text{INT1}}$	INT1PRG[2:0] = 11x		IE1	The edge of the interrupt is selected by Bit IT1 in the TCON register. The IE1 flag bit in the TCON register is not affected. The Interrupt 1 interrupt needs to be serviced and acknowledged prior to entering PSM2 mode.
	Rx Edge	RXPROG[1:0] = 11	PERIPH[7] (RXFLAG)		An Rx edge event occurs if a rising or falling edge is detected on the Rx line. The UART RxD flag needs to be cleared prior to entering PSM2 mode.
External Reset	RESET	Nonmaskable			If the $\overline{\text{RESET}}$ pin is brought low while the ADE7518 is in PSM2, the ADE7518 wakes up to PSM1.
LCD					The LCD can be enabled/disabled in PSM2. The LCD data memory remains intact.
Scratch Pad					The four SCRATCHx registers remain intact in PSM2.

[1] All I/O pins are treated as inputs. The weak pull-up on each I/O pin can be disabled individually in the Port 0 Weak Pull-Up Enable SFR (PINMAP0, 0xB2), Port 1 Weak Pull-Up Enable SFR (PINMAP1, 0xB3), and Port 2 Weak Pull-Up Enable SFR (PINMAP2, 0xB4) to decrease current consumption. The interrupts can be enabled/disabled.

TRANSITIONING BETWEEN OPERATING MODES

The operating mode of the ADE7518 is determined by the power supply connected to V_{SWOUT}. Therefore, changes in the power supply, such as when V_{SWOUT} switches from V_{DD} to V_{BAT} or when V_{SWOUT} switches to V_{DD}, alter the operating mode. This section describes events that change the operating mode.

Automatic Battery Switchover (PSM0 to PSM1)

If any of the enabled battery switchover events occur (see the Battery Switchover section), V_{SWOUT} switches to V_{BAT}. This switchover results in a transition from the PSM0 to PSM1 operating mode. When battery switchover occurs, the analog circuitry used in the ADE energy measurement DSP is disabled. To reduce power consumption, the user code can initiate a transition to PSM2.

Entering Sleep Mode (PSM1 to PSM2)

To reduce power consumption when V_{SWOUT} is connected to V_{BAT}, user code can initiate sleep mode, PSM2, by setting Bit 4 in the Power Control SFR (POWCON, 0xC5) to shut down the MCU core. Events capable of waking the MCU can be enabled (see the 3.3 V Peripherals and Wake-Up Events section).

Servicing Wake-Up Events (PSM2 to PSM1)

The ADE7518 may need to wake up from PSM2 to service wake-up events (see the 3.3 V Peripherals and Wake-Up Events section). PSM1 code execution begins at the power-on reset vector. After servicing the wake-up event, the ADE7518 can be returned to PSM2 by setting Bit 4 in the Power Control SFR (POWCON, 0xC5) to shut down the MCU core.

Automatic Switch to V_{DD} (PSM2 to PSM0)

If the conditions to switch V_{SWOUT} from V_{BAT} to V_{DD} occur (see the Battery Switchover section), the operating mode switches to PSM0. When this switch occurs, the MCU core and the analog circuitry used in the ADE energy measurement DSP automatically restart. PSM0 code execution begins at the power-on reset vector.

Automatic Switch to V_{DD} (PSM1 to PSM0)

If the conditions to switch V_{SWOUT} from V_{BAT} to V_{DD} occur (see the Battery Switchover section), the operating mode switches to PSM0. When this switch occurs, the analog circuitry used in the ADE energy measurement DSP automatically restarts. Note that normal code execution continues. A software reset can be performed to start PSM0 code execution at the power-on reset vector.

USING THE POWER MANAGEMENT FEATURES

Because program flow is different for each operating mode, the status of V_{SWOUT} must be known at all times. The VSWSOURCE bit in the Peripheral Configuration SFR (PERIPH, 0xF4) indicates what V_{SWOUT} is connected to (see Table 18). This bit can be used to control program flow on wake-up. Because code execution always starts at the power-on reset vector, Bit 6 of the PERIPH SRF can be tested to determine which power supply is being used and to branch to normal code execution or to wake up event code execution. Power supply events can also occur when the MCU core is active. To be aware of the events that change what V_{SWOUT} is connected to, use the following guidelines:

- Enable the battery switchover interrupt (EBSO) if $V_{SWOUT} = V_{DD}$ at power-up.
- Enable the power supply restored interrupt (EPSR) if $V_{SWOUT} = V_{BAT}$ at power-up.

An early warning that battery switchover is about to occur is provided by SAG detection and possibly low V_{DCIN} detection (see the Battery Switchover section).

For a user-controlled battery switchover, enable automatic battery switchover on low V_{DD} only. Then, enable the low V_{DCIN} event to generate the PSM interrupt. When a low V_{DCIN} event occurs, start data backup. Upon completion of the data backup, enable battery switchover on low V_{DCIN}. Battery switchover occurs 30 ms later.

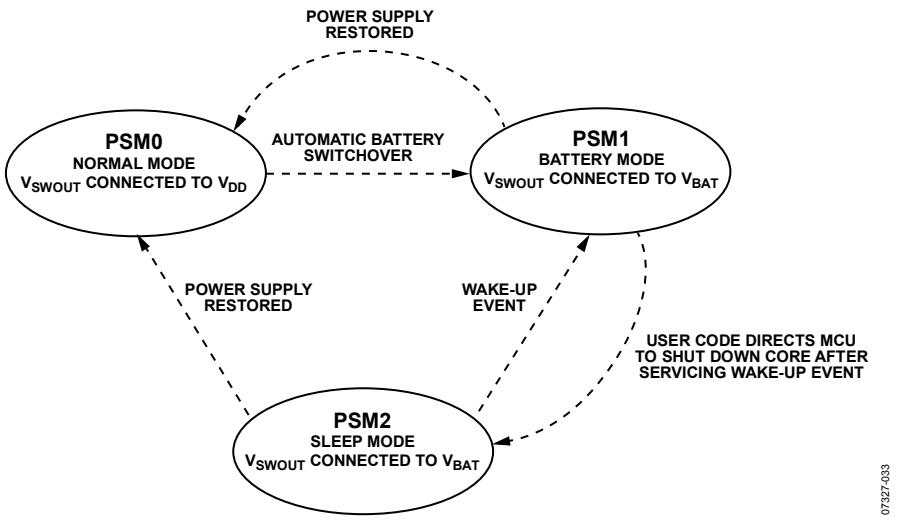


Figure 33. Transitioning Between Operating Modes

ENERGY MEASUREMENT

The ADE7518 offers a fixed function, energy measurement, digital processing core that provides all the information needed to measure energy in single-phase energy meters. The part provides two ways to access the energy measurements: direct access through SFRs for time sensitive information and indirect access through address and data SFR registers for the majority of energy measurements. The I_{rms}, V_{rms}, interrupts, and waveform registers are readily available through SFRs, as shown in Table 29. Other energy measurement information is mapped to a page of memory that is accessed indirectly through the MADDPT, MDATL, MDATM, and MDATH SFRs. The address and data registers act as pointers to the energy measurement internal registers.

ACCESS TO ENERGY MEASUREMENT SFRs

Access to the energy measurement SFRs is achieved by reading or writing to the SFR addresses detailed in Table 29. The internal data for the MIRQx SFRs are latched byte by byte into the SFR when the SFR is read.

The WAV1x, WAV2x, VRMSx, and IRMSx registers are all 3-byte SFRs. The 24-bit data is latched into these SFRs when the high byte is read. Reading the low or medium byte before the high byte results in reading the data from the previous latched sample.

Sample code to read the VRMSx register is as follows:

```
MOV    R1, VRMSH     ;latches data in VRMSH,
                     VRMSM, and VRMSL SFRs
MOV    R2, VRMSM
MOV    R3, VRMSL
```

ACCESS TO INTERNAL ENERGY MEASUREMENT REGISTERS

Access to the internal energy measurement registers is achieved by writing to the Energy Measurement Pointer Address SFR (MADDPT, 0x91). This SFR selects the energy measurement register to be accessed and determines if a read or a write is performed (see Table 28).

Table 28. Energy Measurement Pointer Address SFR (MADDPT, 0x91)

Bit	Description
7	1 = write, 0 = read
6 to 0	Energy measurement internal register address

Writing to the Internal Energy Measurement Registers

When Bit 7 of the Energy Measurement Pointer Address SFR (MADDPT, 0x91) is set, the contents of the MDATx SFRs (MDATL, MDATM, and MDATH) are transferred to the internal energy measurement register designated by the address in the MADDPT SFR. If the internal register is 1 byte long, only the MDATL SFR content is copied to the internal register, and the MDATM SFR and MDATH SFR contents are ignored.

The energy measurement core functions with an internal clock of 4.096 MHz/5, or 819.2 kHz. Because the 8052 core functions with another clock, 4.096 MHz/2^{CD}, synchronization between the two clock environments when CD = 0 or 1 is an issue. When data is written to the internal energy measurement registers, a small wait period needs to be implemented before another read or write to these registers can take place.

Sample code to write 0x0155 to the 2-byte SAGLVL register located at 0x14 in the energy measurement memory space is as follows:

```
MOV    MDATM,#01h
MOV    MDATL,#55h
MOV    MADDPT,#SAGLVL_W (Address 0x94)
MOV    A,#05h
DJNZ   ACC,$
       ;Next write or read to energy
       measurement SFR can be done after
       this.
```

Reading the Internal Energy Measurement Registers

When Bit 7 of Energy Measurement Pointer Address SFR (MADDPT, 0x91) is cleared, the content of the internal energy measurement register designated by the address in MADDPT is transferred to the MDATx SFRs. If the internal register is 1 byte long, only the MDATL SFR content is updated with a new value, whereas the MDATM SFR and MDATH SFR contents are reset to 0x00.

The energy measurement core functions with an internal clock of 4.096 MHz/5, or 819.2 kHz. Because the 8052 core functions with another clock, 4.096 MHz/2^{CD}, synchronization between the two clock environments when CD = 0 or 1 is an issue. When data is read from the internal energy measurement registers, a small wait period needs to be implemented before the MDATx SFRs are transferred to another SFR.

Sample code to read the peak voltage in the 2-byte VPKLVL register located at 0x16 into the data pointer is as follows:

```
MOV    MADDPT,#VPKLVL_R (Address 0x16)
MOV    A,#05h
DJNZ   ACC,$
MOV    DPH,MDATM
MOV    DPL,MDATL
```

Table 29. Energy Measurement SFRs

Address	R/W	Mnemonic	Description
0x91	R/W	MADDPT	Energy Measurement Pointer Address.
0x92	R/W	MDATL	Energy Measurement Pointer Data Lowest Significant Byte.
0x93	R/W	MDATM	Energy Measurement Pointer Data Middle Byte.
0x94	R/W	MDATH	Energy Measurement Pointer Data Most Significant Byte.
0xD1	R	VRMSL	V_{rms} Measurement Lowest Significant Byte.
0xD2	R	VRMSM	V_{rms} Measurement Middle Byte.
0xD3	R	VRMSH	V_{rms} Measurement Most Significant Byte.
0xD4	R	IRMSL	I_{rms} Measurement Lowest Significant Byte.
0xD5	R	IRMSM	I_{rms} Measurement Middle Byte.
0xD6	R	IRMSH	I_{rms} Measurement Most Significant Byte.
0xD9	R/W	MIRQENL	Energy Measurement Interrupt Enable Lowest Significant Byte.
0xDA	R/W	MIRQENM	Energy Measurement Interrupt Enable Middle Byte.
0xDB	R/W	MIRQENH	Energy Measurement Interrupt Enable Most Significant Byte.
0xDC	R/W	MIRQSTL	Energy Measurement Interrupt Status Lowest Significant Byte.
0xDD	R/W	MIRQSTM	Energy Measurement Interrupt Status Middle Byte.
0xDE	R/W	MIRQSTH	Energy Measurement Interrupt Status Most Significant Byte.
0xE2	R	WAV1L	Selection 1 Sample Lowest Significant Byte.
0xE3	R	WAV1M	Selection 1 Sample Middle Byte.
0xE4	R	WAV1H	Selection 1 Sample Most Significant Byte.
0xE5	R	WAV2L	Selection 2 Sample Lowest Significant Byte.
0xE6	R	WAV2M	Selection 2 Sample Middle Byte.
0xE7	R	WAV2H	Selection 2 Sample Most Significant Byte.

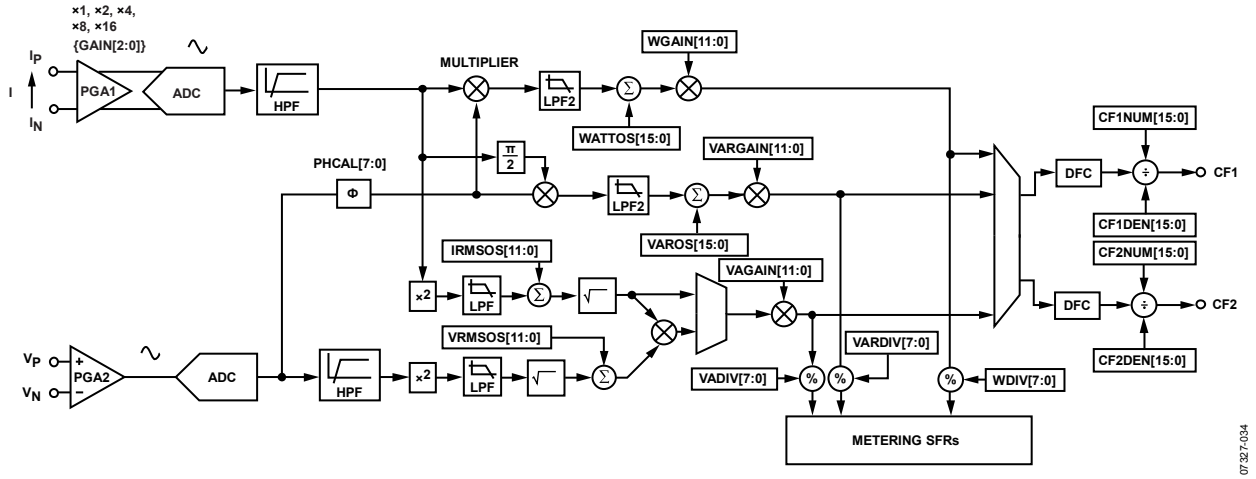


Figure 34. Energy Metering Block Diagram

ENERGY MEASUREMENT REGISTERS

Table 30. Energy Measurement Register List

Address MADDPT[6:0]	Mnemonic	R/W	Length (Bits)	Signed/ Unsigned	Default	Description
0x01	WATTHR	R	24	S	0	Reads Wh accumulator without reset.
0x02	RWATTHR	R	24	S	0	Reads Wh accumulator with reset.
0x03	LWATTHR	R	24	S	0	Reads Wh accumulator synchronous to line cycle.
0x04	VARHR	R	24	S	0	Reads VARh accumulator without reset.
0x05	RVARHR	R	24	S	0	Reads VARh accumulator with reset.
0x06	LVARHR	R	24	S	0	Reads VARh accumulator synchronous to line cycle.
0x07	VAHR	R	24	S	0	Reads VAh accumulator without reset. If the VARMSCFCON bit in MODE2 register (0x0C) is set, this register accumulates I_{rms}.
0x08	RVAHR	R	24	S	0	Reads VAh accumulator with reset. If the VARMSCFCON bit in MODE2 register (0x0C) is set, this register accumulates I_{rms}.
0x09	LVAHR	R	24	S	0	Reads VAh accumulator synchronous to line cycle. If the VARMSCFCON bit in MODE2 register (0x0C) is set, this register accumulates I_{rms}.
0x0A	PER_FREQ	R	16	U	0	Reads line period or frequency register depending on MODE2 register.
0x0B	MODE1	R/W	8	U	0x06	Sets basic configuration of energy measurement (see Table 31).
0x0C	MODE2	R/W	8	U	0x40	Sets basic configuration of energy measurement (see Table 32).
0x0D	WAVMODE	R/W	8	U	0	Sets configuration of Waveform Sample 1 and Waveform Sample 2 (see Table 33).
0x0E	NLMODE	R/W	8	U	0	Sets energy level of no load thresholds (see Table 34).
0x0F	ACCMODE	R/W	8	U	0	Sets configuration of WATT, VAR accumulation, and various tamper alarms (see Table 35).
0x10	PHCAL	R/W	8	S	0x40	Sets phase calibration register (see the Phase Compensation section).
0x11	ZXTOUT	R/W	12	U	0x0FFF	Sets timeout for zero-crossing timeout detection (see the Zero-Crossing Timeout section).
0x12	LINCYC	R/W	16	U	0xFFFF	Sets number of half-line cycles for LWATTHR, LVARHR, and LVAHR accumulators.
0x13	SAGCYC	R/W	8	U	0xFF	Sets number of half-line cycles for SAG detection (see the Line Voltage SAG Detection section).
0x14	SAGLVL	R/W	16	U	0	Sets detection level for SAG detection (see the Line Voltage SAG Detection section).
0x15	IPKLVL	R/W	16	U	0xFFFF	Sets peak detection level for current peak detection (see the Peak Detection section).
0x16	VPKLVL	R/W	16	U	0xFFFF	Sets peak detection level for voltage peak detection (see the Peak Detection section).
0x17	IPEAK	R	24	U	0	Reads current peak level without reset (see the Peak Detection section).
0x18	RSTIPEAK	R	24	U	0	Reads current peak level with reset (see the Peak Detection section).
0x19	VPEAK	R	24	U	0	Reads voltage peak level without reset (see the Peak Detection section).
0x1A	RSTVPEAK	R	24	U	0	Reads voltage peak level with reset (see the Peak Detection section).
0x1B	GAIN	R/W	8	U	0	Sets PGA gain of analog inputs (see Table 36).
0x1C	Reserved	R/W	12	S	0	Reserved.
0x1D	WGAIN	R/W	12	S	0	Sets WATT gain register.
0x1E	VARGAIN	R/W	12	S	0	Sets VAR gain register.
0x1F	VAGAIN	R/W	12	S	0	Sets VA gain register.
0x20	WATTOS	R/W	16	S	0	Sets WATT offset register.
0x21	VAROS	R/W	16	S	0	Sets VAR offset register.
0x22	IRMSOS	R/W	12	S	0	Sets current rms offset register.
0x23	VRMSOS	R/W	12	S	0	Sets voltage rms offset register.
0x24	WDIV	R/W	8	U	0	Sets WATT energy scaling register.
0x25	VARDIV	R/W	8	U	0	Sets VAR energy scaling register.
0x26	VADIV	R/W	8	U	0	Sets VA energy scaling register.
0x27	CF1NUM	R/W	16	U	0	Sets CF1 numerator register.
0x28	CF1DEN	R/W	16	U	0x003F	Sets CF1 denominator register.

Address MADDPT[6:0]	Mnemonic	R/W	Length (Bits)	Signed/ Unsigned	Default	Description
0x29	CF2NUM	R/W	16	U	0	Sets CF2 numerator register.
0x2A	CF2DEN	R/W	16	U	0x003F	Sets CF2 denominator register.
0x3B	Reserved				0	This register must be kept at its default value for proper operation.
0x3C	Reserved				0x0300	This register must be kept at its default value for proper operation.
0x3D	Reserved				0	This register must be kept at its default value for proper operation.
0x3E	Reserved				0	This register must be kept at its default value for proper operation.
0x3F	Reserved				0	This register must be kept at its default value for proper operation.

ENERGY MEASUREMENT INTERNAL REGISTERS DETAILS

Table 31. MODE1 Register (0x0B)

Bit	Mnemonic	Default	Description
7	SWRST	0	Setting this bit resets all of the energy measurement registers to their default values.
6	DISZXLPF	0	Setting this bit disables the zero-crossing low-pass filter.
5	Reserved	0	This bit must be kept at its default value for proper operation.
4	SWAPBITS	0	Setting this bit swaps CH1 ADC and CH2 ADC.
3	PWRDN	0	Setting this bit powers down voltage and current ADCs.
2	DISCF2	1	Setting this bit disables Frequency Output CF2.
1	DISCF1	1	Setting this bit disables Frequency Output CF1.
0	DISHPF	0	Setting this bit disables the HPFs in voltage and current channels.

Table 32. MODE2 Register (0x0C)

Bit	Mnemonic	Default	Description	
7 to 6	CF2SEL[1:0]	01	Configuration Bits for CF2 Output.	
			CF2SEL[1:0]	**Result**
			00	CF2 frequency is proportional to active power.
			01	CF2 frequency is proportional to reactive power.
			1x	CF2 frequency is proportional to apparent power or I_{rms}.
5 to 4	CF1SEL[1:0]	00	Configuration Bits for CF1 Output.	
			CF1SEL[1:0]	**Result**
			00	CF1 frequency is proportional to active power.
			01	CF1 frequency is proportional to reactive power.
			1x	CF1 frequency is proportional to apparent power or I_{rms}.
3	VARMSCFCON	0	Configuration Bits for Apparent Power or I_{rms} for CF1, CF2 Outputs, and VA Accumulation Registers (VAHR, RVAHR, and LVAHR). Note that CF1 cannot be proportional to VA if CF2 is proportional to I_{rms} and vice versa.	
			VARMSCFCON	**Result**
			0	If CF1SEL[1:0] = 1x, CF1 is proportional to VA. If CF2SEL[1:0] = 1x, CF2 is proportional to VA.
			1	If CF1SEL[1:0] = 1x, CF1 is proportional to I_{rms}. If CF2SEL[1:0] = 1x, CF2 is proportional to I_{rms}.
2	ZXRMS	0	Logic 1 enables update of rms values synchronously to Voltage ZX.	
1	FREQSEL		Configuration Bits to Select Period or Frequency Measurement for PER_FREQ Register (0x0A).	
			FREQSEL	**Result**
			0	PER_FREQ register holds a period measurement.
			1	PER_FREQ register holds a frequency measurement.
0	WAVEN	0	When this bit is set, the waveform sampling mode is enabled.	

Table 33. WAVMODE Register (0x0D)

Bit	Mnemonic	Default	Description	
7 to 5	WAV2SEL[2:0]	000	Waveform 2 Selection for Samples Mode.	
			WAV2SEL[2:0]	**Source**
			000	Current
			001	Voltage
			010	Active power multiplier output
			011	Reactive power multiplier output
			100	VA multiplier output
			101	I_{rms} LPF output
			Others	Reserved
4 to 2	WAV1SEL[2:0]	000	Waveform 1 Selection for Samples Mode.	
			WAV1SEL[2:0]	**Source**
			000	Current
			001	Voltage
			010	Active power multiplier output
			011	Reactive power multiplier output
			100	VA multiplier output
			101	I_{rms} LPF output (low 24-bit)
			Others	Reserved
1 to 0	DTRT[1:0]	00	Waveform Samples Output Data Rate.	
			DTRT[1:0]	**Update Rate (Clock = f_{CORE}/5 = 819.2 kHz)**
			00	25.6 kSPS (clock/32)
			01	12.8 kSPS (clock/64)
			10	6.4 kSPS (clock/128)
			11	3.2 kSPS (clock/256)

Table 34. NLMODE Register (0x0E)

Bit	Mnemonic	Default	Description	
7	DISVARCMP	0	Setting this bit disables fundamental VAR gain compensation over line frequency.	
6	IRMSNOLOAD	0	Logic 1 enables I_{rms} no load threshold detection. The level is defined by the setting of the VANOLOAD bits.	
5 to 4	VANOLOAD[1:0]	00	Apparent Power No Load Threshold.	
			VANOLOAD[1:0]	**Result**
			00	No load detection disabled
			01	No load detection enabled with threshold = 0.030% of full scale
			10	No load detection enabled with threshold = 0.015% of full scale
			11	No load detection enabled with threshold = 0.0075% of full scale
3 to 2	VARNOLOAD[1:0]	00	Reactive Power No Load Threshold.	
			VARNOLOAD[1:0]	**Result**
			00	No load detection disabled
			01	No load detection enabled with threshold = 0.015% of full scale
			10	No load detection enabled with threshold = 0.0075% of full scale
			11	No load detection enabled with threshold = 0.0037% of full scale
1 to 0	APNOLOAD[1:0]	00	Active Power No Load Threshold.	
			APNOLOAD[1:0]	**Result**
			00	No load detection disabled
			01	No load detection enabled with threshold = 0.015% of full scale
			10	No load detection enabled with threshold = 0.0075% of full scale
			11	No load detection enabled with threshold = 0.0037% of full scale

Table 35. ACCMODE Register (0x0F)

Bit	Mnemonic	Default	Description
7 to 6	Reserved	0	These bits should be left at their default value for proper operation.
5	VARSIGN	0	Configuration bit to select the event that triggers a reactive power sign interrupt. If set to 0, VARSIGN interrupt occurs when reactive power changes from positive to negative. If this bit is set to 1, VARSIGN interrupt occurs when reactive power changes from negative to positive.
4	APSIGN	0	Configuration bit to select event that triggers an active power sign interrupt. If set to 0, APSIGN interrupt occurs when active power changes from positive to negative. If this bit is set to 1, APSIGN interrupt occurs when active power changes from negative to positive.
3	ABSVARM	0	Logic 1 enables absolute value accumulation of reactive power in energy register and pulse output.
2	SAVARM	0	Logic 1 enables reactive power accumulation depending on the sign of the active power. If active power is positive, VAR is accumulated as it is. If active power is negative, the sign of the VAR is reversed for the accumulation. This accumulation mode affects both the VAR registers (VARHR, RVARHR, LVARHR) and the pulse output when connected to VAR.
1	POAM	0	Logic 1 enables positive-only accumulation of active power in the WATTHR energy register and pulse output.
0	ABSAM	0	Logic 1 enables absolute value accumulation of active power in the WATTHR energy register and pulse output.

Table 36. GAIN Register (0x1B)

Bit	Mnemonic	Default	Description	
7 to 5	PGA2[2:0]	000	These bits define the voltage channel input gain.	
			PGA2[2:0]	**Result**
			000	Gain = 1
			001	Gain = 2
			010	Gain = 4
			011	Gain = 8
			100	Gain = 16
4	Reserved	0	Reserved.	
3	CFSIGN_OPT	0	This bit defines where the CF change of sign detection (APSIGN or VARSIGN) is implemented.	
			CFSIGN_OPT	**Result**
			0	Filtered power signal
			1	On a per CF pulse basis
2 to 0	PGA1[2:0]	000	These bits define the current channel input gain.	
			PGA1[2:0]	**Result**
			000	Gain = 1
			001	Gain = 2
			010	Gain = 4
			011	Gain = 8
			100	Gain = 16

INTERRUPT STATUS/ENABLE SFRS

Table 37. Interrupt Status 1 SFR (MIRQSTL, 0xDC)

Bit	Interrupt Flag	Description
7	ADEIRQFLAG	This bit is set if any of the ADE status flags that are enabled to generate an ADE interrupt are set. This bit is automatically cleared when all of the enabled ADE status flags are cleared.
6	Reserved	Reserved.
5	Reserved	Reserved.
4	VARSIGN	Logic 1 indicates that the reactive power sign has changed according to the configuration of the ACCMODE register.
3	APSIGN	Logic 1 indicates that the active power sign has changed according to the configuration of the ACCMODE register.
2	VANOLOAD	Logic 1 indicates that an interrupt has been caused by an apparent power no load detection. This interrupt is also used to reflect the part entering the I_{rms} no load mode.
1	RNOLOAD	Logic 1 indicates that an interrupt has been caused by a reactive power no load detection.
0	APNOLOAD	Logic 1 indicates that an interrupt has been caused by an active power no load detection.

Table 38. Interrupt Status 2 SFR (MIRQSTM, 0xDD)

Bit	Interrupt Flag	Description
7	CF2	Logic 1 indicates that a pulse on CF2 has been issued. The flag is set even if the CF2 pulse output is not enabled by clearing Bit 2 of the MODE1 register.
6	CF1	Logic 1 indicates that a pulse on CF1 has been issued. The flag is set even if the CF1 pulse output is not enabled by clearing Bit 1 of the MODE1 register.
5	VAEOF	Logic 1 indicates that the VAHR register has overflowed.
4	REOF	Logic 1 indicates that the VARHR register has overflowed.
3	AEOF	Logic 1 indicates that the WATTHR register has overflowed.
2	VAEHF	Logic 1 indicates that the VAHR register is half full.
1	REHF	Logic 1 indicates that the VARHR register is half full.
0	AEHF	Logic 1 indicates that the WATTHR register is half full.

Table 39. Interrupt Status 3 SFR (MIRQSTH, 0xDE)

Bit	Interrupt Flag	Description
7	RESET	Indicates the end of a reset (for both software and hardware reset).
6	Reserved	Reserved.
5	WFSM	Logic 1 indicates that new data is present in the waveform registers (Address 0xE2 to Address 0xE7).
4	PKI	Logic 1 indicates that the current channel has exceeded the IPKLVL value
3	PKV	Logic 1 indicates that the voltage channel has exceeded the VPKLVL value.
2	CYCEND	Logic 1 indicates the end of the energy accumulation over an integer number of half-line cycles.
1	ZXTO	Logic 1 indicates that no zero crossing on the line voltage happened for the last ZXTOUT half-line cycles.
0	ZX	Logic 1 indicates detection of a zero crossing in the voltage channel.

Table 40. Interrupt Enable 1 SFR (MIRQENL, 0xD9)

Bit	Interrupt Enable Bit	Description
7 to 5	Reserved	Reserved.
4	VARSIGN	When this bit is set, the VARSIGN flag set creates a pending ADE interrupt to the 8052 core.
3	APSIGN	When this bit is set, the APSIGN flag set creates a pending ADE interrupt to the 8052 core.
2	VANOLOAD	When this bit is set, the VANOLOAD flag set creates a pending ADE interrupt to the 8052 core.
1	RNOLOAD	When this bit is set, the RNOLOAD flag set creates a pending ADE interrupt to the 8052 core.
0	APNOLOAD	When this bit is set, the APNOLOAD flag set creates a pending ADE interrupt to the 8052 core.

Table 41. Interrupt Enable 2 SFR (MIRQENM, 0xDA)

Bit	Interrupt Enable Bit	Description
7	CF2	When this bit is set, a CF2 pulse creates a pending ADE interrupt to the 8052 core.
6	CF1	When this bit is set, a CF1 pulse creates a pending ADE interrupt to the 8052 core.
5	VAEOF	When this bit is set, the VAEOF flag set creates a pending ADE interrupt to the 8052 core.
4	REOF	When this bit is set, the REOF flag set creates a pending ADE interrupt to the 8052 core.
3	AEOF	When this bit is set, the AEOF flag set creates a pending ADE interrupt to the 8052 core.
2	VAEHF	When this bit is set, the VAEHF flag set creates a pending ADE interrupt to the 8052 core.
1	REHF	When this bit is set, the REHF flag set creates a pending ADE interrupt to the 8052 core.
0	AEHF	When this bit is set, the AEHF flag set creates a pending ADE interrupt to the 8052 core.

Table 42. Interrupt Enable 3 SFR (MIRQENH, 0xDB)

Bit	Interrupt Enable Bit	Description
7 to 6	Reserved	Reserved.
5	WFSM	When this bit is set, the WFSM flag set creates a pending ADE interrupt to the 8052 core.
4	PKI	When this bit is set, the PKI flag set creates a pending ADE interrupt to the 8052 core.
3	PKV	When this bit is set, the PKV flag set creates a pending ADE interrupt to the 8052 core.
2	CYCEND	When this bit is set, the CYCEND flag set creates a pending ADE interrupt to the 8052 core.
1	ZXTO	When this bit is set, the ZXTO flag set creates a pending ADE interrupt to the 8052 core.
0	ZX	When this bit is set, the ZX flag set creates a pending ADE interrupt to the 8052 core.

ANALOG INPUTS

The ADE7518 has two fully differential voltage input channels. The maximum differential input voltage for input pairs V_P/V_N and I_P/I_N is ±0.4 V.

Each analog input channel has a programmable gain amplifier (PGA) with possible gain selections of 1, 2, 4, 8, and 16. The gain selections are made by writing to the GAIN register (see Table 36 and Figure 36). Bit 0 to Bit 2 select the gain for the PGA in the current channel, and Bit 5 to Bit 7 select the gain for the PGA in the voltage channel. Figure 35 shows how a gain selection for the current channel is made using the gain register.

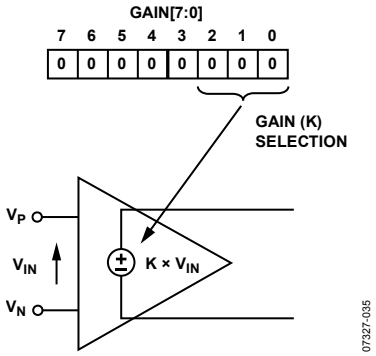


Figure 35. PGA in Current Channel

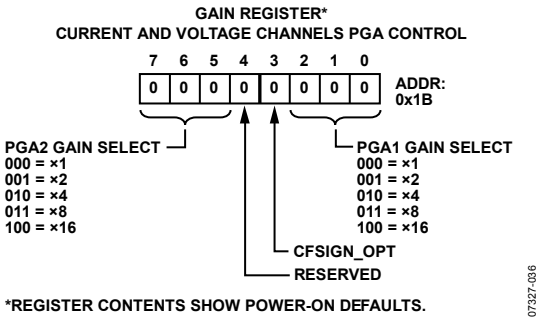


Figure 36. Analog Gain Register

ANALOG-TO-DIGITAL CONVERSION

Each ADE7518 has two Σ-Δ analog-to-digital converters (ADCs). The outputs of these ADCs are mapped directly to waveform sampling SFRs (Address 0xE2 to Address 0xE7) and are used for energy measurement internal digital signal processing. In PSM1 (battery mode) and PSM2 (sleep mode), the ADCs are powered down to minimize power consumption.

For simplicity, the block diagram in Figure 38 shows a first-order Σ-Δ ADC. The converter is made up of the Σ-Δ modulator and the digital low-pass filter.

A Σ-Δ modulator converts the input signal into a continuous serial stream of 1s and 0s at a rate determined by the sampling clock. In the ADE7518, the sampling clock is equal to 4.096 MHz/5. The 1-bit DAC in the feedback loop is driven by the serial data stream. The DAC output is subtracted from the input signal. If the loop gain is high enough, the average value of the DAC output (and, therefore, the bit stream) can approach that of the input signal level.

For any given input value in a single sampling interval, the data from the 1-bit ADC is virtually meaningless. A meaningful result is obtained only when a large number of samples is averaged. This averaging is carried into the second part of the ADC, the digital low-pass filter. By averaging a large number of bits from the modulator, the low-pass filter can produce 24-bit data-words that are proportional to the input signal level.

The Σ-Δ converter uses two techniques to achieve high resolution from what is essentially a 1-bit conversion technique. The first is oversampling. Oversampling means that the signal is sampled at a rate (frequency) that is many times higher than the bandwidth of interest. For example, the sampling rate in the ADE7518 is 4.096 MHz/5, or 819.2 kHz, and the band of interest is 40 Hz to 2 kHz. Oversampling has the effect of spreading the quantization noise (noise due to sampling) over a wider bandwidth. With the noise spread more thinly over a wider bandwidth, the quantization noise in the band of interest is lowered (see Figure 37).

However, oversampling alone is not efficient enough to improve the signal-to-noise ratio (SNR) in the band of interest. For example, an oversampling ratio of four is required to increase the SNR by only 6 dB (1 bit). To keep the oversampling ratio at a reasonable level, it is possible to shape the quantization noise so that the majority of the noise lies at the higher frequencies. In the Σ-Δ modulator, the noise is shaped by the integrator, which has a high-pass-type response for the quantization noise. The result is that most of the noise is at the higher frequencies, where it can be removed by the digital low-pass filter. This noise shaping is shown in Figure 37.

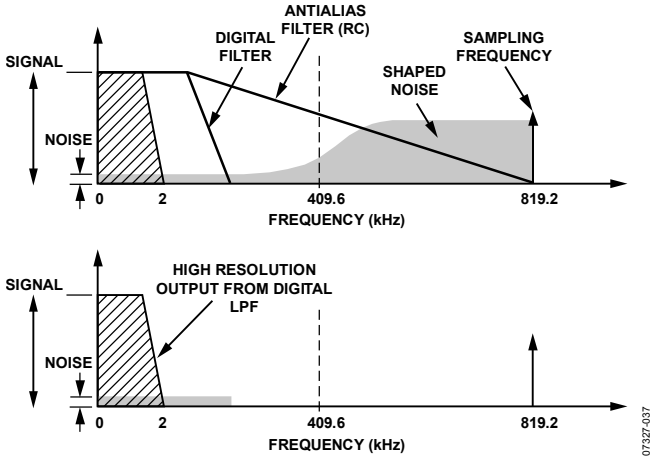


Figure 37. Noise Reduction Due to Oversampling and Noise Shaping in the Analog Modulator

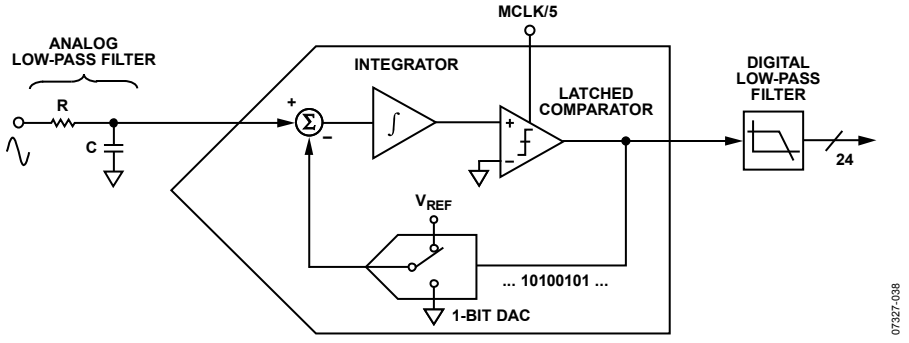


Figure 38. First-Order Σ-Δ ADC

Antialiasing Filter

Figure 38 also shows an analog low-pass filter (RC) on the input to the modulator. This filter is present to prevent aliasing, an artifact of all sampled systems. Aliasing means that frequency components in the input signal to the ADC, which are higher than half the sampling rate of the ADC, appear in the sampled signal at a frequency below half the sampling rate. Figure 39 illustrates the effect. Frequency components (the black arrows) above half the sampling frequency (also known as the Nyquist frequency, that is, 409.6 kHz) are imaged or folded back down below 409.6 kHz. This happens with all ADCs regardless of the architecture. In the example shown in Figure 39, only frequencies near the sampling frequency (819.2 kHz) move into the band of interest for metering (40 Hz to 2 kHz). This allows the use of a very simple low-pass filter (LPF) to attenuate high frequency (near 819.2 kHz) noise and prevents distortion in the band of interest.

For conventional current sensors, a simple RC filter (single-pole LPF) with a corner frequency of 10 kHz produces an attenuation of approximately 40 dB at 819.2 kHz (see Figure 39). The 20 dB per decade attenuation is usually sufficient to eliminate the effects of aliasing for conventional current sensors. However, for a di/dt sensor such as a Rogowski coil, the sensor has a 20 dB per decade gain. This neutralizes the −20 dB per decade attenuation produced by one simple LPF. Therefore, when using a di/dt sensor, care should be taken to offset the 20 dB per decade gain. One simple approach is to cascade two RC filters to produce the −40 dB per decade attenuation needed.

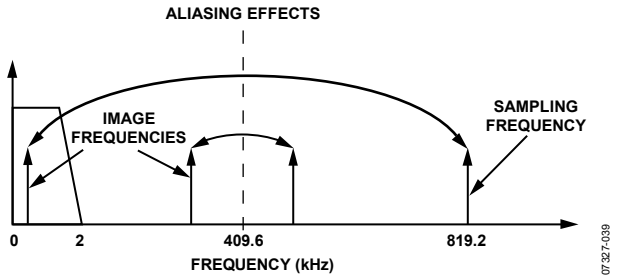


Figure 39. ADC and Signal Processing in Current Channel Outline Dimensions

ADC Transfer Function

Both ADCs in the ADE7518 are designed to produce the same output code for the same input signal level. With a full-scale signal on the input of 0.4 V and an internal reference of 1.2 V, the ADC output code is nominally 2,147,483, or 0x20C49B. The maximum code from the ADC is ±4,194,304; this is equivalent to an input signal level of ±0.794 V. However, for specified performance, it is recommended that the full-scale input signal level of 0.4 V not be exceeded.

Current Channel ADC

Figure 40 shows the ADC and signal processing chain for the current channel. In waveform sampling mode, the ADC outputs a signed, twos complement, 24-bit data-word at a maximum of 25.6 kSPS (4.096 MHz/160).

With the specified full-scale analog input signal of 0.4 V and PGA1 = 1, the ADC produces an output code that is approximately between 0x20C49B (+2,147,483d) and 0xDF3B65 (−2,147,483d). For inputs of 0.25 V, 0.125 V, 82.6 mV, and 31.3 mV with PGA1 = 2, 4, 8, and 16, respectively, the ADC produces an output code that is approximately between 0x28F5C2 (+2,684,354d) and 0xD70A3E (−2,684,354d).

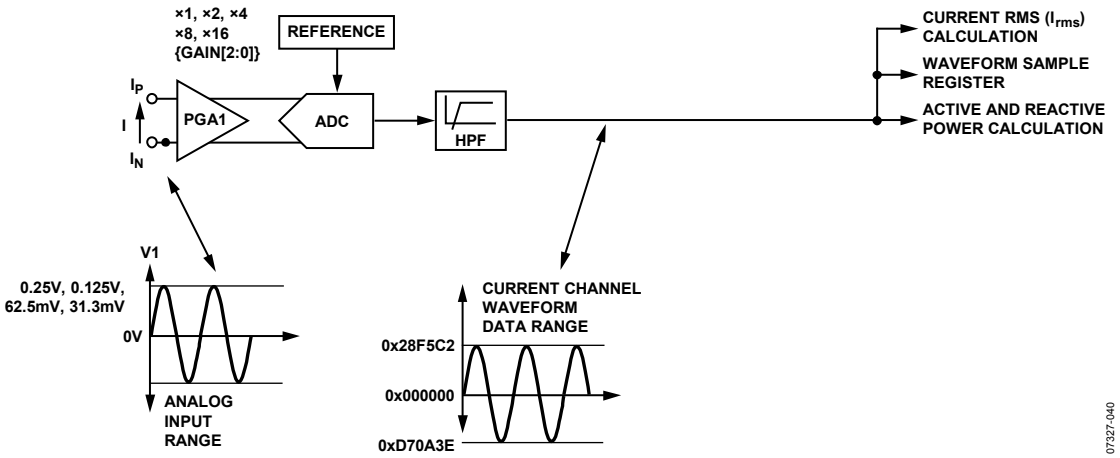


Figure 40. ADC and Signal Processing in Current Channel with PGA1 = 1, 2, 4, 8, or 16

Voltage Channel ADC

Figure 41 shows the ADC and signal processing chain for the voltage channel. In waveform sampling mode, the ADC outputs a signed, twos complement, 24-bit data-word at a maximum of 25.6 kSPS (MCLK/160). The ADC produces an output code that is approximately between 0x28F5 (+10,485d) and 0xD70B (−10,485d).

Channel Sampling

The waveform samples of the current ADC and voltage ADC can also be routed to the waveform registers to be read by the MCU core. The active, reactive, apparent power, and energy calculation remain uninterrupted during waveform sampling.

When in waveform sampling mode, one of four output sample rates can be chosen by using the DTRT[1:0] bits of the WAVMODE register (see Table 33). The output sample rate can be 25.6 kSPS, 12.8 kSPS, 6.4 kSPS, or 3.2 kSPS. If the WFSM enable bit is set in the Interrupt Enable 3 SFR (MIRQENH, 0xDB), the 8052 core has a pending ADE interrupt. The sampled signals selected in the WAVMODE register are latched into the Waveform SFRs when the waveform high byte (WAV1H or WAV2H) is read.

The ADE interrupt stays active until the WFSM status bit is cleared (see the Energy Measurement Interrupts section).

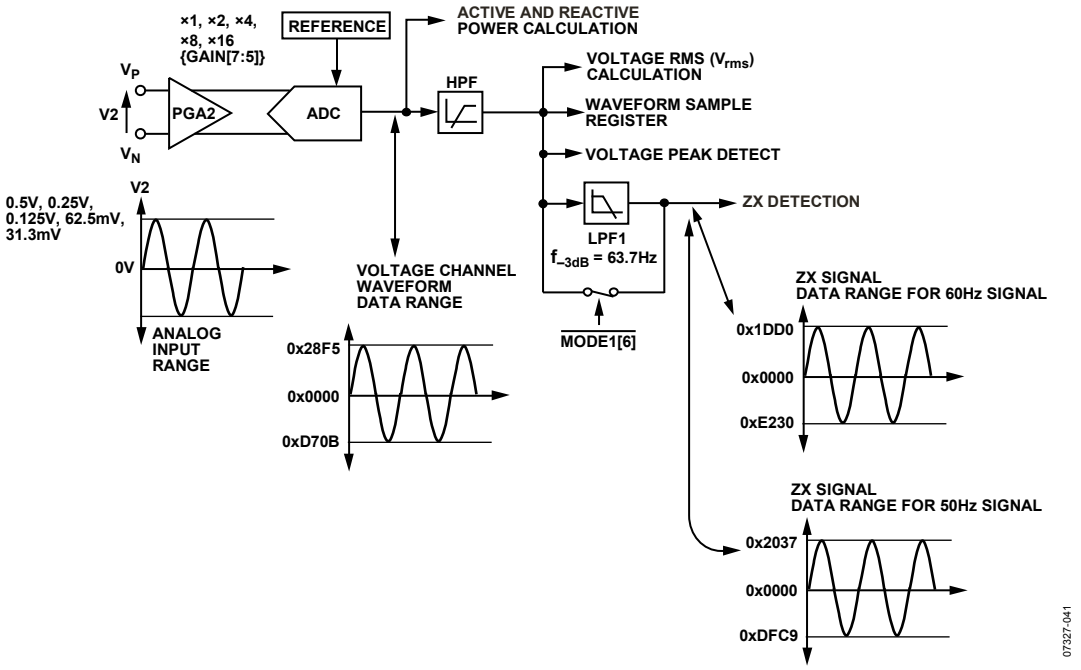


Figure 41. ADC and Signal Processing in Voltage Channel

POWER QUALITY MEASUREMENTS

Zero-Crossing Detection

Each ADE7518 has a zero-crossing detection circuit on the voltage channel. This zero crossing is used to produce a zero-crossing internal signal (ZX) and is used in calibration mode.

The zero-crossing is generated by default from the output of LPF1. This filter has a low cutoff frequency and is intended for 50 Hz and 60 Hz systems. If needed, this filter can be disabled to allow a higher frequency signal to be detected or to limit the group delay of the detection. If the voltage input fundamental frequency is below 60 Hz and a time delay in ZX detection is acceptable, it is recommended to enable LPF1. Enabling LPF1 limits the variability in the ZX detection by eliminating the high frequency components. Figure 42 shows how the zero-crossing signal is generated.

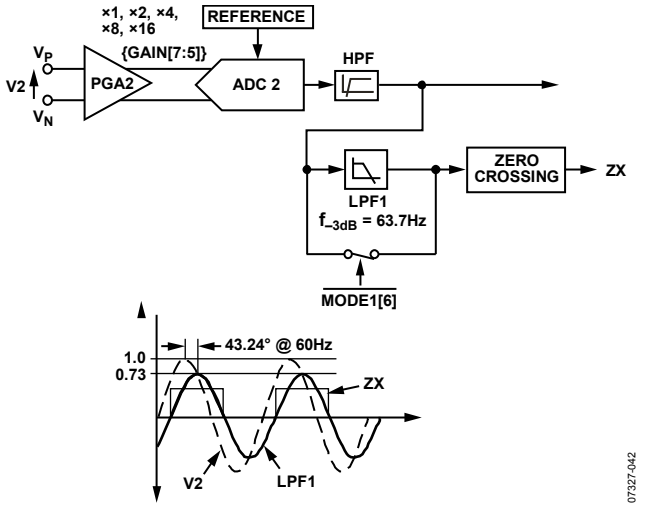


Figure 42. Zero-Crossing Detection on the Voltage Channel

The zero-crossing signal ZX is generated from the output of LPF1 (bypassed or not). LPF1 has a single pole at 63.7 Hz (at MCLK = 4.096 MHz). As a result, there is a phase lag between the analog input signal V2 and the output of LPF1. The phase lag response of LPF1 results in a time delay of approximately 2 ms (@ 60 Hz) between the zero crossing on the analog inputs of the voltage channel and ZX detection.

The zero-crossing detection also drives the ZX flag in the Interrupt Status 3 SFR (MIRQSTH, 0xDE). If the ZX bit in the Interrupt Enable 3 SFR (MIRQENH, 0xDB) is set, the 8052 core has a pending ADE interrupt. The ADE interrupt stays active until the ZX status bit is cleared (see the Energy Measurement Interrupts section).

Zero-Crossing Timeout

The zero-crossing detection also has an associated timeout register, ZXTOUT. This unsigned, 12-bit register is decremented (1 LSB) every 160/MCLK seconds. The register is reset to its user-programmed full-scale value every time a zero crossing is detected on the voltage channel. The default power-on value in this register is 0xFFF. If the internal register decrements to 0 before a zero crossing is detected in the Interrupt Status 3 SFR (MIRQSTH, 0xDE) and the ZXTO bit in the Interrupt Enable 3 SFR (MIRQENH, 0xDB) is set, the 8052 core has a pending ADE interrupt.

The ADE interrupt stays active until the ZXTO status bit is cleared (see the Energy Measurement Interrupts section). The ZXTOUT register (Address 0x11) can be written to or read from the 8052 by the user (see the energy measurement register list in Table 30). The resolution of the register is 160/MCLK seconds per LSB. Thus, the maximum delay for an interrupt is 0.16 sec ($1/MCLK \times 2^{12}$) when MCLK = 4.096 MHz.

Figure 43 shows the mechanism of the zero-crossing timeout detection when the line voltage stays at a fixed dc level for more than MCLK/160 × ZXTOUT seconds.

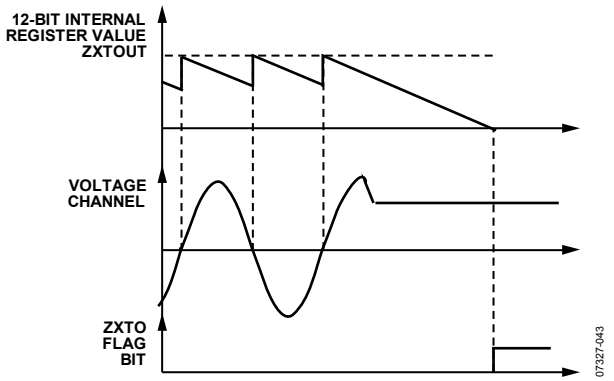


Figure 43. Zero-Crossing Timeout Detection

Period or Frequency Measurements

The ADE7518 provides the period or frequency measurement of the line. The period or frequency measurement is selected by clearing or setting the FREQSEL bit in the MODE2 register (0x0C). The period/frequency register, PER_FREQ register (0x0A), is an unsigned 16-bit register that is updated every period. If LPF1 is enabled, a settling time of 1.8 seconds is associated with this filter before the measurement is stable.

When the period measurement is selected, the measurement has a 2.44 µs/LSB (4.096 MHz/10) resolution, which represents 0.014% when the line frequency is 60 Hz. When the line frequency is 60 Hz, the value of the period register is approximately 0d6827. The length of the register enables the measurement of line frequencies as low as 12.5 Hz. The period register is stable at ±1 LSB when the line is established and the measurement does not change.

When the frequency measurement is selected, the measurement has a 0.0625 Hz/LSB resolution when MCLK = 4.096 MHz, which represents 0.104% when the line frequency is 60 Hz. When the line frequency is 60 Hz, the value of the frequency register is 0d960. The frequency register is stable at ±4 LSB when the line is established and the measurement does not change.

Line Voltage SAG Detection

In addition to detection of the loss of the line voltage signal (zero crossing), the ADE7518 can also be programmed to detect when the absolute value of the line voltage drops below a certain peak value for a number of line cycles. This condition is illustrated in Figure 44.

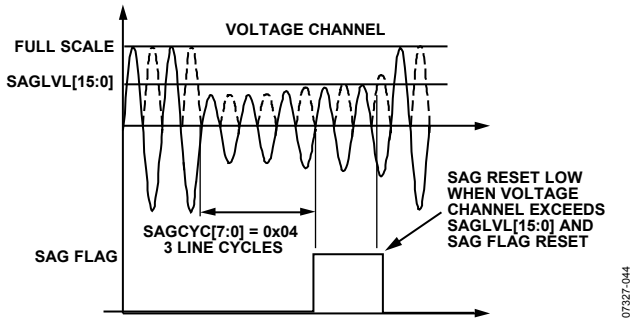


Figure 44. SAG Detection

Figure 44 shows the line voltage falling below a threshold that is set in the SAG level register (SAGLVL[15:0]) for three line cycles. The quantities 0 and 1 are not valid for the SAGCYC register, and the contents represent one more than the desired number of full line cycles. For example, when the SAG cycle (SAGCYC[7:0]) contains 0x04, FSAG in the Power Management Interrupt Flag SFR (IPSMF, 0xF8) is set at the end of the third line cycle after the line voltage falls below the threshold. If the SAG enable bit (ESAG) in the Power Management Interrupt Enable SFR (IPSME, 0xEC) is set, the 8052 core has a pending power supply management interrupt. The PSM interrupt stays active until the ESAG bit is cleared (see the Power Supply Management (PSM) Interrupt section).

In Figure 44, the SAG flag (FSAG) is set on the fifth line cycle after the signal on the voltage channel first drops below the threshold level.

SAG Level Set

The 2-byte contents of the SAG level register (SAGLVL, 0x14) are compared to the absolute value of the output from LPF1.

Therefore, when LPF1 is enabled, writing 0x2038 to the SAG level register puts the SAG detection level at full scale (see Figure 44). Writing 0x00 or 0x01 puts the SAG detection level at 0. The SAG level register is compared to the input of the ZX detection, and detection is made when the contents of the SAG level register are greater.

Peak Detection

The ADE7518 can also be programmed to detect when the absolute value of the voltage or current channel exceeds a specified peak value. Figure 45 illustrates the behavior of the peak detection for the voltage channel. Both voltage and current channels are monitored at the same time.

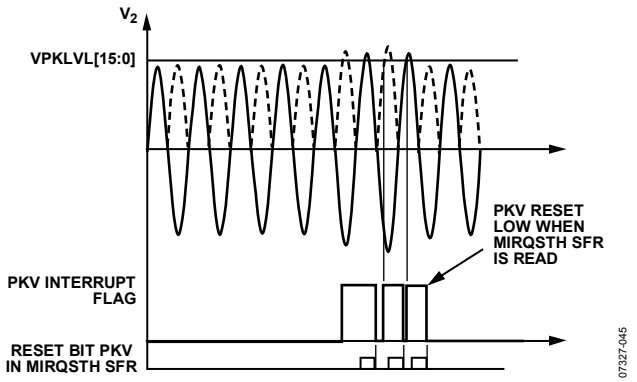


Figure 45. Peak Level Detection

Figure 45 shows a line voltage exceeding a threshold that is set in the voltage peak register (VPKLVL[15:0]). The voltage peak event is recorded by setting the PKV flag in the Interrupt Status 3 SFR (MIRQSTH, 0xDE). If the PKV enable bit is set in the Interrupt Enable 3 SFR (MIRQENH, 0xDB), the 8052 core has a pending ADE interrupt. Similarly, the current peak event is recorded by setting the PKI flag in Interrupt Status 3 SFR (MIRQSTH, 0xDE). The ADE interrupt stays active until the PKV or PKI status bit is cleared (see the Energy Measurement Interrupts section).

Peak Level Set

The contents of the VPKLVL and IPKLVL registers are compared to the absolute value of the voltage and the 2 MSBs of the current channel, respectively. Thus, for example, the nominal maximum code from the current channel ADC with a full-scale signal is 0x28F5C2 (see the Current Channel ADC section). Therefore, writing 0x28F5 to the IPKLVL register puts the peak detection level of the current channel at full scale and sets the current peak detection to its least sensitive value. Writing 0x00 puts the current channel detection level at 0. The detection is done by comparing the contents of the IPKLVL register to the incoming current channel sample. The PKI flag indicates that the peak level is exceeded. If the PKI or PKV bit is set in the Interrupt Enable 3 SFR (MIRQENH, 0xDB), the 8052 core has a pending ADE interrupt.

Peak Level Record

Each ADE7518 records the maximum absolute value reached by the voltage and current channels in two different registers, IPEAK and VPEAK, respectively. Each register is a 24-bit unsigned register that is updated each time the absolute value of the waveform sample from the corresponding channel is above the value stored in the VPEAK or IPEAK register. The contents of the VPEAK register correspond to the maximum absolute value observed on the voltage channel input. The contents of IPEAK and VPEAK represent the maximum absolute value observed on the current and voltage input, respectively. Reading the RSTVPEAK and RSTIPEAK registers clears their respective contents after the read operation.

PHASE COMPENSATION

The ADE7518 must work with transducers that can have inherent phase errors. For example, a phase error of 0.1° to 0.3° is not uncommon for a current transformer (CT). These phase errors can vary from part to part, and they must be corrected to perform accurate power calculations. The errors associated with phase mismatch are particularly noticeable at low power factors. The ADE7518 provides a means of digitally calibrating these small phase errors. The part allows a small time delay or time advance to be introduced into the signal processing chain to compensate for small phase errors. Because the compensation is in time, this technique should only be used for small phase errors in the range of 0.1° to 0.5°. Correcting large phase errors using a time shift technique can introduce significant phase errors at higher harmonics.

The phase calibration register (PHCAL[7:0]) is a twos complement, signed, single-byte register that has values ranging from 0x82 (−126d) to 0x68 (+104d).

The PHCAL register is centered at 0x40, meaning that writing 0x40 to the register results in 0 delay. By changing this register, the time delay in the voltage channel signal path can change from −231.93 µs to +48.83 µs (MCLK = 4.096 MHz). One LSB is equivalent to a 1.22 µs (4.096 MHz/5) time delay or advance. A line frequency of 60 Hz gives a phase resolution of 0.026° at the fundamental (that is, 360° × 1.22 µs × 60 Hz).

Figure 46 illustrates how the phase compensation is used to remove a 0.1° phase lead in the current channel due to the external transducer. To cancel the lead (0.1°) in the current channel, a phase lead must also be introduced into the voltage channel. The resolution of the phase adjustment allows the introduction of a phase lead in increments of 0.026°. The phase lead is achieved by introducing a time advance into the voltage channel. A time advance of 4.88 µs is made by writing −4 (0x3C) to the time delay block, thus reducing the amount of time delay by 4.88 µs, or equivalently, a phase lead of approximately 0.1° at a line frequency of 60 Hz (0x3C represents −4 because the register is centered with 0 at 0x40).

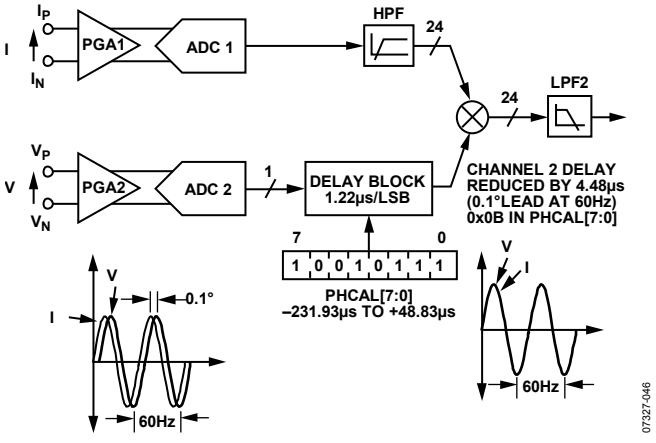


Figure 46. Phase Calibration

RMS CALCULATION

The root mean square (rms) value of a continuous signal V(t) is defined as

$$V_{rms} = \sqrt{\frac{1}{T} \times \int_0^T V^2(t)dt} \quad (1)$$

For time sampling signals, rms calculation involves squaring the signal, taking the average, and obtaining the square root. The ADE7518 implements this method by serially squaring the input, averaging them, and then taking the square root of the average. The averaging part of this signal processing is done by implementing a low-pass filter (LPF3 in Figure 47, Figure 48, and Figure 50). This LPF has a −3 dB cutoff frequency of 2 Hz when MCLK = 4.096 MHz.

$$V(t) = \sqrt{2} \times V \sin(\omega t) \quad (2)$$

where V is the rms voltage.

$$V^2(t) = V^2 - V^2 \cos(2\omega t) \quad (3)$$

When this signal goes through LPF3, the cos(2ωt) term is attenuated and only the dc term V_{rms}^2 goes through (shown as V^2 in Figure 47).

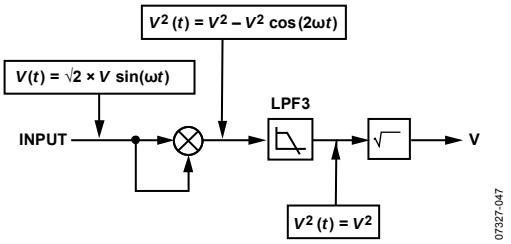


Figure 47. RMS Signal Processing

The I_{rms} signal can be read from the waveform register by setting the WAVMODE register (0x0D) and setting the WFSM bit in the Interrupt Enable 3 SFR (MIRQENH, 0xDB). Like the current and voltage channels waveform sampling modes, the waveform data is available at a sample rate of 25.6 kSPS, 12.8 kSPS, 6.4 kSPS, or 3.2 kSPS.

It is important to note that when the current input is larger than 40% of full scale, the I_{rms} waveform sample register does not represent the true processed rms value. The rms value processed with this level of input is larger than the 24-bit read by the waveform register, making the value read truncated on the high end.

Current Channel RMS Calculation

Each ADE7518 simultaneously calculates the rms values for the current and voltage channels in different registers. Figure 48 shows the detail of the signal processing chain for the rms calculation on the current channel. The current channel rms value is processed from the samples used in the current channel waveform sampling mode and is stored in an unsigned 24-bit register (I_{rms}). One LSB of the current channel rms register is equivalent to one LSB of a current channel waveform sample.

The update rate of the current channel rms measurement is 4.096 MHz/5. To minimize noise in the reading of the register, the I_{rms} register can also be configured to update only with the zero crossing of the voltage input. This configuration is done by setting the ZXRMS bit in the MODE2 register (0x0C).

With the different specified full-scale analog input signal PGA1 values, the ADC produces an output code that is approximately ±0d2,147,483 (PGA1 = 1) or ±0d2,684,354 (PGA1 = 2, 4, 8, or 16). See the Current Channel ADC section. Similarly, the equivalent rms value of a full-scale ac signal is 0d1,518,499 (0x172BA3) when PGA = 1 and 0d1,898,124 (0x1CF68C) when PGA1 = 2, 4, 8, or 16. The current rms measurement provided in the ADE7518 is accurate to within 0.5% for signal inputs between full scale and full scale/500. The conversion from the register value to amps must be done externally in the microprocessor using an amps/LSB constant.

Current Channel RMS Offset Compensation

The ADE7518 incorporates a current channel rms offset compensation register (IRMSOS). This is a 12-bit signed register that can be used to remove offset in the current channel rms calculation. An offset can exist in the rms calculation due to input noises that are integrated into the dc component of $V^2(t)$.

One LSB of the current channel rms offset is equivalent to 16,384 LSBs of the square of the current channel rms register. Assuming that the maximum value from the current channel rms calculation is 0d1,898,124 with full-scale ac inputs, then 1 LSB of the current channel rms offset represents 0.23% of measurement error at −60 dB down from full scale.

$$I_{rms} = \sqrt{I_{rms0}{}^2 + IRMSOS \times 32{,}768} \quad (4)$$

where I_{rms0} is the rms measurement without offset correction.

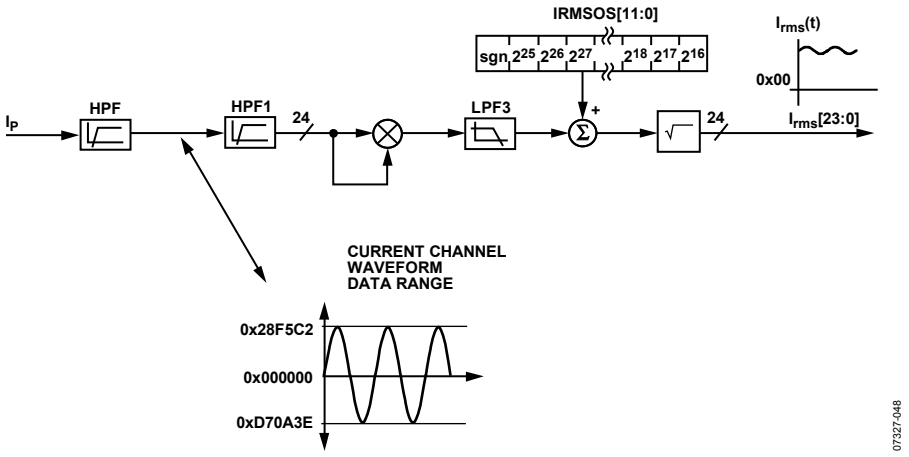


Figure 48. Current Channel RMS Signal Processing with PGA1 = 1, 2, 4, 8, or 16

Voltage Channel RMS Calculation

Figure 50 shows details of the signal processing chain for the rms calculation on the voltage channel. The voltage channel rms value is processed from the samples used in the voltage channel waveform sampling mode and is stored in the unsigned 24-bit V_{rms} register.

The update rate of the voltage channel rms measurement is MCLK/5. To minimize noise in the reading of the register, the V_{rms} register can also be configured to update only with the zero crossing of the voltage input. This configuration is done by setting the ZXRMS bit in the MODE2 register (0x0C).

With the specified full-scale ac analog input signal of 0.4 V, the output from the LPF1 in Figure 50 swings between 0x28F5 and 0xD70B at 60 Hz (see the Voltage Channel ADC section). The equivalent rms value of this full-scale ac signal is approximately 0d1,898,124 (0x1CF68C) in the V_{rms} register. The voltage rms measurement provided in the ADE7518 is accurate to within ±0.5% for signal input between full scale and full scale/20. The conversion from the register value to volts must be done externally in the microprocessor using a V/LSB constant.

Voltage Channel RMS Offset Compensation

The ADE7518 incorporates a voltage channel rms offset compensation register (VRMSOS). This is a 12-bit signed register that can be used to remove offset in the voltage channel rms calculation. An offset can exist in the rms calculation due to input noises and dc offset in the input samples. One LSB of the voltage channel rms offset is equivalent to 64 LSBs of the rms register. Assuming that the maximum value from the voltage channel rms calculation is 0d1,898,124 with full-scale ac inputs, then 1 LSB of the voltage channel rms offset represents 3.37% of measurement error at −60 dB down from full scale.

$$V_{rms} = V_{rms0} + 64 \times VRMSOS \quad (5)$$

where V_{rms0} is the rms measurement without offset correction.

ACTIVE POWER CALCULATION

Active power is defined as the rate of energy flow from source to load. It is the product of the voltage and current waveforms. The resulting waveform is called the instantaneous power signal and is equal to the rate of energy flow at every instant of time. The unit of power is watt or joules/second. Equation 8 gives an expression for the instantaneous power signal in an ac system.

$$v(t) = \sqrt{2} \times V \sin(\omega t) \quad (6)$$

$$i(t) = \sqrt{2} \times I \sin(\omega t) \quad (7)$$

where:
v is the rms voltage.
i is the rms current.

$$p(t) = v(t) \times i(t)$$

$$p(t) = VI - VI\cos(2\omega t) \quad (8)$$

The average power over an integral number of line cycles (n) is given by the expression in Equation 9.

$$P = \frac{1}{nT}\int_0^{nT} p(t)dt = VI \quad (9)$$

where:
T is the line cycle period.
P is referred to as the active or real power.

Note that the active power is equal to the dc component of the instantaneous power signal p(t) in Equation 9, that is, VI. This is the relationship used to calculate active power in the ADE7518. The instantaneous power signal p(t) is generated by multiplying the current and voltage signals. The dc component of the instantaneous power signal is then extracted by LPF2 (low-pass filter) to obtain the active power information. This process is illustrated in Figure 49.

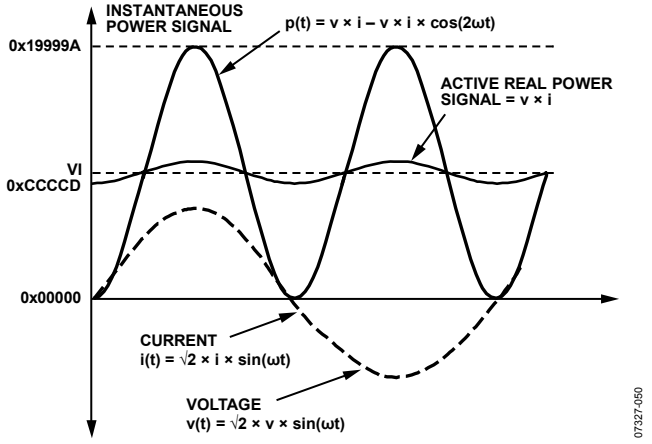


Figure 49. Active Power Calculation

Because LPF2 does not have an ideal brick wall frequency response (see Figure 51), the active power signal has some ripple due to the instantaneous power signal. This ripple is sinusoidal and has a frequency equal to twice the line frequency. Because of its sinusoidal nature, the ripple is removed when the active power signal is integrated to calculate energy (see the Active Energy Calculation section).

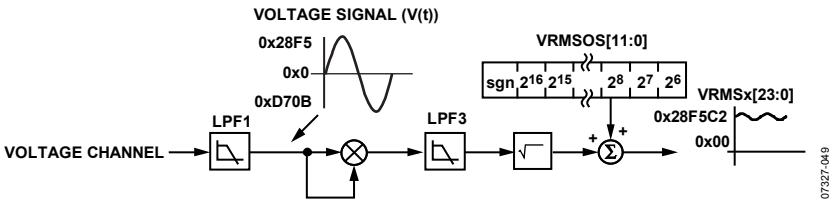


Figure 50. Voltage Channel RMS Signal Processing

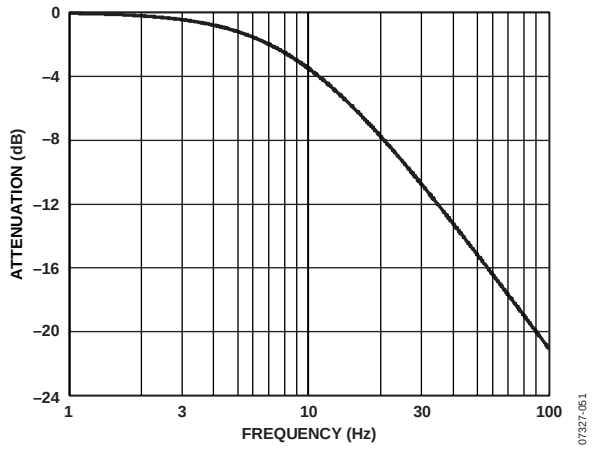


Figure 51. Frequency Response of LPF2

Active Power Gain Calibration

Figure 52 shows the signal processing chain for the active power calculation in the ADE7518. As explained previously, the active power is calculated by filtering the output of the multiplier with a low-pass filter. Note that when reading the waveform samples from the output of LPF2, the gain of the active energy can be adjusted by using the multiplier and watt gain register (WGAIN[11:0]). The gain is adjusted by writing a twos complement 12-bit word to the watt gain register. Equation 10 shows how the gain adjustment is related to the contents of the watt gain register.

$$Output\ WGAIN = \left(Active\ Power \times \left\{ 1 + \frac{WGAIN}{2^{12}} \right\} \right) \quad (10)$$

For example, when 0x7FF is written to the watt gain register, the power output is scaled up by 50% (0x7FF = 2047d, $2047/2^{12} = 0.5$). Similarly, 0x800 = −2048d (signed, twos complement) and power output is scaled by −50%. Each LSB scales the power output by 0.0244%. The minimum output range is given when the watt gain register contents are equal to 0x800 and the maximum range is given by writing 0x7FF to the watt gain register. This watt gain register can be used to calibrate the active power (or energy) calculation in the ADE7518.

Active Power Offset Calibration

The ADE7518 also incorporates an active power offset register (WATTOS[15:0]). It is a signed, twos complement, 16-bit register that can be used to remove offsets in the active power calculation (see Figure 49). An offset can exist in the power calculation due to crosstalk between channels on the PCB or in the IC itself. The offset calibration allows the contents of the active power register to be maintained at 0 when no power is being consumed.

The 256 LSBs (WATTOS = 0x0100) written to the active power offset register are equivalent to 1 LSB in the waveform sample register. Assuming the average value, output from LPF2 is 0xCCCCD (838,861d) when inputs on the voltage and current channels are both at full scale. At −60 dB below full scale on the current channel (1/1000 of the current channel full-scale input), the average word value output from LPF2 is 838.861 (838,861/1000). One LSB in the LPF2 output has a measurement error of 1/838.861 × 100% = 0.119% of the average value. The active power offset register has a resolution equal to 1/256 LSB of the waveform register. Therefore, the power offset correction resolution is 0.000464%/LSB (0.119%/256) at −60 dB.

Active Power Sign Detection

The ADE7518 detects a change of sign in the active power. The APSIGN flag in the Interrupt Status 1 SFR (MIRQSTL, 0xDC) records when a change of sign has occurred according to Bit APSIGN in the ACCMODE register (0x0F). If the APSIGN flag is set in the Interrupt Enable 1 SFR (MIRQENL, 0xD9), the 8052 core has a pending ADE interrupt. The ADE interrupt stays active until the APSIGN status bit is cleared (see the Energy Measurement Interrupts section).

When APSIGN in the ACCMODE register (0x0F) is cleared (default), the APSIGN flag in the Interrupt Status 1 SFR (MIRQSTL, 0xDC) is set when a transition from positive to negative active power has occurred.

If APSIGN in the ACCMODE register (0x0F) is set, the APSIGN flag in the MIRQSTL SFR is set when a transition from negative to positive active power occurs.

Active Power No Load Detection

The ADE7518 includes a no load threshold feature on the active energy that eliminates any creep effects in the meter. The part accomplishes this by not accumulating energy if the multiplier output is below the no load threshold. When the active power is below the no load threshold, the APNOLOAD flag in the Interrupt Status 1 SFR (MIRQSTL, 0xDC) is set. If the APNOLOAD bit is set in the Interrupt Enable 1 SFR (MIRQENL, 0xD9), the 8052 core has a pending ADE interrupt. The ADE interrupt stays active until the APNOLOAD status bit is cleared (see the Energy Measurement Interrupts section).

The no load threshold level is selectable by setting the APNOLOAD bits in the NLMODE register (0x0E). Setting these bits to 0b00 disables the no load detection, and setting them to 0b01, 0b10, or 0b11 sets the no load detection threshold to 0.015%, 0.0075%, or 0.0037%, respectively, of the multiplier's full-scale output frequency. The IEC 62053-21 specification states that the meter must start up with a load equal to or less than 0.4% I_P, which translates to 0.0167% of the full-scale output frequency of the multiplier.

ACTIVE ENERGY CALCULATION

As stated in the Active Power Calculation section, power is defined as the rate of energy flow. This relationship can be expressed mathematically in Equation 11.

$$P = \frac{dE}{dt} \tag{11}$$

where:
P is power.
E is energy.

Conversely, energy is given as the integral of power.

$$E = \int P(t)dt \tag{12}$$

The ADE7518 achieves the integration of the active power signal by continuously accumulating the active power signal in an internal, nonreadable, 49-bit energy register. The active energy register (WATTHR[23:0]) represents the upper 24 bits of this internal register. This discrete time accumulation or summation is equivalent to integration in continuous time. Equation 13 expresses the relationship.

$$E = \int p(t)dt = \lim_{t \to 0} \left\{ \sum_{n=1}^{\infty} p(nT) \times T \right\} \tag{13}$$

where:
n is the discrete time sample number.
T is the sample period.

The discrete time sample period (T) for the accumulation register in the ADE7518 is 1.22 µs (5/MCLK). In addition to calculating the energy, this integration removes any sinusoidal components that may be in the active power signal. Figure 52 shows this discrete time integration or accumulation. The active power signal in the waveform register is continuously added to the internal active energy register.

The active energy accumulation depends on the setting of the POAM and ABSAM bits in the ACCMODE register (0x0F). When both bits are cleared, the addition is signed and, therefore, negative energy is subtracted from the active energy contents. When both bits are set, the ADE7518 is set to be in the more restrictive mode, the positive-only accumulation mode.

When POAM in the ACCMODE register (0x0F) is set, only positive power contributes to the active energy accumulation. When ABSAM in the ACCMODE register (0x0F) is set, the absolute active power is used for the active energy accumulation (see the Watt-Absolute Accumulation Mode section).

The output of the multiplier is divided by the value in the WDIV register. If the value in the WDIV register is equal to 0, the internal active energy register is divided by 1. WDIV is an 8-bit unsigned register. After dividing by WDIV, the active energy is accumulated in a 49-bit internal energy accumulation register. The upper 24 bits of this register are accessible through a read to the active energy register (WATTHR[23:0]). A read to the RWATTHR register returns the content of the WATTHR register, and the upper 24 bits of the internal register are cleared. As shown in Figure 52, the active power signal is accumulated in an internal 49-bit signed register. The active power signal can be read from the waveform register by setting the WAVMODE register (0x0D) and setting the WFSM bit in the Interrupt Enable 3 SFR (MIRQENH, 0xDB). Like the current and voltage channels waveform sampling modes, the waveform data is available at a sample rate of 25.6 kSPS, 12.8 kSPS, 6.4 kSPS, or 3.2 kSPS.

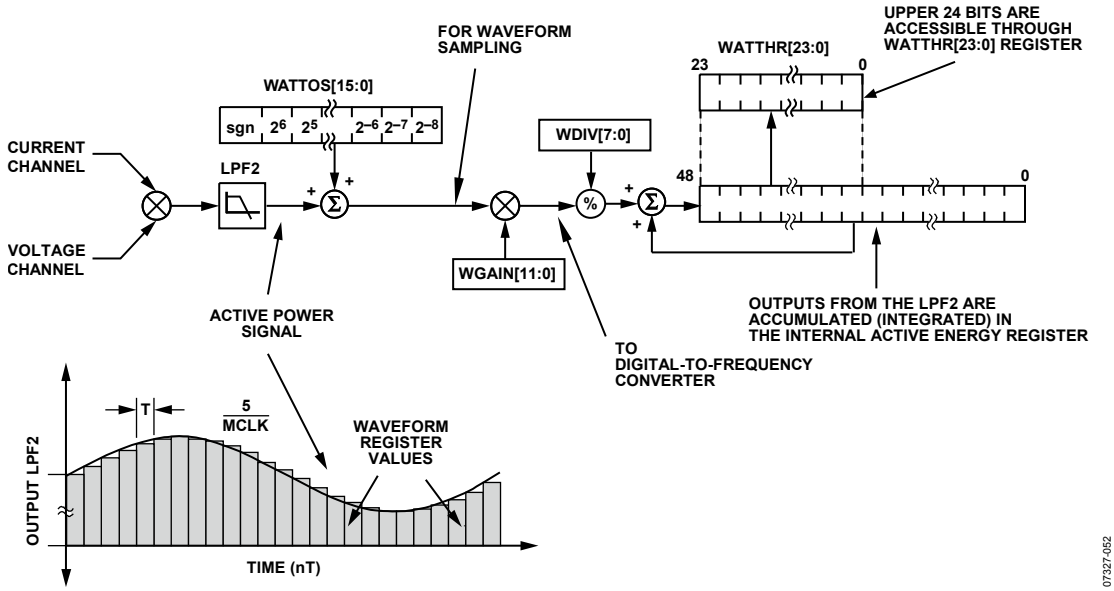


Figure 52. Active Energy Calculation

Figure 53 shows this energy accumulation for full-scale signals (sinusoidal) on the analog inputs. The three displayed curves illustrate the minimum period of time it takes the energy register to roll over when the active power gain register contents are 0x7FF, 0x000, and 0x800. The watt gain register is used to carry out power calibration in the ADE7518. As shown, the fastest integration time occurs when the watt gain register is set to maximum full scale, that is, 0x7FF.

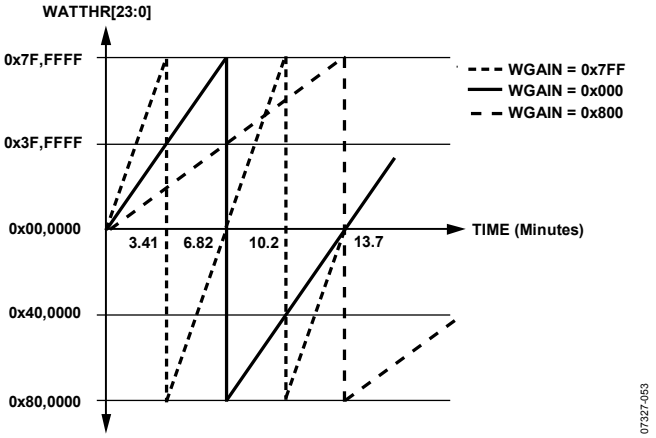


Figure 53. Energy Register Rollover Time for Full-Scale Power (Minimum and Maximum Power Gain)

Note that the energy register contents roll over to full-scale negative (0x800000) and continue to increase in value when the power or energy flow is positive (see Figure 53). Conversely, if the power is negative, the energy register underflows to full-scale positive (0x7FFFFF) and continues to decrease in value.

By using the interrupt enable register, the ADE7518 can be configured to issue an ADE interrupt to the 8052 core when the active energy register is half full (positive or negative) or when an overflow or underflow occurs.

Integration Time Under Steady Load: Active Energy

As mentioned previously, the discrete time sample period (T) for the accumulation register is 1.22 µs (5/MCLK). With full-scale sinusoidal signals on the analog inputs and the WGAIN register set to 0x000, the average word value from each LPF2 is 0xCCCCD (see Figure 49). The maximum positive value that can be stored in the internal 49-bit register is 2^{48} (or 0xFFFF,FFFF,FFFF) before it overflows. The integration time under these conditions when WDIV = 0 is calculated in the following equation:

$$Time = \frac{0xFFFF,FFFF,FFFF}{0xCCCCD} \times 1.22\ \mu s = 409.6\,sec = 6.82\,min \quad (14)$$

When WDIV is set to a value other than 0, the integration time varies, as shown in Equation 15.

$$Time = Time_{WDIV=0} \times WDIV \quad (15)$$

Active Energy Accumulation Modes

Watt-Signed Accumulation Mode

The ADE7518 active energy default accumulation mode is a watt-signed accumulation based on the active power information.

Watt Positive-Only Accumulation Mode

The ADE7518 is placed in watt positive-only accumulation mode by setting the POAM bit in the ACCMODE register (0x0F). In this mode, the energy accumulation is only done for positive power, ignoring any occurrence of negative power above or below the no load threshold (see Figure 54). The CF pulse also reflects this accumulation method when in this mode. The default setting for this mode is off. Detection of the transitions in the direction of power flow and detection of no load threshold are active in this mode.

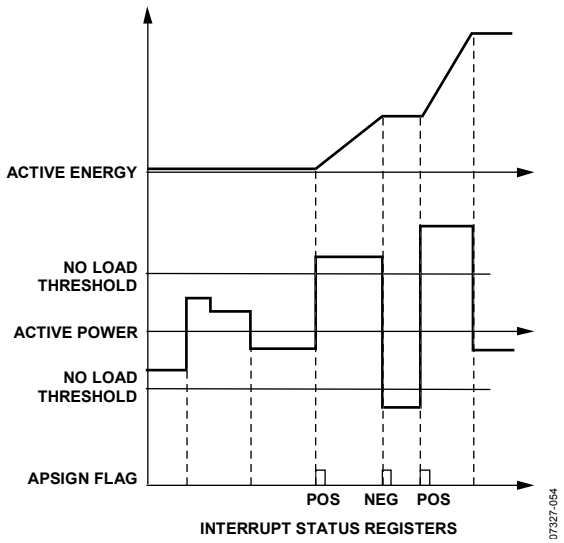


Figure 54. Energy Accumulation in Positive-Only Accumulation Mode

Watt-Absolute Accumulation Mode

The ADE7518 is placed in watt-absolute accumulation mode by setting the ABSAM bit in the ACCMODE register (0x0F). In this mode, the energy accumulation is done using the absolute active power, ignoring any occurrence of power below the no load threshold (see Figure 55). The CF pulse also reflects this accumulation method when in this mode. The default setting for this mode is off. Detection of the transitions in the direction of power flow and detection of a no load threshold are active in this mode.

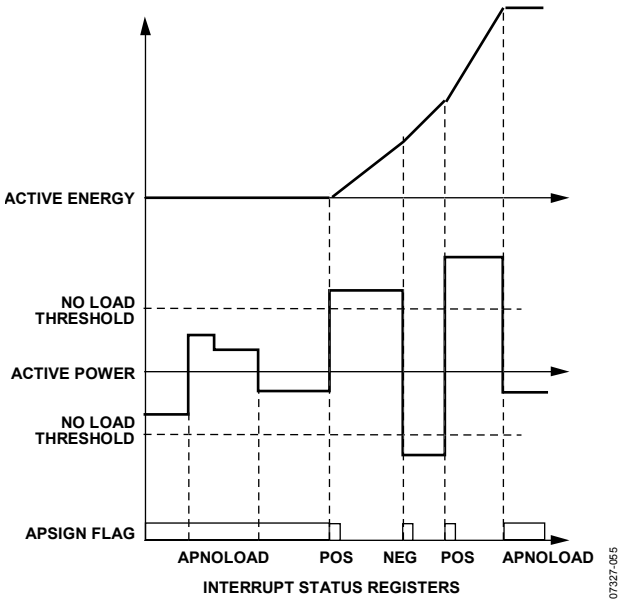


Figure 55. Energy Accumulation in Watt-Absolute Accumulation Mode

Active Energy Pulse Output

All of the ADE7518 circuitry has a pulse output whose frequency is proportional to active power (see the Active Power Calculation section). This pulse frequency output uses the calibrated signal from the WGAIN register output, and its behavior is consistent with the setting of the active energy accumulation mode in the ACCMODE register (0x0F). The pulse output is active low and should be preferably connected to an LED, as shown in Figure 66.

Line Cycle Active Energy Accumulation Mode

In line cycle active energy accumulation mode, the energy accumulation of the ADE7518 can be synchronized to the voltage channel zero crossing so that active energy can be accumulated over an integer number of half-line cycles. The advantage of summing the active energy over an integer number of line cycles is that the sinusoidal component in the active energy is reduced to 0. This eliminates any ripple in the energy calculation. Energy is calculated more accurately and more quickly because the integration period can be shortened. By using this mode, the energy calibration can be greatly simplified, and the time required to calibrate the meter can be significantly reduced.

In line cycle active energy accumulation mode, the ADE7518 accumulates the active power signal in the LWATTHR register for an integral number of line cycles, as shown in Figure 56. The number of half-line cycles is specified in the LINCYC register.

The ADE7518 can accumulate active power for up to 65,535 half-line cycles. Because the active power is integrated on an integer number of line cycles, the CYCEND flag in the Interrupt Status 3 SFR (MIRQSTH, 0xDE) is set at the end of an active energy accumulation line cycle. If the CYCEND enable bit in the Interrupt Enable 3 SFR (MIRQENH, 0xDB) is set, the 8052 core has a pending ADE interrupt. The ADE interrupt stays active until the CYCEND status bit is cleared (see the Energy Measurement Interrupts section). Another calibration cycle starts as soon as the CYCEND flag is set. If the LWATTHR register is not read before a new CYCEND flag is set, the LWATTHR register is overwritten by a new value.

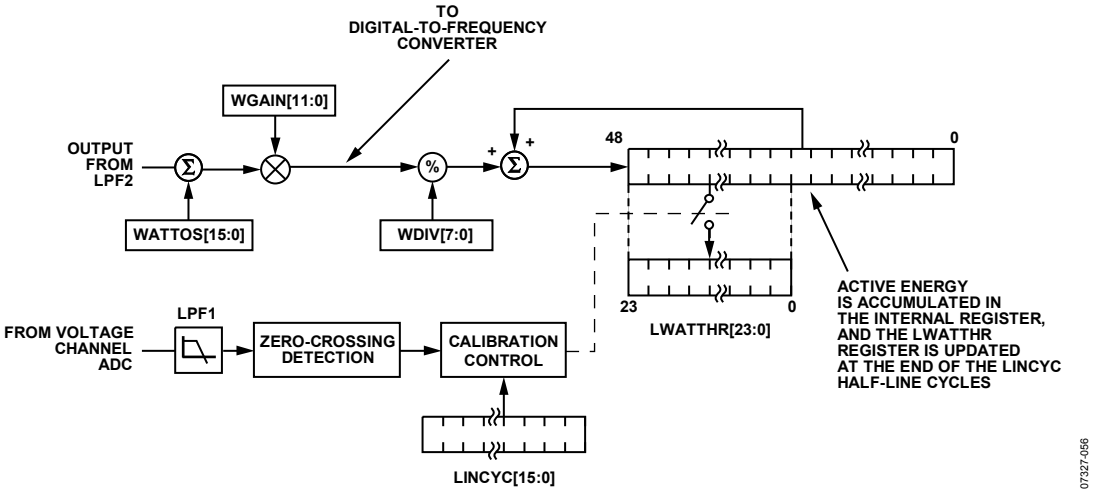


Figure 56. Line Cycle Active Energy Accumulation

When a new half-line cycle is written in the LINCYC register, the LWATTHR register is reset, and a new accumulation starts at the next zero crossing. The number of half-line cycles is then counted until LINCYC is reached. This implementation provides a valid measurement at the first CYCEND interrupt after writing to the LINCYC register (see Figure 57). The line active energy accumulation uses the same signal path as the active energy accumulation. The LSB size of these two registers is equivalent.

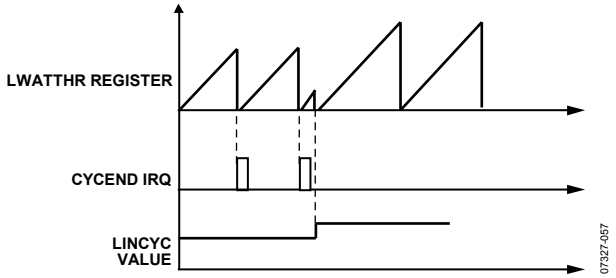


Figure 57. Energy Accumulation When LINCYC Changes

From the information in Equation 8 and Equation 9,

$$E(t) = \int_0^{nT} VI dt - \left\{ \frac{VI}{\sqrt{1+\left(\frac{f}{8.9}\right)^2}} \right\} \int_0^{nT} \cos(2\pi ft) dt \quad (16)$$

where:
n is an integer.
T is the line cycle period.

Because the sinusoidal component is integrated over an integer number of line cycles, its value is always 0. Therefore,

$$E = \int_0^{nT} VI dt + 0 \quad (17)$$

$$E(t) = VInT \quad (18)$$

Note that in this mode, the 16-bit LINCYC register can hold a maximum value of 65,535. In other words, the line energy accumulation mode can be used to accumulate active energy for a maximum duration of over 65,535 half-line cycles. At a 60 Hz line frequency, this translates to a total duration of 65,535/120 Hz = 546 sec.

REACTIVE POWER CALCULATION

Reactive power is defined as the product of the voltage and current waveforms when one of these signals is phase-shifted by 90°. The resulting waveform is called the instantaneous reactive power signal. Equation 21 gives an expression for the instantaneous reactive power signal in an ac system when the phase of the current channel is shifted by 90°.

$$v(t) = \sqrt{2}\, V \sin(\omega t + \theta) \quad (19)$$

$$i(t) = \sqrt{2}\, I \sin(\omega t)$$

$$i'(t) = \sqrt{2}\, I \sin\left(\omega t + \frac{\pi}{2}\right) \quad (20)$$

where:
θ is the phase difference between the voltage and current channel.
v is the rms voltage.
i is the rms current.

$$q(t) = v(t) \times i'(t) \quad (21)$$

$$q(t) = VI \sin(\theta) + VI \sin(2\omega t + \theta)$$

The average reactive power over an integer number of lines (n) is given in Equation 22.

$$Q = \frac{1}{nT} \int_0^{nT} q(t) dt = VI \sin(\theta) \quad (22)$$

where:
T is the line cycle period.
q is referred to as the reactive power.

Note that the reactive power is equal to the dc component of the instantaneous reactive power signal q(t) in Equation 21.

The instantaneous reactive power signal q(t) is generated by multiplying the voltage and current channels. In this case, the phase of the current channel is shifted by 90°. The dc component of the instantaneous reactive power signal is then extracted by a low-pass filter to obtain the reactive power information (see Figure 58).

In addition, the phase-shifting filter has a nonunity magnitude response. Because the phase-shifted filter has a large attenuation at high frequency, the reactive power is primarily for calculation at line frequency. The effect of harmonics is largely ignored in the reactive power calculation. Note that, because of the magnitude characteristic of the phase shifting filter, the weight of the reactive power is slightly different from that of the active power calculation (see the Energy Register Scaling section).

The frequency response of the LPF in the reactive signal path is identical to the one used for LPF2 in the average active power calculation. Because LPF2 does not have an ideal brick wall frequency response (see Figure 51), the reactive power signal has some ripple due to the instantaneous reactive power signal. This ripple is sinusoidal and has a frequency equal to twice the line frequency. Because the ripple is sinusoidal in nature, it is removed when the reactive power signal is integrated to calculate energy.

The reactive power signal can be read from the waveform register by setting the WAVMODE register (0x0D) and the WFSM bit in the Interrupt Enable 3 SFR (MIRQENH, 0xDB). Like the current and voltage channels waveform sampling modes, the waveform data is available at a sample rate of 25.6 kSPS, 12.8 kSPS, 6.4 kSPS, or 3.2 kSPS.

Reactive Power Gain Calibration

Figure 58 shows the signal processing chain for the ADE7518 reactive power calculation. As explained in the Reactive Power Calculation section, the reactive power is calculated by applying a low-pass filter to the instantaneous reactive power signal. Note that, when reading the waveform samples from the output of LPF2, the gain of the reactive energy can be adjusted by using the multiplier and by writing a twos complement, 12-bit word to the VAR gain register (VARGAIN[11:0]). Equation 23 shows how the gain adjustment is related to the contents of the watt gain register.

$$Output\ VARGAIN = \left(Reactive\ Power \times \left\{ 1 + \frac{VARGAIN}{2^{12}} \right\} \right) \quad (23)$$

The resolution of the VARGAIN register is the same as the WGAIN register (see the Active Power Gain Calibration section). VARGAIN can be used to calibrate the reactive power (or energy) calculation in the ADE7518.

Reactive Power Offset Calibration

The ADE7518 also incorporates a reactive power offset register (VAROS[15:0]). This is a signed, twos complement, 16-bit register that can be used to remove offsets in the reactive power calculation (see Figure 58). An offset may exist in the reactive power calculation due to crosstalk between channels on the PCB or in the IC itself. The offset calibration allows the contents of the reactive power register to be maintained at 0 when no power is being consumed.

The 256 LSBs (VAROS = 0x100) written to the reactive power offset register are equivalent to 1 LSB in the WAVMODE register.

Sign of Reactive Power Calculation

Note that the average reactive power is a signed calculation. The phase-shift filter has −90° phase shift when the integrator is enabled, and +90° phase shift when the integrator is disabled. Table 43 summarizes how the relationship of the phase difference between the voltage and the current affects the sign of the resulting VAR calculation.

Table 43. Sign of Reactive Power Calculation

Angle	Integrator	Sign
Between 0° to +90°	Off	Positive
Between −90° to 0°	Off	Negative
Between 0° to +90°	On	Positive
Between −90° to 0°	On	Negative

Reactive Power Sign Detection

The ADE7518 detects a change of sign in the reactive power. The VARSIGN flag in the Interrupt Status 1 SFR (MIRQSTL, 0xDC) records when a change of sign has occurred according to the VARSIGN bit in the ACCMODE register (0x0F). If the VARSIGN bit is set in the Interrupt Enable 1 SFR (MIRQENL, 0xD9), the 8052 core has a pending ADE interrupt. The ADE interrupt stays active until the VARSIGN status bit is cleared (see the Energy Measurement Interrupts section).

When VARSIGN in the ACCMODE register (0x0F) is cleared (default), the VARSIGN flag in the Interrupt Status 1 SFR (MIRQSTL, 0xDC) is set when a transition from positive to negative reactive power occurs.

If VARSIGN in the ACCMODE register (0x0F) is set, the VARSIGN flag in the Interrupt Status 1 SFR (MIRQSTL, 0xDC) is set when a transition from negative to positive reactive power occurs.

Reactive Power No Load Detection

The ADE7518 includes a no load threshold feature on the reactive energy that eliminates any creep effects in the meter. The ADE7518 accomplishes this by not accumulating reactive energy when the multiplier output is below the no load threshold. When the reactive power is below the no load threshold, the RNOLOAD flag in the Interrupt Status 1 SFR (MIRQSTL, 0xDC) is set. If the RNOLOAD bit is set in the Interrupt Enable 1 SFR (MIRQENL, 0xD9), the 8052 core has a pending ADE interrupt. The ADE interrupt stays active until the RNOLOAD status bit is cleared (see the Energy Measurement Interrupts section).

The no load threshold level is selectable by setting the VARNOLOAD bits in the NLMODE register (0x0E). Setting these bits to 0b00 disables the no load detection, and setting them to 0b01, 0b10, or 0b11 sets the no load detection threshold to 0.015%, 0.0075%, and 0.0037% of the full-scale output frequency of the multiplier, respectively.

REACTIVE ENERGY CALCULATION

As for reactive energy, the ADE7518 achieves the integration of the reactive power signal by continuously accumulating the reactive power signal in an internal, nonreadable, 49-bit energy register. The reactive energy register (VARHR[23:0]) represents the upper 24 bits of this internal register.

The discrete time sample period (T) for the accumulation register in the ADE7518 is 1.22 μs (5/MCLK). As well as calculating the energy, this integration removes any sinusoidal components that may be in the active power signal. Figure 58 shows this discrete time integration or accumulation. The reactive power signal in the waveform register is continuously added to the internal reactive energy register.

The reactive energy accumulation depends on the setting of the SAVARM and ABSVARM bits in the ACCMODE register (0x0F). When both bits are cleared, the addition is signed and, therefore, negative energy is subtracted from the reactive energy contents. When both bits are set, the ADE7518 is set to be in the more restrictive mode, the absolute accumulation mode.

When SAVARM in the ACCMODE register (0x0F) is set, the reactive power is accumulated depending on the sign of the active power. When active power is positive, the reactive power is added as it is to the reactive energy register. When active power is negative, the reactive power is subtracted from the reactive energy accumulator (see the VAR Antitamper Accumulation Mode section).

When ABSVARM in the ACCMODE register (0x0F) is set, the absolute reactive power is used for the reactive energy accumulation (see the VAR Absolute Accumulation Mode section).

The output of the multiplier is divided by VARDIV. If the value in the VARDIV register is equal to 0, the internal reactive energy register is divided by 1. VARDIV is an 8-bit, unsigned register. After dividing by VARDIV, the reactive energy is accumulated in a 49-bit internal energy accumulation register. The upper 24 bits of this register are accessible through a read to the reactive energy register (VARHR[23:0]). A read to the RVARHR register returns the content of the VARHR register, and the upper 24 bits of the internal register are cleared.

As shown in Figure 58, the reactive power signal is accumulated in an internal 49-bit signed register. The reactive power signal can be read from the waveform register by setting the WAVMODE register (0x0D) and setting the WFSM bit in the Interrupt Enable 3 SFR (MIRQENH, 0xDB). Like the current and voltage channel waveform sampling modes, the waveform data is available at a sample rate of 25.6 kSPS, 12.8 kSPS, 6.4 kSPS, or 3.2 kSPS.

Figure 53 shows this energy accumulation for full-scale signals (sinusoidal) on the analog inputs. These curves also apply for the reactive energy accumulation.

Note that the energy register contents roll over to full-scale negative (0x800000) and continue to increase in value when the power or energy flow is positive. Conversely, if the power is negative, the reactive energy register underflows to full-scale positive (0x7FFFFF) and continues to decrease in value.

By using the interrupt enable register, the ADE7518 can be configured to issue an ADE interrupt to the 8052 core when the reactive energy register is half full (positive or negative) or when an overflow or underflow occurs.

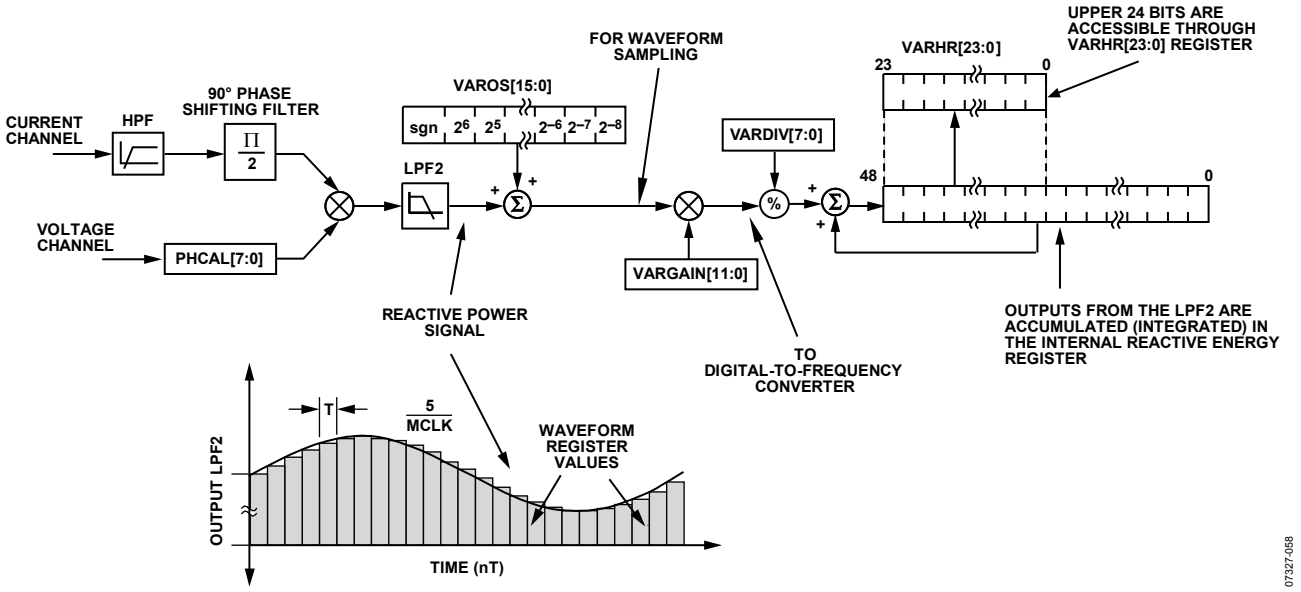


Figure 58. Reactive Energy Calculation

Integration Time Under Steady Load: Reactive Energy

As mentioned in the Active Energy Calculation section, the discrete time sample period (T) for the accumulation register is 1.22 µs (5/MCLK). With full-scale sinusoidal signals on the analog inputs and the VARGAIN and VARDIV registers set to 0x000, the integration time before the reactive energy register overflows is calculated in Equation 24.

$$Time = \frac{0xFFFF,FFFF,FFFF}{0xCCCCD} \times 1.22\,\mu s = 409.6\ sec = 6.82\ min \quad (24)$$

When VARDIV is set to a value other than 0, the integration time varies, as shown in Equation 25.

$$Time = Time_{WDIV=0} \times VARDIV \quad (25)$$

Reactive Energy Accumulation Modes

VAR-Signed Accumulation Mode

The ADE7518 reactive energy default accumulation mode is a signed accumulation based on the reactive power information.

VAR Antitamper Accumulation Mode

The ADE7518 is placed in VAR antitamper accumulation mode by setting the SAVARM bit in the ACCMODE register (0x0F). In this mode, the reactive power is accumulated depending on the sign of the active power. When active power is positive, the reactive power is added as it is to the reactive energy register. When active power is negative, the reactive power is subtracted from the reactive energy accumulator (see Figure 59). The CF pulse also reflects this accumulation method when in this mode. The default setting for this mode is off. Transitions in the direction of power flow and no load threshold are active in this mode.

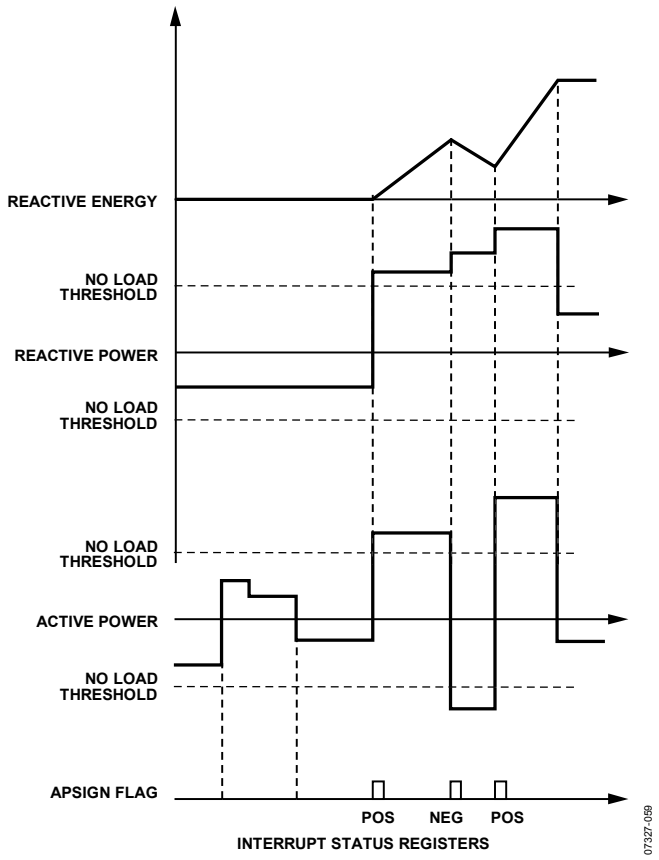


Figure 59. Reactive Energy Accumulation in Antitamper Accumulation Mode

VAR Absolute Accumulation Mode

The ADE7518 is placed in absolute accumulation mode by setting the ABSVARM bit in the ACCMODE register (0x0F). In absolute accumulation mode, the reactive energy accumulation is done by using the absolute reactive power and ignoring any occurrence of power below the no load threshold for the active energy (see Figure 60). The CF pulse also reflects this accumulation method when in absolute accumulation mode. The default setting for this mode is off. Transitions in the direction of power flow and no load threshold are active in this mode.

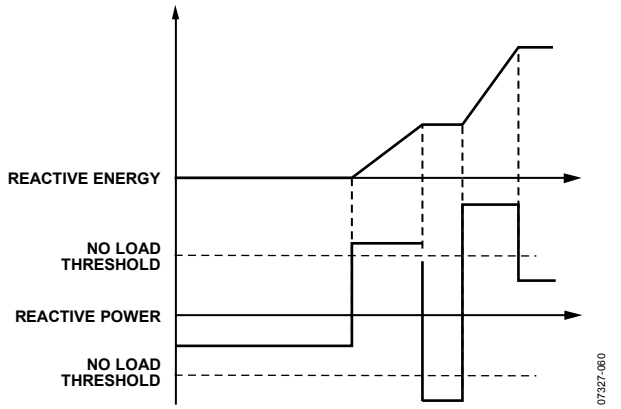


Figure 60. Reactive Energy Accumulation in Absolute Accumulation Mode

Reactive Energy Pulse Output

The ADE7518 provides all the circuitry with a pulse output whose frequency is proportional to reactive power (see the Energy-to-Frequency Conversion section). This pulse frequency output uses the calibrated signal after VARGAIN, and its behavior is consistent with the setting of the reactive energy accumulation mode in the ACCMODE register (0x0F). The pulse output is active low and should preferably be connected to an LED, as shown in Figure 66.

Line Cycle Reactive Energy Accumulation Mode

In line cycle reactive energy accumulation mode, the energy accumulation of the ADE7518 can be synchronized to the voltage channel zero crossing so that reactive energy can be accumulated over an integer number of half-line cycles. The advantage of this mode is similar to that described in the Line Cycle Active Energy Accumulation Mode section.

In line cycle active energy accumulation mode, the ADE7518 accumulates the reactive power signal in the LVARHR register for an integral number of line cycles, as shown in Figure 61. The number of half-line cycles is specified in the LINCYC register. The ADE7518 can accumulate active power for up to 65,535 half-line cycles.

Because the reactive power is integrated on an integer number of line cycles, the CYCEND flag in the Interrupt Status 3 SFR (MIRQSTH, 0xDE) is set at the end of an active energy accumulation line cycle. If the CYCEND enable bit in the Interrupt Enable 3 SFR (MIRQENH, 0xDB) is set, the 8052 core has a pending ADE interrupt. The ADE interrupt stays active until the CYCEND status bit is cleared (see the Energy Measurement Interrupts section). Another calibration cycle starts as soon as the CYCEND flag is set. If the LVARHR register is not read before a new CYCEND flag is set, the LVARHR register is overwritten by a new value.

When a new half-line cycle is written in the LINCYC register, the LVARHR register is reset, and a new accumulation starts at the next zero crossing. The number of half-line cycles is then counted until LINCYC is reached. This implementation provides a valid measurement at the first CYCEND interrupt after writing to the LINCYC register. The line reactive energy accumulation uses the same signal path as the reactive energy accumulation. The LSB size of these two registers is equivalent.

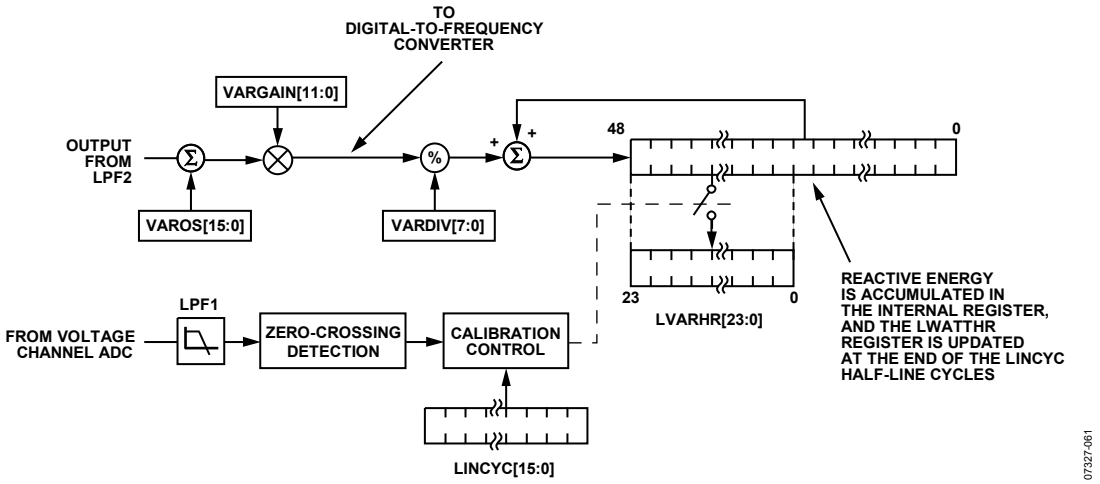


Figure 61. Line Cycle Reactive Energy Accumulation Mode

APPARENT POWER CALCULATION

Apparent power is defined as the maximum power that can be delivered to a load. V_{rms} and I_{rms} are the effective voltage and current delivered to the load, respectively. Therefore, the apparent power (AP) = $V_{rms} \times I_{rms}$. This equation is independent from the phase angle between the current and the voltage.

Equation 29 gives an expression of the instantaneous power signal in an ac system with a phase shift.

$$v(t) = \sqrt{2}\, V_{rms} \sin(\omega t) \quad (26)$$

$$i(t) = \sqrt{2}\ I_{rms} \sin(\omega t + \theta) \quad (27)$$

$$p(t) = v(t) \times i(t) \quad (28)$$

$$p(t) = V_{rms} I_{rms} \cos(\theta) - V_{rms} I_{rms} \cos(2\omega t + \theta) \quad (29)$$

Figure 62 illustrates the signal processing for the calculation of the apparent power in the ADE7518.

The apparent power signal can be read from the waveform register by setting the WAVMODE register (0x0D) and setting the WFSM bit in the Interrupt Enable 3 SFR (MIRQENH, 0xDB). Like the current and voltage channel waveform sampling modes, the waveform data is available at a sample rate of 25.6 kSPS, 12.8 kSPS, 6.4 kSPS, or 3.2 kSPS.

The gain of the apparent energy can be adjusted by using the multiplier and by writing a twos complement, 12-bit word to the VAGAIN register (VAGAIN[11:0]). Equation 30 shows how the gain adjustment is related to the contents of the VAGAIN register.

$$Output\ VAGAIN = \left(Apparent\ Power \times \left\{ 1 + \frac{VAGAIN}{2^{12}} \right\} \right) \quad (30)$$

For example, when 0x7FF is written to the VAGAIN register, the power output is scaled up by 50% (0x7FF = 2047d, $2047/2^{12} = 0.5$). Similarly, 0x800 = –2047d (signed twos complement) and power output is scaled by –50%. Each LSB represents 0.0244% of the power output. The apparent power is calculated with the current and voltage rms values obtained in the rms blocks of the ADE7518.

Apparent Power Offset Calibration

Each rms measurement includes an offset compensation register to calibrate and eliminate the dc component in the rms value (see the Current Channel RMS Calculation section and the Voltage Channel RMS Calculation section). The voltage and current channels rms values are then multiplied together in the apparent power signal processing. Because no additional offsets are created in the multiplication of the rms values, there is no specific offset compensation in the apparent power signal processing. The offset compensation of the apparent power measurement is done by calibrating each individual rms measurement.

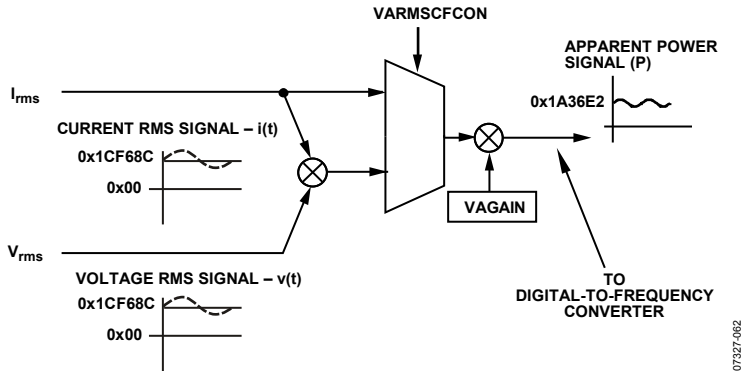


Figure 62. Apparent Power Signal Processing

APPARENT ENERGY CALCULATION

The apparent energy is given as the integer of the apparent power.

$$Apparent\ Energy = \int Apparent\ Power(t)dt \quad (31)$$

The ADE7518 achieves the integration of the apparent power signal by continuously accumulating the apparent power signal in an internal 48-bit register. The apparent energy register (VAHR[23:0]) represents the upper 24 bits of this internal register. This discrete time accumulation or summation is equivalent to integration in continuous time. Equation 32 expresses the relationship.

$$Apparent\ Energy = \lim_{T \to 0} \left\{ \sum_{n=0}^{\infty} Apparent\ Power(nT) \times T \right\} \quad (32)$$

where:
n is the discrete time sample number.
T is the sample period.

The discrete time sample period (T) for the accumulation register in the ADE7518 is 1.22 µs (5/MCLK).

Figure 63 shows this discrete time integration or accumulation. The apparent power signal is continuously added to the internal register. This addition is a signed addition even if the apparent energy theoretically remains positive.

The 49 bits of the internal register are divided by VADIV. If the value in the VADIV register is 0, the internal apparent energy register is divided by 1. VADIV is an 8-bit unsigned register. The upper 24 bits are then written in the 24-bit apparent energy register (VAHR[23:0]). The RVAHR register (24 bits long) is provided to read the apparent energy. This register is reset to 0 after a read operation.

Note that the apparent energy register is unsigned. By setting the VAEHF and VAEOF bits in the Interrupt Enable 2 SFR (MIRQENM, 0xDA), the ADE7518 can be configured to issue an ADE interrupt to the 8052 core when the apparent energy register is half-full or when an overflow occurs. The half-full interrupt for the unsigned apparent energy register is based on 24 bits as opposed to 23 bits for the signed active energy register.

Integration Times Under Steady Load: Apparent Energy

As mentioned in the Apparent Energy Calculation section, the discrete time sample period (T) for the accumulation register is 1.22 µs (5/MCLK). With full-scale sinusoidal signals on the analog inputs and the VAGAIN register set to 0x000, the average word value from the apparent power stage is 0x1A36E2 (see the Apparent Power Calculation section). The maximum value that can be stored in the apparent energy register before it overflows is 2^{24} or 0xFF,FFFF. The average word value is added to the internal register, which can store 248 or 0xFFFF,FFFF,FFFF before it overflows. Therefore, the integration time under these conditions with VADIV = 0 is calculated as follows:

$$Time = \frac{0xFFFF,FFFF,FFFF}{0xD055} \times 1.22\ \mu s = 199\ sec = 3.33\ min \quad (33)$$

When VADIV is set to a value other than 0, the integration time varies, as shown in Equation 34.

$$Time = Time_{WDIV=0} \times VADIV \quad (34)$$

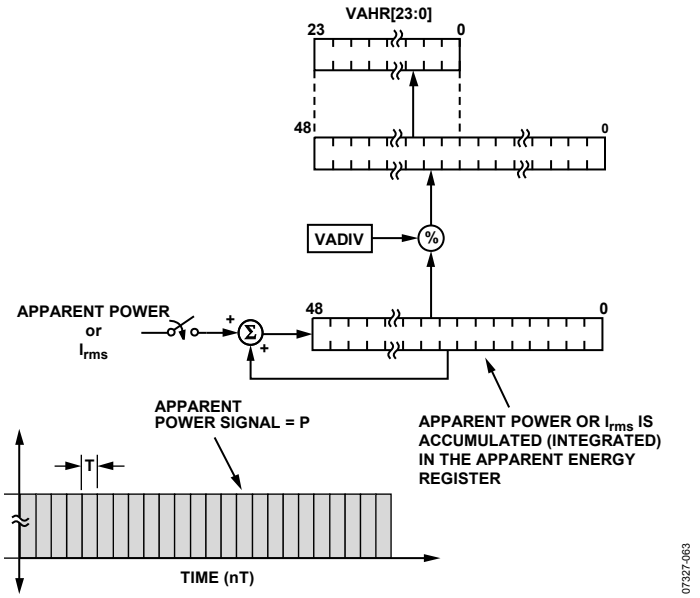


Figure 63. Apparent Energy Calculation

Apparent Energy Pulse Output

All ADE7518 circuitry has a pulse output whose frequency is proportional to apparent power (see the Energy-to-Frequency Conversion section). This pulse frequency output uses the calibrated signal after VAGAIN. This output can also be used to output a pulse whose frequency is proportional to I_{rms}.

The pulse output is active low and should preferably be connected to an LED, as shown in Figure 66.

Line Apparent Energy Accumulation

The ADE7518 is designed with a special apparent energy accumulation mode that simplifies the calibration process. By using the on-chip zero-crossing detection, the ADE7518 accumulates the apparent power signal in the LVAHR register for an integral number of half cycles, as shown in Figure 64. Line apparent energy accumulation mode is always active.

The number of half-line cycles is specified in the LINCYC register, which is an unsigned 16-bit register. The ADE7518 can accumulate apparent power for up to 65,535 combined half cycles. Because the apparent power is integrated on the same integral number of line cycles as the line active register and reactive energy register, these values can easily be compared. The energies are calculated more accurately because of this precise timing control, and provide all the information needed for reactive power and power factor calculation.

At the end of an energy calibration cycle, the CYCEND flag in the Interrupt Status 3 SFR (MIRQSTH, 0xDE) is set. If the CYCEND enable bit in the Interrupt Enable 3 SFR (MIRQENH, 0xDB) is enabled, the 8052 core has a pending ADE interrupt.

As for LWATTHR, when a new half-line cycle is written in the LINCYC register, the LVAHR register is reset and a new accumulation starts at the next zero crossing. The number of half-line cycles is then counted until LINCYC is reached.

This implementation provides a valid measurement at the first CYCEND interrupt after writing to the LINCYC register. The line apparent energy accumulation uses the same signal path as the apparent energy accumulation. The LSB size of these two registers is equivalent.

Apparent Power No Load Detection

The ADE7518 includes a no load threshold feature on the apparent power that eliminates any creep effects in the meter. The ADE7518 accomplishes this by not accumulating energy if the multiplier output is below the no load threshold. When the apparent power is below the no load threshold, the VANOLOAD flag in the Interrupt Status 1 SFR (MIRQSTL, 0xDC) is set. If the VANOLOAD bit is set in the Interrupt Enable 1 SFR (MIRQENL, 0xD9), the 8052 core has a pending ADE interrupt. The ADE interrupt stays active until the APNOLOAD status bit is cleared (see the Energy Measurement Interrupts section).

The no load threshold level is selectable by setting the VANOLOAD bits in the NLMODE register (0x0E). Setting these bits to 0b00 disables the no load detection, and setting them to 0b01, 0b10, or 0b11 sets the no load detection threshold to 0.030%, 0.015%, and 0.0075% of the full-scale output frequency of the multiplier, respectively.

This no load threshold can also be applied to the I_{rms} pulse output when selected. In this case, the level of no load threshold is the same as for the apparent energy.

AMPERE-HOUR ACCUMULATION

In a tampering situation where no voltage is available to the energy meter, the ADE7518 is capable of accumulating the ampere-hour instead of apparent power into VAHR, RVAHR, and LVAHR. When Bit 3 (VARMSCFCON) of the MODE2 register (0x0C) is set, VAHR, RVAHR, LVAHR, and the input for the digital-to-frequency converter accumulate I_{rms} instead of apparent power. All the signal processing and calibration registers available for apparent power and energy accumulation remain the same when ampere-hour accumulation is selected. However, the scaling difference between I_{rms} and apparent power requires independent values for gain calibration in the VAGAIN, VADIV, CFxNUM, and CFxDEN registers.

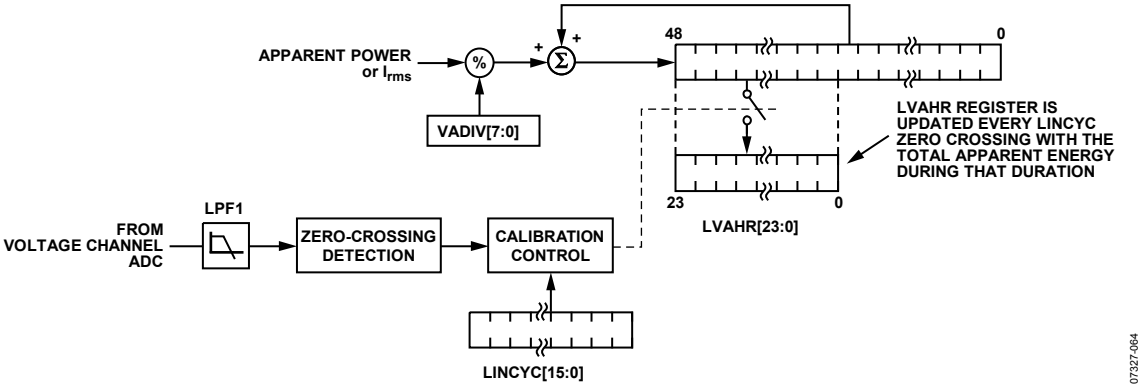


Figure 64. Line Cycle Apparent Energy Accumulation

ENERGY-TO-FREQUENCY CONVERSION

The ADE7518 also provides two energy-to-frequency conversions for calibration purposes. After initial calibration at manufacturing, the manufacturer or end customer often verifies the energy meter calibration. One convenient way to do this is for the manufacturer to provide an output frequency that is proportional to the active power, reactive power, apparent power, or I_{rms} under steady load conditions. This output frequency can provide a simple, single-wire, optically isolated interface to external calibration equipment. Figure 65 illustrates the energy-to-frequency conversion in the ADE7518.

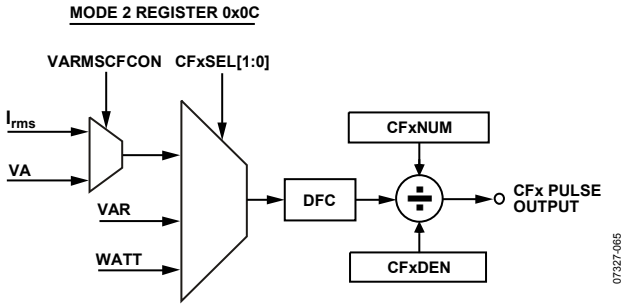


Figure 65. Energy-to-Frequency Conversion

Two digital-to-frequency converters (DFC) are used to generate the pulsed outputs. When WDIV = 0 or 1, the DFC generates a pulse each time 1 LSB in the energy register is accumulated. An output pulse is generated when a CFxNUM/CFxDEN number of pulses are generated at the DFC output. Under steady load conditions, the output frequency is proportional to the active power, reactive power, apparent power, or I_{rms}, depending on the CFxSEL bits in the MODE2 register (0x0C).

Both pulse outputs can be enabled or disabled by clearing or setting Bit DISCF1 and Bit DISCF2 in the MODE1 register (0x0B), respectively.

Both pulse outputs set separate flags in the Interrupt Status 2 SFR (MIRQSTM, 0xDD), CF1 and CF2. If the CF1 and CF2 enable bits in the Interrupt Enable 2 SFR (MIRQENM, 0xDA) are set, the 8052 core has a pending ADE interrupt. The ADE interrupt stays active until the CF1 or CF2 status bits are cleared (see the Energy Measurement Interrupts section).

Pulse Output Configuration

The two pulse output circuits have separate configuration bits in the MODE2 register (0x0C). Setting the CFxSEL bits to 0b00, 0b01, or 0b1x configures the DFC to create a pulse output proportional to active power, to reactive power, or to apparent power or I_{rms}, respectively.

The selection between I_{rms} and apparent power is done by the VARMSCFCON bit in the MODE2 register (0x0C). With this selection, CF2 cannot be proportional to apparent power if CF1 is proportional to I_{rms}, and CF1 cannot be proportional to apparent power if CF2 is proportional to I_{rms}.

Pulse Output Characteristic

The pulse output for both DFCs stays low for 90 ms if the pulse period is longer than 180 ms (5.56 Hz). If the pulse period is shorter than 180 ms, the duty cycle of the pulse output is 50%. The pulse output is active low and should preferably be connected to an LED, as shown in Figure 66.

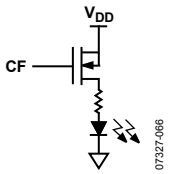


Figure 66. CF Pulse Output

The maximum output frequency with ac input signals at full scale and CFxNUM = 0x00 and CFxDEN = 0x00 is approximately 21.1 kHz.

The ADE7518 incorporates two registers per DFC, CFxNUM[15:0] and CFxDEN[15:0], to set the CFx frequency. These are unsigned 16-bit registers that can be used to adjust the CFx frequency to a wide range of values. These frequency scaling registers are 16-bit registers that can scale the output frequency by $1/2^{16}$ to 1 with a step of $1/2^{16}$.

If 0 is written to any of these registers, 1 is applied to the register. The ratio CFxNUM/CFxDEN should be less than 1 to ensure proper operation. If the ratio of the CFxNUM/CFxDEN registers is greater than 1, the register values are adjusted to a ratio of 1. For example, if the output frequency is 1.562 kHz and the content of CFxDEN is 0 (0x000), the output frequency can be set to 6.1 Hz by writing 0xFF to the CFxDEN register.

ENERGY REGISTER SCALING

The ADE7518 provides measurements of active, reactive, and apparent energies that use separate paths and filtering for calculation. The difference in data paths may result in small differences in LSB weight between active, reactive, and apparent energy registers. These measurements are internally compensated so that the scaling is nearly one to one. The relationship between these registers is shown in Table 44.

Table 44. Energy Registers Scaling

Line Frequency = 50 Hz	Line Frequency = 60 Hz	Integrator
VAR = 0.9952 × WATT	VAR = 0.9949 × WATT	Off
VA = 0.9978 × WATT	VA = 1.0015 × WATT	Off
VAR = 0.9997 × WATT	VAR = 0.9999 × WATT	On
VA = 0.9977 × WATT	VA = 1.0015 × WATT	On

ENERGY MEASUREMENT INTERRUPTS

The energy measurement part of the ADE7518 has its own interrupt vector for the 8052 core, Vector Address 0x004B (see the Interrupt Vectors section). The bits set in the Interrupt Enable 1 SFR (MIRQENL, 0xD9), Interrupt Enable 2 SFR (MIRQENM, 0xDA), and Interrupt Enable 3 SFR (MIRQENH, 0xDB) enable the energy measurement interrupts that are allowed to interrupt the 8052 core. If an event is not enabled, it cannot create a system interrupt.

The ADE interrupt stays active until the status bit that has created the interrupt is cleared. The status bit is cleared when a zero is written to this register bit.

8052 MCU CORE ARCHITECTURE

The ADE7518 has an 8052 MCU core and uses the 8051 instruction set. Some of the standard 8052 peripherals, such as the UART, have been enhanced. This section describes the standard 8052 core and its enhancements used in the ADE7518.

The special function register (SFR) space is mapped into the upper 128 bytes of internal data memory space and is accessed by direct addressing only. It provides an interface between the CPU and all on-chip peripherals. A block diagram showing the programming model of the ADE7518 via the SFR area is shown in Figure 67.

All registers except the program counter (PC), the instruction register (IR), and the four general-purpose register banks reside in the SFR area. The SFR registers include power control, configuration, and data registers that provide an interface between the CPU and all on-chip peripherals.

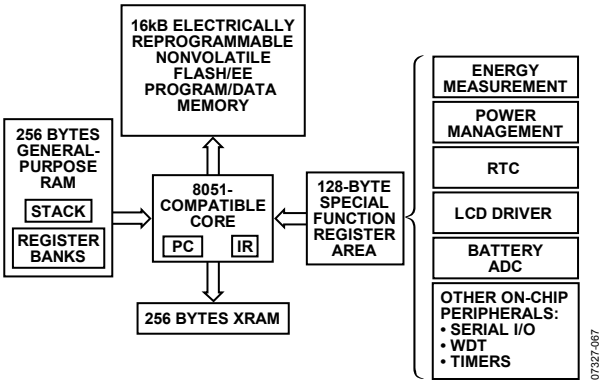


Figure 67. Block Diagram

MCU REGISTERS

The registers used by the MCU are summarized in this section.

Table 45. 8052 SFRs

Address	Mnemonic	Bit Addressable	Description
0xE0	ACC	Yes	Accumulator.
0xF0	B	Yes	Auxiliary Math.
0xD0	PSW	Yes	Program Status Word (see Table 46).
0x87	PCON	No	Program Control (see Table 47).
0x82	DPL	No	Data Pointer Low (see Table 48).
0x83	DPH	No	Data Pointer High (see Table 49).
0x83 and 0x82	DPTR	No	Data Pointer (see Table 50).
0x81	SP	No	Stack Pointer (see Table 51).
0xAF	CFG	No	Configuration (see Table 52).

Table 46. Program Status Word SFR (PSW, 0xD0)

Bit	Address	Mnemonic	Description		
7	0xD7	CY	Carry Flag. Modified by ADD, ADDC, SUBB, MUL, and DIV instructions.		
6	0xD6	AC	Auxiliary Carry Flag. Modified by ADD and ADDC instructions.		
5	0xD5	F0	General-Purpose Flag Available to the User.		
4 to 3	0xD4, 0xD3	RS1, RS0	Register Bank Select Bits.		
			RS1	**RS0**	**Result (Selected Bank)**
			0	0	0
			0	1	1
			1	0	2
			1	1	3
2	0xD2	OV	Overflow Flag. Modified by ADD, ADDC, SUBB, MUL, and DIV instructions.		
1	0xD1	F1	General-Purpose Flag Available to the User.		
0	0xD0	P	Parity Bit. The number of bits set in the accumulator added to the value of the parity bit is always an even number.		

Table 47. Program Control SFR (PCON, 0x87)

Bit	Default	Description
7	0	SMOD Bit. Double baud rate control.
6 to 0	0	Reserved. Should be left cleared.

Table 48. Data Pointer Low SFR (DPL, 0x82)

Bit	Default	Description
7 to 0	0	Contain the low byte of the data pointer.

Table 49. Data Pointer High SFR (DPH, 0x83)

Bit	Default	Description
7 to 0	0	Contain the high byte of the data pointer.

Table 50. Data Pointer SFR (DPTR, 0x82 and 0x83)

Bit	Default	Description
15 to 0	0	Contain the 2-byte address of the data pointer. DPTR is a combination of DPH and DPL SFRs.

Table 51. Stack Pointer SFR (SP, 0x81)

Bit	Default	Description
7 to 0	7	Contain the eight LSBs of the pointer for the stack.

Table 52. Configuration SFR (CFG, 0xAF)

Bit	Mnemonic	Description	
7	Reserved	This bit should be left set for proper operation.	
6	EXTEN	Enhanced UART Enable Bit.	
		EXTEN	**Result**
		0	Standard 8052 UART without enhanced error-checking features.
		1	Enhanced UART with enhanced error checking (see the UART Additional Features section).
5	SCPS	Synchronous Communication Selection Bit.	
		SCPS	**Result**
		0	I^2C port is selected for control of the shared I^2C/SPI pins (MOSI, MISO, SCLK, and $\overline{SS}$) and SFRs.
		1	SPI port is selected for control of the shared I^2C/SPI pins (MOSI, MISO, SCLK, and $\overline{SS}$) and SFRs.
4	MOD38EN	38 kHz Modulation Enable Bit.	
		MOD38EN	**Result**
		0	38 kHz modulation is disabled.
		1	38 kHz modulation is enabled on the pins selected by the MOD38[7:0] bits in the Extended Port Configuration SFR (EPCFG, 0x9F).
3 to 2	Reserved		
1 to 0	XREN1, XREN0	**XRENx**	**Result**
		XREN1 OR XREN0 = 1	Enables MOVX instruction to use 256 bytes of extended RAM.
		XREN1 AND XREN0 = 0	Disables MOVX instruction.

BASIC 8052 REGISTERS

Program Counter (PC)

The program counter holds the 2-byte address of the next instruction to be fetched. The PC is initialized with 0x00 at reset and is incremented after each instruction is performed. Note that the amount added to the PC depends on the number of bytes in the instruction, so the increment can range from one byte to three bytes. The program counter is not directly accessible to the user but can be directly modified by CALL and JMP instructions that change which part of the program is active.

Instruction Register (IR)

The instruction register holds the operations code of the instruction being executed. The operations code is the binary code that results from assembling an instruction. This register is not directly accessible to the user.

Register Banks

There are four banks that each contains eight byte-wide registers for a total of 32 bytes of registers. These registers are convenient for temporary storage of mathematical operands. An instruction involving the accumulator and a register can be executed in one clock cycle, as opposed to two clock cycles, to perform an instruction involving the accumulator and a literal or a byte of general-purpose RAM. The register banks are located in the first 32 bytes of RAM.

The active register bank is selected by the RS0 and RS1 bits in the Program Status Word SFR (PSW, 0xD0).

Accumulator

The accumulator is a working register, storing the results of many arithmetic or logical operations. The accumulator is used in more than half of the 8052 instructions, where it is usually referred to as "A." The program status register (PSW) constantly monitors the number of bits that are set in the accumulator to determine if it has even or odd parity. The accumulator is stored in the SFR space (see Table 45).

B Register

The B register is used by the multiply and divide instructions, MUL AB and DIV AB, to hold one of the operands. Because the B register is not used for many instructions, it can be used as a scratch pad register, such as those in the register banks. The B register is stored in the SFR space (see Table 45).

Program Status Word (PSW)

The PSW register reflects the status of arithmetic and logical operations through carry, auxiliary carry, and overflow flags. The parity flag reflects the parity of the accumulator contents, which can be helpful for communication protocols. The PSW bits are described in Table 46. The Program Status Word SFR (PSW, 0xD0) is bit addressable.

Data Pointer (DPTR)

The data pointer is made up of two 8-bit registers: DPH (high byte) and DPL (low byte). These provide memory addresses for internal code and data access. The DPTR can be manipulated as a 16-bit register (DPTR = DPH, DPL) or as two independent 8-bit registers (DPH, DPL). See Table 48 and Table 49.

The ADE7518 supports dual data pointers. See the Dual Data Pointers section. Note that the Dual Data Pointers section is the only section in the data sheet where the main and shadow data pointers are distinguished. Whenever the data pointer (DPTR) is mentioned elsewhere in the data sheet, active DPTR is implied.

Stack Pointer (SP)

The stack pointer keeps track of the current address at the top of the stack. To push a byte of data onto the stack, the stack pointer is incremented, and the data is moved to the new top of the stack. To pop a byte of data off the stack, the top byte of data is moved into the awaiting address, and the stack pointer is decremented. The stack is a last in, first out (LIFO) method of data storage because the most recent addition to the stack is the first to come off it.

The stack is utilized to store the program address when CALL and RET instructions are executed so that the program can return to this address when returning from the function call. The stack is also manipulated when vectoring for interrupts to keep track of the prior state of the PC.

The stack resides in the internal extended RAM, and the SP register holds the address of the stack in the extended RAM (XRAM). The advantage of this solution is that the stack is segregated to the internal XRAM. The use of the general-purpose RAM can be limited to data storage, and the use of the extended internal RAM can be limited to the stack pointer. This separation limits the chance of data RAM corruption when the stack pointer overflows in data RAM.

Data can still be stored in XRAM by using the MOVX command.

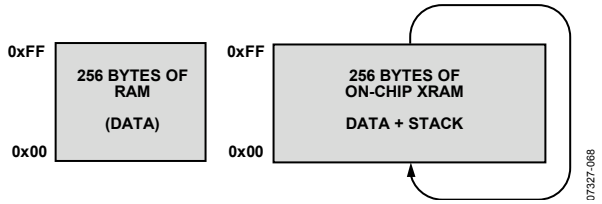


Figure 68. Extended Stack Pointer Operation

To change the default starting address for the stack, move a value into the stack pointer (SP). For example, to enable the extended stack pointer and initialize it at the beginning of the XRAM space, use the following code:

```
MOV    SP,#00H
```

STANDARD 8052 SFRS

The standard 8052 special function registers include the ACC, B, PSW, DPTR, and SP SFRs described in the Basic 8052 Registers section. The standard 8052 SFRs also define the timers, the serial port interface, the interrupts, the I/O ports, and the power-down modes.

Timer SFRs

The 8052 contains three 16-bit timers: the identical Timer0 and Timer1, as well as a Timer2. These timers can also function as event counters. Timer2 has a capture feature where the value of the timer can be captured in two 8-bit registers upon the assertion of an external input signal (see Table 91 and the Timers section).

Serial Port SFRs

The full-duplex serial port peripheral requires two registers: one for setting up the baud rate and other communication parameters, and another for the transmit/receive buffer. The ADE7518 also has enhanced serial port functionality with a dedicated timer for baud rate generation with a fractional divisor and additional error detection. See Table 120 and the UART Serial Interface section.

Interrupt SFRs

There is a two-tiered interrupt system standard in the 8052 core. The priority level for each interrupt source is individually selectable as high or low. The ADE7518 enhances this interrupt system by creating, in essence, a third interrupt tier for the highest priority, the power supply management (PSM) interrupt (see the Interrupt System section).

I/O Port SFRs

The 8052 core supports four I/O ports, Port 0 through Port 3, where Port 0 and Port 2 are typically used to access external code and data spaces. The ADE7518, unlike standard 8052 products, provides internal nonvolatile flash memory so that an external code space is unnecessary. The on-chip LCD driver requires many pins, some of which are dedicated for LCD functionality, and others that can be configured as LCD or general-purpose inputs/outputs. Due to the limited number of I/O pins, the ADE7518 does not allow access to external code and data spaces.

The ADE7518 provides 20 pins that can be used for general-purpose I/O. These pins are mapped to Port 0, Port 1, and Port 2. They are accessed through three bit-addressable 8052 SFRs, P0, P1, and P2. Another enhanced feature of the ADE7518 is that the weak pull-ups that are standard on 8052 Port 1, Port 2, and Port 3 can be disabled to make open-drain outputs, as is standard on Port 0. The weak pull-ups can be enabled on a pin-by-pin basis (see the I/O Ports section).

Program Control Register (PCON, 0x87)

The 8052 core defines two power-down modes: power-down and idle. The ADE7518 enhances the power control capability of the traditional 8052 MCU with additional power management functions. The Power Control SFR (POWCON, 0xC5) is used to define power control-specific functionality for the ADE7518. The Program Control SFR (PCON, 0x87) is not bit addressable (see the Power Management section).

The ADE7518 has many other peripherals not standard to the 8052 core, including

- ADE energy measurement DSP
- RTC
- LCD driver
- Battery switchover/power management
- SPI/I^2C communication
- Flash memory controller
- Watchdog timer

MEMORY OVERVIEW

The ADE7518 contains the following memory blocks:

- 16 kB of on-chip Flash/EE program and data memory
- 256 bytes of general-purpose RAM
- 256 bytes of internal extended RAM (XRAM)

The 256 bytes of general-purpose RAM share the upper 128 bytes of its address space with special function registers. All of the memory spaces are shown in Figure 69. The addressing mode specifies which memory space to access.

General-Purpose RAM

General-purpose RAM resides in the 0x00 through 0xFF memory locations and contains the register banks.

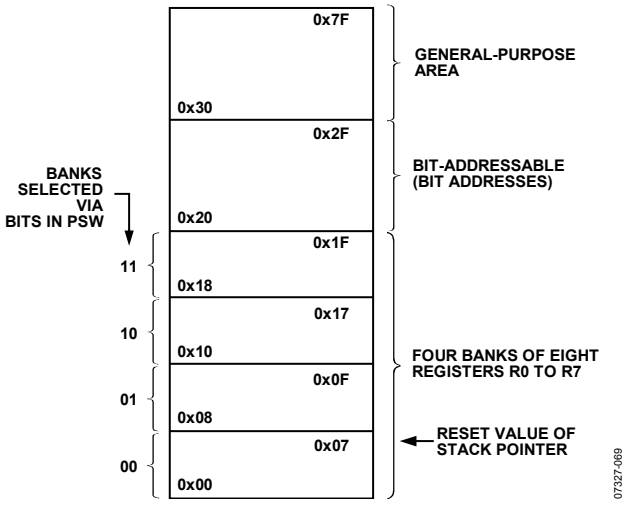


Figure 69. Lower 128 Bytes of Internal Data Memory

Address 0x80 through Address 0xFF of general-purpose RAM are shared with the special function registers. The mode of addressing determines which memory space is accessed, as shown in Figure 70.

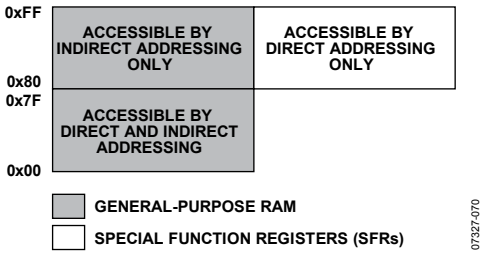


Figure 70. General-Purpose RAM and SFR Memory Address Overlap

Both direct and indirect addressing can be used to access general-purpose RAM from 0x00 through 0x7F. However, only indirect addressing can be used to access general-purpose RAM from 0x80 through 0xFF because this address space shares the same space with the special function registers (SFRs).

The 8052 core also has the means to access individual bits of certain addresses in the general-purpose RAM and special function memory spaces. The individual bits of general-purpose RAM Address 0x20 to RAM Address 0x2F can be accessed through Bit Address 0x00 through Bit Address 0x7F. The benefit of bit addressing is that the individual bits can be accessed quickly without the need for bit masking, which takes more code memory and execution time. The bit addresses for general-purpose RAM Address 0x20 through RAM Address 0x2F can be seen in Figure 71.

BYTE ADDRESS	BIT ADDRESSES (HEXA)							
0x2F	7F	7E	7D	7C	7B	7A	79	78
0x2E	77	76	75	74	73	72	71	70
0x2D	6F	6E	6D	6C	6B	6A	69	68
0x2C	67	66	65	64	63	62	61	60
0x2B	5F	5E	5D	5C	5B	5A	59	58
0x2A	57	56	55	54	53	52	51	50
0x29	4F	4E	4D	4C	4B	4A	49	48
0x28	47	46	45	44	43	42	41	40
0x27	3F	3E	3D	3C	3B	3A	39	38
0x26	37	36	35	34	33	32	31	30
0x25	2F	2E	2D	2C	2B	2A	29	28
0x24	27	26	25	24	23	22	21	20
0x23	1F	1E	1D	1C	1B	1A	19	18
0x22	17	16	15	14	13	12	11	10
0x21	0F	0E	0D	0C	0B	0A	09	08
0x20	07	06	05	04	03	02	01	00

07327-071

Figure 71. Bit Addressable Area of General-Purpose RAM

Bit addressing can be used for instructions that involve Boolean variable manipulation and program branching (see the Instruction Set section).

Special Function Registers

Special function registers are registers that affect the function of the 8052 core or its peripherals. These registers are located in RAM in Address 0x80 through Address 0xFF. They are only accessible through direct addressing, as shown in Figure 70.

The individual bits of some SFRs can be accessed for use in Boolean and program branching instructions. These SFRs are labeled as bit-addressable and the bit addresses are given in the SFR Mapping section.

Extended Internal RAM (XRAM)

The ADE7518 provides 256 bytes of extended on-chip RAM, which is located in Address 0x0000 through Address 0x00FF in the extended RAM space. No external RAM is supported. To select the extended RAM memory space, the extended indirect addressing modes are used. The internal XRAM is enabled in the Configuration SFR (CFG, 0xAF) by writing 01 to CFG[1:0].

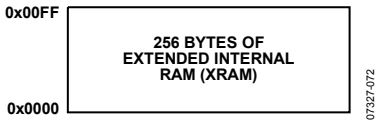


Figure 72. Extended Internal RAM (XRAM) Space

Code Memory

Code and data memory are stored in the 16 kB flash memory space. No external code memory is supported. To access code memory, code indirect addressing is used.

ADDRESSING MODES

The 8052 core provides several addressing modes. The addressing mode determines how the core interprets the memory location or data value specified in assembly language code. There are six addressing modes, as shown in Table 53.

Table 53. 8052 Addressing Modes

Addressing Mode	Example	Bytes	Core Clock Cycles
Immediate	MOV A, #A8h	2	2
	MOV DPTR, #A8h	3	3
Direct	MOV A, A8h	2	2
	MOV A, IE	2	2
	MOV A, R0	1	1
Indirect	MOV A, @R0	1	2
Extended Direct	MOVX A, @DPTR	1	4
Extended Indirect	MOVX A, @R0	1	4
Code Indirect	MOVC A, @A+DPTR	1	4
	MOVC A, @A+PC	1	4
	JMP @A+DPTR	1	3

Immediate Addressing

In immediate addressing, the expression entered after the number sign (#) is evaluated by the assembler and stored in the specified memory address. This number is referred to as a literal because it refers only to a value and not to a memory location.

Instructions using this addressing mode are slower than those between two registers because the literal must be stored and fetched from memory. The expression can be entered as a symbolic variable or an arithmetic expression; the value is computed by the assembler.

Direct Addressing

With direct addressing, the value at the source address is moved to the destination address. Direct addressing provides the fastest execution time of all the addressing modes when an instruction is performed between registers. Note that indirect or direct addressing modes can be used to access general-purpose RAM Address 0x00 through RAM Address 0x7F. An instruction with direct addressing that uses an address between 0x80 and 0xFF is referring to a special function memory location.

Indirect Addressing

With indirect addressing, the value pointed to by the register is moved to the destination address. For example, to move the contents of internal RAM Address 0x82 to the accumulator, use the following instructions:

```
MOV     R0,#82h
MOV     A,@R0
```

These two instructions require a total of four clock cycles and three bytes of storage in the program memory.

Indirect addressing allows addresses to be computed, which is useful for indexing into data arrays stored in RAM.

Note that an instruction that refers to Address 0x00 through Address 0x7F is referring to internal RAM, and indirect or direct addressing modes can be used. An instruction with indirect addressing that uses an address between 0x80 and 0xFF is referring to internal RAM, not to an SFR.

Extended Direct Addressing

The DPTR register (see Table 50) is used to access internal extended RAM in extended indirect addressing mode. The ADE7518 has 256 bytes of XRAM, accessed through MOVX instructions. External memory spaces are not supported on this device.

In extended direct addressing mode, the DPTR register points to the address of the byte of extended RAM. The following code moves the contents of extended RAM Address 0x100 to the accumulator:

```
MOV     DPTR,#100h
MOVX    A,@DPTR
```

These two instructions require a total of seven clock cycles and four bytes of storage in the program memory.

Extended Indirect Addressing

The internal extended RAM is accessed through a pointer to the address in indirect addressing mode. The ADE7518 has 256 bytes of internal extended RAM, accessed through MOVX instructions. External memory is not supported on the devices.

In extended indirect addressing mode, a register holds the address of the byte of extended RAM. The following code moves the contents of extended RAM Address 0x80 to the accumulator:

```
MOV     R0,#80h
MOVX    A,@R0
```

These two instructions require six clock cycles and three bytes of storage.

Note that there are 256 bytes of extended RAM; therefore, both extended direct and extended indirect addressing can cover the whole address range. There is a storage and speed advantage to using extended indirect addressing because the additional byte of addressing available through the DPTR register that is not needed is not stored.

From the three examples demonstrating the access of internal RAM from 0x80 through 0xFF, and the access of extended internal RAM from 0x00 through 0xFF, it can be seen that it is most efficient to use the entire internal RAM accessible through indirect access before moving to extended RAM.

Code Indirect Addressing

The internal code memory can be accessed indirectly. This can be useful for implementing lookup tables and other arrays of constants that are stored in flash. For example, to move the data stored in flash memory at Address 0x8002 into the accumulator, use the following code:

```
MOV     DPTR,#8002h
CLR     A
MOVX    A,@A+DPTR
```

The accumulator can be used as a variable index into the array of flash memory located at DPTR.

INSTRUCTION SET

Table 54 documents the number of clock cycles required for each instruction. Most instructions are executed in one or two clock cycles, resulting in a 4-MIPS peak performance.

Table 54. Instruction Set

Mnemonic	Description	Bytes	Cycles
Arithmetic			
ADD A, Rn	Add register to A	1	1
ADD A, @Ri	Add indirect memory to A	1	2
ADD A, dir	Add direct byte to A	2	2
ADD A, #data	Add immediate to A	2	2
ADDC A, Rn 1 1	Add register to A with carry	1	1
ADDC A, @Ri	Add indirect memory to A with carry	1	2
ADDC A, dir	Add direct byte to A with carry	2	2
ADDC A, #data	Add immediate to A with carry	2	2
SUBB A, Rn	Subtract register from A with borrow	1	1
SUBB A, @Ri	Subtract indirect memory from A with borrow	1	2
SUBB A, dir	Subtract direct from A with borrow	2	2
SUBB A, #data	Subtract immediate from A with borrow	2	2
INC A	Increment A	1	1
INC Rn	Increment register	1	1
INC @	Ri increment indirect memory	1	2
INC dir	Increment direct byte	2	2
INC DPTR	Increment data pointer	1	3
DEC A	Decrement A	1	1
DEC Rn	Decrement register	1	1
DEC @Ri	Decrement indirect memory	1	2
DEC dir	Decrement direct byte	2	2
MUL AB	Multiply A by B	1	9
DIV AB	Divide A by B	1	9
DA A	Decimal Adjust A	1	2
Logic			
ANL A, Rn	AND register to A	1	1
ANL A, @Ri	AND indirect memory to A	1	2
ANL A, dir	AND direct byte to A	2	2
ANL A, #data	AND immediate to A	2	2
ANL dir, A	AND A to direct byte	2	2
ANL dir, #data	AND immediate data to direct byte	3	3
ORL A, Rn	OR register to A	1	1
ORL A, @Ri	OR indirect memory to A	1	2
ORL A, dir	OR direct byte to A	2	2
ORL A, #data	OR immediate to A	2	2
ORL dir, A	OR A to direct byte	2	2
ORL dir, #data	OR immediate data to direct byte	3	3
XRL A, Rn	Exclusive OR register to A	1	1
XRL A, @Ri	Exclusive OR indirect memory to A	2	2
XRL A, #data	Exclusive OR immediate to A	2	2
XRL dir, A	Exclusive OR A to direct byte	2	2
XRL A, dir	Exclusive OR indirect memory to A	2	2
XRL dir, #data	Exclusive OR immediate data to direct	3	3
CLR A	Clear A	1	1
CPL A	Complement A	1	1
SWAP A	Swap nibbles of A	1	1
RL A	Rotate A left	1	1

Mnemonic	Description	Bytes	Cycles
RLC A	Rotate A left through carry	1	1
RR A	Rotate A right	1	1
RRC A	Rotate A right through carry	1	1
Data Transfer			
MOV A, Rn	Move register to A	1	1
MOV A, @Ri	Move indirect memory to A	1	2
MOV Rn, A	Move A to register	1	1
MOV @Ri, A	Move A to indirect memory	1	2
MOV A, dir	Move direct byte to A	2	2
MOV A, #data	Move immediate to A	2	2
MOV Rn, #data	Move register to immediate	2	2
MOV dir, A	Move A to direct byte	2	2
MOV Rn, dir	Move register to direct byte	2	2
MOV dir, Rn	Move direct to register	2	2
MOV @Ri, #data	Move immediate to indirect memory	2	2
MOV dir, @Ri	Move indirect to direct memory	2	2
MOV @Ri, dir	Move direct to indirect memory	2	2
MOV dir, dir	Move direct byte to direct byte	3	3
MOV dir, #data	Move immediate to direct byte	3	3
MOV DPTR, #data	Move immediate to data pointer	3	3
MOVC A, @A+DPTR	Move code byte relative DPTR to A	1	4
MOVC A, @A+PC	Move code byte relative PC to A	1	4
MOVX A, @Ri	Move external (A8) data to A	1	4
MOVX A, @DPTR	Move external (A16) data to A	1	4
MOVX @Ri, A	Move A to external data (A8)	1	4
MOVX @DPTR, A	Move A to external data (A16)	1	4
PUSH dir	Push direct byte onto stack	2	2
POP dir	Pop direct byte from stack	2	2
XCH A, Rn	Exchange A and register	1	1
XCH A, @Ri	Exchange A and indirect memory	1	2
XCHD A, @Ri	Exchange A and indirect memory nibble	1	2
XCH A, dir	Exchange A and direct byte	2	2
Boolean			
CLR C	Clear carry	1	1
CLR bit	Clear direct bit	2	2
SETB C	Set carry	1	1
SETB bit	Set direct bit	2	2
CPL C	Complement carry	1	1
CPL bit	Complement direct bit	2	2
ANL C, bit	AND direct bit and carry	2	2
ANL C, /bit	AND direct bit inverse to carry	2	2
ORL C, bit	OR direct bit and carry	2	2
ORL C, /bit OR	Direct bit inverse to carry	2	2
MOV C, bit	Move direct bit to carry	2	2
MOV bit, C	Move carry to direct bit	2	2
Branching			
JMP @A+DPTR	Jump indirect relative to DPTR	1	3
RET	Return from subroutine	1	4
RETI	Return from interrupt	1	4
ACALL addr11	Absolute jump to subroutine	2	3
AJMP addr11	Absolute jump unconditional	2	3
SJMP rel	Short jump (relative address)	2	3
JC rel	Jump on carry equal to 1	2	3

Mnemonic	Description	Bytes	Cycles
JNC rel	Jump on carry = 0	2	3
JZ rel	Jump on accumulator = 0	2	3
JNZ rel	Jump on accumulator ≠ 0	2	3
DJNZ Rn, rel	Decrement register, JNZ relative	2	3
LJMP	Long jump unconditional	3	4
LCALL addr16	Long jump to subroutine	3	4
JB bit, rel	Jump on direct bit = 1	3	4
JNB bit, rel	Jump on direct bit = 0	3	4
JBC bit, rel	Jump on direct bit = 1 and clear	3	4
CJNE A, dir, rel	Compare A, direct JNE relative	3	4
CJNE A, #data, rel	Compare A, immediate JNE relative	3	4
CJNE Rn, #data, rel	Compare register, immediate JNE relative	3	4
CJNE @Ri, #data, rel	Compare indirect, immediate JNE relative	3	4
DJNZ dir, rel	Decrement direct byte, JNZ relative	3	4
Miscellaneous			
NOP	No operation	1	1

READ-MODIFY-WRITE INSTRUCTIONS

Some 8052 instructions read the latch and others read the pin. The state of the pin is read for instructions that input a port bit. Instructions that read the latch rather than the pin are the ones that read a value, possibly change it, and rewrite it to the latch. Because these instructions involve modifying the port, it is assumed that the pin being modified is an output, so the output state of the pin is read from the latch. This prevents a possible misinterpretation of the voltage level of a pin. For example, if a port pin is used to drive the base of a transistor, a 1 is written to the bit to turn on the transistor. If the CPU reads the same port bit at the pin rather than the latch, it reads the base voltage of the transistor and interprets it as Logic 0. Reading the latch rather than the pin returns the correct value of 1.

The instructions that read the latch rather than the pin are called read-modify-write instructions and are listed in Table 55. When the destination operand is a port or a port bit, these instructions read the latch rather than the pin.

Table 55. Read-Modify-Write Instructions

Instruction	Example	Description
ANL	ANL P0, A	Logic AND.
ORL	ORL P1, A	Logic OR.
XRL	XRL P2, A	Logic XOR.
JBC	JBC P1.1, LABEL	Jump if Bit = 1 and Clear Bit.
CPL	CPL P2.0	Complement Bit.
INC	INC P2	Increment.
DEC	DEC P2	Decrement.
DJNZ	DJNZ P0, LABEL	Decrement and Jump if Not Zero.
MOV PX.Y,C[1]	MOV P0.0, C	Move Carry to Bit Y of Port X.
CLR PX.Y[1]	CLR P0.0	Clear Bit Y of Port X.
SETB PX.Y[1]	SETB P0.0	Set Bit Y of Port X.

[1] These instructions read the port byte (all eight bits), modify the addressed bit, and write the new byte back to the latch.

INSTRUCTIONS THAT AFFECT FLAGS

Many instructions explicitly modify the carry bit, such as the MOV C bit and CLR C instructions. Other instructions that affect status flags are listed in this section.

ADD A, Source

This instruction adds the source to the accumulator. No status flags are referenced by the instruction.

Affected Status Flags

C — Set if there is a carry out of Bit 7. Cleared otherwise. Used to indicate an overflow if the operands are unsigned.

OV — Set if there is a carry out of Bit 6 or a carry out of Bit 7, but not if both are set. Used to indicate an overflow for signed addition. This flag is set if two positive operands yield a negative result or if two negative operands yield a positive result.

AC — Set if there is a carry out of Bit 3. Cleared otherwise.

ADDC A, Source

This instruction adds the source and the carry bit to the accumulator. The carry status flag is referenced by the instruction.

Affected Status Flags

C — Set if there is a carry out of Bit 7. Cleared otherwise. Used to indicate an overflow if the operands are unsigned.

OV — Set if there is a carry out of Bit 6 or a carry out of Bit 7, but not if both are set. Used to indicate an overflow for signed addition. This flag is set if two positive operands yield a negative result or if two negative operands yield a positive result.

AC — Set if there is a carry out of Bit 3. Cleared otherwise.

SUBB A, Source

This instruction subtracts the source byte and the carry (borrow) flag from the accumulator. It references the carry (borrow) status flag.

Affected Status Flags

C Set if there is a borrow needed for Bit 7. Cleared otherwise. Used to indicate an overflow if the operands are unsigned.

OV Set if there is a borrow needed for Bit 6 or Bit 7, but not for both. Used to indicate an overflow for signed subtraction. This flag is set if a negative number subtracted from a positive yields a negative result or if a positive number subtracted from a negative number yields a positive result.

AC Set if a borrow is needed for Bit 3. Cleared otherwise.

MUL AB

This instruction multiplies the accumulator by the B register. This operation is unsigned. The lower byte of the 16-bit product is stored in the accumulator and the higher byte is left in the B register. No status flags are referenced by the instruction.

Affected Status Flags

C Cleared.

OV Set if the result is greater than 255. Cleared otherwise.

DIV AB

This instruction divides the accumulator by the B register. This operation is unsigned. The integer part of the quotient is stored in the accumulator and the remainder goes into the B register. No status flags are referenced by the instruction.

Affected Status Flags

C Cleared.

OV Cleared unless the B register is equal to 0, in which case the results of the division are undefined and the OV flag is set.

DA A

This instruction adjusts the accumulator to hold two 4-bit digits after the addition of two binary coded decimals (BCDs) with the ADD or ADDC instructions. If the AC bit is set or if the value of Bit 0 to Bit 3 exceeds nine, 0x06 is added to the accumulator to correct the lower four bits. If the carry bit is set when the instruction begins, or if 0x06 is added to the accumulator in the first step, 0x60 is added to the accumulator to correct the higher four bits.

The carry and AC status flags are referenced by this instruction.

Affected Status Flag

C Set if the result is greater than 0x99. Cleared otherwise.

RRC A

This instruction rotates the accumulator to the right through the carry flag. The old LSB of the accumulator becomes the new carry flag, and the old carry flag is loaded into the new MSB of the accumulator.

The carry status flag is referenced by this instruction.

Affected Status Flag

C Equal to the state of ACC.0 before execution of the instruction.

RLC A

This instruction rotates the accumulator to the left through the carry flag. The old MSB of the accumulator becomes the new carry flag, and the old carry flag is loaded into the new LSB of the accumulator.

The carry status flag is referenced by this instruction.

Affected Status Flag

C Equal to the state of ACC.7 before execution of the instruction.

CJNE Destination, Source, Relative Jump

This instruction compares the source value to the destination value and branches to the location set by the relative jump if they are not equal. If the values are equal, program execution continues with the instruction after the CJNE instruction.

No status flags are referenced by this instruction.

Affected Status Flag

C Set if the source value is greater than the destination value. Cleared otherwise.

DUAL DATA POINTERS

The ADE7518 incorporates two data pointers. The second data pointer is a shadow data pointer and is selected via the Data Pointer Control SFR (DPCON, 0xA7). DPCON features automatic hardware postincrement and postdecrement, as well as an automatic data pointer toggle.

Note that this is the only section of the data sheet where the main and shadow data pointers are distinguished. Whenever the data pointer (DPTR) is mentioned elsewhere in the data sheet, active DPTR is implied.

In addition, only the MOVC/MOVX @DPTR instructions automatically postincrement and postdecrement the DPTR. Other MOVC/MOVX instructions, such as MOVC PC or MOVC @Ri, do not cause the DPTR to automatically postincrement and postdecrement.

To illustrate the operation of DPCON, the following code copies 256 bytes of code memory at Address 0xD000 into XRAM, starting from Address 0x0000:

```
  MOV DPTR,#0       ;Main DPTR = 0
  MOV DPCON,#55H    ;Select shadow DPTR
    ;DPTR1 increment mode
    ;DPTR0 increment mode
    ;DPTR auto toggling ON
  MOV DPTR,#0D000H  ;DPTR = D000H
MOVELOOP: CLR A
  MOVC A,@A+DPTR    ;Get data
    ;Post Inc DPTR
    ;Swap to Main DPTR(Data)
             MOVX @DPTR,A    ;Put ACC in XRAM
    ;Increment main DPTR
    ;Swap Shadow DPTR(Code)
   MOV A, DPL
   JNZ MOVELOOP
```

Table 56. Data Pointer Control SFR (DPCON, 0xA7)

Bit	Mnemonic	Default	Description		
7		0	Not Implemented. Write don't care.		
6	DPT	0	Data Pointer Automatic Toggle Enable. Cleared by the user to disable autoswapping of the DPTR. Set in user software to enable automatic toggling of the DPTR after each MOVX or MOVC instruction.		
5 to 4	DP1m1, DP1m0	00	Shadow Data Pointer Mode. These bits enable extra modes of the shadow data pointer operation, allowing more compact and more efficient code size and execution.		
			DP1m1	**DP1m0**	**Result (Behavior of the Shadow Data Pointer)**
			0	0	8052 behavior.
			0	1	DPTR is postincremented after a MOVX or MOVC instruction.
			1	0	DPTR is postdecremented after a MOVX or MOVC instruction.
			1	1	DPTR LSB is toggled after a MOVX or MOVC instruction. This instruction can be useful for moving 8-bit blocks to/from 16-bit devices.
3to 2	DP0m1, DP0m0	00	Main Data Pointer Mode. These bits enable extra modes of the main data pointer operation, allowing more compact and more efficient code size and execution.		
			DP0m1	**DP0m0**	**Result (Behavior of the Main Data Pointer)**
			0	0	8052 behavior.
			0	1	DPTR is postincremented after a MOVX or MOVC instruction.
			1	0	DPTR is postdecremented after a MOVX or MOVC instruction.
			1	1	DPTR LSB is toggled after a MOVX or MOVC instruction. This instruction is useful for moving 8-bit blocks to/from 16-bit devices.
1		0	Not Implemented. Write don't care.		
0	DPSEL	0	Data Pointer Select. Cleared by the user to select the main data pointer, meaning that the contents of this 16-bit register are placed into the DPL SFR and DPH SFR. Set by the user to select the shadow data pointer, meaning that the contents of a separate 16-bit register appear in the DPL SFR and DPH SFR.		

INTERRUPT SYSTEM

The unique power management architecture of the ADE7518 includes an operating mode (PSM2) where the 8052 MCU core is shut down. Events can be configured to wake the 8052 MCU core from the PSM2 operating mode. A distinction is drawn here between events that can trigger the wake-up of the 8052 MCU core and events that can trigger an interrupt when the MCU core is active. Events that can wake the core are referred to as wake-up events, whereas events that can interrupt the program flow when the MCU is active are called interrupts. See the 3.3 V Peripherals and Wake-Up Events section to learn more about events that can wake the 8052 core from PSM2.

The ADE7518 provides 12 interrupt sources with three priority levels. The power management interrupt is at the highest priority level. The other two priority levels are configurable through the Interrupt Priority SFR (IP, 0xB8) and the Interrupt Enable and Priority 2 SFR (IEIP2, 0xA9).

STANDARD 8052 INTERRUPT ARCHITECTURE

The 8052 standard interrupt architecture includes two tiers of interrupts, where some interrupts are assigned a high priority and others are assigned a low priority.

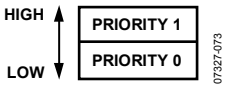


Figure 73. Standard 8052 Interrupt Priority Levels

A Priority 1 interrupt can interrupt the service routine of a Priority 0 interrupt, and if two interrupts of different priorities occur at the same time, the Priority 1 interrupt is serviced first. An interrupt cannot be interrupted by another interrupt of the same priority level. If two interrupts of the same priority level occur simultaneously, a polling sequence is observed (see the Interrupt Priority section).

INTERRUPT ARCHITECTURE

The ADE7518 possesses advanced power supply managment features. To ensure a fast response to time-critical power supply issues, such as a loss of line power, the power supply managment interrupt should be able to interrupt any interrupt service routine. To enable the user to have full use of the standard 8052 interrupt priority levels, an additional priority level is added for the power supply management (PSM) interrupt. The PSM interrupt is the only interrupt at this highest interrupt priority level.

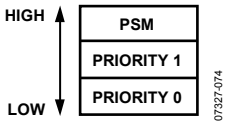


Figure 74. Interrupt Architecture

See the Power Supply Management (PSM) Interrupt section for more information on the PSM interrupt.

INTERRUPT REGISTERS

The control and configuration of the interrupt system is carried out through four interrupt-related SFRs discussed in this section.

Table 57. Interrupt SFRs

SFR	Address	Default	Bit Addressable	Description
IE	0xA8	0x00	Yes	Interrupt Enable (see Table 58).
IP	0xB8	0x00	Yes	Interrupt Priority (see Table 59).
IEIP2	0xA9	0xA0	No	Interrupt Enable and Priority 2 (see Table 60).
WDCON	0xC0	0x10	Yes	Watchdog Timer (see Table 65 and the Writing to the Watchdog Timer SFR (WDCON, 0xC0) section).

Table 58. Interrupt Enable SFR (IE, 0xA8)

Bit	Address	Mnemonic	Description
7	0xAF	EA	Enables All Interrupt Sources. Set by the user. Cleared by the user to disable all interrupt sources.
6	0xAE	Reserved	This bit should be left cleared for proper operation.
5	0xAD	ET2	Enables the Timer 2 Interrupt. Set by the user.
4	0xAC	ES	Enables the UART Serial Port Interrupt. Set by the user.
3	0xAB	ET1	Enables the Timer 1 Interrupt. Set by the user.
2	0xAA	EX1	Enables the External Interrupt 1 ($\overline{INT1}$). Set by the user.
1	0xA9	ET0	Enables the Timer 0 Interrupt. Set by the user.
0	0xA8	EX0	Enables External Interrupt 0 ($\overline{INT0}$). Set by the user.

Table 59. Interrupt Priority SFR (IP, 0xB8)

Bit	Address	Mnemonic	Description
7	0xBF	PADE	ADE Energy Measurement Interrupt Priority (1 = high, 0 = low).
6	0xBE	Reserved	This bit should be left cleared for proper operation.
5	0xBD	PT2	Timer 2 Interrupt Priority (1 = high, 0 = low).
4	0xBC	PS	UART Serial Port Interrupt Priority (1 = high, 0 = low).
3	0xBB	PT1	Timer 1 Interrupt Priority (1 = high, 0 = low).
2	0xBA	PX1	$\overline{\text{INT1}}$ (External Interrupt 1) Priority (1 = high, 0 = low).
1	0xB9	PT0	Timer 0 Interrupt Priority (1 = high, 0 = low).
0	0xB8	PX0	$\overline{\text{INT0}}$ (External Interrupt 0) Priority (1 = high, 0 = low).

Table 60. Interrupt Enable and Priority 2 SFR (IEIP2, 0xA9)

Bit	Mnemonic	Description
7	Reserved	Reserved.
6	PTI	RTC Interrupt Priority (1 = high, 0 = low).
5	Reserved	Reserved.
4	PSI	SPI/I^2C Interrupt Priority (1 = high, 0 = low).
3	EADE	Enables the Energy Metering Interrupt (ADE). Set by the user.
2	ETI	Enables the RTC Interval Timer Interrupt. Set by the user.
1	EPSM	Enables the PSM Power Supply Management Interrupt. Set by the user.
0	ESI	Enables the SPI/I^2C Interrupt. Set by the user.

INTERRUPT PRIORITY

If two interrupts of the same priority level occur simultaneously, the polling sequence is observed (as shown in Table 61).

Table 61. Priority Within Interrupt Level

Source	Priority	Description
IPSM	0 (Highest)	Power Supply Management Interrupt.
IRTC	1	RTC Interval Timer Interrupt.
IADE	2	ADE Energy Measurement Interrupt.
WDT	3	Watchdog Timer Overflow Interrupt.
IE0	4	External Interrupt 0.
TF0	5	Timer/Counter 0 Interrupt.
IE1	6	External Interrupt 1.
TF1	7	Timer/Counter 1 Interrupt.
ISPI/I2CI	8	SPI/I^2C Interrupt.
RI/TI	9	UART Serial Port Interrupt.
TF2/EXF2	10 (Lowest)	Timer/Counter 2 Interrupt.

INTERRUPT FLAGS

The interrupt flags and status flags associated with the interrupt vectors are shown in Table 62 and Table 63. Most of the interrupts have flags associated with them.

Table 62. Interrupt Flags

Interrupt Source	Flag	Bit Name	Description
IE0	TCON.1	IE0	External Interrupt 0.
TF0	TCON.5	TF0	Timer 0.
IE1	TCON.3	IE1	External Interrupt 1.
TF1	TCON.7	TF1	Timer 1.
RI + TI	SCON.1	TI	Transmit Interrupt.
	SCON.0	RI	Receive Interrupt.
TF2 + EXF2	T2CON.7	TF2	Timer 2 Overflow Flag.
	T2CON.6	EXF2	Timer 2 External Flag.
IPSM (Power Supply)	IPSMF.6	FPSM	PSM Interrupt Flag.
IADE (Energy Measurement DSP)	MIRQSTL.7	ADEIRQFLAG	Read MIRQSTH, MIRQSTM, MIRQSTL.

Table 63. Status Flags

Interrupt Source	Flag	Bit Name	Description
ISPI/I2CI	SPI2CSTAT[1]	N/A	SPI Interrupt Status Register.
	SPI2CSTAT[1]	N/A	I^2C Interrupt Status Register.
IRTC (RTC Interval Timer)	TIMECON.7	MIDNIGHT	RTC Midnight Flag.
	TIMECON.2	ALARM	RTC Alarm Flag.
WDT (Watchdog Timer)	WDCON.2	WDS	Watchdog Timeout Flag.

[1] There is no specific flag for ISPI/I2CI; however, all flags for SPI2CSTAT need to be read to assess the reason for the interrupt.

A functional block diagram of the interrupt system is shown in Figure 75. Note that the PSM interrupt is the only interrupt in the highest priority level.

If an external wake-up event occurs to wake the ADE7518 from PSM2, a pending external interrupt is generated. When the EX0 or EX1 bit in the Interrupt Enable SFR (IE, 0xA8) is set to enable external interrupts, the program counter is loaded with the IE0 or IE1 interrupt vector. The IE0 and IE1 interrupt flags in the TCON register are not affected by events that occur when the 8052 MCU core is shut down during PSM2. See the Power Supply Management (PSM) Interrupt section.

The RTC and I^2C/SPI interrupts are latched such that pending interrupts cannot be cleared without entering their respective interrupt service routines. Clearing the RTC midnight flags and alarm flags does not clear a pending RTC interrupt. Similarly, clearing the I^2C/SPI status bits in the SPI Interrupt Status SFR (SPISTAT, 0xEA) does not cancel a pending I^2C/SPI interrupt. These interrupts remain pending until the RTC or I^2C/SPI interrupt vectors are enabled. Their respective interrupt service routines are entered shortly thereafter.

Figure 75 shows how the interrupts are cleared when the interrupt service routines are entered. Some interrupts with multiple interrupt sources are not automatically cleared; specifically, the PSM, ADE, UART, and Timer 2 interrupt vectors. Note that the $\overline{\text{INT0}}$ and $\overline{\text{INT1}}$ interrupts are only cleared if the external interrupt is configured to be triggered by a falling edge by setting IT0 in the Timer/Counter 0 and Timer/Counter 1 Control SFR (TCON, 0x88). If $\overline{\text{INT0}}$ or $\overline{\text{INT1}}$ is configured to interrupt on a low level, the interrupt service routine is re-entered until the respective pin goes high.

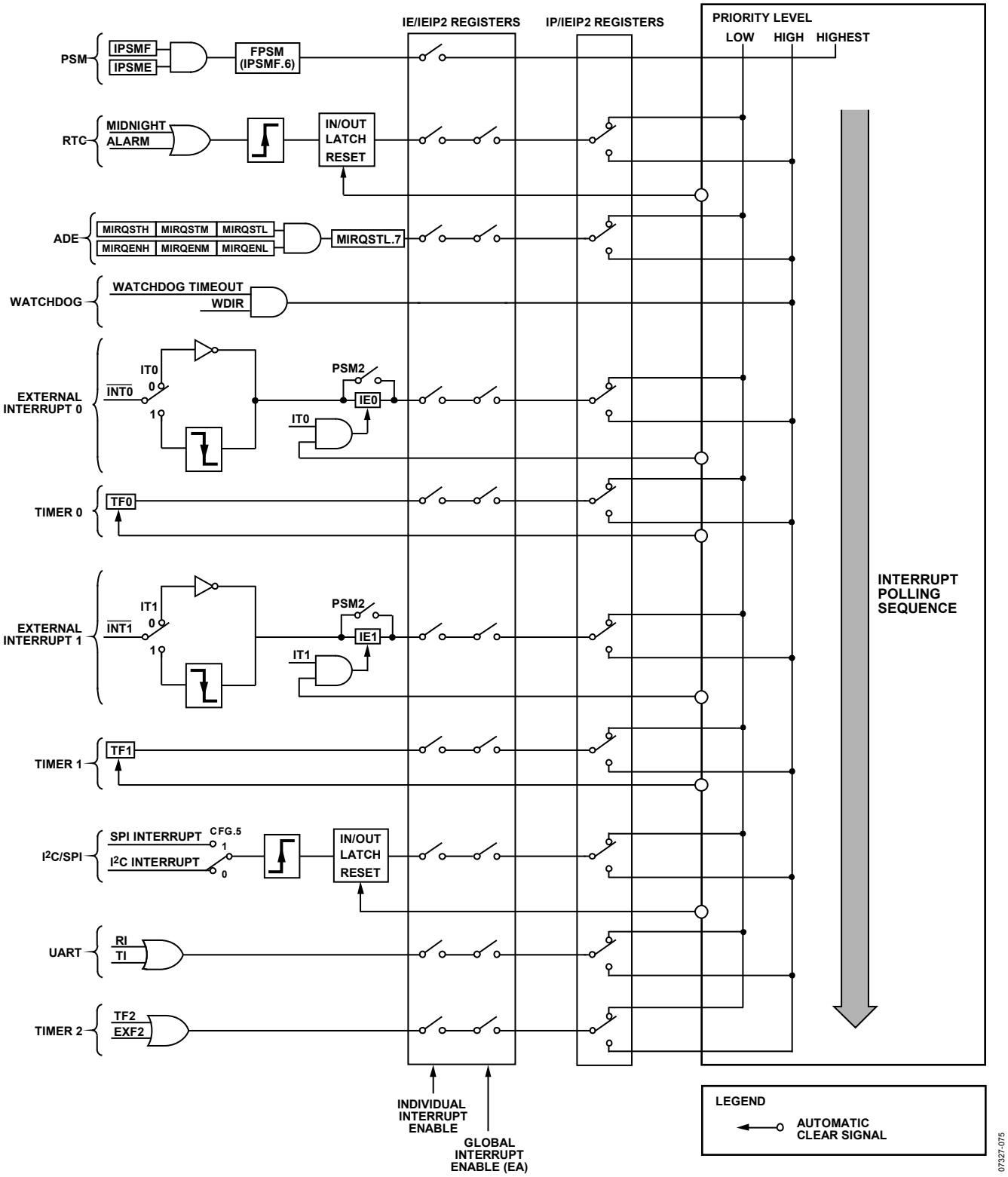


Figure 75. Interrupt System Functional Block Diagram

INTERRUPT VECTORS

When an interrupt occurs, the program counter is pushed onto the stack, and the corresponding interrupt vector address is loaded into the program counter. When the interrupt service routine is complete, the program counter is popped off the stack by a RETI instruction. This allows program execution to resume from where it was interrupted. The interrupt vector addresses are shown in Table 64.

Table 64. Interrupt Vector Addresses

Source	Vector Address
IE0	0x0003
TF0	0x000B
IE1	0x0013
TF1	0x001B
RI + TI	0x0023
TF2 + EXF2	0x002B
Reserved	0x0033
ISPI/I2CI	0x003B
IPSM (Power Supply)	0x0043
IADE (Energy Measurement DSP)	0x004B
IRTC (RTC Interval Timer)	0x0053
WDT (Watchdog Timer)	0x005B

INTERRUPT LATENCY

The 8052 architecture requires that at least one instruction executes between interrupts. To ensure this, the 8052 MCU core hardware prevents the program counter from jumping to an ISR immediately after completing an RETI instruction or an access of the IP and IE registers.

The shortest interrupt latency is 3.25 instruction cycles, 800 ns with a clock of 4.096 MHz. The longest interrupt latency for a high priority interrupt results when a pending interrupt is generated during a low priority interrupt RETI, followed by a multiply instruction. This results in a maximum interrupt latency of 16.25 instruction cycles, 4 μs with a clock of 4.096 MHz.

CONTEXT SAVING

When the 8052 vectors to an interrupt, only the program counter is saved on the stack. Therefore, the interrupt service routine must be written to ensure that registers used in the main program are restored to their preinterrupt state. Common registers that can be modified in the ISR are the accumulator register and the PSW register. Any general-purpose registers that are used as scratch pads in the ISR should also be restored before exiting the interrupt. The following example 8052 code shows how to restore some commonly used registers:

```
GeneralISR:
; save the current accumulator value
       PUSH   ACC
; save the current status and register bank
selection
       PUSH   PSW

; service interrupt
…

; restore the status and register bank
selection
       POP    PSW
; restore the accumulator
       POP    ACC
       RETI
```

WATCHDOG TIMER

The watchdog timer generates a device reset or interrupt within a reasonable amount of time if the ADE7518 enters an erroneous state, possibly due to a programming error or electrical noise. The watchdog is enabled by default with a timeout of two seconds and creates a system reset if not cleared within two seconds. The watchdog function can be disabled by clearing the watchdog enable bit (WDE) in the Watchdog Timer SFR (WDCON, 0xC0).

The watchdog circuit generates a system reset or interrupt (WDS) if the user program fails to set the WDE bit within a predetermined amount of time (set by PRE[3:0]). The watchdog timer is clocked from the 32.768 kHz external crystal connected between the XTAL1 and XTAL2 pins.

The WDCON SFR can be written only by user software if the double write sequence described in the Writing to the Watchdog Timer SFR (WDCON, 0xC0) section is initiated on every write access to the WDCON SFR.

To prevent any code from inadvertently disabling the watchdog, a watchdog protection can be activated. This watchdog protection locks in the watchdog enable and event settings so that they cannot be changed by user code. The protection is activated by clearing a watchdog protection bit in the flash memory. The watchdog protection bit is the most significant bit at Address 0x3FFA of the flash memory. When this bit is cleared, the WDIR bit is forced to 0, and the WDE bit is forced to 1. Note that the sequence for configuring the flash protection bits must be followed to modify the watchdog protection bit at Address 0x3FFA (see the Protecting the Flash Memory section).

Table 65. Watchdog Timer SFR (WDCON, 0xC0)

Bit	Address	Mnemonic	Default	Description
7 to 4	0xC7 to 0xC4	PRE[3:0]	7	Watchdog Prescaler. In normal mode, the 16-bit watchdog timer is clocked by the input clock (32.768 kHz). The PREx bits set which of the upper bits of the counter are used as the watchdog output, as follows: $t_{WATCHDOG} = 2^{PRE} \times \frac{2^9}{XTAL1}$
				PRE[3:0] / **Result (Watchdog Timeout)**
				0000 / 15.6 ms
				0001 / 31.2 ms
				0010 / 62.5 ms
				0011 / 125 ms
				0100 / 250 ms
				0101 / 500 ms
				0110 / 1 sec
				0111 / 2 sec
				1000 / 0 sec, automatic reset
				1001 / 0 sec, serial download reset
				1010 to 1111 / Not a valid selection
3	0xC3	WDIR	0	Watchdog Interrupt Response Bit. When cleared, the watchdog generates a system reset when the watchdog timeout period has expired. When set, the watchdog generates an interrupt when the watchdog timeout period has expired.
2	0xC2	WDS	0	Watchdog Status Bit. This bit is set to indicate that a watchdog timeout has occurred. It is cleared by writing a 0 or by an external hardware reset. A watchdog reset does not clear WDS; therefore, it can be used to distinguish between a watchdog reset and a hardware reset from the $\overline{\text{RESET}}$ pin.
1	0xC1	WDE	1	Watchdog Enable Bit. When set, this bit enables the watchdog and clears its counter. The watchdog counter is subsequently cleared again whenever WDE is set. If the watchdog is not cleared within its selected timeout period, it generates a system reset or watchdog interrupt, depending on the WDIR bit.
0	0xC0	WDWR	0	Watchdog Write Enable Bit. See the Writing to the Watchdog Timer SFR (WDCON, 0xC0) section.

Table 66. Watchdog and Flash Protection Byte in Flash (Flash Address = 0x3FFA)

Bit	Mnemonic	Default	Description
7	WDPROT_PROTKY7	1	This bit holds the protection for the watchdog timer and the seventh bit of the flash protection key. When this bit is cleared, the watchdog enable (WDE) and interrupt response bits (WDIR) cannot be changed by user code. The watchdog configuration is then fixed to WDIR = 0 and WDE = 1. The watchdog timeout in PRE[3:0] can still be modified by user code. The value of this bit is also used to set the flash protection key. If this bit is cleared to protect the watchdog, then the default value for the flash protection key is 0x7F instead of 0xFF (see the Protecting the Flash Memory section for more information on how to clear this bit).
6 to 0	PROTKY[6:0]	0xFF	These bits hold the flash protection key. The content of this flash address is compared to the Flash Protection Key SFR (PROTKY, 0xBB) when the protection is being set or changed. If the two values match, the new protection is written to Flash Address 0x3FFF to Flash Address 0x3FFB. See the Protecting the Flash Memory section for more information on how to configure these bits.

Writing to the Watchdog Timer SFR (WDCON, 0xC0)

Writing data to the WDCON SFR involves a double instruction sequence. The WDWR bit must be set and the following instruction must be a write instruction to the WDCON SFR.

```
Disable Watch dog
CLR EA
SETB WDWR
CLR WDE
SETB EA
```

This sequence is necessary to protect the WDCON SFR from code execution upsets that may unintentionally modify this SFR. Interrupts should be disabled during this operation due to the consecutive instruction cycles.

Watchdog Timer Interrupt

If the watchdog timer is not cleared within the watchdog timeout period, a system reset occurs unless the watchdog timer interrupt is enabled. The watchdog timer interrupt enable bit (WDIR) is located in the Watchdog Timer SFR (WDCON, 0xC0). Enabling the WDIR bit allows the program to examine the stack or other variables that may have led the program to execute inappropriate code. The watchdog timer interrupt also allows the watchdog to be used as a long interval timer.

Note that WDIR is automatically configured as a high priority interrupt. This interrupt cannot be disabled by the EA bit in the IE register (see Table 58). Even if all of the other interrupts are disabled, the watchdog is kept active to watch over the program.

LCD DRIVER

Using shared pins, the LCD module is capable of directly driving an LCD panel of 17 × 4 segments without compromising any ADE7518 functions. It is capable of driving LCDs with 2×, 3×, and 4× multiplexing. The LCD waveform voltages are generated through an external resistor ladder.

Each ADE7518 has an embedded LCD control circuit, driver, and power supply circuit. The LCD module is functional in all operating modes (see the Operating Modes section).

LCD REGISTERS

There are six LCD control registers that configure the driver for the specific type of LCD in the end system and set up the user display preferences. The LCD Configuration SFR (LCDCON, 0x95), the LCD Configuration X SFR (LCDCONX, 0x9C), and the LCD Configuration Y SFR (LCDCONY, 0xB1) contain general LCD driver configuration information, including the LCD enable and reset, as well as the method of LCD voltage generation and multiplex level. The LCD Clock SFR (LCDCLK, 0x96) configures timing settings for LCD frame rate and blink rate. LCD pins are configured for LCD functionality in the LCD Segment Enable SFR (LCDSEGE, 0x97) and the LCD Segment Enable 2 SFR (LCDSEGE2, 0xED).

Table 67. LCD Driver SFRs

SFR Address	Mnemonic	R/W	Description
0x95	LCDCON	R/W	LCD Configuration (see Table 68).
0x96	LCDCLK	R/W	LCD Clock (see Table 71).
0x97	LCDSEGE	R/W	LCD Segment Enable (see Table 74).
0x9C	LCDCONX	R/W	LCD Configuration X (see Table 69).
0xAC	LCDPTR	R/W	LCD Pointer (see Table 75).
0xAE	LCDDAT	R/W	LCD Data (see Table 76).
0xB1	LCDCONY	R/W	LCD Configuration Y (see Table 70).
0xED	LCDSEGE2	R/W	LCD Segment Enable 2 (see Table 77).

Table 68. LCD Configuration SFR (LCDCON, 0x95)

Bit	Mnemonic	Default	Description	
7	LCDEN	0	LCD Enable. If this bit is set, the LCD driver is enabled.	
6	LCDRST	0	LCD Data Registers Reset. If this bit is set, the LCD data registers are reset to zero.	
5	BLINKEN	0	Blink Mode Enable Bit. If this bit is set, blink mode is enabled. The blink mode is configured by the BLKMOD[1:0] and BLKFREQ[1:0] bits in the LCD Clock SFR (LCDCLK, 0x96).	
4	LCDPSM2	0	Forces LCD off when in PSM2 (sleep mode).	
			LCDPSM2	**Result**
			0	The LCD is disabled or enabled in PSM2 by the LCDEN bit.
			1	The LCD is disabled in PSM2 regardless of LCDEN setting.
3	CLKSEL	0	LCD Clock Selection.	
			CLKSEL	**Result**
			0	f_{LCDCLK} = 2048 Hz.
			1	f_{LCDCLK} = 128 Hz.
2	BIAS	0	Bias Mode.	
			BIAS	**Result**
			0	1/2. In this mode, LCDVA is internally connected to LCDVB (see Figure 76).
			1	1/3 (see Figure 77).
1 to 0	LMUX[1:0]	00	LCD Multiplex Level.	
			LMUX[1:0]	**Result**
			00	Reserved.
			01	2× Multiplexing. FP27/COM3 is used as FP27. FP28/COM2 is used as FP28.
			10	3× Mulitplexing. FP27/COM3 is used as FP27. FP28/COM2 is used as COM2.
			11	4× Multiplexing. FP27/COM3 is used as COM3. FP28/COM2 is used as COM2.

Table 69. LCD Configuration X SFR (LCDCONX, 0x9C)

Bit	Mnemonic	Default	Description	
7	Reserved	0	Reserved.	
6	EXTRES	0	External Resistor Ladder Selection Bit.	
			EXTRES	**Result**
			0	External resistor ladder is disabled.
			1	External resistor ladder is enabled.
5 to 0	Reserved	0	These bits should be set to 0 for proper operation.	

Table 70. LCD Configuration Y SFR (LCDCONY, 0xB1)

Bit	Mnemonic	Default	Description
7	Reserved	0	This bit should be kept cleared for proper operation.
6	INV_LVL	0	Frame Inversion Mode Enable Bit. If this bit is set, frames are inverted every other frame. If this bit is cleared, frames are not inverted.
5 to 2	Reserved	0	These bits should be kept cleared for proper operation.
1	UPDATEOVER	0	Update Finished Flag Bit. This bit is updated by the LCD driver. When set, this bit indicates that the LCD memory has been updated and a new frame has begun.
0	REFRESH	0	Refresh LCD Data Memory Bit. This bit should be set by the user. When this bit is set, the LCD driver does not use the data in the LCD data registers to update the display. The LCD data registers can be updated by the 8052. When this bit is cleared, the LCD driver uses the data in the LCD data registers to update the display at the next frame.

Table 71. LCD Clock SFR (LCDCLK, 0x96)

Bit	Mnemonic	Default	Description	
7 to 6	BLKMOD[1:0]	00	Blink Mode Clock Source Configuration Bits.	
			BLKMOD[1:0]	**Result**
			00	The blink rate is controlled by software. The display is off.
			01	The blink rate is controlled by software. The display is on.
			10	The blink rate is 2 Hz.
			11	The blink rate is set by BLKFREQ[1:0].
5 to 4	BLKFREQ[1:0]	00	Blink Rate Configuration Bits. These bits control the LCD blink rate if BLKMOD[1:0] = 11.	
			BLKFREQ[1:0]	**Result (Blink Rate)**
			00	1 Hz
			01	1/2 Hz
			10	1/3 Hz
			11	1/4 Hz
3 to 0	FD[3:0]	0	LCD Frame Rate Selection Bits. See Table 72 and Table 73.	

Table 72. LCD Frame Rate Selection for f_{LCDCLK} = 2048 Hz (LCDCON[3] = 0)

				2× Multiplexing		3× Multiplexing		4× Multiplexing	
FD3	FD2	FD1	FD0	f_{LCD} (Hz)	Frame Rate (Hz)	f_{LCD} (Hz)	Frame Rate (Hz)	f_{LCD} (Hz)	Frame Rate (Hz)
0	0	0	1	256	128[1]	341.3	170.7[1]	512	128[1]
0	0	1	0	170.7	85.3	341.3	113.8[1]	341.3	85.3
0	0	1	1	128	64	256	85.3	256	64
0	1	0	0	102.4	51.2	204.8	68.3	204.8	51.2
0	1	0	1	85.3	42.7	170.7	56.9	170.7	42.7
0	1	1	0	73.1	36.6	146.3	48.8	146.3	36.6
0	1	1	1	64	32	128	42.7	128	32
1	0	0	0	56.9	28.5	113.8	37.9	113.8	28.5
1	0	0	1	51.2	25.6	102.4	34.1	102.4	25.6
1	0	1	0	46.5	23.25	93.1	31	93.1	23.25
1	0	1	1	42.7	21.35	85.3	28.4	85.3	21.35
1	1	0	0	39.4	19.7	78.8	26.3	78.8	19.7
1	1	0	1	36.6	18.3	73.1	24.4	73.1	18.3
1	1	1	0	34.1	17.05	68.3	22.8	68.3	17.05
1	1	1	1	32	16	64	21.3	64	16
0	0	0	0	16	8	32	10.7	32	8

[1] Not within the range of typical LCD frame rates.

Table 73. LCD Frame Rate Selection for f_{LCDCLK} = 128 Hz (LCDCON[3] = 1)

				2× Multiplexing		3× Multiplexing		4× Multiplexing	
FD3	FD2	FD1	FD0	f_{LCD} (Hz)	Frame Rate (Hz)	f_{LCD} (Hz)	Frame Rate (Hz)	f_{LCD} (Hz)	Frame Rate (Hz)
0	0	0	1	32	16[1]	32	10.7	32	8
0	0	1	0	21.3	10.6	32	10.7	32	8
0	0	1	1	16	8	32	10.7	32	8
0	1	0	0	16	8	32	10.7	32	8
0	1	0	1	16	8	32	10.7	32	8
0	1	1	0	16	8	32	10.7	32	8
0	1	1	1	16	8	32	10.7	32	8
1	0	0	0	16	8	32	10.7	32	8
1	0	0	1	16	8	32	10.7	32	8
1	0	1	0	16	8	32	10.7	32	8
1	0	1	1	16	8	32	10.7	32	8
1	1	0	0	16	8	32	10.7	32	8
1	1	0	1	16	8	32	10.7	32	8
1	1	1	0	16	8	32	10.7	32	8
1	1	1	1	128	64	128	42.7	128	32
0	0	0	0	64	32	64	21.3	64	16

[1] Not within the range of typical LCD frame rates.

Table 74. LCD Segment Enable SFR (LCDSEGE, 0x97)

Bit	Mnemonic	Default	Description
7	FP25EN	0	FP25 Function Select Bit. 0 = general-purpose I/O, 1 = LCD function.
6	FP24EN	0	FP24 Function Select Bit. 0 = general-purpose I/O, 1 = LCD function.
5	FP23EN	0	FP23 Function Select Bit. 0 = general-purpose I/O, 1 = LCD function.
4	FP22EN	0	FP22 Function Select Bit. 0 = general-purpose I/O, 1 = LCD function.
3	FP21EN	0	FP21 Function Select Bit. 0 = general-purpose I/O, 1 = LCD function.
2	FP20EN	0	FP20 Function Select Bit. 0 = general-purpose I/O, 1 = LCD function.
1 to 0	Reserved	0	These bits should be left at 0 for proper operation.

Table 75. LCD Pointer SFR (LCDPTR, 0xAC)

Bit	Mnemonic	Default	Description
7	$\overline{R}$/W	0	Read or Write LCD Bit. If this bit = 1, the data in LCDDAT is written to the address indicated by the LCDPTR[5:0] bits.
6	Reserved	0	Reserved.
5 to 0	ADDRESS	0	LCD Memory Address (see Table 78).

Table 76. LCD Data SFR (LCDDAT, 0xAE)

Bit	Mnemonic	Default	Description
7 to 0	LCDDATA	0	Data to be written into or read out of the LCD Memory SFRs.

Table 77. LCD Segment Enable 2 SFR (LCDSEGE2, 0xED)

Bit	Mnemonic	Default	Description
7 to 4	Reserved	0	Reserved.
3	FP19EN	0	FP19 Function Select Bit. 0 = general-purpose I/O, 1 = LCD function.
2	FP18EN	0	FP18 Function Select Bit. 0 = general-purpose I/O, 1 = LCD function.
1	FP17EN	0	FP17 Function Select Bit. 0 = general-purpose I/O, 1 = LCD function.
0	FP16EN	0	FP16 Function Select Bit. 0 = general-purpose I/O, 1 = LCD function.

LCD SETUP

The LCD Configuration SFR (LCDCON, 0x95) configures the LCD module to drive the type of LCD in the user end system. The BIAS and LMUX[1:0] bits in this SFR should be set according to the LCD specifications.

The COM2/FP28 and COM3/FP27 pins default to LCD segment lines. Selecting the 3× multiplex level in the LCD Configuration SFR (LCDCON, 0x95) by setting LMUX[1:0] = 10 changes the FP28 pin functionality to COM2. The 4× multiplex level selection, LMUX[1:0] = 11, changes the FP28 pin functionality to COM2 and the FP27 pin functionality to COM3.

LCD segments FP0 to FP15 and FP26 are enabled by default. Additional pins are selected for LCD functionality in the LCD Segment Enable SFR (LCDSEGE, 0x97) and the LCD Segment Enable 2 SFR (LCDSEGE2, 0xED), where there are individual enable bits for the FP16 to FP25 segment pins. The LCD pins do not have to be enabled sequentially. For example, if the alternate function of FP23, the Timer 2 input, is required, any of the other shared pins, FP16 to FP25, can be enabled instead.

The Display Element Control section contains details about setting up the LCD data memory to turn individual LCD segments on and off. Setting the LCDRST bit in the LCD Configuration SFR (LCDCON, 0x95) resets the LCD data memory to its default (0). A power-on reset also clears the LCD data memory.

LCD TIMING AND WAVEFORMS

An LCD segment acts like a capacitor that is charged and discharged at a certain rate. This rate, the refresh rate, determines the visual characteristics of the LCD. A slow refresh rate results in the LCD blinking on and off between refreshes. A fast refresh rate presents a screen that appears to be continuously lit. In addition, a faster refresh rate consumes more power.

The frame rate, or refresh rate, for the LCD module is derived from the LCD clock, f_{LCDCLK}. The LCD clock is selected as 2048 Hz or 128 Hz by the CLKSEL bit in the LCD Configuration SFR (LCDCON, 0x95). The minimum refresh rate needed for the LCD to appear solid (without blinking) is independent of the multiplex level.

The LCD waveform frequency, f_{LCD}, is the frequency at which the LCD switches the active common line. Thus, the LCD waveform frequency depends heavily on the multiplex level. The frame rate and LCD waveform frequency are set by the f_{LCDCLK}, the multiplex level, and the FD[3:0] frame rate selection bits in the LCD Clock SFR (LCDCLK, 0x96).

The LCD module provides 16 different frame rates for f_{LCDCLK} = 2048 Hz, ranging from 8 Hz to 128 Hz for an LCD with 4× multiplexing. Fewer options are available with f_{LCDCLK} = 128 Hz, ranging from 8 Hz to 32 Hz for a 4× multiplexed LCD. The 128 Hz clock is beneficial for battery operation because it consumes less power than the 2048 Hz clock. The frame rate is set by the FD[3:0] bits in the LCD Clock SFR (LCDCLK, 0x96); see Table 72 and Table 73.

The LCD waveform is inverted at twice the LCD waveform frequency, f_{LCD}. This way, each frame has an average dc offset of zero. ADC offset degrades the lifetime and performance of the LCD.

BLINK MODE

Blink mode is enabled by setting the BLINKEN bit in the LCD Configuration SFR (LCDCON, 0x95). This mode is used to alternate between the LCD on state and LCD off state so that the LCD screen appears to blink. There are two blinking modes: a software controlled blink mode and an automatic blink mode.

Software Controlled Blink Mode

The LCD blink rate can be controlled by user code with the BLKMOD[1:0] bits in the LCD Clock SFR (LCDCLK, 0x96) by toggling the bits to turn the display on and off at a rate determined by the MCU code.

Automatic Blink Mode

There are five blink rates available. These blink rates are selected by the BLKMOD[1:0] and BLKFREQ[1:0] bits in the LCD Clock SFR (LCDCLK, 0x96); see Table 71.

DISPLAY ELEMENT CONTROL

A bank of 15 bytes of data memory located in the LCD module controls the on or off state of each LCD segment. The LCD data memory is stored in Address 0 through Address 14 in the LCD module. Each byte configures the on and off states of two segment lines. The LSBs store the state of the even numbered segment lines, and the MSBs store the state of the odd numbered segment lines. For example, LCD Memory Address 0 refers to segment lines one and zero (see Table 78). Note that the LCD data memory is maintained in PSM2 operating mode.

The LCD data memory is accessed indirectly through the LCD Pointer SFR (LCDPTR, 0xAC) and LCD Data SFR (LCDDAT, 0xAE). Moving a value to the LCDPTR SFR selects the LCD data byte to be accessed and initiates a read or write operation (see Table 75).

Writing to LCD Data Registers

To update the LCD data memory, first set the LSB of the LCD Configuration Y SFR (LCDCONY, 0xB1) to freeze the data being displayed on the LCD while updating it. Then, move the data to the LCD Data SFR (LCDDAT, 0xAE) prior to accessing the LCD Pointer SFR (LCDPTR, 0xAC). When the MSB of the LCDPTR SFR is set, the content of the LCDDAT SFR is transferred to the internal LCD data memory designated by the address in the LCDPTR SFR. Clear the LSB of the LCD Configuration Y SFR (LCDCONY, 0xB1) when all of the data memory has been updated to allow the use of the new LCD setup for display.

To update the segments attached to the FP10 and FP11 pins, use the following sample 8052 code:

```
ORL    LCDCONY,#01h ;start updating the data
MOV    LCDDAT,#FFh
MOV    LCDPTR,#80h OR 05h
ANL    LCDCONY,#0FEh ;update finished
```

Reading LCD Data Registers

When the MSB of the LCD Pointer SFR (LCDPTR, 0xAC) is cleared, the content of the LCD data memory address designated by LCDPTR is transferred to the LCD Data SFR (LCDDAT, 0xAE).

Sample 8052 code to read the contents of LCD Data Memory Address 0x07, which holds the on and off state of the segments attached to FP14 and FP15, is as follows:

```
MOV    LCDPTR,#07h
MOV    R1, LCDDAT
```

Table 78. LCD Data Memory Accessed Indirectly Through LCD Pointer SFR (LCDPTR, 0xAC) and LCD Data SFR (LCDDAT, 0xAE)[1,2]

	LCD Pointer SFR (LCDPTR, 0xAC)				LCD Pointer SFR (LCDDAT, 0xAE)			
LCD Memory Address	**COM3**	**COM2**	**COM1**	**COM0**	**COM3**	**COM2**	**COM1**	**COM0**
0x0E					FP28	FP28	FP28	FP28
0x0D	FP27	FP27	FP27	FP27	FP26	FP26	FP26	FP26
0x0C	FP25	FP25	FP25	FP25	FP24	FP24	FP24	FP24
0x0B	FP23	FP23	FP23	FP23	FP22	FP22	FP22	FP22
0x0A	FP21	FP21	FP21	FP21	FP20	FP20	FP20	FP20
0x09	FP19	FP19	FP19	FP19	FP18	FP18	FP18	FP18
0x08	FP17	FP17	FP17	FP17	FP16	FP16	FP16	FP16
0x07	FP15	FP15	FP15	FP15	FP14	FP14	FP14	FP14
0x06	FP13	FP13	FP13	FP13	FP12	FP12	FP12	FP12
0x05	FP11	FP11	FP11	FP11	FP10	FP10	FP10	FP10
0x04	FP9	FP9	FP9	FP9	FP8	FP8	FP8	FP8
0x03	FP7	FP7	FP7	FP7	FP6	FP6	FP6	FP6
0x02	FP5	FP5	FP5	FP5	FP4	FP4	FP4	FP4
0x01	FP3	FP3	FP3	FP3	FP2	FP2	FP2	FP2
0x00	FP1	FP1	FP1	FP1	FP0	FP0	FP0	FP0

[1] COMx designates the common lines.
[2] FPx designates the segment lines.

LCD EXTERNAL CIRCUITRY

The voltage generation selection is made by setting Bit EXTRES in the LCD Configuration X SFR (LCDCONX, 0x9C). This bit is cleared by default and needs to be set to enable an external resistor ladder.

External Resistor Ladder

To enable the external resistor ladder, set the EXTRES bit in the LCD Configuration X SFR (LCDCONX, 0x9C). When EXTRES = 1, the LCD waveform voltages are supplied by the external resistor ladder. Because the LCD voltages are not generated on chip, the LCD bias compensation implemented to maintain contrast over temperature and supply is not possible.

The external circuitry needed for the resistor ladder option is shown in Figure 77. The resistors required should be in the range of 10 kΩ to 100 kΩ and based on the current required by the LCD being used.

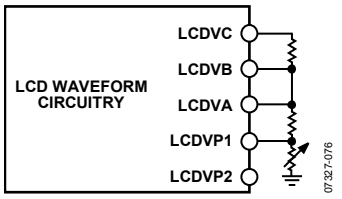


Figure 76. External Circuitry for External Resistor Ladder Option 1/2 Bias Configuration

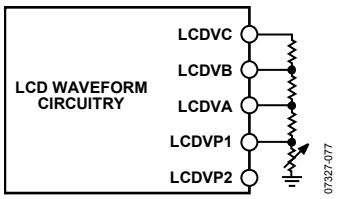


Figure 77. External Circuitry for External Resistor Ladder Option1/3 Bias Configuration

LCD FUNCTION IN PSM2

The LCDPSM2 and LCDEN bits in the LCD Configuration SFR (LCDCON, 0x95) control LCD functionality in PSM2 operating mode (see Table 79).

Table 79. Bits Controlling LCD Functionality in PSM2 Mode

LCDPSM2	LCDEN	Result
0	0	The display is off in PSM2.
0	1	The display is on in PSM2.
1	X	The display is off in PSM2.

In addition, note that the LCD configuration and data memory is retained when the display is turned off.

Example LCD Setup

An example of how to set up the LCD peripheral for a specific LCD is described in this section with the following parameters:

- Type of LCD: 4× multiplexed with 1/3 bias, 96 segments
- Refresh rate: 64 Hz

A 96-segment LCD with 4× multiplexing requires 96/4 = 24 segment lines. Sixteen pins, FP0 to FP15, are automatically dedicated for use as LCD segments. Eight more pins must be chosen for the LCD function. Because the LCD has 4× multiplexing, all four common lines are used. As a result, COM2/FP28 and COM3/FP27 cannot be used as segment lines. Based on the alternate functions of the pins used for FP16 through FP25, FP16 to FP23 are chosen for the eight remaining segment lines. These pins are enabled for LCD functionality in the LCD Segment Enable SFR (LCDSEGE, 0x97) and LCD Segment Enable 2 SFR (LCDSEGE2, 0xED).

The LCD is set up with the following 8052 code:

```
; setup LCD pins to have LCD functionality
MOV    LCDSEG,#FP20EN+FP21EN+FP22EN+FP23EN
MOV    LCDSEGX,#FP16EN+FP17EN+FP18EN+FP19EN


; set up LCDCON for f_LCDCLK = 2048 Hz, 1/3
bias and 4× multiplexing
MOV    LCDCON,#BIAS+LMUX1+LMUX0
; set up LCDCONX for resistor ladder
MOV    LCDCONX,#40h
; set up refresh rate for 64 Hz with f_LCDCLK =
2048 Hz
MOV    LCDCLK,#FD3+FD2+FD1+FD0
; set up LCD data registers with data to be
displayed using
; LCDPTR and LCDDATA registers
; turn all segments on FP27 on and FP26 off
ORL    LCDCONY,#01h ; start data memory
refresh
MOV    LCDDAT,#F0H
MOV         LCDPTR, #80h OR 0DH
ANL    LCDCONY,#0FEh ; end of data memory
refresh
ORL    LCDCON,#LCDEN ; enable LCD
```

To set up the same 3.3 V LCD for use with an external resistor ladder,

```
; set up LCDCONX for external resistor
ladder
MOV    LCDCONX,#EXTRES
```

FLASH MEMORY

OVERVIEW

Flash memory is a type of nonvolatile memory that is in-circuit programmable. The default state of a byte of flash memory is 0xFF (erased). When a byte of flash memory is programmed, the required bits change from 1 to 0. The flash memory must be erased to turn the 0s back to 1s. However, a byte of flash memory cannot be erased individually. The entire segment, or page, of flash memory that contains the byte must be erased.

The ADE7518 provides 16 kB of flash program/information memory. This memory is segmented into 32 pages of 512 bytes each. Therefore, to reprogram one byte of flash memory, the other 511 bytes in that page must be erased. The flash memory can be erased by page or all at once in a mass erase. There is a command to verify that a flash write operation has completed successfully. The ADE7518 flash memory controller also offers configurable flash memory protection.

The 16 kB of flash memory are provided on-chip to facilitate code execution without any external discrete ROM device requirements. The program memory can be programmed in-circuit, using the serial download or emulation options provided or using conventional third party memory programmers.

Flash/EE Memory Reliability

The flash memory arrays on the ADE7518 are fully qualified for two key Flash/EE memory characteristics: Flash/EE memory cycling endurance and Flash/EE memory data retention.

Endurance quantifies the ability of the Flash/EE memory to be cycled through many program, read, and erase cycles. In real terms, a single endurance cycle is composed of the following four independent, sequential events:

1. Initial page erase sequence.
2. Read/verify sequence.
3. Byte program sequence.
4. Second read/verify sequence.

In reliability qualification, every byte in both the program and data Flash/EE memory is cycled from 0x00 to 0xFF until a first fail is recorded, signifying the endurance limit of the on-chip Flash/EE memory.

As indicated in the Specifications section, the ADE7518 flash memory endurance qualification has been carried out in accordance with JEDEC Standard 22 Method A117 over the industrial temperature range of −40°C, +25°C, and +85°C. The results allow the specification of a minimum endurance figure over supply and temperature of 100,000 cycles, with a minimum endurance figure of 20,000 cycles of operation at 25°C.

Retention is the ability of the flash memory to retain its programmed data over time. Again, the parts have been qualified in accordance with the formal JEDEC Standard 22 Method A117 at a specific junction temperature (TJ = 55°C). As part of this qualification procedure, the flash memory is cycled to its specified endurance limit before data retention is characterized. This means that the flash memory is guaranteed to retain its data for its full specified retention lifetime every time the flash memory is reprogrammed. It should also be noted that retention lifetime, based on an activation energy of 0.6 eV, derates with T_J, as shown in Figure 78.

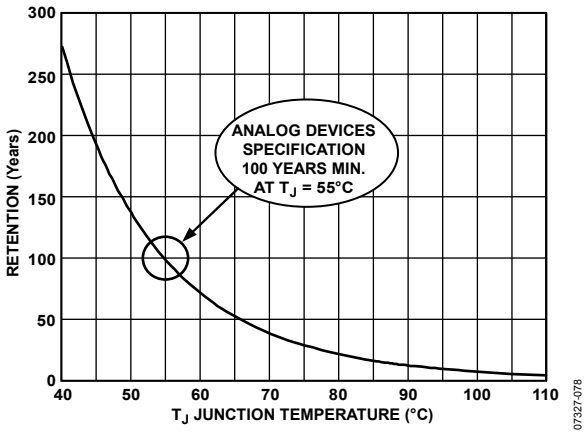


Figure 78. Flash/EE Memory Data Retention

FLASH MEMORY ORGANIZATION

The 16 kB of flash memory provided by the ADE7518 are segmented into 32 pages of 512 bytes each. It is up to the user to decide which flash memory to allocate for data memory. It is recommended that each page be dedicated solely to program memory or to data memory. Doing so prevents the program counter from being loaded with data memory instead of an operations code from the program memory. It also prevents program memory used to update a byte of data memory from being erased.

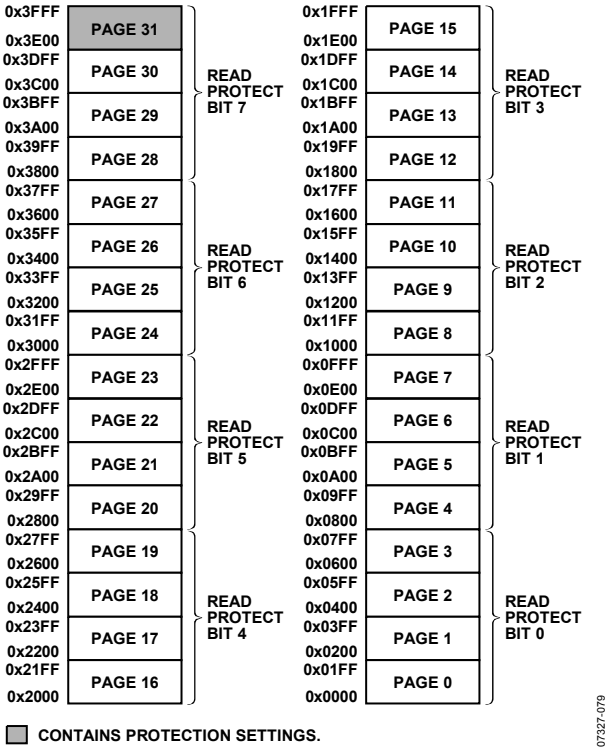


Figure 79. Flash Memory Organization

The flash memory can be protected from read or write/erase (W/E) access. The protection is implemented in part of the last page of the flash memory, Page 31. Four of the bytes from this page are used to set up write/erase protection for each page. Another byte is used for configuring read protection of the flash memory. The read protection is selected for groups of four pages. Finally, one byte is used to store the key required for modifying the protection scheme. The last page of flash memory must be write/erase protected for any flash protection to be active.

The implication of write/erase protecting the last page is that the content of the 506 bytes in this page that are available to the user must not change.

Thus, if code protection is enabled, it is recommended to use this last page for program memory only (if the firmware does not need to be updated in the field). If the firmware must be protected and can be updated at a future date, the last page should be used only for constants utilized by the program code.

Therefore, Page 0 through Page 30 are for general program and data memory use. It is recommended that Page 31 be used for constants or code that do not need to be updated. Note that the last six bytes of Page 31 are reserved for protecting the flash memory.

USING THE FLASH MEMORY

The 16 kB of flash memory are configured as 32 pages, each of 512 bytes. As with the other ADE7518 peripherals, the interface to this memory space is via a group of registers mapped in the SFR space (see Table 80).

A data register, EDATA, holds the byte of data to be accessed. The byte of flash memory is addressed via the EADRH and EADRL registers. Finally, ECON is an 8-bit control register that can be written to with one of seven flash memory access commands to trigger various read, write, erase, and verify functions.

Table 80. The Flash SFRs

SFR	Address	Default	Bit Addressable	Description
ECON	0xB9	0x00	No	Flash Control
FLSHKY	0xBA	0xFF	No	Flash Key
PROTKY	0xBB	0xFF	No	Flash Protection Key
EDATA	0xBC	0x00	No	Flash Data
PROTB0	0xBD	0xFF	No	Flash W/E Protection 0
PROTB1	0xBE	0xFF	No	Flash W/E Protection 1
PROTR	0xBF	0xFF	No	Flash Read Protection
EADRL	0xC6	0x00	No	Flash Low Byte Address
EADRH	0xC7	0x00	No	Flash High Byte Address

Figure 80 demonstrates the steps required for access to the flash memory.

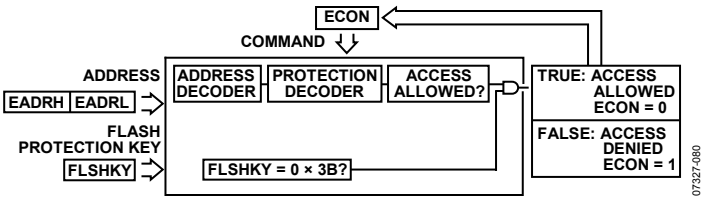


Figure 80. Flash Memory Read/Write/Erase Protection Block Diagram

ECON—Flash/EE Memory Control SFR

Programming flash memory is done through the Flash Control SFR (ECON, 0xB9). This SFR allows the user to read, write, erase, or verify the 16 kB of flash memory. As a method of security, a key must be written to the FLSHKY register to initiate any user access to the flash memory. Upon completion of the flash memory operation, the FLSHKY register is reset so that it must be written to prior to another flash memory operation. Requiring the key to be set before an access to the flash memory decreases the likelihood of user code or data being overwritten by a program inappropriately modified during its execution.

The program counter (PC) is held on the instruction where the ECON register is written to until the flash memory controller is done performing the requested operation. Then, the PC increments to continue with the next instruction.

Any interrupt requests that occur while the flash controller is performing an operation are not handled until the flash operation is complete. All peripherals, such as timers and counters, continue to operate as configured throughout the flash memory access.

Table 81. Flash Control SFR (ECON, 0xB9)

Bit	Mnemonic	Value	Description
7 to 0	ECON	1	Write Byte. The value in EDATA is written to the flash memory at the page address given by EADRH and EADRL. Note that the byte being addressed must be pre-erased.
		2	Erase Page. A 512-byte page of flash memory address is erased. The page is selected by the address in EADRH/EADRL. Any address in the page can be written to EADRH/EADRL to select it for erasure.
		3	Erase All. All 16 kB of the flash memory are erased. Note that this command is used during serial and parallel download modes but should not be executed by user code.
		4	Read Byte. The byte in the flash memory addressed by EADRH/EADRL is read into EDATA.
		5	Erase Page and Write Byte. The page that holds the byte addressed by EADRH/EADRL is erased. Data in EDATA is then written to the byte of flash memory addressed by EADRH/EADRL.
		8	Protect Code (see the Protecting the Flash Memory section).

Table 82. Flash Key SFR (FLSHKY, 0xBA)

Bit	Mnemonic	Default	Description
7 to 0	FLSHKY	0xFF	The content of this SFR is compared to the flash key, 0x3B. If the two values match, the next ECON operation is allowed (see the Protecting the Flash Memory section).

Table 83. Flash Protection Key SFR (PROTKY, 0xBB)

Bit	Mnemonic	Default	Description
7 to 0	PROTKY	0xFF	The content of this SFR is compared to the flash memory location at Address 0x3FFA. If the two values match, the update of the write/erase and read protection setup is allowed (see the Protecting the Flash Memory section). If the protection key in the flash is 0xFF, the PROTKY SFR value is not used for comparison. This SFR is also used to write the protection key in the flash. This is done by writing the desired value in PROTKY and by writing 0x08 in the ECON SFR. This operation can only be done once.

Table 84. Flash Data SFR (EDATA, 0xBC)

Bit	Mnemonic	Default	Description
7 to 0	EDATA	0	Flash Pointer Data.

Table 85. Flash Write/Erase Protection 0 SFR (PROTB0, 0xBD)

Bit	Mnemonic	Default	Description							
7 to 0	PROTB0	0xFF	This SFR is used to write the write/erase protection bits for Page 0 to Page 7 of the flash memory (see the Protecting the Flash Memory section). Clearing the bits enables the protection.							
			PROTB0.7	**PROTB0.6**	**PROTB0.5**	**PROTB0.4**	**PROTB0.3**	**PROTB0.2**	**PROTB0.1**	**PROTB0.0**
			Page 7	Page 6	Page 5	Page 4	Page 3	Page 2	Page 1	Page 0

Table 86. Flash Write/Erase Protection 1 SFR (PROTB1, 0xBE)

Bit	Mnemonic	Default	Description							
7 to 0	PROTB1	0xFF	This SFR is used to write the write/erase protection bits for Page 8 to Page15 of the flash memory (see the Protecting the Flash Memory section). Clearing the bits enables the protection.							
			PROTB1.7	**PROTB1.6**	**PROTB1.5**	**PROTB1.4**	**PROTB1.3**	**PROTB1.2**	**PROTB1.1**	**PROTB1.0**
			Page 15	Page 14	Page 13	Page 12	Page 11	Page 10	Page 9	Page 8

Table 87. Flash Read Protection SFR (PROTR, 0xBF)

Bit	Mnemonic	Default	Description							
7 to 0	PROTR	0xFF	This SFR is used to write the read protection bits for Page 0 to Page 31 of the flash memory (see the Protecting the Flash Memory section). Clearing the bits enables the protection.							
			PROTR.7	**PROTR.6**	**PROTR.5**	**PROTR.4**	**PROTR.3**	**PROTR.2**	**PROTR.1**	**PROTR.0**
			Page 28 to Page 31	Page 24 to Page 27	Page 20 to Page 23	Page 16 to Page 19	Page 12 to Page 15	Page 8 to Page 11	Page 4 to Page 7	Page 0 to Page 3

Table 88. Flash Low Byte Address SFR (EADRL, 0xC6)

Bit	Mnemonic	Default	Description							
7 to 0	EADRL	0	Flash Pointer Low Byte Address. This SFR is also used to write the write/erase protection bits for Page 16 to Page 23 of the flash memory (see the Protecting the Flash Memory section). Clearing the bits enables the protection.							
			EADRL.7	**EADRL.6**	**EADRL.5**	**EADRL.4**	**EADRL.3**	**EADRL.2**	**EADRL.1**	**EADRL.0**
			Page 23	Page 22	Page 21	Page 20	Page 19	Page 18	Page 17	Page 16

Table 89. Flash High Byte Address SFR (EADRH, 0xC7)

Bit	Mnemonic	Default	Description							
7 to 0	EADRH	0	Flash Pointer High Byte Address. This SFR is also used to write the write/erase protection bits for Page 24 to Page 31 of the flash memory (see the Protecting the Flash Memory section). Clearing the bits enables the protection.							
			EADRH.7	**EADRH.6**	**EADRH.5**	**EADRH.4**	**EADRH.3**	**EADRH.2**	**EADRH.1**	**EADRH.0**
			Page 31	Page 30	Page 29	Page 28	Page 27	Page 26	Page 25	Page 24

Flash Functions

Sample 8052 code is provided in this section to demonstrate how to use the flash functions. For these examples, the byte of Flash Memory 0x3C00 is accessed.

Write Byte

Write 0xF3 into Flash Memory Byte 0x3C00.

```
MOV EDATA,#F3h      ; Data to be written
MOV EADRH,#3Ch      ; Set up byte address
MOV EADRL,#00h
MOV FLSHKY,#3Bh     ; Write flash security
key.
MOV ECON,#01h       ; Write byte
```

Erase Page

Erase the page containing Flash Memory Byte 0x3C00.

```
MOV EADRh,#3Ch      ; Select page through
byte address
MOV EADRL,#00h
MOV FLSHKY,#3Bh     ; Write flash security
key
MOV ECON,#02h       ; Erase Page
```

Erase All

Erase all of the 16 kB flash memory.

```
MOV FLSHKY,#3Bh     ; Write flash security
key
MOV ECON,#03h       ; Erase all
```

Read Byte

Read Flash Memory Byte 0x3C00.

```
MOV EADRH,#3Ch      ; Set up byte address
MOV EADRL,#00h
MOV FLSHKY,#3Bh     ; Write flash security
key
MOV ECON,#04h       ; Read byte
                    ; Data is ready in EDATA
register
```

Erase Page and Write Byte

Erase the page containing Flash Memory Byte 0x3C00 and then write 0xF3 to that address. Note that the other 511 bytes in this page are erased.

```
MOV EDATA,#F3h      ; Data to be written
MOV EADRH,#3Ch      ; Set up byte address
MOV EADRL,#00h
MOV FLSHKY,#3Bh     ; Write flash security
key
MOV ECON,#05h       ; Erase page and then
write byte
```

PROTECTING THE FLASH MEMORY

Two forms of protection are offered for this flash memory: read protection and write/erase protection. The read protection ensures that any pages that are read protected are not able to be read by the end user. The write protection ensures that the flash memory cannot be erased or written over. This protects the end system from tampering and can prevent the code from being overwritten in the event of an unexpected disruption of the normal execution of the program.

Write/erase protection is individually selectable for all 32 pages. Read protection is selected in groups of four pages (see Figure 79 for the groupings). The protection bits are stored in the last flash memory locations, Address 0x3FFA through Address 0x3FFF (see Figure 81); four bytes are reserved for write/erase protection, one byte is for read protection, and another byte sets the protection security key. The user must enable read and write/erase protection for the last page for the entire protection scheme to work.

Note that the read protection does not prevent MOVC commands from being executed within the code.

There is an additional layer of protection offered by a protection security key. The user can set up this security key so that the protection scheme cannot be changed without this key. Once the protection key has been configured, it cannot be modified.

Enabling Flash Protection by Code

The protection bytes in the flash memory can be programmed using the flash controller command and programming ECON to 0x08. In this case, the EADRH, EADRL, PROTB1, and PROTB0 bytes are used to store the data to be written to the 32 bits of write protection. Note that the EADRH and EADRL registers are not used as data pointers here but to store write protection data.

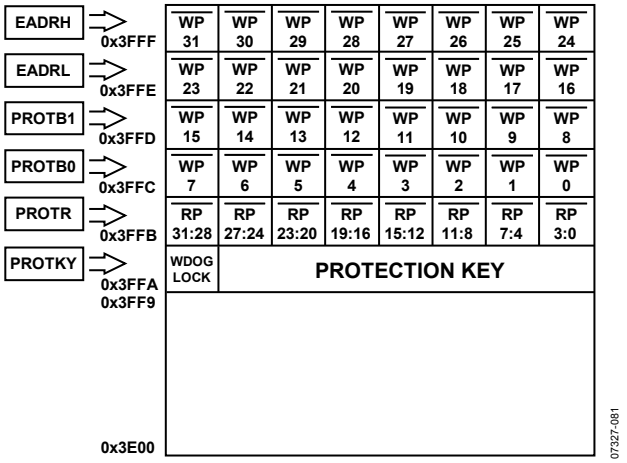


Figure 81. Flash Protection in Page 31

The sequence for writing the protection bits is as follows:

1. Set up the EADRH, EADRL, PROTB1, and PROTB0 registers with the write/erase protection bits. When erased, the protection bits default to 1 (like any other bit of flash memory). The default protection setting is for no protection. To enable protection, write a 0 to the bits corresponding to the pages that should be protected.
2. Set up the PROTR register with the read protection bits. Note that every read protection bit protects four pages. To enable the read protection bit, write a 0 to the bits that should be read protected.
3. To enable the protection key, write to the PROTKY register. If enabled, the protection key is required to modify the protection scheme. The protection key, Flash Memory Address 0x3FFA, defaults to 0xFF; if the PROTKY register is not written to, it remains 0xFF. If the protection key is written to, the PROTKY register must be written with this value every time the protection functionality is accessed. Note that once the protection key is configured, it cannot be modified. Also, note that the most significant bit of Address 0x3FFA is used to enable a lock mechanism for the watchdog settings (see the Watchdog Timer section for more information).
4. Run the protection command by writing 0x08 to the ECON register.
5. Reset the chip to activate the new protection.

To enable read and write/erase protection for the last page only, use the following 8052 code. Writing the flash protection command to the ECON register initiates programming of the protection bits in the flash.

```
; enable read protection on the last four
pages only
MOV PROTR,#07Fh


; set up a protection key of 0A3h. This
command can be
; omitted to use the default protection key
of 0xFF
MOV PROTKY,#0A3h


; write the flash key to the FLSHKY register
to enable flash
; access. The flash access key is not
configurable.
MOV FLSHKY,#3Bh


; write flash protection command to the ECON
register
MOV ECON,#08h
```

Enabling Flash Protection by Emulator Commands

Another way to set the flash protection bytes is to use some reserved emulator commands available only in download mode. These commands write directly to the SFRs and can be used to duplicate the operation mentioned in the Enabling Flash Protection by Code section. When these flash bytes are written, the part can exit emulation mode by a reset and the protections are effective. This method can be used in production and implemented after downloading the program. The commands used for this operation are an extension of the commands listed in Application Note uC004, *Understanding the Serial Download Protocol*, available at www.analog.com.

- Command with ASCII Code I or 0x49 writes the data into R0.
- Command with ASCII Code F or 0x46 writes R0 into the SFR address defined in the data of this command.

By omitting the protocol defined in Application Note uC004, *Understanding the Serial Download Protocol*, the sequence to load protections is similar to the sequence presented in the Enabling Flash Protection by Code section, except that two emulator commands are necessary to replace one assembly command. For example, to write the protection value in EADRH, the two following commands need to be executed:

- Command I with data = value of Protection Byte 0x3FFF.
- Command F with data = 0xC7.

Following this protocol, the protection can be written to the flash using the same sequence as mentioned in the Enabling Flash Protection by Code section. When the part is reset, the protection is effective.

Notes on Flash Protection

The flash protection scheme is disabled by default so that none of the pages of the flash are protected from reading or writing/erasing.

The last page must be read and write/erase protected for the protection scheme to work.

To activate the protection settings, the ADE7518 must be reset after configuring the protection.

After configuring protection on the last page and resetting the part, protections that have been enabled can only be removed by mass erasing the flash memory. The protection bits are read and erase protected by enabling read and write/erase protection on the last page, but the protection bits are never truly write protected.

Protection bits can be modified from 1 to 0, even after the last page has been protected. In this way, more protection can be added but none can be removed.

The protection scheme is intended to protect the end system. Protection should be disabled while developing and emulating code.

Flash Memory Timing

Typical program and erase times for the flash memory are shown in Table 90.

Table 90. Flash Memory Program and Erase Times

Command	Bytes Affected	Flash Memory Timing
Write Byte	1 byte	30 µs
Erase Page	512 bytes	20 ms
Erase All	16 kB	200 ms
Read Byte	1 byte	100 ns
Erase Page and Write Byte	512 bytes	21 ms
Verify Byte	1 byte	100 ns

Note that the core microcontroller operation is idled until the requested flash memory operation is complete. In practice, this means that even though the flash operation is typically initiated with a two-machine-cycle MOV instruction to write to the Flash Control SFR (ECON, 0xB9), the next instruction is not executed until the Flash/EE operation is complete. This means that the core cannot respond to interrupt requests until the Flash/EE operation is complete, although the core peripheral functions, such as counters and timers, continue to count as configured throughout this period.

IN-CIRCUIT PROGRAMMING

Serial Downloading

The ADE7518 facilitates code download via the standard UART serial port. The parts enter serial download mode after a reset or a power cycle if the $\overline{\text{SDEN}}$ pin is pulled low through an external 1 kΩ resistor. When in serial download mode, the hidden embedded download kernel executes. This allows the user to download code to the full 16 kB of flash memory while the device is in-circuit in its target application hardware.

Protection configured in the last page of the ADE7518 affects whether flash memory can be accessed in serial download mode. Read protected pages cannot be read. Write/erase protected pages cannot be written or erased.

TIMERS

The ADE7518 has three 16-bit timer/counters: Timer/Counter 0, Timer/Counter 1, and Timer/Counter 2. The timer/counter hardware is included on chip to relieve the processor core of overhead inherent in implementing timer/counter functionality in software. Each timer/counter consists of two 8-bit registers: THx and TLx (x = 0, 1, or 2). All three timers can be configured to operate as timers or as event counters.

When functioning as a timer, the TLx register is incremented every machine cycle. Thus, users can think of it as counting machine cycles. Because a machine cycle on a single cycle core consists of one core clock period, the maximum count rate is the core clock frequency.

When functioning as a counter, the TLx register is incremented by a 1-to-0 transition at its corresponding external input pin: T0, T1, or T2. When the samples show a high in one cycle and a low in the next cycle, the count is incremented. Because it takes two machine cycles (two core clock periods) to recognize a 1-to-0 transition, the maximum count rate is half the core clock frequency.

There are no restrictions on the duty cycle of the external input signal, but to ensure that a given level is sampled at least once before it changes, it must be held for a minimum of one full machine cycle. User configuration and control of all timer operating modes is achieved via the SFRs listed in Table 91.

Table 91. Timer SFRs

SFR	Address	Bit Addressable	Description
TCON	0x88	Yes	Timer/Counter 0 and Timer/Counter 1 Control (see Table 93).
TMOD	0x89	No	Timer/Counter 0 and Timer/Counter 1 Mode (see Table 92).
TL0	0x8A	No	Timer 0 Low Byte (see Table 96).
TL1	0x8B	No	Timer 1 Low Byte (see Table 98).
TH0	0x8C	No	Timer 0 High Byte (see Table 95).
TH1	0x8D	No	Timer 1 High Byte (see Table 97).
T2CON	0xC8	Yes	Timer/Counter 2 Control (see Table 94).
RCAP2L	0xCA	No	Timer 2 Reload/Capture Low Byte (see Table 102).
RCAP2H	0xCB	No	Timer 2 Reload/Capture High Byte (see Table 101).
TL2	0xCC	No	Timer 2 Low Byte (see Table 100).
TH2	0xCD	No	Timer 2 High Byte (see Table 99).

TIMER REGISTERS

Table 92. Timer/Counter 0 and Timer/Counter 1 Mode SFR (TMOD, 0x89)

Bit	Mnemonic	Default	Description	
7	Gate1	0	Timer 1 Gating Control. Set by software to enable Timer/Counter 1 only when the $\overline{INT1}$ pin is high and the TR1 control is set. Cleared by software to enable Timer 1 whenever the TR1 control bit is set.	
6	C/$\overline{T1}$	0	Timer 1 Timer or Counter Select Bit. Set by software to select counter operation (input from the T1 pin). Cleared by software to select the timer operation (input from the internal system clock).	
5 to 4	T1/M1, T1/M0	00	Timer 1 Mode Select Bits.	
			T1/M[1:0]	**Result**
			00	TH1 operates as an 8-bit timer/counter. TL1 serves as a 5-bit prescaler.
			01	16-Bit Timer/Counter. TH1 and TL1 are cascaded; there is no prescaler.
			10	8-Bit Autoreload Timer/Counter. TH1 holds a value to reload into TL1 each time it overflows.
			11	Timer/Counter 1 stopped.
3	Gate0	0	Timer 0 Gating Control. Set by software to enable Timer/Counter 0 only when the $\overline{INT0}$ pin is high and the TR0 control bit is set. Cleared by software to enable Timer 0 whenever the TR0 control bit is set.	
2	C/$\overline{T0}$	0	Timer 0 Timer or Counter Select Bit. Set by software to the select counter operation (input from the T0 pin). Cleared by software to the select timer operation (input from the internal system clock).	
1 to 0	T0/M1, T0/M0	00	Timer 0 Mode Select Bits.	
			T0/M[1:0]	**Result**
			00	TH0 operates as an 8-bit timer/counter. TL0 serves as a 5-bit prescaler.
			01	16-Bit Timer/Counter. TH0 and TL0 are cascaded; there is no prescaler.
			10	8-Bit Autoreload Timer/Counter. TH0 holds a value to reload into TL0 each time it overflows.
			11	TL0 is an 8-bit timer/counter controlled by the standard Timer 0 control bits. TH0 is an 8-bit timer only, controlled by Timer 1 control bits.

Table 93. Timer/Counter 0 and Timer/Counter 1 Control SFR (TCON, 0x88)

Bit	Address	Mnemonic	Default	Description
7	0x8F	TF1	0	Timer 1 Overflow Flag. Set by hardware on a Timer/Counter 1 overflow. Cleared by hardware when the program counter (PC) vectors to the interrupt service routine.
6	0x8E	TR1	0	Timer 1 Run Control Bit. Set by the user to turn on Timer/Counter 1. Cleared by the user to turn off Timer/Counter 1.
5	0x8D	TF0	0	Timer 0 Overflow Flag. Set by hardware on a Timer/Counter 0 overflow. Cleared by hardware when the PC vectors to the interrupt service routine.
4	0x8C	TR0	0	Timer 0 Run Control Bit. Set by the user to turn on Timer/Counter 0. Cleared by the user to turn off Timer/Counter 0.
3	0x8B	IE1[1]	0	External Interrupt 1 ($\overline{INT1}$) Flag. Set by hardware by a falling edge or by a zero level applied to the external interrupt pin, $\overline{INT1}$, depending on the state of Bit IT1. Cleared by hardware when the PC vectors to the interrupt service routine only if the interrupt was transition activated. If level activated, the external requesting source controls the request flag rather than the on-chip hardware.
2	0x8A	IT1[1]	0	External Interrupt 1 (IE1) Trigger Type. Set by software to specify edge sensitive detection, that is, 1-to-0 transition. Cleared by software to specify level sensitive detection, that is, zero level.
1	0x89	IE0[1]	0	External Interrupt 0 ($\overline{INT0}$) Flag. Set by hardware by a falling edge or by a zero level being applied to the external interrupt pin, $\overline{INT0}$, depending on the state of Bit IT0. Cleared by hardware when the PC vectors to the interrupt service routine only if the interrupt was transition activated. If level activated, the external requesting source controls the request flag rather than the on-chip hardware.
0	0x88	IT0[1]	0	External Interrupt 0 (IE0) Trigger Type. Set by software to specify edge sensitive detection, that is, 1-to-0 transition. Cleared by software to specify level sensitive detection, that is, zero level.

[1] These bits are not used to control Timer/Counter 0 and Timer/Counter 1 but are instead used to control and monitor the external $\overline{INT0}$ and $\overline{INT1}$ interrupt pins.

Table 94. Timer/Counter 2 Control SFR (T2CON, 0xC8)

Bit	Address	Mnemonic	Default	Description
7	0xCF	TF2	0	Timer 2 Overflow Flag. Set by hardware on a Timer 2 overflow. TF2 cannot be set when either RCLK = 1 or TCLK = 1. Cleared by user software.
6	0xCE	EXF2	0	Timer 2 External Flag. Set by hardware when either a capture or reload is caused by a negative transition on T2EX pin and EXEN2 = 1. Cleared by user software.
5	0xCD	RCLK	0	Receive Clock Enable Bit. Set by the user to enable the serial port to use Timer 2 overflow pulses for its receive clock in Serial Port Mode 1 and Serial Port Mode 3. Cleared by the user to enable Timer 1 overflow to be used for the receive clock.
4	0xCC	TCLK	0	Transmit Clock Enable Bit. Set by the user to enable the serial port to use Timer 2 overflow pulses for its transmit clock in Serial Port Mode 1 and Serial Port Mode 3. Cleared by the user to enable Timer 1 overflow to be used for the transmit clock.
3	0xCB	EXEN2	0	Timer 2 External Enable Flag. Set by the user to enable a capture or reload to occur as a result of a negative transition on T2EX if Timer 2 is not being used to clock the serial port. Cleared by the user for Timer 2 to ignore events at T2EX.
2	0xCA	TR2	0	Timer 2 Start/Stop Control Bit. Set by the user to start Timer 2. Cleared by the user to stop Timer 2.
1	0xC9	C/$\overline{T2}$	0	Timer 2 Timer or Counter Function Select Bit. Set by the user to select the counter function (input from external T2 pin). Cleared by the user to select the timer function (input from on-chip core clock).
0	0xC8	CAP2	0	Timer 2 Capture/Reload Select Bit. Set by the user to enable captures on negative transitions at T2EX if EXEN2 = 1. Cleared by the user to enable autoreloads with Timer 2 overflows or negative transitions at T2EX when EXEN2 = 1. When either RCLK = 1 or TCLK = 1, this bit is ignored and the timer is forced to autoreload on Timer 2 overflow.

Table 95. Timer 0 High Byte SFR (TH0, 0x8C)

Bit	Mnemonic	Default	Description
7 to 0	TH0	0	Timer 0 Data High Byte.

Table 96. Timer 0 Low Byte SFR (TL0, 0x8A)

Bit	Mnemonic	Default	Description
7 to 0	TL0	0	Timer 0 Data Low Byte.

Table 97. Timer 1 High Byte SFR (TH1, 0x8D)

Bit	Mnemonic	Default	Description
7 to 0	TH1	0	Timer 1 Data High Byte.

Table 98. Timer 1 Low Byte SFR (TL1, 0x8B)

Bit	Mnemonic	Default	Description
7 to 0	TL1	0	Timer 1 Data Low Byte.

Table 99. Timer 2 High Byte SFR (TH2, 0xCD)

Bit	Mnemonic	Default	Description
7 to 0	TH2	0	Timer 2 Data High Byte.

Table 100. Timer 2 Low Byte SFR (TL2, 0xCC)

Bit	Mnemonic	Default	Description
7 to 0	TL2	0	Timer 2 Data Low Byte.

Table 101. Timer 2 Reload/Capture High Byte SFR (RCAP2H, 0xCB)

Bit	Mnemonic	Default	Description
7 to 0	TH2	0	Timer 2 Reload/ Capture High Byte.

Table 102. Timer 2 Reload/Capture Low Byte SFR (RCAP2L, 0xCA)

Bit	Mnemonic	Default	Description
7 to 0	TL2	0	Timer 2 Reload/ Capture Low Byte.

TIMER 0 AND TIMER 1

Timer/Counter 0 and Timer/Counter 1 Data Registers

Each timer consists of two 8-bit registers. They are Timer 0 High Byte SFR (TH0, 0x8C), Timer 0 Low Byte SFR (TL0, 0x8A), Timer 1 High Byte SFR (TH1, 0x8D), and Timer 1 Low Byte SFR (TL1, 0x8B). These can be used as independent registers or combined into a single 16-bit register, depending on the timer mode configuration (see Table 95 to Table 98).

Timer/Counter 0 and Timer/Counter 1 Operating Modes

This section describes the operating modes for Timer/Counter 0 and Timer/Counter 1. Unless otherwise noted, these modes of operation are the same for both Timer 0 and Timer 1.

Mode 0 (13-Bit Timer/Counter)

Mode 0 configures an 8-bit timer/counter. Figure 82 shows Mode 0 operation. Note that the divide-by-12 prescaler is not present on the single cycle core.

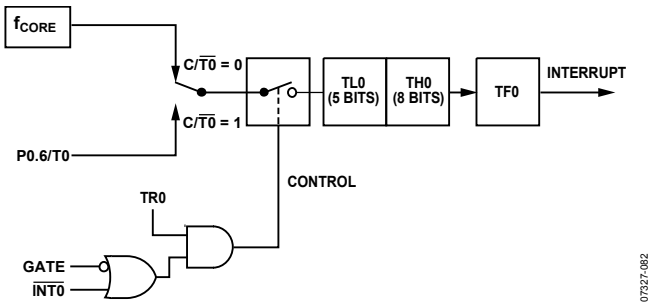


Figure 82. Timer/Counter 0, Mode 0

In this mode, the timer register is configured as a 13-bit register. As the count rolls over from all 1s to all 0s, it sets the timer overflow flag, TF0. TF0 can then be used to request an interrupt. The counted input is enabled to the timer when TR0 = 1 and either Gate0 = 0 or $\overline{INT0}$ = 1. Setting Gate0 = 1 allows the timer to be controlled by external input $\overline{INT0}$ to facilitate pulse width measurements. TR0 is a control bit in the Timer/Counter 0 and Timer/Counter 1 Control SFR (TCON, 0x88); the Gate0/Gate1 bits are in the Timer/Counter 0 and Timer/Counter 1 Mode SFR (TMOD, 0x89). The 13-bit register consists of all eight bits of Timer 0 High Byte SFR (TH0, 0x8C) and the lower five bits of Timer 0 Low Byte SFR (TL0, 0x8A). The upper three bits of the TL0 SFR are indeterminate and should be ignored. Setting the run flag (TR0) does not clear the registers.

Mode 1 (16-Bit Timer/Counter)

Mode 1 is the same as Mode 0 except that the Mode 1 timer register runs with all 16 bits. Mode 1 is shown in Figure 83.

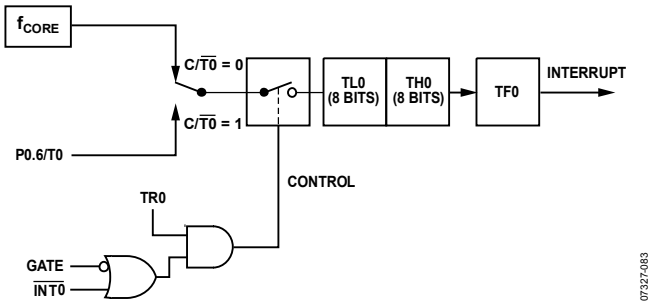


Figure 83. Timer/Counter 0, Mode 1

Mode 2 (8-Bit Timer/Counter with Autoreload)

Mode 2 configures the timer register as an 8-bit counter (TL0) with automatic reload, as shown in Figure 84. Overflow from TL0 not only sets TF0 but also reloads TL0 with the contents of TH0, which is preset by software. The reload leaves TH0 unchanged.

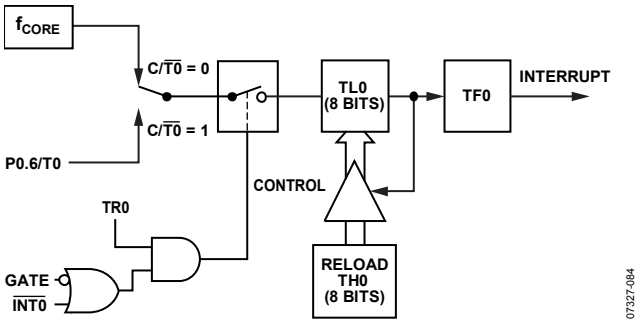


Figure 84. Timer/Counter 0, Mode 2

Mode 3 (Two 8-Bit Timer/Counters)

Mode 3 has different effects on Timer 0 and Timer 1. Timer 1 in Mode 3 simply holds its count. The effect is the same as setting TR1 = 0. Timer 0 in Mode 3 establishes TL0 and TH0 as two separate counters. This configuration is shown in Figure 85. TL0 uses the Timer 0 control bits, C/$\overline{T0}$, Gate0 (see Table 92), TR0, TF0 (see Table 93), and $\overline{INT0}$. TH0 is locked into a timer function (counting machine cycles) and takes over the use of TR1 and TF1 from Timer 1. Therefore, TH0 controls the Timer 1 interrupt. Mode 3 is provided for applications requiring an extra 8-bit timer or counter.

When Timer 0 is in Mode 3, Timer 1 can be turned on and off by switching it out of and into its own Mode 3, or it can be used by the serial interface as a baud rate generator. In fact, Timer 1 can be used in any application not requiring an interrupt from Timer 1 itself.

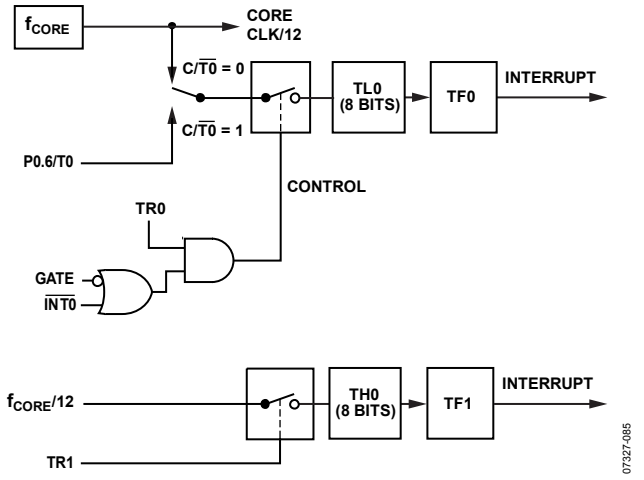


Figure 85. Timer/Counter 0, Mode 3

TIMER 2

Timer/Counter 2 Data Registers

Timer/Counter 2 also has two pairs of 8-bit data registers associated with it: Timer 2 High Byte SFR (TH2, 0xCD), Timer 2 Low Byte SFR (TL2, 0xCC), Timer 2 Reload/Capture High Byte SFR (RCAP2H, 0xCB), and Timer 2 Reload/Capture Low Byte SFR (RCAP2L, 0xCA). These are used as both timer data registers and as timer capture/reload registers (see Table 99 to Table 102).

Timer/Counter 2 Operating Modes

The following sections describe the operating modes for Timer/Counter 2. The operating modes are selected by bits in the Timer/Counter 2 Control SFR (T2CON, 0xC8), as shown in Table 94 and Table 103.

Table 103. T2CON Operating Modes

RCLK or TCLK	CAP2	TR2	Mode
0	0	1	16-bit autoreload
0	1	1	16-bit capture
1	X	1	Baud rate
X	X	0	Off

16-Bit Autoreload Mode

Autoreload mode has two options that are selected by Bit EXEN2 in Timer/Counter 2 Control SFR (T2CON, 0xC8). If EXEN2 = 0 when Timer 2 rolls over, it not only sets TF2 but also causes the Timer 2 registers to be reloaded with the 16-bit value in both the Timer 2 Reload/Capture High Byte SFR (RCAP2H, 0xCB) and Timer 2 Reload/Capture Low Byte SFR (RCAP2L, 0xCA) registers, which are preset by software. If EXEN2 = 1, Timer 2 performs the same events as when EXEN2 = 0 but adds a 1-to-0 transition at the external input T2EX, which triggers the 16-bit reload and sets EXF2. Autoreload mode is shown in Figure 86.

16-Bit Capture Mode

Capture mode has two options that are selected by Bit EXEN2 in Timer/Counter 2 Control SFR (T2CON, 0xC8). If EXEN2 = 0, Timer 2 is a 16-bit timer or counter that, upon overflowing, sets Bit TF2, the Timer 2 overflow bit, which can be used to generate an interrupt. If EXEN2 = 1, Timer 2 performs the same events as when EXEN2 = 0 but adds a l-to-0 transition on external input T2EX, which causes the current value in the Timer 2 registers, TL2 and TH2, to be captured into the RCAP2L and RCAP2H registers, respectively. In addition, the transition at T2EX causes Bit EXF2 in T2CON to be set, and EXF2, like TF2, can generate an interrupt. Capture mode is shown in Figure 87. The baud rate generator mode is selected by RCLK = 1 and/or TCLK = 1.

In either case, if Timer 2 is used to generate the baud rate, the TF2 interrupt flag does not occur. Therefore, Timer 2 interrupts do not occur and do not have to be disabled. In this mode, the EXF2 flag can, however, still cause interrupts that can be used as a third external interrupt. Baud rate generation is described as part of the UART serial port operation in the UART Serial Interface section.

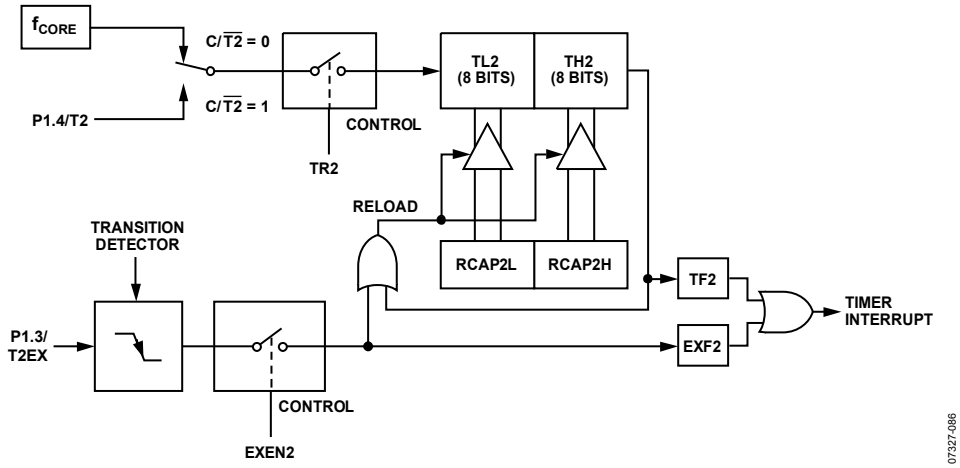


Figure 86. Timer/Counter 2, 16-Bit Autoreload Mode

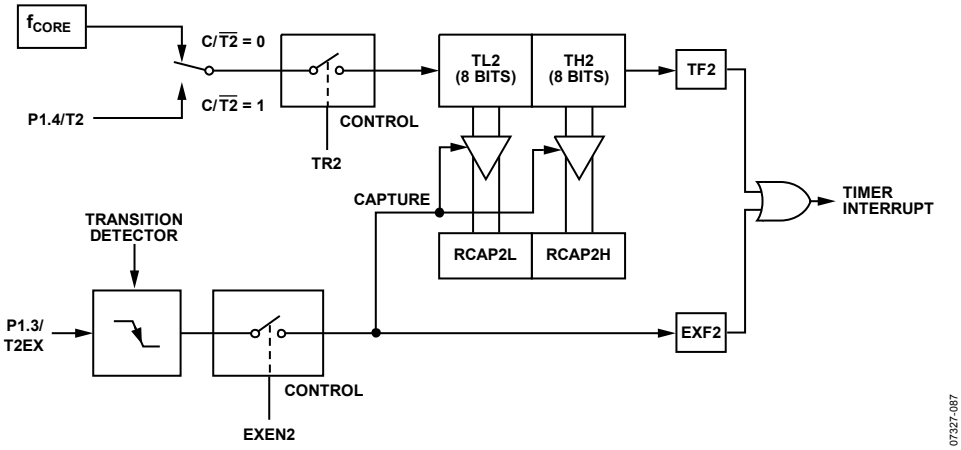


Figure 87. Timer/Counter 2, 16-Bit Capture Mode

PLL

The ADE7518 is intended for use with a 32.768 kHz watch crystal. A PLL locks onto a multiple of this frequency to provide a stable 4.096 MHz clock for the system. The core can operate at this frequency or at binary submultiples of it to allow power savings when maximum core performance is not required. The default core clock is the PLL clock divided by 4, or 1.024 MHz. The ADE energy measurement clock is derived from the PLL clock and is maintained at 4.096 MHz/5 MHz, or 819.2 kHz, across all CD settings.

The PLL is controlled by the CD[2:0] bits in the Power Control SFR (POWCON, 0xC5). To protect erroneous changes to the POWCON SRF, a key is required to modify the register. First, the Key SFR (KYREG, 0xC1) is written with the key, 0xA7, and then a new value is written to the POWCON SFR.

If the PLL loses lock, the MCU is reset and the PLL_FLT bit is set in the Peripheral Configuration SFR (PERIPH, 0xF4). Set the PLLACK bit in the Start ADC Measurement SFR (ADCGO, 0xD8) to acknowledge the PLL fault, clearing the PLL_FLT bit.

PLL REGISTERS

Table 104. Power Control SFR (POWCON, 0xC5)

Bit	Mnemonic	Default	Description	
7	Reserved	1	Reserved.	
6	METER_OFF	0	Set this bit to turn off the modulators and energy metering DSP circuitry to reduce power if metering functions are not needed in PSM0.	
5	Reserved	0	This bit should be kept at 0 for proper operation.	
4	COREOFF	0	Set this bit to shut down the core if in PSM1 operating mode.	
3	Reserved		Reserved.	
2 to 0	CD[2:0]	010	Controls the core clock frequency (f_{CORE}). f_{CORE} = 4.096 MHz/2^{CD}.	
			CD[2:0]	**Result (f_{CORE} in MHz)**
			000	4.096
			001	2.048
			010	1.024
			011	0.512
			100	0.256
			101	0.128
			110	0.064
			111	0.032

Writing to the Power Control SFR (POWCON, 0xC5)

Note that writing data to the POWCON SFR involves writing 0xA7 into the Key SFR (KYREG, 0xC1) followed by a write to the POWCON SFR.

Table 105. Key SFR (KYREG, 0xC1)

Bit	Mnemonic	Default	Description
7 to 0	KYREG	0	Write 0xA7 to the KYREG SFR before writing to the POWCON SFR to unlock it. Write 0xEA to the KYREG SFR before writing to the INTPR, HTHSEC, SEC, MIN, or HOUR timekeeping registers to unlock it.

Table 106. Peripheral Configuration SFR (PERIPH, 0xF4)

Bit	Mnemonic	Default	Description	
7	RXFLAG	0	If this bit is set, indicates that an Rx edge event triggered wake-up from PSM2.	
6	VSWSOURCE	1	Indicates the power supply that is connected internally to V_{SWOUT}. If this bit is set, V_{SWOUT} = V_{DD}. If this bit is cleared, V_{SWOUT} = V_{BAT}.	
5	VDD_OK	1	If this bit is set, indicates that V_{DD} power supply is acceptable for operation.	
4	PLL_FLT	0	If this bit is set, indicates that PLL is not locked.	
3	REF_BAT_EN	0	If this bit is set, the internal voltage reference is enabled in PSM2 mode.	
2	Reserved	0	This bit should be kept to zero.	
1 to 0	RXPROG[1:0]	00	Controls the function of the P1.0/RxD pin.	
			RXPROG[1:0]	**Result**
			00	GPIO
			01	Rx with wake-up disabled
			11	Rx with wake-up enabled

Table 107. Start ADC Measurement SFR (ADCGO, 0xD8)

Bit	Address	Mnemonic	Default	Description
7	0xDF	PLL_FTL_ACK	0	Set this bit to clear the PLL fault bit, PLL_FLT in the PERIPH register. A PLL fault is generated if a reset was caused because the PLL lost lock.
6 to 0	0xDE to 0xD8	Reserved	0	Reserved.

REAL-TIME CLOCK

The ADE7518 has an embedded real-time clock (RTC), as shown in Figure 88. The external 32.768 kHz crystal is used as the clock source for the RTC. Calibration is provided to compensate the nominal crystal frequency and for variations in the external crystal frequency over temperature. By default, the RTC is maintained active in all power saving modes. The RTC counters retain their values through watchdog resets and external resets. They are only reset during a power-on reset.

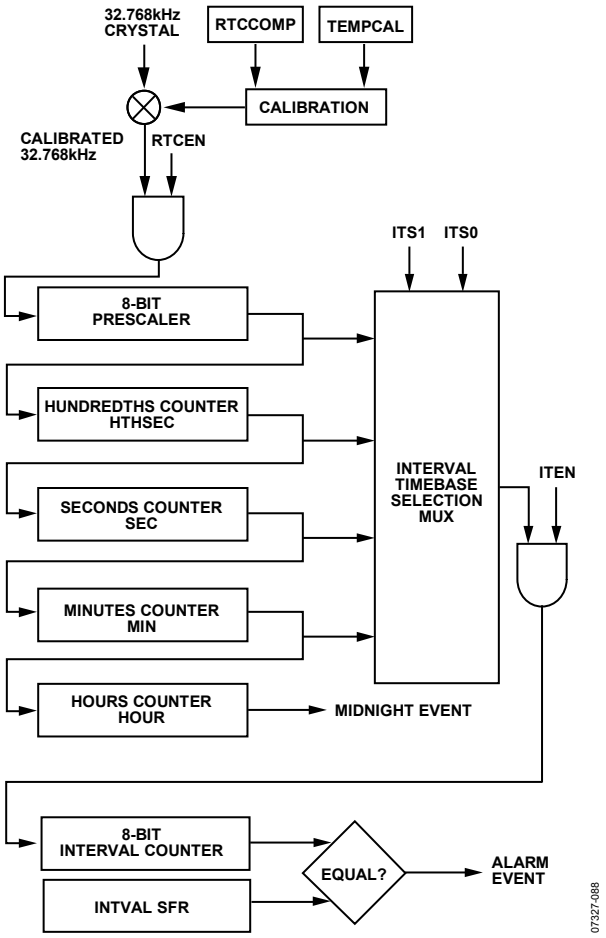


Figure 88. RTC Implementation

RTC REGISTERS

Note that all the real-time clock SFRs are not bit addressable.

Table 108. Real-Time Clock SFR

SFR	Address	Description
TIMECON	0xA1	RTC Configuration (see Table 109).
HTHSEC	0xA2	Hundredths of a Second Counter (see Table 110).
SEC	0xA3	Seconds Counter (see Table 111).
MIN	0xA4	Minutes Counter (see Table 112).
HOUR	0xA5	Hours Counter (see Table 113).
INTVAL	0xA6	Alarm Interval (see Table 114).
RTCCOMP	0xF6	RTC Nominal Compensation (see Table 115).
TEMPCAL	0xF7	RTC Temperature Compensation (see Table 116).

Protecting the RTC from Runaway Code

To protect the RTC from runaway code, a key must be written to the KYREG register to obtain write access to the Interrupt Pins Configuration SFR (INTPR, 0xFF), Hundredths of a Second Counter SFR (HTHSEC, 0xA2), Seconds Counter SFR (SEC, 0xA3), Minutes Counter SFR (MIN, 0xA4), and Hours Counter SFR (HOUR, 0xA5). KYREG should be set to 0xEA to unlock it and reset it to zero after a timekeeping register is written to. The RTC registers can be written using the following 8052 assembly code:

```
MOV     KYREG,#0EAh
MOV     INTPR,#080h
```

Table 109. RTC Configuration SFR (TIMECON, 0xA1)

Bit	Mnemonic	Default	Description	
7	MIDNIGHT	0	Midnight Flag. This bit is set when the RTC rolls over to 00:00:00:00. It can be cleared by the user to indicate that the midnight event has been serviced. In 24-hour mode, the midnight flag is raised once a day at midnight. When this interrupt is used for wake-up from PSM2 to PSM1, the RTC interrupt must be serviced and the flag cleared to be allowed to enter PSM2.	
6	TFH	0	24-Hour Mode. This bit is retained during a watchdog reset or an external reset. It is reset after a power-on reset (POR).	
			TFH	**Result**
			0	256-Hour Mode. The HOUR register rolls over from 255 to 0.
			1	24-Hour Mode. The HOUR register rolls over from 23 to 0.
5 to 4	ITS[1:0]	00	Interval Timer Time Base Selection.	
			ITS[1:0]	**Result (Time Base)**
			00	1/128 sec.
			01	Second.
			10	Minute.
			11	Hour.
3	SIT	0	Interval Timer 1 Alarm.	
			SIT	**Result**
			0	The ALARM flag is set after INTVAL counts and then another interval count starts.
			1	The ALARM flag is set after one time interval.
2	ALARM	0	Interval Timer Alarm Flag. This bit is set when the configured time interval has elapsed. It can be cleared by the user to indicate that the alarm event has been serviced. This bit cannot be set to 1 by user code.	
1	ITEN	0	Interval Timer Enable.	
			ITEN	**Result**
			0	The interval timer is disabled. The 8-bit interval timer counter is reset.
			1	Set this bit to enable the interval timer.
0	Reserved	1	This bit must be left set for proper operation.	

Table 110. Hundredths of a Second Counter SFR (HTHSEC, 0xA2)

Bit	Mnemonic	Default	Description
7 to 0	HTHSEC	0	This counter updates every 1/128 second, referenced from the calibrated 32.768 kHz clock. It overflows from 127 to 00, incrementing the seconds counter (SEC). This register is retained during a watchdog reset or an external reset. It is reset after a POR.

Table 111. Seconds Counter SFR (SEC, 0xA3)

Bit	Mnemonic	Default	Description
7 to 0	SEC	0	This counter updates every second, referenced from the calibrated 32.768 kHz clock. It overflows from 59 to 00, incrementing the minutes counter (MIN). This register is retained during a watchdog reset or an external reset. It is reset after a POR.

Table 112. Minutes Counter SFR (MIN, 0xA4)

Bit	Mnemonic	Default	Description
7 to 0	MIN	0	This counter updates every minute, referenced from the calibrated 32.768 kHz clock. It overflows from 59 to 00, incrementing the hours counter (HOUR). This register is retained during a watchdog reset or an external reset. It is reset after a POR.

Table 113. Hours Counter SFR (HOUR, 0xA5)

Bit	Mnemonic	Default	Description
7 to 0	HOUR	0	This counter updates every hour, referenced from the calibrated 32.768 kHz clock. If the TFH bit in the RTC Configuration SFR (TIMECON, 0xA1) is set, the HOUR SFR overflows from 23 to 00, setting the MIDNIGHT bit and creating a pending RTC interrupt. If the TFH bit is cleared, the HOUR SFR overflows from 255 to 00, setting the MIDNIGHT bit and creating a pending RTC interrupt. This register is retained during a watchdog reset or an external reset. It is reset after a POR.

Table 114. Alarm Interval SFR (INTVAL, 0xA6)

Bit	Mnemonic	Default	Description
7 to 0	INTVAL	0	The interval timer counts according to the time base established in the ITS[1:0] bits of the RTC Configuration SFR (TIMECON, 0xA1). Once the number of counts is equal to INTVAL, the ALARM flag is set and a pending RTC interrupt is created. Note that the interval counter is eight bits. Therefore, it can count up to 255 seconds, for example.

Table 115. RTC Nominal Compensation SFR (RTCCOMP, 0xF6)

Bit	Mnemonic	Default	Description
7 to 0	RTCCOMP	0	The RTCCOMP SFR holds the nominal RTC compensation value at 25°C. This register is retained during a watchdog reset or an external reset. It is reset after a POR.

Table 116. RTC Temperature Compensation SFR (TEMPCAL, 0xF7)

Bit	Mnemonic	Default	Description
7 to 0	TEMPCAL	0	The TEMPCAL SFR is adjusted based on a temperature read. This allows the external crystal shift to be compensated over temperature. This register is retained during a watchdog reset or an external reset. It is reset after a POR.

Table 117. Interrupt Pins Configuration SFR (INTPR, 0xFF)

Bit	Mnemonic	Default	Description	
7	RTCCAL	0	Controls the RTC calibration output. When set, the RTC calibration frequency selected by FSEL[1:0] is output on the P0.2/CF1/RTCCAL pin.	
6 to 5	FSEL[1:0]	00	Sets RTC calibration output frequency and calibration window.	
			FSEL[1:0]	**Result (Calibration Window, Frequency)**
			00	30.5 sec, 1 Hz
			01	30.5 sec, 512 Hz
			10	0.244 sec, 500 Hz
			11	0.244 sec, 16.384 kHz
4	Reserved	0	This bit must be set to 0 for proper operation.	
3 to 1	INT1PRG[2:0]	000	Controls the function of $\overline{\text{INT1}}$.	
			INT1PRG[2:0]	**Result**
			x00	GPIO
			x01	BCTRL
			01x	$\overline{\text{INT1}}$ input disabled
			11x	$\overline{\text{INT1}}$ input enabled
0	INT0PRG	0	Controls the function of $\overline{\text{INT0}}$.	
			INT0PRG	**Result**
			0	$\overline{\text{INT0}}$ input disabled
			1	$\overline{\text{INT0}}$ input enabled

Table 118. Key SFR (KYREG, 0xC1)

Bit	Mnemonic	Default	Description
7 to 0	KYREG	0	Write 0xA7 to this SFR before writing to the POWCON SFR, which unlocks KYREG. Write 0xEA to this SFR before writing to the INTPR, HTHSEC, SEC, MIN, or HOUR timekeeping registers to unlock KYREG.

READ AND WRITE OPERATIONS

Writing to the RTC Registers

The RTC circuitry runs off a 32.768 kHz clock. The timekeeping registers, Hundredths of a Second Counter SFR (HTHSEC, 0xA2), Seconds Counter SFR (SEC, 0xA3), Minutes Counter SFR (MIN, 0xA4), and Hours Counter SFR (HOUR, 0xA5), are updated with a 32.768 kHz clock. However, the RTC Configuration SFR (TIMECON, 0xA1) and Alarm Interval SFR (INTVAL, 0xA6) are updated with a 128 Hz clock. It takes up to two 128 Hz clock cycles from when the MCU writes to the TIMECON SFR or the INTVAL SFR until there is a successful update in the RTC.

To protect the RTC timekeeping registers from runaway code, a key must be written to the Key SFR (KYREG, 0xC1), which is described in Table 105, to obtain write access to the HTHSEC, SEC, MIN, and HOUR SFRs. KYREG should be set to 0xEA to unlock the timekeeping registers and reset to 0 after a timekeeping register is written to. The RTC registers can be written to using the following 8052 assembly code:

```
MOV    RTCKey,#0EAh
CALL   UpdateRTC
…
UpdateRTC:
    MOV  KYREG,RTCKey
    MOV  SEC,#30
    MOV  KYREG,RTCKey
    MOV  MIN,#05
    MOV  KYREG,RTCKey
    MOV  HOUR,#04
    MOV  KYREG,#00h
    RET
```

Reading the RTC Counter SFRs

The RTC cannot be stopped to read the current time because stopping the RTC introduces an error in its timekeeping. Therefore, the RTC is read on the fly, and the counter registers must be checked for overflow. This can be accomplished through the following 8052 assembly code:

```
ReadAgain:
    MOV  R0,HTHSEC          ; using Bank 0
    MOV  R1,SEC
    MOV  R2,MIN
    MOV  R3,HOUR
    MOV  A,HTHSEC
    CJNE A, 00h, ReadAgain ; 00h is R0 in
Bank 0
```

RTC MODES

The RTC can be configured in a 24-hour mode or a 256-hour mode. A midnight event is generated when the RTC hour counter rolls over from 23 to 0 or 255 to 0, depending on whether the TFH bit is set in the RTC Configuration SFR (TIMECON, 0xA1). The midnight event sets the MIDNIGHT flag in the TIMECON SFR, and a pending RTC interrupt is created. The RTC midnight event wakes the 8052 MCU core if the MCU is asleep in PSM2 when the midnight event occurs.

In the 24-hour mode, the midnight event is generated once a day at midnight. The 24-hour mode is useful for updating a software calendar to keep track of the current day. The 256-hour mode results in power savings during extended operation in PSM2 because the MCU core wakes up less frequently.

RTC INTERRUPTS

The RTC midnight interrupt and alarm interrupt are enabled by setting the ETI bit in the Interrupt Enable and Priority 2 SFR (IEIP2, 0xA9). When a midnight or alarm event occurs, a pending RTC interrupt is generated. If the RTC interrupt is enabled, the program vectors to the RTC interrupt address and the pending interrupt is cleared. If the RTC interrupt is disabled, the RTC interrupt remains pending until the RTC interrupt is enabled. The program then vectors to the RTC interrupt address.

The MIDNIGHT flag and ALARM flag are set when the midnight event and alarm event occur, respectively. The user should manage these flags to keep track of which event caused an RTC interrupt by servicing the event and clearing the appropriate flag in the RTC interrupt servicing routine.

Note that if the ADE7518 is awakened by an RTC event, either by the MIDNIGHT event or the ALARM event, the pending RTC interrupt must be serviced before the device can go back to sleep again. The ADE7518 keeps waking up until this interrupt has been serviced.

Interval Timer Alarm

The RTC can be used as an interval timer. When the interval timer is enabled by setting the ITEN bit in the RTC Configuration SFR (TIMECON, 0xA1), the interval timer clock source selected by the ITS1 and ITS0 bits is passed through an 8-bit counter. This counter increments on every interval timer clock pulse until it is equal to the value in the Alarm Interval SFR (INTVAL, 0xA6). Then, an alarm event is generated, setting the ALARM flag and creating a pending RTC interrupt. If the SIT bit in the RTC Configuration SFR (TIMECON, 0xA1) is cleared, the 8-bit counter is also cleared and starts counting again. If the SIT bit is set, the 8-bit counter is held in reset after the alarm occurs.

Take care when changing the interval timer time base. The recommended procedure is as follows:

1. If the Alarm Interval SFR (INTVAL, 0xA6) is going to be modified, write to this register first. Then, wait for one 128 Hz clock cycle to synchronize with the RTC, 64,000 cycles at a 4.096 MHz instruction cycle clock.
2. Disable the interval timer by clearing the ITEN bit in the RTC Configuration SFR (TIMECON, 0xA1). Then, wait for one 128 Hz clock cycle to synchronize with the RTC, 64,000 cycles at a 4.096 MHz instruction cycle clock.
3. Read the TIMECON SFR to ensure that the ITEN bit is clear. If it is not, wait for another 128 Hz clock cycle.
4. Set the time base bits (ITS[1:0]) in the TIMECON SFR to configure the interval. Wait for a 128 Hz clock cycle for this change to take effect.

The RTC alarm event wakes the 8052 MCU core if the MCU is in PSM2 when the alarm event occurs.

RTC CALIBRATION

The RTC provides registers to calibrate the nominal external crystal frequency and its variation over temperature. A frequency error up to ±248 ppm can be calibrated by the RTC circuitry, which adds or subtracts pulses from the external crystal signal.

The nominal crystal frequency should be calibrated with the RTC nominal compensation register so that the clock going into the RTC is precisely 32.768 kHz at 25°C. The RTC Temperature Compensation SFR (TEMPCAL, 0xF7) is used to compensate for the external crystal drift over temperature by adding or subtracting additional pulses based on temperature.

The LSB of each RTC compensation register represents a ±2 ppm frequency error. The RTC compensation circuitry adds the RTC Temperature Compensation SFR (TEMPCAL, 0xF7) and the RTC Nominal Compensation SFR (RTCCOMP, 0xF6) to determine how much compensation is required. Note that the sum of these two registers is limited to ±248 ppm.

Calibration Flow

An RTC calibration pulse output is provided on the P0.2/CF1/RTCCAL pin. Enable the RTC output by setting the RTCCAL bit in the Interrupt Pins Configuration SFR (INTPR, 0xFF).

The RTC calibration is accurate to within ±2 ppm over a 30.5 sec window in all operational modes: PSM0, PSM1, and PSM2. Two output frequencies are offered for the normal RTC mode: 1 Hz with FSEL[1:0] = 00 and 512 Hz with FSEL[1:0] = 01 in the Interrupt Pins Configuration SFR (INTPR, 0xFF).

A shorter window of 0.244 sec is offered for fast calibration during PSM0 or PSM1. Two output frequencies are offered for this RTC calibration output mode: 500 Hz with FSEL[1:0] = 10 and 16.384 kHz with FSEL[1:0] = 11 in the INTPR SFR. Note that for the 0.244 sec calibration window, the RTC is clocked 125 times faster than in normal mode, resulting in timekeeping registers that represent seconds/125, minutes/125, and hours/125 instead of seconds, minutes, and hours. Therefore, this mode should be used for calibration only.

Table 119. RTC Calibration Options

Option	FSEL[1:0]	Calibration Window (Sec)	f_{RTCCAL} (Hz)
Normal Mode 0	00	30.5	1
Normal Mode 1	01	30.5	512
Calibration Mode 0	10	0.244	500
Calibration Mode 1	11	0.244	16,384

When no RTC compensation is applied, that is, when RTC Nominal Compensation SFR (RTCCOMP, 0xF6) and RTC Temperature Compensation SFR (TEMPCAL, 0xF7) are equal to 0, the nominal compensation required to account for the error in the external crystal can be determined. In this case, it is not necessary to wait for an entire calibration window to determine the error in the pulse output. Calculating the error in frequency between two consecutive pulses on the P0.2/CF1/RTCCAL pin is sufficient.

The value to write to the RTC Nominal Compensation SFR (RTCCOMP, 0xF6) is calculated from the % error or seconds per day error on the frequency output. Each LSB of the RTCCOMP SFR represents 2 ppm of correction where 1 sec/day error is equal to 11.57 ppm.

$$RTCCOMP = 5000 \times (\%\ Error)$$

$$RTCCOMP = \frac{1}{2 \times 11.57} \times (sec/day\ Error)$$

During calibration, user software writes the RTC with the current time. Refer to the Read and Write Operations section for more information on how to read and write the RTC timekeeping registers.

UART SERIAL INTERFACE

The ADE7518 UART can be configured in one of four modes.

- Shift register with baud rate fixed at $f_{CORE}/12$
- 8-bit UART with variable baud rate
- 9-bit UART with baud rate fixed at $f_{CORE}/64$ or $f_{CORE}/32$
- 9-bit UART with variable baud rate

Variable baud rates are defined by using an internal timer to generate any rate between 300 baud/sec and 115,200 baud/sec.

The UART serial interface provided in the ADE7518 is a full-duplex serial interface. It is also receive-buffered by storing the first received byte in a receive buffer until the reception of the second byte is complete. The physical interface to the UART is provided via the RxD (P1.0) and TxD (P1.1) pins, whereas the firmware interface is through the SFRs presented in Table 120.

Both the serial port receive and transmit registers are accessed through the Serial Port Buffer SFR (SBUF, 0x99). Writing to SBUF loads the transmit register, and reading SBUF accesses a physically separate receive register.

An enhanced UART mode is offered by using the UART timer and by providing enhanced frame error, break error, and overwrite error detection. This mode is enabled by setting the EXTEN bit in the Configuration SFR (CFG, 0xAF) (see the UART Additional Features section). The Enhanced Serial Baud Rate Control SFR (SBAUDT, 0x9E) and UART Timer Fractional Divider SFR (SBAUDF, 0x9D) are used to configure the UART timer and to indicate the enhanced UART errors.

UART REGISTERS

Table 120. Serial Port SFRs

SFR	Address	Bit Addressable	Description
SCON	0x98	Yes	Serial Communications Control Register (see Table 121).
SBUF	0x99	No	Serial Port Buffer (see Table 122).
SBAUDT	0x9E	No	Enhanced Serial Baud Rate Control (see Table 123).
SBAUDF	0x9D	No	UART Timer Fractional Divider (see Table 124).

Table 121. Serial Communications Control Register SFR (SCON, 0x98)

Bit	Address	Mnemonic	Default	Description	
7 to 6	0x9F, 0x9E	SM0, SM1	00	UART Serial Mode Select Bits. These bits select the serial port operating mode.	
				SM[1:0]	**Result (Selected Operating Mode)**
				00	Mode 0, shift register, fixed baud rate at $f_{CORE}/12$.
				01	Mode 1, 8-bit UART, variable baud rate.
				10	Mode 2, 9-bit UART, fixed baud rate at $f_{CORE}/32$ or $f_{CORE}/16$.
				11	Mode 3, 9-bit UART, variable baud rate.
5	0x9D	SM2	0	Multiprocessor Communication Enable Bit. Enables multiprocessor communication in Mode 2 and Mode 3, and framing error detection in Mode 1. In Mode 0, SM2 should be cleared. In Mode 1, if SM2 is set, RI is not activated if a valid stop bit was not received. If SM2 is cleared, RI is set as soon as the byte of data is received. In Mode 2 or Mode 3, if SM2 is set, RI is not activated if the received ninth data bit in RB8 is 0. If SM2 is cleared, RI is set as soon as the byte of data is received.	
4	0x9C	REN	0	Serial Port Receive Enable Bit. Set by user software to enable serial port reception. Cleared by user software to disable serial port reception.	
3	0x9B	TB8	0	Serial Port Transmit Bit 9. The data loaded into TB8 is the ninth data bit transmitted in Mode 2 and Mode 3.	
2	0x9A	RB8	0	Serial Port Receiver Bit 9. The ninth data bit received in Mode 2 and Mode 3 is latched into RB8. For Mode 1, the stop bit is latched into RB8.	
1	0x99	TI	0	Serial Port Transmit Interrupt Flag. Set by hardware at the end of the eighth bit in Mode 0 or at the beginning of the stop bit in Mode 1, Mode 2, and Mode 3. TI must be cleared by user software.	
0	0x98	RI	0	Serial Port Receive Interrupt Flag. Set by hardware at the end of the eighth bit in Mode 0 or halfway through the stop bit in Mode 1, Mode 2, and Mode 3. RI must be cleared by user software.	

Table 122. Serial Port Buffer SFR (SBUF, 0x99)

Bit	Mnemonic	Default	Description
7 to 0	SBUF	0	Serial Port Data Buffer.

Table 123. Enhanced Serial Baud Rate Control SFR (SBAUDT, 0x9E)

Bit	Mnemonic	Default	Description	
7	OWE	0	Overwrite Error. This bit is set when new data is received and RI = 1. It indicates that SBUF was not read before the next character was transferred in, causing the prior SBUF data to be lost. Write a 0 to this bit to clear it.	
6	FE	0	Frame Error. This bit is set when the received frame does not have a valid stop bit. This bit is read only and is updated every time a frame is received.	
5	BE	0	Break Error. This bit is set whenever the receive data line (Rx) is low for longer than a full transmission frame, which is the time required for a start bit, eight data bits, a parity bit, and half a stop bit. This bit is updated every time a frame is received.	
4, 3	SBTH[1:0]	0	Extended divider ratio for baud rate setting, as shown in Table 125.	
2 to 0	DIV[2:0]	000	Binary Divider. See Table 125.	
			DIV[2:0]	**Result**
			000	Divide by 1.
			001	Divide by 2.
			010	Divide by 4.
			011	Divide by 8.
			100	Divide by 16.
			101	Divide by 32.
			110	Divide by 64.
			111	Divide by 128.

Table 124. UART Timer Fractional Divider SFR (SBAUDF, 0x9D)

Bit	Mnemonic	Default	Description
7	UARTBAUDEN	0	UART Baud Rate Enable. Set to enable UART timer to generate the baud rate. When this bit is set, PCON[7] (SMOD), T2CON[4] (TCLK), and T2CON[5] (RCLK) are ignored. Cleared to let the baud rate be generated as per a standard 8052.
6			Not implemented, write don't care.
5	SBAUDF.5	0	UART Timer Fractional Divider Bit 5.
4	SBAUDF.4	0	UART Timer Fractional Divider Bit 4.
3	SBAUDF.3	0	UART Timer Fractional Divider Bit 3.
2	SBAUDF.2	0	UART Timer Fractional Divider Bit 2.
1	SBAUDF.1	0	UART Timer Fractional Divider Bit 1.
0	SBAUDF.0	0	UART Timer Fractional Divider Bit 0.

Table 125. Common Baud Rates Using UART Timer with a 4.096 MHz PLL Clock

Ideal Baud	CD	SBTH	DIV	SBAUDT	SBAUDF	% Error
115,200	0	0	1	0x01	0x87	+0.16
115,200	1	0	0	0x00	0x87	+0.16
57,600	0	0	2	0x02	0x87	+0.16
57,600	1	0	1	0x01	0x87	+0.16
38,400	0	0	2	0x02	0xAB	−0.31
38,400	1	0	1	0x01	0xAB	−0.31
38,400	2	0	0	0x00	0xAB	−0.31
19,200	0	0	3	0x03	0xAB	−0.31
19,200	1	0	2	0x02	0xAB	−0.31
19,200	2	0	1	0x01	0xAB	−0.31
19,200	3	0	0	0x00	0xAB	−0.31
9600	0	0	4	0x04	0xAB	−0.31
9600	1	0	3	0x03	0xAB	−0.31
9600	2	0	2	0x02	0xAB	−0.31
9600	3	0	1	0x01	0xAB	−0.31
9600	4	0	0	0x00	0xAB	−0.31
4800	0	0	5	0x05	0xAB	−0.31
4800	1	0	4	0x04	0xAB	−0.31
4800	2	0	3	0x03	0xAB	−0.31
4800	3	0	2	0x02	0xAB	−0.31
4800	4	0	1	0x01	0xAB	−0.31
4800	5	0	0	0x00	0xAB	−0.31
2400	0	0	6	0x06	0xAB	−0.31
2400	1	0	5	0x05	0xAB	−0.31
2400	2	0	4	0x04	0xAB	−0.31
2400	3	0	3	0x03	0xAB	−0.31
2400	4	0	2	0x02	0xAB	−0.31
2400	5	0	1	0x01	0xAB	−0.31
2400	6	0	0	0x00	0xAB	−0.31
300	0	2	7	0x17	0xAB	−0.31
300	1	1	7	0x0F	0xAB	−0.31
300	2	0	7	0x07	0xAB	−0.31
300	3	0	6	0x06	0xAB	−0.31
300	4	0	5	0x05	0xAB	−0.31
300	5	0	4	0x04	0xAB	−0.31
300	6	0	3	0x03	0xAB	−0.31
300	7	0	2	0x02	0xAB	−0.31

UART OPERATION MODES

Mode 0 (Shift Register with Baud Rate Fixed at f_{CORE}/12)

Mode 0 is selected when the SM0 and SM1 bits in the Serial Communications Control Register Bit Description SFR (SCON, 0x98) are cleared. In this shift register mode, serial data enters and exits through RxD. TxD outputs the shift clock. The baud rate is fixed at f_{CORE}/12. Eight data bits are transmitted or received.

Transmission is initiated by any instruction that writes to the Serial Port Buffer SFR (SBUF, 0x99). The data is shifted out of the RxD line. The eight bits are transmitted with the least significant bit (LSB) first.

Reception is initiated when the receive enable bit (REN) is 1 and the receive interrupt bit (RI) is 0. When RI is cleared, the data is clocked into the RxD line, and the clock pulses are output from the TxD line, as shown in Figure 89.

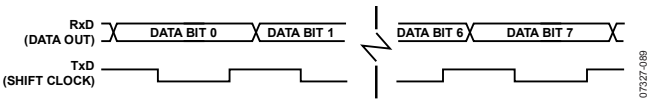


Figure 89. 8-Bit Shift Register Mode

Mode 1 (8-Bit UART, Variable Baud Rate)

Mode 1 is selected by clearing SM0 and setting SM1. Each data byte (LSB first) is preceded by a start bit (0) and followed by a stop bit (1). Therefore, each frame consists of 10 bits transmitted on TxD or received on RxD.

The baud rate is set by a timer overflow rate. Timer 1 or Timer 2 can be used to generate baud rates, or both timers can be used simultaneously where one generates the transmit rate and the other generates the receive rate. There is also a dedicated timer for baud rate generation, the UART timer, which has a fractional divisor to precisely generate any baud rate (see the UART Timer Generated Baud Rates section).

Transmission is initiated by a write to the Serial Port Buffer SFR (SBUF, 0x99). Next, a stop bit (1) is loaded into the ninth bit position of the transmit shift register. The data is output bit by bit until the stop bit appears on TxD and the transmit interrupt flag (TI) is automatically set as shown in Figure 90.

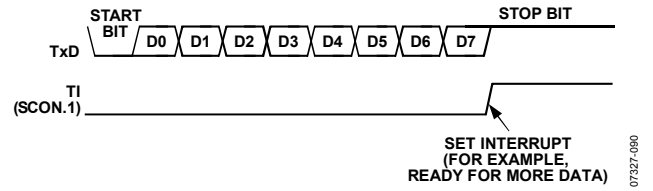


Figure 90. 8-Bit Variable Baud Rate

Reception is initiated when a 1-to-0 transition is detected on RxD. Assuming that a valid start bit is detected, character reception continues. The eight data bits are clocked into the serial port shift register.

All of the following conditions must be met at the time the final shift pulse is generated to receive a character:

- If the extended UART is disabled (EXTEN = 0 in the CFG SFR), RI must be 0 to receive a character. This ensures that the data in the SBUF SFR is not overwritten if the last received character has not been read.
- If frame error checking is enabled by setting SM2, the received stop bit must be set to receive a character. This ensures that every character received comes from a valid frame, with both a start bit and a stop bit.

If any of these conditions are not met, the received frame is irretrievably lost, and the receive interrupt flag (RI) is not set.

If the received frame has met the previous criteria, the following events occur:

- The eight bits in the receive shift register are latched into the SBUF SFR.
- The ninth bit (stop bit) is clocked into RB8 in the SCON SFR.
- The receiver interrupt flag (RI) is set.

Mode 2 (9-Bit UART with Baud Fixed at f_{CORE}/64 or f_{CORE}/32)

Mode 2 is selected by setting SM0 and clearing SM1. In this mode, the UART operates in 9-bit mode with a fixed baud rate. The baud rate is fixed at f_{CORE}/64 by default, although setting the SMOD bit in the Program Control SFR (PCON, 0x87) doubles the frequency to f_{CORE}/32. Eleven bits are transmitted or received: a start bit (0), eight data bits, a programmable ninth bit, and a stop bit (1). The ninth bit is most often used as a parity bit or as part of a multiprocessor communication protocol, although it can be used for anything, including a ninth data bit, if required.

To use the ninth data bit as part of a communication protocol for a multiprocessor network such as RS-485, the ninth bit is set to indicate that the frame contains the address of the device with which the master wants to communicate. The devices on the network are always listening for a packet with the ninth bit set and are configured such that if the ninth bit is cleared, the frame is not valid, and a receive interrupt is not generated. If the ninth bit is set, all devices on the network receive the address and obtain a receive character interrupt. The devices examine the address and, if it matches one of the device's preprogrammed addresses, that device configures itself to listen to all incoming frames, even those with the ninth bit cleared. Because the master has initiated communication with that device, all the following packets with the ninth bit cleared are intended specifically for that addressed device until another packet with the ninth bit set is received. If the address does not match, the device continues to listen for address packets.

To transmit, the eight data bits must be written into the Serial Port Buffer SFR (SBUF, 0x99). The ninth bit must be written to TB8 in the Serial Communications Control Register SFR (SCON, 0x98). When transmission is initiated, the eight data bits from SBUF are loaded into the transmit shift register (LSB first). The ninth data bit, held in TB8, is loaded into the ninth bit position of the transmit shift register. The transmission starts at the next valid baud rate clock. The transmit interrupt flag (TI) is set as soon as the transmission completes, when the stop bit appears on TxD.

All of the following conditions must be met at the time the final shift pulse is generated to receive a character:

- If the extended UART is disabled (EXTEN = 0 in the CFG SFR), RI must be 0 to receive a character. This ensures that the data in SBUF is not overwritten if the last received character has not been read.
- If multiprocessor communication is enabled by setting SM2, the received ninth bit must be set to receive a character. This ensures that only frames with the ninth bit set, that is, frames that contain addresses, generate a receive interrupt.

If any of these conditions are not met, the received frame is irretrievably lost, and the receive interrupt flag (RI) is not set.

Reception for Mode 2 is similar to that of Mode 1. The eight data bytes are input at RxD (LSB first) and loaded onto the receive shift register. If the received frame has met the previous criteria, the following events occur:

- The eight bits in the receive shift register are latched into the SBUF SFR.
- The ninth data bit is latched into RB8 in the SCON SFR.
- The receiver interrupt flag (RI) is set.

Mode 3 (9-Bit UART with Variable Baud Rate)

Mode 3 is selected by setting both SM0 and SM1. In this mode, the 8052 UART serial port operates in 9-bit mode with a variable baud rate. The baud rate is set by a timer overflow rate. Timer 1 or Timer 2 can be used to generate baud rates, or both timers can be used simultaneously, where one generates the transmit rate and the other generates the receive rate. There is also a dedicated timer for baud rate generation, the UART timer, which has a fractional divisor to precisely generate any baud rate (see the UART Timer Generated Baud Rates section). The operation of the 9-bit UART is the same as for Mode 2, but the baud rate can be varied.

In all four modes, transmission is initiated by any instruction that uses SBUF as a destination register. Reception is initiated in Mode 0 when RI = 0 and REN = 1. Reception is initiated in the other modes by the incoming start bit if REN = 1.

UART BAUD RATE GENERATION

Mode 0 Baud Rate Generation

The baud rate in Mode 0 is fixed.

$$Mode\ 0\ Baud\ Rate = \left(\frac{f_{CORE}}{12}\right)$$

Mode 2 Baud Rate Generation

The baud rate in Mode 2 depends on the value of the PCON[7] (SMOD) bit in the Program Control SFR (PCON, 0x87). If SMOD = 0, the baud rate is 1/32 of the core clock. If SMOD = 1, the baud rate is 1/16 of the core clock.

$$Mode\ 2\ Baud\ Rate = \frac{2^{SMOD}}{32} \times f_{CORE}$$

Mode 1 and Mode 3 Baud Rate Generation

The baud rates in Mode 1 and Mode 3 are determined by the overflow rate of the timer generating the baud rate, that is, either Timer 1, Timer 2, or the dedicated baud rate generator, UART timer, which has an integer and fractional divisor.

Timer 1 Generated Baud Rates

When Timer 1 is used as the baud rate generator, the baud rates in Mode 1 and Mode 3 are determined by the Timer 1 overflow rate. The value of SMOD is as follows:

$$Mode\ 1\ or\ Mode\ 3\ Baud\ Rate = \frac{2^{SMOD}}{32} \times Timer\ 1\ Overflow\ Rate$$

The Timer 1 interrupt should be disabled in this application. The timer itself can be configured for either timer or counter operation, in any of its three running modes. In the most typical application, it is configured for timer operation in autoreload mode (high nibble of TMOD = 0010 binary). In that case, the baud rate is given by the following formula:

$$Mode\ 1\ or\ Mode\ 3\ Baud\ Rate = \frac{2^{SMOD}}{32} \times \frac{f_{CORE}}{(256 - TH1)}$$

Timer 2 Generated Baud Rates

Baud rates can also be generated by using Timer 2. Using Timer 2 is similar to using Timer 1 in that the timer must overflow 16 times before a bit is transmitted or received. Because Timer 2 has a 16-bit autoreload mode, a wider range of baud rates is possible.

$$Mode\ 1\ or\ Mode\ 3\ Baud\ Rate = \frac{1}{16} \times Timer\ 2\ Overflow\ Rate$$

Therefore, when Timer 2 is used to generate baud rates, the timer increments every two clock cycles rather than every core machine cycle as before. It increments six times faster than Timer 1, and, therefore, baud rates six times faster are possible. Because Timer 2 has 16-bit autoreload capability, very low baud rates are still possible. Timer 2 is selected as the baud rate generator by setting TCLK and/or RCLK in Timer/Counter 2 Control SFR (T2CON, 0xC8). The baud rates for transmit and receive can be simultaneously different. Setting RCLK and/or

TCLK puts Timer 2 into its baud rate generator mode, as shown in Figure 92.

In this case, the baud rate is given by the following formula:

$$Mode\ 1\ or\ Mode\ 3\ Baud\ Rate = \frac{f_{CORE}}{(16 \times [65536 - (RCAP2H : RCAP2L)])}$$

UART Timer Generated Baud Rates

The high integer dividers in a UART block mean that high speed baud rates are not always possible. In addition, generating baud rates requires the exclusive use of a timer, rendering it unusable for other applications when the UART is required. To address this problem, each ADE7518 has a dedicated baud rate timer (UART timer) specifically for generating highly accurate baud rates. The UART timer can be used instead of Timer 1 or Timer 2 for generating very accurate high speed UART baud rates, including 115,200 bps. This timer also allows a much wider range of baud rates to be obtained. In fact, every desired bit rate from 12 bps to 393,216 bps can be generated to within an error of ±0.8%. The UART timer also frees up the other three timers, allowing them to be used for different applications. A block diagram of the UART timer is shown in Figure 91.

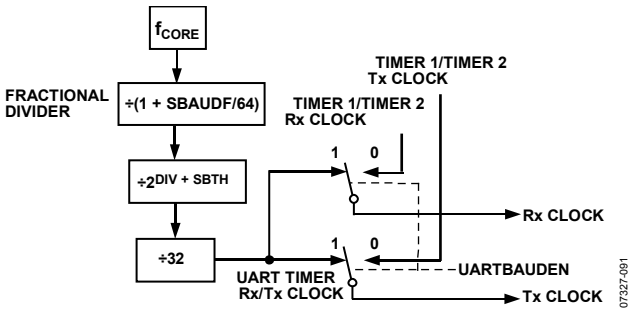


Figure 91. UART Timer, UART Baud Rate

Two SFRs, Enhanced Serial Baud Rate Control SFR (SBAUDT, 0x9E) and UART Timer Fractional Divider SFR (SBAUDF, 0x9D), are used to control the UART timer. SBAUDT is the baud rate control SFR; it sets up the integer divider (DIV) and the extended divider (SBTH) for the UART timer.

The appropriate value to write to the DIV[2:0] and SBTH[1:0] bits can be calculated using the following formula, where f_{CORE} is defined in the POWCON SFR (see Table 24). Note that the DIV value must be rounded down to the nearest integer.

$$DIV + SBTH = \frac{\log\left(\frac{f_{CORE}}{16 \times Baud\ Rate}\right)}{\log(2)}$$

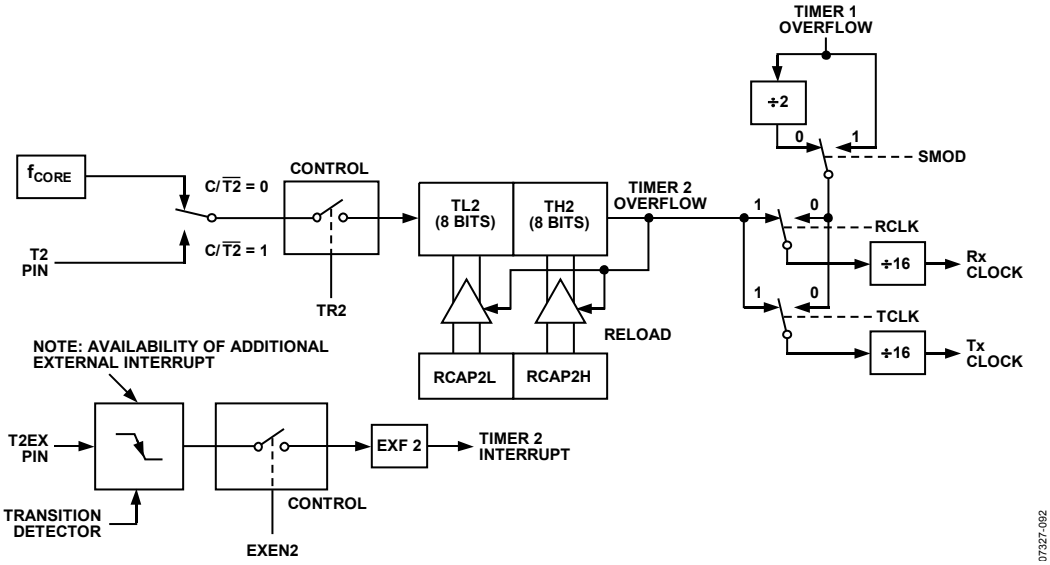


Figure 92. Timer 2, UART Baud Rates

SBAUDF is the fractional divider ratio required to achieve the required baud rate. The appropriate value for SBAUDF can be calculated with the following formula:

$$SBAUDF = 64 \times \left(\frac{f_{CORE}}{16 \times 2^{DIV+SBTH} \times Baud\ Rate} - 1 \right)$$

Note that SBAUDF should be rounded to the nearest integer. After the values for DIV and SBAUDF are calculated, the actual baud rate can be calculated with the following formula:

$$Actual\ Baud\ Rate = \frac{f_{CORE}}{16 \times 2^{DIV+SBTH} \times \left(1 + \frac{SBAUDF}{64} \right)}$$

For example, to obtain a baud rate of 9600 bps while operating at a core clock frequency of 4.096 MHz with the PLL CD bits equal to 0,

$$DIV + SBTH = \frac{\log\left(\frac{4{,}096{,}000}{16 \times 9600} \right)}{\log(2)} = 4.74 = 4$$

Note that the DIV result is rounded down.

$$SBAUDF = 64 \times \left(\frac{4{,}096{,}000}{16 \times 2^3 \times 9600} - 1 \right) = 42.67 = 0x2B$$

Thus, the actual baud rate is 9570 bps, resulting in a 0.31% error.

UART ADDITIONAL FEATURES

Enhanced Error Checking

The extended UART provides frame error, break error, and overwrite error detection. Framing errors occur when a stop bit is not present at the end of the frame. A missing stop bit implies that the data in the frame may not have been received properly. Break error detection indicates whether the Rx line has been low for longer than a 9-bit frame. It indicates that the data just received, a 0 or null character, is not valid because the master has disconnected. Overwrite error detection indicates when the received data has not been read fast enough and, as a result, a byte of data has been lost.

The 8052 standard UART offers frame-error checking for an 8-bit UART through the SM2 and RB8 bits. Setting the SM2 bit prevents frames without a stop bit from being received. The stop bit is latched into the RB8 bit in the Serial Communications Control Register SFR (SCON, 0x98). This bit can be examined to determine if a valid frame was received. The 8052 does not, however, provide frame error checking for a 9-bit UART. This enhanced error checking functionality is available through the frame error bit, FE, in the Enhanced Serial Baud Rate Control SFR (SBAUDT, 0x9E). The FE bit is set on framing errors for both 8-bit and 9-bit UARTs.

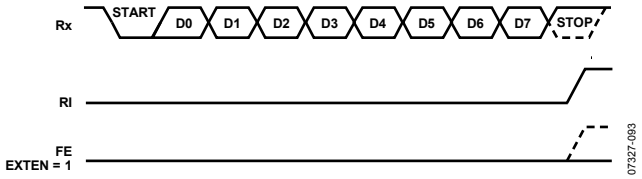


Figure 93. UART Timing in Mode 1

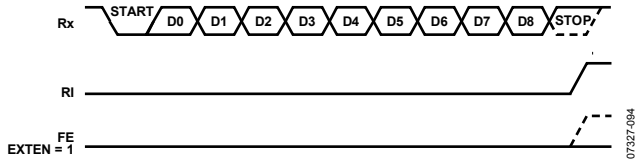


Figure 94. UART Timing in Mode 2 and Mode 3

The 8052 standard UART does not provide break error detection. However, for an 8-bit UART, a break error can be detected when the received character is 0, a null character, and when there is a no stop bit because the RB8 bit is low. Break error detection is not possible for a 9-bit 8052 UART because the stop bit is not recorded. The ADE7518 enhanced break error detection is available through the BE bit in the SBAUDT SFR.

The 8052 standard UART prevents overwrite errors by not allowing a character to be received when the receive interrupt flag, RI, is set. However, it does not indicate if a character has been lost because the RI bit is set when the frame is received. The enhanced UART overwrite error detection provides this information. When the enhanced 8052 UART is enabled, a frame is received regardless of the state of the RI flag. If RI = 1 when a new byte is received, the byte in SCON is overwritten, and the overwrite error flag is set. The overwrite error flag is cleared when SBUF is read.

The extended UART is enabled by setting the EXTEN bit in the Configuration SFR (CFG, 0xAF).

UART TxD Signal Modulation

There is an internal 38 kHz signal that can be OR'ed with the UART transmit signal for use in remote control applications (see the 38 kHz Modulation section).

One of the events that can wake the MCU from sleep mode is activity on the RxD pin (see the 3.3 V Peripherals and Wake-Up Events section).

SERIAL PERIPHERAL INTERFACE (SPI)

The ADE7518 integrates a complete hardware serial peripheral interface on-chip. The SPI is full duplex so that eight bits of data are synchronously transmitted and simultaneously received. This SPI implementation is double buffered, allowing users to read the last byte of received data while a new byte is shifted in. The next byte to be transmitted can be loaded while the current byte is shifted out.

The SPI port can be configured for master or slave operation. The physical interface to the SPI is via the MISO (P0.5), MOSI (P0.4), SCLK (P0.6), and $\overline{SS}$ (P0.7) pins, whereas the firmware interface is via the SPI Configuration SFR 1 (SPIMOD1, 0xE8), the SPI Configuration SFR 2 (SPIMOD2, 0xE9), the SPI Interrupt Status SFR (SPISTAT, 0xEA), the SPI/I²C Transmit Buffer SFR (SPI2CTx, 0x9A), and the SPI/I²C Receive Buffer SFR (SPI2CRx, 0x9B).

Note that the SPI pins are shared with the I²C pins. Therefore, the user can enable only one interface at a time. The SCPS bit in the Configuration SFR (CFG, 0xAF) selects which peripheral is active.

SPI REGISTERS

Table 126. SPI SFR List

SFR Address	Name	R/W	Length (Bits)	Default	Description
0x9A	SPI2CTx	W	8	0	SPI/I²C Transmit Buffer (see Table 127).
0x9B	SPI2CRx	R	8	0	SPI/I²C Receive Buffer (see Table 128).
0xE8	SPIMOD1	R/W	8	0x10	SPI Configuration SFR 1 (see Table 129).
0xE9	SPIMOD2	R/W	8	0	SPI Configuration SFR 2 (see Table 130).
0xEA	SPISTAT	R/W	8	0	SPI Interrupt Status (see Table 131).

Table 127. SPI/I²C Transmit Buffer SFR (SPI2CTx, 0x9A)

Bit	Mnemonic	Default	Description
7 to 0	SPI2CTx	0	SPI or I²C Transmit Buffer. When SPI2CTx SFR is written, its content is transferred to the transmit FIFO input. When a write is requested, the FIFO output is sent on the SPI or I²C bus.

Table 128. SPI/I²C Receive Buffer SFR (SPI2CRx, 0x9B)

Bit	Mnemonic	Default	Description
7 to 0	SPI2CRx	0	SPI or I²C Receive Buffer. When SPI2CRx SFR is read, one byte from the receive FIFO output is transferred to the SPI2CRx SFR. A new data byte from the SPI or I²C bus is written to the FIFO input.

Table 129. SPI Configuration SFR 1 (SPIMOD1, 0xE8)

Bit	Address	Mnemonic	Default	Description	
7 to 6	0xEF to 0xEE	Reserved	0	Reserved.	
5	0xED	INTMOD	0	SPI Interrupt Mode.	
				INTMOD	**Result**
				0	SPI interrupt is set when SPI Rx buffer is full.
				1	SPI interrupt is set when SPI Tx buffer is empty.
4	0xEC	AUTO_SS	1	Master Mode, $\overline{SS}$ Output Control (see Figure 95).	
				AUTO_SS	**Result**
				0	The $\overline{SS}$ pin is held low while this bit is cleared. This allows manual chip select control using the $\overline{SS}$ pin.
				1	Single Byte Read or Write. The $\overline{SS}$ pin goes low during a single byte transmission and then returns high. Continuous Transfer. The $\overline{SS}$ pin goes low during the duration of the multibyte continuous transfer and then returns high.
3	0xEB	SS_EN	0	Slave Mode, $\overline{SS}$ Input Enable.	
				When this bit is set to Logic 1, the $\overline{SS}$ pin is defined as the slave select input pin for the SPI slave interface.	
2	0xEA	RxOFW	0	Receive Buffer Overflow Write Enable.	
				RxOFW	**Result**
				0	If the SPI2CRx SFR has not been read when a new data byte is received, the new byte is discarded.
				1	If the SPI2CRx SFR has not been read when a new data byte is received, the new byte overwrites the old data.
1 to 0	0xE9 to0xE8	SPIR[1:0]	0	Master Mode, SPI SCLK Frequency.	
				SPIR[1:0]	**Result**
				00	$f_{CORE}/8$ = 512 kHz (if f_{CORE} = 4.096 MHz).
				01	$f_{CORE}/16$ = 256 kHz (if f_{CORE} = 4.096 MHz).
				10	$f_{CORE}/32$ = 128 kHz (if f_{CORE} = 4.096 MHz).
				11	$f_{CORE}/64$ = 64 kHz (if f_{CORE} = 4.096 MHz).

Table 130. SPI Configuration SFR 2 (SPIMOD2, 0xE9)

Bit	Mnemonic	Default	Description	
7	SPICONT	0	Master Mode, SPI Continuous Transfer Mode Enable Bit.	
			SPICONT	**Result**
			0	The SPI interface stops after one byte is transferred and $\overline{SS}$ is deasserted. A new data transfer can be initiated after a stalled period.
			1	The SPI interface continues to transfer data until no valid data is available in the SPI2CTx SFR. $\overline{SS}$ remains asserted until the SPI2CTx SFR and the transmit shift registers are empty.
6	SPIEN	0	SPI Interface Enable Bit.	
			SPIEN	**Result**
			0	The SPI interface is disabled.
			1	The SPI interface is enabled.
5	SPIODO	0	SPI Open-Drain Output Configuration Bit.	
			SPIODO	**Result**
			0	Internal pull-up resistors are connected to the SPI outputs.
			1	The SPI outputs are open drain and need external pull-up resistors. The pull-up voltage should not exceed the specified operating voltage.
4	SPIMS_b	0	SPI Master Mode Enable Bit.	
			SPIMS_b	**Result**
			0	The SPI interface is defined as a slave.
			1	The SPI interface is defined as a master.
3	SPICPOL	0	SPI Clock Polarity Configuration Bit (see Figure 97).	
			SPICPOL	**Result**
			0	The default state of SCLK is low, and the first SCLK edge is rising. Depending on the SPICPHA bit, the SPI data output changes state on the falling or rising edge of SCLK while the SPI data input is sampled on the rising or falling edge of SCLK.
			1	The default state of SCLK is high, and the first SCLK edge is falling. Depending on the SPICPHA bit, the SPI data output changes state on the rising or falling edge of SCLK while the SPI data input is sampled on the falling or rising edge of SCLK.
2	SPICPHA	0	SPI Clock Phase Configuration Bit (see Figure 97).	
			SPICPHA	**Result**
			0	The SPI data output changes state when $\overline{SS}$ goes low at the second edge of SCLK and then every two subsequent edges, whereas the SPI data input is sampled at the first SCLK edge and then every two subsequent edges.
			1	The SPI data output changes state at the first edge of SCLK and then every two subsequent edges, whereas the SPI data input is sampled at the second SCLK edge and then every two subsequent edges.
1	SPILSBF	0	Master Mode, LSB First Configuration Bit.	
			SPILSBF	**Result**
			0	The MSB of the SPI outputs is transmitted first.
			1	The LSB of the SPI outputs is transmitted first.
0	TIMODE	1	Transfer and Interrupt Mode of the SPI Interface.	
			TIMODE	**Result**
			1	This bit must be left set for proper operation.

Table 131. SPI Interrupt Status SFR (SPISTAT, 0xEA)

Bit	Mnemonic	Default	Description		
7	BUSY	0	SPI Peripheral Busy Flag.		
			BUSY	**Result**	
			0	The SPI peripheral is idle.	
			1	The SPI peripheral is busy transferring data in slave or master mode.	
6	MMERR	0	SPI Multimaster Error Flag.		
			MMERR	**Result**	
			0	A multiple master error has not occurred.	
			1	If the SS_EN bit is set, enabling the slave select input and asserting the $\overline{SS}$ pin while the SPI peripheral is transferring data as a master, this flag is raised to indicate the error. Write a 0 to this bit to clear it.	
5	SPIRxOF	0	SPI Receive Overflow Error Flag. Reading the SPI2CRx SFR clears this bit.		
			SPIRxOF	**TIMODE**	**Result**
			0	X	The SPI2CRx register contains valid data.
			1	1	This bit is set if the SPI2CRx register is not read before the end of the next byte transfer. If the RxOFW bit is set and this condition occurs, SPI2CRx is overwritten.
4	SPIRxIRQ	0	SPI Receive Mode Interrupt Flag. Reading the SPI2CRx SFR clears this bit.		
			SPIRxIRQ	**TIMODE**	**Result**
			0	X	The SPI2CRx register does not contain new data.
			1	0	This bit is set when the SPI2CRx register contains new data. If the SPI/I²C interrupt is enabled, an interrupt is generated when this bit is set. If the SPI2CRx register is not read before the end of the current byte transfer, the transfer stops and the $\overline{SS}$ pin is deasserted.
			1	1	The SPI2CRx register contains new data.
3	SPIRxBF	0	Status Bit for SPI Rx Buffer. When set, the Rx FIFO is full. A read of the SPI2CRx clears this flag.		
2	SPITxUF	0	Status Bit for SPI Tx Buffer. When set, the Tx FIFO is underflowing and data can be written into SPI2CTx. Write a 0 to this bit to clear it.		
1	SPITxIRQ	0	SPI Transmit Mode Interrupt Flag. Writing new data to the SPI2CTx SFR clears this bit.		
			SPITxIRQ	**TIMODE**	**Result**
			0	X	The SPI2CTx register is full.
			1	0	The SPI2CTx register is empty.
			1	1	This bit is set when the SPI2CTx register is empty. If the SPI/I²C interrupt is enabled, an interrupt is generated when this bit is set. If new data is not written into the SPI2CTx SFR before the end of the current byte transfer, the transfer stops, and the $\overline{SS}$ pin is deasserted. Write a 0 to this bit to clear it.
0	SPITxBF	0	Status Bit for SPI Tx Buffer. When set, the SPI Tx buffer is full. Write a 0 to this bit to clear it.		

SPI PINS

MISO (Master In, Slave Out Data I/O Pin)

The MISO pin is configured as an input line in master mode and as an output line in slave mode. The MISO line on the master (data in) should be connected to the MISO line in the slave device (data out). The data is transferred as byte-wide (8-bit) serial data, MSB first.

MOSI (Master Out, Slave In Pin)

The MOSI pin is configured as an output line in master mode and as an input line in slave mode. The MOSI line on the master (data out) should be connected to the MOSI line in the slave device (data in). The data is transferred as byte-wide (8-bit) serial data, MSB first.

SCLK (Serial Clock I/O Pin)

The master serial clock (SCLK) is used to synchronize the data being transmitted and received through the MOSI and MISO data lines. The SCLK pin is configured as an output in master mode and as an input in slave mode.

In master mode, the bit rate, polarity, and phase of the clock are controlled by the SPI Configuration SFR 1 (SPIMOD1, 0xE8) and SPI Configuration SFR 2 (SPIMOD2, 0xE9).

In slave mode, the SPI Configuration SFR 2 (SPIMOD2, 0xE9) must be configured with the phase and polarity of the expected input clock.

In both master and slave modes, the data is transmitted on one edge of the SCLK signal and sampled on the other. It is important, therefore, that the SPICPHA and SPICPOL bits be configured the same for the master and slave devices.

$\overline{SS}$ (Slave Select Pin)

In SPI slave mode, a transfer is initiated by the assertion of $\overline{SS}$ low. The SPI port then transmits and receives 8-bit data until the data is concluded by the deassertion of $\overline{SS}$ according to the SPICON bit setting. In slave mode, $\overline{SS}$ is always an input.

In SPI master mode, the $\overline{SS}$ can be used to control data transfer to a slave device. In automatic slave select control mode, the $\overline{SS}$ is asserted low to select the slave device and then raised to deselect the slave device after the transfer is complete. Automatic slave select control is enabled by setting the AUTO_SS bit in the SPI Configuration SFR 1 (SPIMOD1, 0xE8).

In a multimaster system, the $\overline{SS}$ can be configured as an input so that the SPI peripheral can operate as a slave in some situations and as a master in others. In this case, the slave selects for the slaves that are controlled by this SPI peripheral should be generated with general I/O pins.

SPI MASTER OPERATING MODES

The double-buffered receive and transmit registers can be used to maximize the throughput of the SPI peripheral by continuously streaming out data in master mode. Continuous transmit mode is designed to use the full capacity of the SPI. In this mode, the master transmits and receives data until the SPI/I²C Transmit Buffer SFR (SPI2CTx, 0x9A) is empty at the start of a byte transfer. Continuous mode is enabled by setting the SPICONT bit in the SPI Configuration SFR 2 (SPIMOD2, 0xE9). The SPI peripheral also offers a single byte read/write function.

In master mode, the type of transfer is handled automatically, depending on the configuration of the SPICONT bit in the SPI Configuration SFR 2 (SPIMOD2, 0xE9). The following procedures show the sequence of events that should be performed for each master operating mode. Based on the $\overline{SS}$ configuration, some of these events take place automatically.

Procedures for Using SPI as a Master

Single Byte Mode—SPICONT (SPIMOD2[7]) = 0

1. Write to SPI2CTx SFR.
2. $\overline{SS}$ is asserted low and a write routine is initiated.
3. SPITxIRQ interrupt flag is set when the SPI2CTx register is empty.
4. $\overline{SS}$ is deasserted high.
5. Write to SPI2CTx SFR to clear the SPITxIRQ interrupt flag.

Continuous Byte Mode—SPICONT (SPIMOD2[7]) = 1

1. Write to SPI2CTx SFR.
2. $\overline{SS}$ is asserted low and write routine is initiated.
3. Wait for the SPITxIRQ interrupt flag to write to SPI2CTx SFR. Transfer continues until the SPI2CTx register and transmit shift registers are empty.
4. SPITxIRQ interrupt flag is set when the SPI2CTx register is empty.
5. $\overline{SS}$ is deasserted high.
6. Write to SPI2CTx SFR to clear the SPITxIRQ interrupt flag.

Figure 95 shows the SPI output for certain automatic chip select and continuous mode selections. Note that if the continuous mode is not used, a short delay is inserted between transfers.

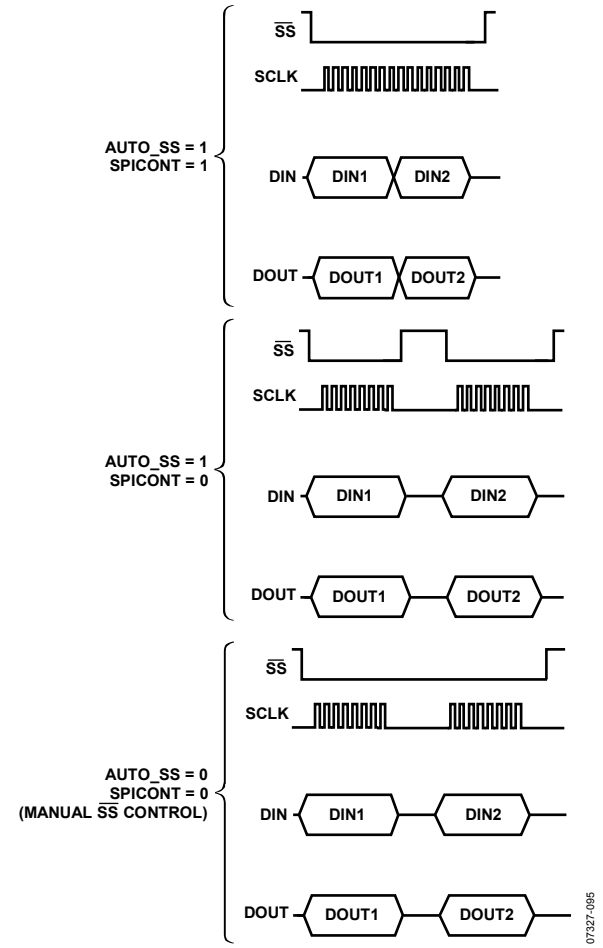


Figure 95. Automatic Chip Select and Continuous Mode Output

Note that reading the content of the SPI/I²C Receive Buffer SFR (SPI2CRx, 0x9B) should be done using a 2-cycle instruction set, such as MOV A or SPI2CRX. Using a 3-cycle instruction, such as MOV 0x3D or SPI2CRX, does not transfer the correct information into the target register.

SPI INTERRUPT AND STATUS FLAGS

The SPI interface has several status flags that indicate the status of the double-buffered receive and transmit registers. Figure 96 shows when the status and interrupt flags are raised. The transmit interrupt occurs when the transmit shift register is loaded with the data in the SPI/I²C Transmit Buffer SFR (SPI2CTx, 0x9A). If the SPI master is in transmit operating mode, and the SPI/I²C Transmit Buffer SFR (SPI2CTx, 0x9A) register has not been written with new data by the beginning of the next byte transfer, the transmit operation stops.

When a new byte of data is received in the SPI/I²C Receive Buffer SFR (SPI2CRx, 0x9B), the SPI receive interrupt flag is raised. If the data in the SPI/I²C Receive Buffer SFR (SPI2CRx, 0x9B) is not read before new data is ready to be loaded into the SPI/I²C Receive Buffer SFR (SPI2CRx, 0x9B), an overflow condition has occurred. This overflow condition, indicated by the SPIRxOF flag, forces the new data to be discarded or overwritten if the RxOFW bit is set.

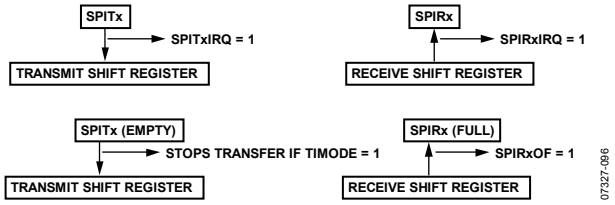


Figure 96. SPI Receive and Transmit Interrupt and Status Flags

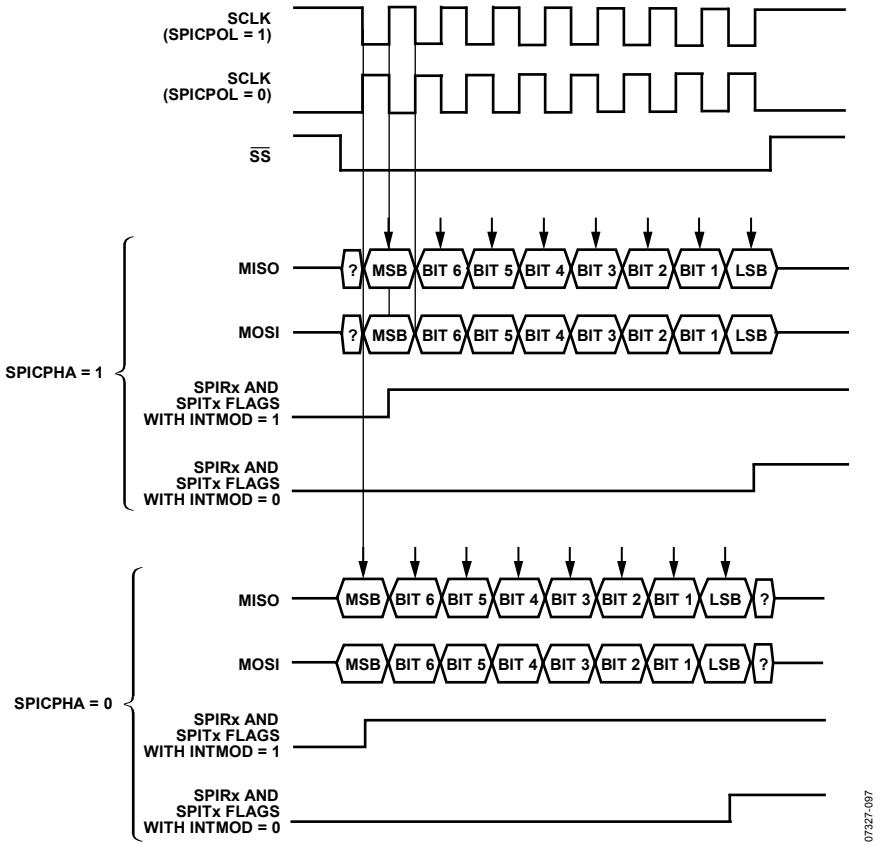


Figure 97. SPI Timing Configurations

I²C-COMPATIBLE INTERFACE

The ADE7518 supports a fully licensed I²C interface. The I²C interface is implemented as a full hardware master.

SDATA is the data I/O pin, and SCLK is the serial clock. These two pins are shared with the MOSI and SCLK pins of the on-chip SPI interface. Therefore, the user can enable only one interface on these pins at any given time. The SCPS bit in the Configuration SFR (CFG, 0xAF) selects which peripheral is active.

The two pins used for data transfer, SDATA and SCLK, are configured in a wire-AND format that allows arbitration in a multimaster system.

The transfer sequence of an I²C system consists of a master device initiating a transfer by generating a start condition while the bus is idle. The master transmits the address of the slave device and the direction of the data transfer in the initial address transfer. If the slave acknowledges the start condition, the data transfer is initiated. This continues until the master issues a stop condition and the bus becomes idle.

SERIAL CLOCK GENERATION

The I²C master in the system generates the serial clock for a transfer. The master channel can be configured to operate in fast mode (256 kHz) or standard mode (32 kHz).

The bit rate is defined in the I2CMOD SFR as follows:

$$f_{SCLK} = \frac{f_{CORE}}{16 \times 2^{I2CR[1:0]}}$$

SLAVE ADDRESSES

The I²C Slave Address SFR (I2CADR, 0xE9) contains the slave device ID. The LSB of this register contains a read/write request. A write to this SFR starts the I²C communication.

I²C REGISTERS

The I²C peripheral interface consists of five SFRs.

- I2CMOD
- SPI2CSTAT
- I2CADR
- SPI2CTx
- SPI2CRx

Because the SPI and I²C serial interfaces share the same pins, they also share the same SFRs, such as the SPI2CTx and SPI2CRx SFRs. In addition, the I2CMOD, I2CADR, and SPI2CSTAT SFRs are shared with the SPIMOD1, SPIMOD2, and SPISTAT SFRs, respectively.

Table 132. I²C SFR List

SFR Address	Name	R/W	Length	Default	Description
0x9A	SPI2CTx	W	8	0	SPI/I²C Transmit Buffer (see Table 127).
0x9B	SPI2CRx	R	8	0	SPI/I²C Receive Buffer (see Table 128).
0xE8	I2CMOD	R/W	8	0	I²C Mode (see Table 133).
0xE9	I2CADR	R/W	8	0	I²C Slave Address (see Table 134).
0xEA	SPI2CSTAT	R/W	8	0	I²C Interrupt Status Register (see Table 135).

Table 133. I²C Mode SFR (I2CMOD, 0xE8)

Bit	Address	Mnemonic	Default	Description	
7	0xEF	I2CEN	0	I²C Enable Bit. When this bit is set to Logic 1, the I²C interface is enabled. A write to the I2CADR SFR starts a communication.	
6 to 5	0xEE to 0xED	I2CR[1:0]	00	I²C SCLK Frequency.	
				I2CR[1:0]	**Result**
				00	f_{CORE}/16 = 256 kHz if f_{CORE} = 4.096 MHz.
				01	f_{CORE}/32 = 128 kHz if f_{CORE} = 4.096 MHz.
				10	f_{CORE}/64 = 64 Hz if f_{CORE} = 4.096 MHz.
				11	f_{CORE}/128 = 32 kHz if f_{CORE} = 4.096 MHz.
4 to 0	0xEC to 0xE8	I2CRCT[4:0]	0	Configures the length of the I²C received FIFO buffer. The I²C peripheral stops when I2CRCT, Bits[4:0] + 1 byte have been read or if an error occurs.	

Table 134. I²C Slave Address SFR (I2CADR, 0xE9)

Bit	Mnemonic	Default	Description
7 to 1	I2CSLVADR	0	Address of the I²C Slave Being Addressed. Writing to this register starts the I²C transmission (read or write).
0	I2CR_W	0	Command Bit for Read or Write. When this bit is set to Logic 1, a read command is transmitted on the I²C bus. Data from the slave in the SPI2CRx SFR is expected after a command byte. When this bit is set to Logic 0, a write command is transmitted on the I²C bus. Data to slave is expected in the SPI2CTx SFR.

Table 135. I²C Interrupt Status Register SFR (SPI2CSTAT, 0xEA)

Bit	Mnemonic	Default	Description
7	I2CBUSY	0	This bit is set to Logic 1 when the I²C interface is used. When this bit is set, the Tx FIFO is emptied.
6	I2CNOACK	0	I²C No Acknowledgement Transmit Interrupt. This bit is set to Logic 1 when the slave device does not send an acknowledgement. The I²C communication is stopped after this event. Write a 0 to this bit to clear it.
5	I2CRxIRQ	0	I²C Receive Interrupt. This bit is set to Logic 1 when the receive FIFO is not empty. Write a 0 to this bit to clear it.
4	I2CTxIRQ	0	I²C Transmit Interrupt. This bit is set to Logic 1 when the transmit FIFO is empty. Write a 0 to this bit to clear it.
3 to 2	I2CFIFOSTAT[1:0]	00	Status Bits for 3- or 4-Byte Deep I²C FIFO. The FIFO monitored in these two bits is the one currently used in I²C communication (receive or transmit) because only one FIFO is active at a time.
			I2CFIFOSTAT[1:0] / **Result**
			00 / FIFO empty
			01 / Reserved
			10 / FIFO half full
			11 / FIFO full
1	I2CACC_ERR	0	Set when trying to write and read at the same time. Write a 0 to this bit to clear it.
0	I2CTxWR_ERR	0	Set when write was attempted when I²C transmit FIFO was full. Write a 0 to this bit to clear it.

READ AND WRITE OPERATIONS

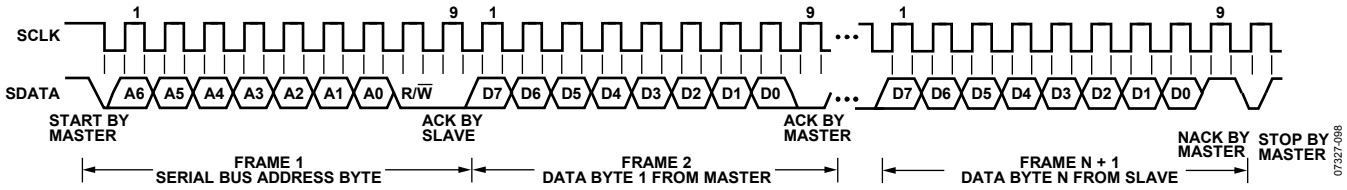


Figure 98. I²C Read Operation

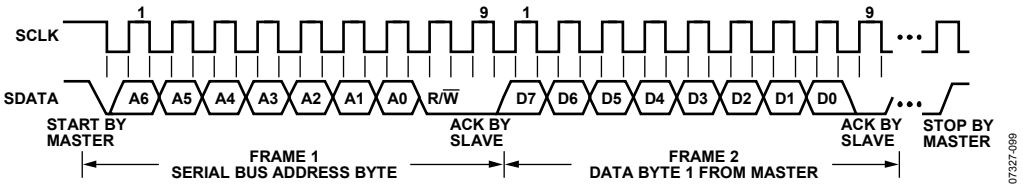


Figure 99. I²C Write Operation

Figure 98 and Figure 99 depict I²C read and write operations, respectively. Note that the LSB of the I2CADR register is used to select whether a read or write operation is performed on the slave device. During the read operation, the master acknowledges are generated automatically by the I²C peripheral. The master-generated NACK (no acknowledge) before the end of a read operation is also automatically generated after the I2CRCT, Bits[4:0] have been read from the slave. If the I2CADR register is updated during a transmission, instead of generating a stop at the end of the read or write operation, the master generates a start condition and continues with the next communication.

Reading the SPI/I²C Receive Buffer SFR (SPI2CRx, 0x9B)

Reading the SPI2CRx SFR should be done with a 2-cycle instruction, such as

```
Mov a, spi2crx or Mov R0, spi2crx.
```

A 3-cycle instruction such as

```
Mov 3dh, spi2crx
```

does not transfer the right data into RAM Address 0x3D.

I²C RECEIVE AND TRANSMIT FIFOS

The I²C peripheral has a 4-byte receive FIFO and a 4-byte transmit FIFO. The buffers reduce the overhead associated with using the I²C peripheral. Figure 100 shows the operation of the I²C receive and transmit FIFOs.

The Tx FIFO can be loaded with four bytes to be transmitted to the slave at the beginning of a write operation. When the transmit FIFO is empty, the I²C transmit interrupt flag is set, and the PC vectors to the I²C interrupt vector if this interrupt is enabled. If a new byte is not loaded into the Tx FIFO before it is needed in the transmit shift register, the communication stops. An error, such as not receiving an acknowledge, also causes the communication to terminate. In case of an error during a write operation, the Tx FIFO is flushed.

The Rx FIFO allows four bytes to be read in from the slave before the MCU has to read the data. A receive interrupt can be generated after each byte is received or when the Rx FIFO is full. If the peripheral is reading from a slave address, the communication stops once the number of received bytes equals the number set in I2CRCT, Bits [4:0]. An error, such as not receiving an acknowledge, also causes the communication to terminate.

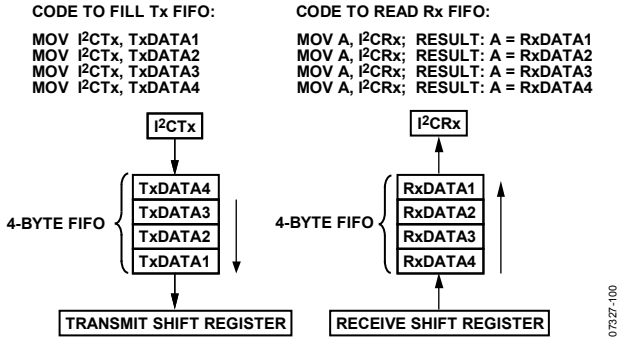


Figure 100. I²C FIFO Operation

I/O PORTS

PARALLEL I/O

The ADE7518 uses three input/output ports to exchange data with external devices. In addition to performing general-purpose I/O, some are capable of driving an LCD or performing alternate functions for the peripherals available on-chip. In general, when a peripheral is enabled, the pins associated with it cannot be used as a general-purpose I/O. The I/O port can be configured through the SFRs listed in Table 136.

Table 136. I/O Port SFRs

SFR	Address	Bit Addressable	Description
P0	0x80	Yes	Port 0.
P1	0x90	Yes	Port 1.
P2	0xA0	Yes	Port 2.
EPCFG	0x9F	No	Extended Port Configuration.
PINMAP0	0xB2	No	Port 0 Weak Pull-Up Enable.
PINMAP1	0xB3	No	Port 1 Weak Pull-Up Enable.
PINMAP2	0xB4	No	Port 2 Weak Pull-Up Enable.

The three bidirectional I/O ports have internal pull-ups that can be enabled or disabled individually for each pin. The internal pull-ups are enabled by default. Disabling an internal pull-up causes a pin to become open drain. Weak internal pull-ups are configured through the PINMAPx SFRs.

Figure 101 shows a typical bit latch and I/O buffer for an I/O pin. The bit latch (one bit in each port's SFR) is represented as a Type D flip-flop, which clocks in a value from the internal bus in response to a write-to-latch signal from the CPU. The Q output of the flip-flop is placed on the internal bus in response to a read latch signal from the CPU. The level of the port pin itself is placed on the internal bus in response to a read pin signal from the CPU. Some instructions that read a port activate the read latch signal, and others activate the read pin signal. See the Read-Modify-Write Instructions section for details.

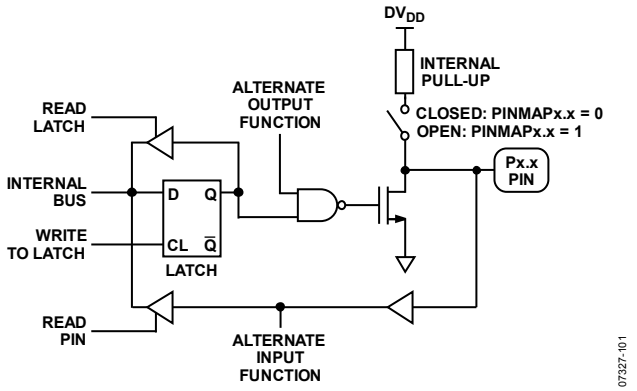


Figure 101. Port 0 Bit Latch and I/O Buffer

Weak Internal Pull-Ups Enabled

A pin with weak internal pull-up enabled is used as an input by writing a 1 to the pin. The pin is pulled high by the internal pull-ups, and the pin is read using the circuitry shown in Figure 101. If the pin is driven low externally, it sources current because of the internal pull-ups.

A pin with internal pull-up enabled is used as an output by writing a 1 or a 0 to the pin to control the level of the output. If a 0 is written to the pin, it drives a logic low output voltage (V_{OL}) and is capable of sinking 1.6 mA.

Open Drain (Weak Internal Pull-Ups Disabled)

When the weak internal pull-up on a pin is disabled, the pin becomes open drain. Use this open-drain pin as a high impedance input by writing a 1 to the pin. The pin is read using the circuitry shown in Figure 101. The open-drain option is preferable for inputs because it draws less current than the internal pull-ups that were enabled.

38 kHz Modulation

The ADE7518 provides a 38 kHz modulation signal. The 38 kHz modulation is accomplished by internally XOR'ing the level written to the I/O pin with a 38 kHz square wave. Then, when a 0 is written to the I/O pin, it is modulated as shown in Figure 102.

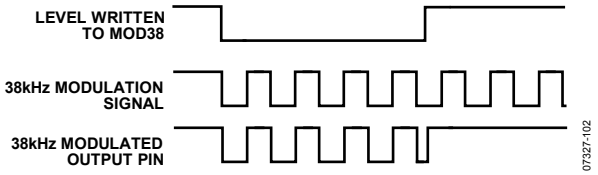


Figure 102. 38 kHz Modulation

Uses for this 38 kHz modulation include IR modulation of a UART transmit signal or a low power signal to drive an LED. The modulation can be enabled or disabled with the MOD38EN bit in the CFG SFR. The 38 kHz modulation is available on eight pins, selected by the MOD38[7:0] bits in the Extended Port Configuration SFR (EPCFG, 0x9F).

I/O REGISTERS

Table 137. Extended Port Configuration SFR (EPCFG, 0x9F)

Bit	Mnemonic	Default	Description
7	MOD38_FP21	0	Enable 38 kHz modulation on P1.6/FP21 pin.
6	MOD38_FP22	0	Enable 38 kHz modulation on P1.5/FP22 pin.
5	MOD38_FP23	0	Enable 38 kHz modulation on P1.4/T2/FP23 pin.
4	MOD38_TxD	0	Enable 38 kHz modulation on P1.1/TxD pin.
3	MOD38_CF1	0	Enable 38 kHz modulation on P0.2/CF1/RTCCAL pin.
2	MOD38_SSb	0	Enable 38 kHz modulation on P0.7/$\overline{SS}$/T1 pin.
1	MOD38_MISO	0	Enable 38 kHz modulation on P0.5/MISO pin.
0	MOD38_CF2	0	Enable 38 kHz modulation on P0.3/CF2 pin.

Table 138. Port 0 Weak Pull-Up Enable SFR (PINMAP0, 0xB2)

Bit	Mnemonic	Default	Description
7	PINMAP0.7	0	The weak pull-up on P0.7 is disabled when this bit is set.
6	PINMAP0.6	0	The weak pull-up on P0.6 is disabled when this bit is set.
5	PINMAP0.5	0	The weak pull-up on P0.5 is disabled when this bit is set.
4	PINMAP0.4	0	The weak pull-up on P0.4 is disabled when this bit is set.
3	PINMAP0.3	0	The weak pull-up on P0.3 is disabled when this bit is set.
2	PINMAP0.2	0	The weak pull-up on P0.2 is disabled when this bit is set.
1	PINMAP0.1	0	The weak pull-up on P0.1 is disabled when this bit is set.
0	PINMAP0.0	0	The weak pull-up on P0.0 is disabled when this bit is set.

Table 139. Port 1 Weak Pull-Up Enable SFR (PINMAP1, 0xB3)

Bit	Mnemonic	Default	Description
7	PINMAP1.7	0	The weak pull-up on P1.7 is disabled when this bit is set.
6	PINMAP1.6	0	The weak pull-up on P1.6 is disabled when this bit is set.
5	PINMAP1.5	0	The weak pull-up on P1.5 is disabled when this bit is set.
4	PINMAP1.4	0	The weak pull-up on P1.4 is disabled when this bit is set.
3	PINMAP1.3	0	The weak pull-up on P1.3 is disabled when this bit is set.
2	PINMAP1.2	0	The weak pull-up on P1.2 is disabled when this bit is set.
1	PINMAP1.1	0	The weak pull-up on P1.1 is disabled when this bit is set.
0	PINMAP1.0	0	The weak pull-up on P1.0 is disabled when this bit is set.

Table 140. Port 2 Weak Pull-Up Enable SFR (PINMAP2, 0xB4)

Bit	Mnemonic	Default	Description
7 to 6	Reserved	0	Reserved. Should be left cleared.
5	PINMAP2.5	0	The weak pull-up on $\overline{RESET}$ is disabled when this bit is set.
4	Reserved	0	Reserved. Should be left cleared.
3	PINMAP2.3	0	Reserved. Should be left cleared.
2	PINMAP2.2	0	The weak pull-up on P2.2 is disabled when this bit is set.
1	PINMAP2.1	0	The weak pull-up on P2.1 is disabled when this bit is set.
0	PINMAP2.0	0	The weak pull-up on P2.0 is disabled when this bit is set.

Table 141. Port 0 SFR (P0, 0x80)

Bit	Address	Mnemonic	Default	Description[1]
7	0x87	T1	1	This bit reflects the state of the P0.7/$\overline{SS}$/T1 pin. It can be written or read.
6	0x86	T0	1	This bit reflects the state of the P0.6/SCLK/T0 pin. It can be written or read.
5	0x85		1	This bit reflects the state of the P0.5/MISO pin. It can be written or read.
4	0x84		1	This bit reflects the state of the P0.4/MOSI/SDATA pin. It can be written or read.
3	0x83	CF2	1	This bit reflects the state of the P0.3/CF2 pin. It can be written or read.
2	0x82	CF1	1	This bit reflects the state of the P0.2/CF1/RTCCAL pin. It can be written or read.
1	0x81		1	This bit reflects the state of the P0.1/FP19 pin. It can be written or read.
0	0x80	$\overline{INT1}$	1	This bit reflects the state of the BCTRL/$\overline{INT1}$/P0.0 pin. It can be written or read.

[1] When an alternate function is chosen for a pin of this port, the bit controlling this pin should always be set.

Table 142. Port 1 SFR (P1, 0x90)

Bit	Address	Mnemonic	Default	Description[1]
7	0x97		1	This bit reflects the state of the P1.7/FP20 pin. It can be written or read.
6	0x96		1	This bit reflects the state of the P1.6/FP21 pin. It can be written or read.
5	0x95		1	This bit reflects the state of the P1.5/FP22 pin. It can be written or read.
4	0x94	T2	1	This bit reflects the state of the P1.4/T2/FP23 pin. It can be written or read.
3	0x93	T2EX	1	This bit reflects the state of the P1.3/T2EX/FP24 pin. It can be written or read.
2	0x92		1	This bit reflects the state of the P1.2/FP25 pin. It can be written or read.
1	0x91	TxD	1	This bit reflects the state of the P1.1/TxD pin. It can be written or read.
0	0x90	RxD	1	This bit reflects the state of the P1.0/RxD pin. It can be written or read.

[1] When an alternate function is chosen for a pin of this port, the bit controlling this pin should always be set.

Table 143. Port 2 SFR (P2, 0xA0)

Bit	Address	Mnemonic	Default	Description[1]
7 to 4	0x97 to 0x94		0x1F	These bits are unused and should remain set.
3	0x93	P2.3	1	This bit reflects the state of the SDEN/P2.3 pin. It can be written only.
2	0x92	P2.2	1	This bit reflects the state of the P2.2/FP16 pin. It can be written or read.
1	0x91	P2.1	1	This bit reflects the state of the P2.1/FP17 pin. It can be written or read.
0	0x90	P2.0	1	This bit reflects the state of the P2.0/FP18 pin. It can be written or read.

[1] When an alternate function is chosen for a pin of this port, the bit controlling this pin should always be set.

Table 144. Port 0 Alternate Functions

Pin No.	Alternate Function	Alternate Function Enable
P0.0	BCTRL External Battery Control Input	Set INT1PRG[2:0] = x01 in the Interrupt Pins Configuration SFR (INTPR, 0xFF).
	$\overline{\text{INT1}}$ External Interrupt	Set EX1 in the Interrupt Enable SFR (IE, 0xA8).
	$\overline{\text{INT1}}$ Wake-up from PSM2 Operating Mode	Set INT1PRG[2:0] = 11x in the Interrupt Pins Configuration SFR (INTPR, 0xFF).
P0.1	FP19 LCD Segment Pin	Set FP19EN in the LCD Segment Enable 2 SFR (LCDSEGE2, 0xED).
P0.2	CF1 ADE Calibration Frequency Output	Clear the DISCF1 bit in the ADE energy measurement internal MODE1 register (0x0B).
P0.3	CF2 ADE Calibration Frequency Output	Clear the DISCF2 bit in the ADE energy measurement internal MODE1 register (0x0B).
P0.4	MOSI SPI Data Line	Set the SCPS bit in the Configuration SFR (CFG, 0xAF) and set the SPIEN bit in the SPI Configuration SFR 2 (SPIMOD2, 0xE9).
	SDATA I^2C Data Line	Clear the SCPS bit in the Configuration SFR (CFG, 0xAF) and set the I2CEN bit in the I^2C Mode SFR (I2CMOD, 0xE8).
P0.5	MISO SPI Data Line	Set the SCPS bit in the Configuration SFR (CFG, 0xAF) and set the SPIEN bit in the SPI Configuration SFR 2 (SPIMOD2, 0xE9).
P0.6	SCLK Serial Clock for I^2C or SPI	Set the I2CEN bit in the I^2C Mode SFR (I2CMOD, 0xE8) or the SPIEN bit in the SPI Configuration SFR 2 (SPIMOD2, 0xE9) to enable the I^2C or SPI interface.
	T0 Timer 0 Input	Set the C/$\overline{\text{T0}}$ bit in the Timer/Counter 0 and Timer/Counter 1 Mode SFR (TMOD, 0x89) to enable T0 as an external event counter.
P0.7	$\overline{\text{SS}}$ SPI Slave Select Input for SPI in Slave Mode	Set the SS_EN bit in the SPI Configuration SFR 1 (SPIMOD1, 0xE8).
	$\overline{\text{SS}}$ SPI Slave Select Output for SPI in Master Mode	Set the SPIMS_b bit in the SPI Configuration SFR 2 (SPIMOD2, 0xE9).
	T1 Timer 1 Input	Set the C/$\overline{\text{T1}}$ bit in the Timer/Counter 0 and Timer/Counter 1 Mode SFR (TMOD, 0x89) to enable T1 as an external event counter.

Table 145. Port 1 Alternate Functions

Pin No.	Alternate Function	Alternate Function Enable
P1.0	RxD Receiver Data Input for UART	Set the REN bit in the Serial Communications Control Register SFR (SCON, 0x98).
	Rx Edge Wake-up from PSM2 Operating Mode	Set RXPROG[1:0] = 11 in the Peripheral Configuration SFR (PERIPH, 0xF4).
P1.1	TxD Transmitter Data Output for UART	This pin becomes TxD as soon as data is written into SBUF.
P1.2	FP25 LCD Segment Pin	Set FP25EN in the LCD Segment Enable SFR (LCDSEGE, 0x97).
P1.3	FP24 LCD Segment Pin	Set FP24EN in the LCD Segment Enable SFR (LCDSEGE, 0x97).
	T2EX Timer 2 Control Input	Set EXEN2 in the Timer/Counter 2 Control SFR (T2CON, 0xC8).
P1.4	FP23 LCD Segment Pin	Set FP23EN in the LCD Segment Enable SFR (LCDSEGE, 0x97).
	T2 Timer 2 Input	Set the C/$\overline{\text{T2}}$ bit in the Timer/Counter 2 Control SFR (T2CON, 0xC8) to enable T2 as an external event counter.
P1.5	FP22 LCD Segment Pin	Set FP22EN in the LCD Segment Enable SFR (LCDSEGE, 0x97).
P1.6	FP21 LCD Segment Pin	Set FP21EN in the LCD Segment Enable SFR (LCDSEGE, 0x97).
P1.7	FP20 LCD Segment Pin	Set FP20EN in the LCD Segment Enable SFR (LCDSEGE, 0x97).

Table 146. Port 2 Alternate Functions

Pin No.	Alternate Function	Alternate Function Enable
P2.0	FP18 LCD Segment Pin	Set FP18EN in the LCD Segment Enable 2 SFR (LCDSEGE2, 0xED).
P2.1	FP17 LCD Segment Pin	Set FP17EN in the LCD Segment Enable 2 SFR (LCDSEGE2, 0xED).
P2.2	FP16 LCD Segment Pin	Set FP16EN in the LCD Segment Enable 2 SFR (LCDSEGE2, 0xED).
P2.3	$\overline{\text{SDEN}}$ serial download pin sampled on reset. P2.3 is an output only.	Enabled by default.

PORT 0

Port 0 is controlled directly through the bit-addressable Port 0 SFR (P0, 0x80). The weak internal pull-ups for Port 0 are configured through the Port 0 Weak Pull-Up Enable SFR (PINMAP0, 0xB2); they are enabled by default. The weak internal pull-up is disabled by writing a 1 to PINMAP0.x.

Port 0 pins also have various secondary functions as described in Table 144. The alternate functions of Port 0 pins can be activated only if the corresponding bit latch in the Port 0 SFR contains a 1. Otherwise, the port pin remains at 0.

PORT 1

Port 1 is an 8-bit bidirectional port controlled directly through the bit-addressable Port 1 SFR (P1, 0x90). The weak internal pull-ups for Port 1 are configured through the Port 1 Weak Pull-Up Enable SFR (PINMAP1, 0xB3); they are enabled by default. The weak internal pull-up is disabled by writing a 1 to PINMAP1.x.

Port 1 pins also have various secondary functions as described in Table 145. The alternate functions of Port 1 pins can be activated only if the corresponding bit latch in the Port 1 SFR contains a 1. Otherwise, the port pin remains at 0.

PORT 2

Port 2 is a 4-bit bidirectional port controlled directly through the bit-addressable Port 2 SFR (P2, 0xA0). Note that P2.3 can be used as an output only. Consequently, any read operation, such as a CPL P2.3, cannot be executed on this I/O. The weak internal pull-ups for Port 2 are configured through the Port 2 Weak Pull-Up Enable SFR (PINMAP2, 0xB4); they are enabled by default. The weak internal pull-up is disabled by writing a 1 to PINMAP2.x.

Port 2 pins also have various secondary functions as described in Table 146. The alternate functions of Port 2 pins can be activated only if the corresponding bit latch in the Port 2 SFR contains a 1. Otherwise, the port pin remains at 0.

DETERMINING THE VERSION OF THE ADE7518

The ADE7518 holds in its internal flash registers a value that defines its version. This value helps to determine if users have the latest version of the part. The ADE7518 version corresponding to this data sheet is ADE7518V3.4.

To access this value, the following procedure can be followed:

1. Launch HyperTerminal with a 9600 baud rate.
2. Put the part in serial download mode by first holding $\overline{\text{SDEN}}$ to logic low and then resetting the part.
3. Hold the $\overline{\text{SDEN}}$ pin.
4. Press and release the $\overline{\text{RESET}}$ pin.
5. The following string should appear on the HyperTerminal screen: ADE7518V3.4

OUTLINE DIMENSIONS

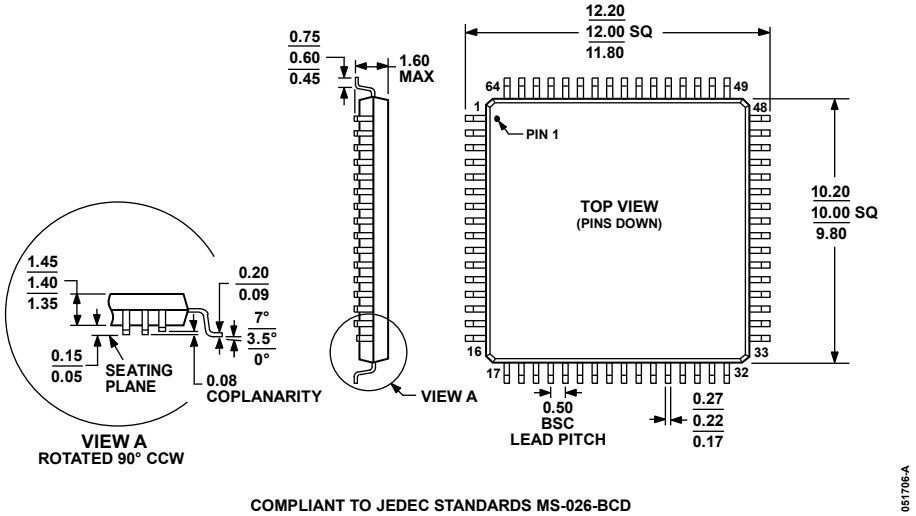


Figure 103. 64-Lead Low Profile Quad Flat Package [LQFP]
(ST-64-2)
Dimensions shown in millimeters

ORDERING GUIDE

Model	Antitamper	di/dt Sensor Interface	VAR	Flash (kB)	Temperature Range	Package Description	Package Option
ADE7518ASTZF8[1]	No	No	Yes	8	−40°C to +85°C	64-Lead LQFP	ST-64-2
ADE7518ASTZF8-RL[1]	No	No	Yes	8	−40°C to +85°C	64-Lead LQFP, Reel	ST-64-2
ADE7518ASTZF16[1]	No	No	Yes	16	−40°C to +85°C	64-Lead LQFP	ST-64-2
ADE7518ASTZF16-RL[1]	No	No	Yes	16	−40°C to +85°C	64-Lead LQFP, Reel	ST-64-2

[1] Z = RoHS Compliant Part.

NOTES

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