Spread Aware™, Ten/Eleven Output Zero Delay Buffer

Features

- **Spread Aware™—designed to work with SSFTG reference signals**
- **Well suited to both 100- and 133-MHz designs**
- **Ten (CY2509) or eleven (CY2510) LVCMOS/LVTTL outputs**
- **50 ps typical peak cycle-to-cycle jitter**
- **Single output enable pin for CY2510 version, dual pins on CY2509 devices allow shutting down a portion of the outputs**
- **3.3V power supply**
- **On board 25Ω damping resistors**
- **Available in 24-pin TSSOP package**
- **Improved tracking skew, but narrower frequency support limit when compared to W132-09B/10B**

Key Specifications

Operating Voltage: .....3.3V±10%

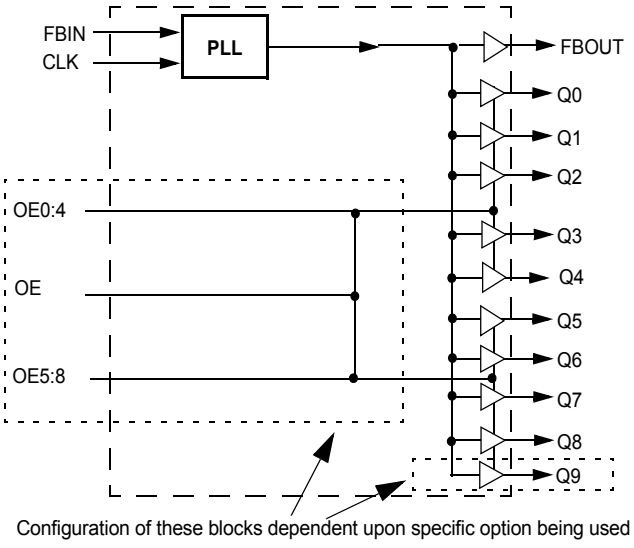
Operating Range: ..... 40 MHz < f_{OUT} < 140 MHz

Cycle-to-Cycle Jitter: ..... <100 ps

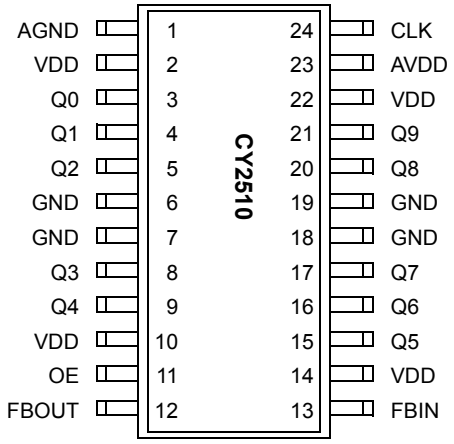
Output to Output Skew: ..... <100 ps

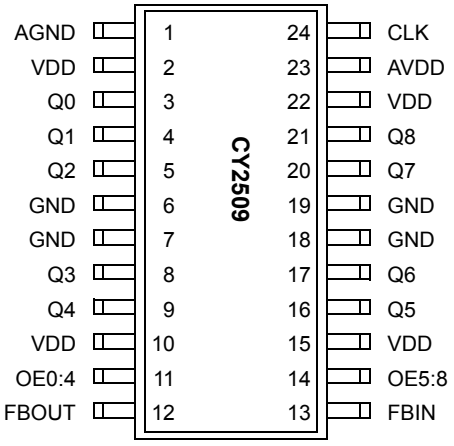
Phase Error Jitter:..... <100 ps

Block Diagram



Pin Configurations





Pin Definitions

Pin Name	Pin No. (2509)	Pin No. (2510)	Pin Type	Pin Description
CLK	24	24	I	***Reference Input:*** Output signals Q0:9 will be synchronized to this signal.
FBIN	13	13	I	***Feedback Input:*** This input must be fed by one of the outputs (typically FBOUT) to ensure proper functionality. If the trace between FBIN and FBOUT is equal in length to the traces between the outputs and the signal destinations, then the signals received at the destinations will be synchronized to the CLK signal input.
Q0:8	3, 4, 5, 8, 9, 16, 17, 20, 21	3, 4, 5, 8, 9, 15, 16, 17, 20	O	***Integrated Series Resistor Outputs:*** The frequency and phase of the signals provided by these pins will be equal to the reference signal if properly laid out. Each output has a 25Ω series damping resistor integrated.
Q9	n/a	21	O	***Integrated Series Resistor Output:*** The frequency and phase of the signal provided by this pin will be equal to the reference signal if properly laid out. This output has a 25Ω series damping resistor integrated.
FBOUT	12	12	O	***Feedback Output:*** This output has a 25Ω series resistor integrated on chip. Typically it is connected directly to the FBIN input with a trace equal in length to the traces between outputs Q0:9 and the destination points of these output signals.
AVDD	23	23	P	***Analog Power Connection:*** Connect to 3.3V. Use ferrite beads to help reduce noise for optimal jitter performance.
AGND	1	1	G	***Analog Ground Connection:*** Connect to common system ground plane.
VDD	2, 10, 15, 22	2, 10, 14, 22	P	***Power Connections:*** Connect to 3.3V. Use ferrite beads to help reduce noise for optimal jitter performance.
GND	6, 7, 18, 19	6, 7, 18, 19	G	***Ground Connections:*** Connect to common system ground plane.
OE	n/a	11	I	***Output Enable Input:*** Tie to VDD (HIGH, 1) for normal operation. When brought to GND (LOW, 0) all outputs are disabled to a LOW state.
OE0:4	11	n/a	I	***Output Enable Input:*** Tie to VDD (HIGH, 1) for normal operation. When brought to GND (LOW, 0) outputs Q0:4 are disabled to a LOW state.
OE5:8	14	n/a	I	***Output Enable Input:*** Tie to VDD (HIGH, 1) for normal operation. When brought to GND (LOW, 0) outputs Q5:8 are disabled to a LOW state.

Overview

The CY2509/10 is a PLL-based clock driver designed for use in dual inline memory modules. The clock driver has output frequencies of up to 133 MHz and output to output skews of less than 250 ps. The CY2509/10 provides minimum cycle-to-cycle and long-term jitter, which is of significant importance to meet the tight input-to-input skew budget in DIMM applications.

The current generation of 256- and 512-megabyte memory modules needs to support 100-MHz clocking speeds. Especially for cards configured in 16x4 or 8x8 format, the clock signal provided from the motherboard is generally not strong enough to meet all the requirements of the memory and logic on the DIMM. The CY2509/10 takes in the signal from the motherboard and buffers out clock signals with enough drive to support all the DIMM board clocking needs. The CY2509/10 is also designed to meet the needs of new PC133 SDRAM designs, operating to 133 MHz.

The CY2509/10 was specifically designed to accept SSFTG signals currently being used in motherboard designs to reduce EMI. Zero delay buffers which are not designed to pass this feature through may cause skewing failures.

Output enable pins allow for shutdown of output when they are not being used. This reduces EMI and power consumption.

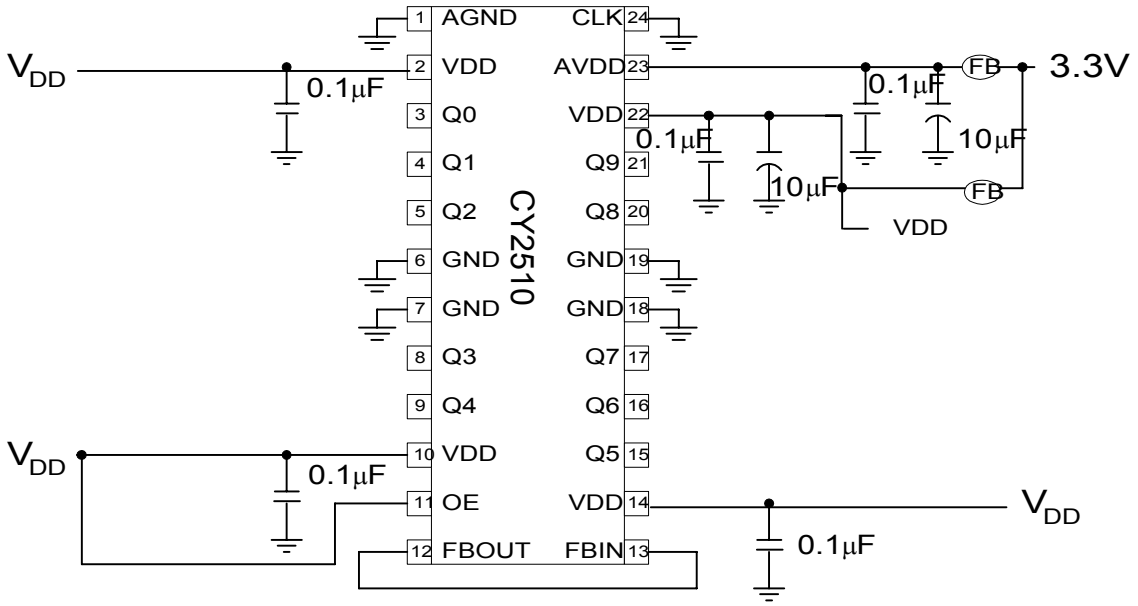


Figure 1. Schematic

Spread Aware™

Many systems being designed now utilize a technology called Spread Spectrum Frequency Timing Generation. Cypress has been one of the pioneers of SSFTG development, and we designed this product so as not to filter off the Spread Spectrum feature of the Reference input, assuming it exists. When a zero delay buffer is not designed to pass the SS feature through, the result is a significant amount of tracking skew which may cause problems in systems requiring synchronization.

For more details on Spread Spectrum timing technology, please see the Cypress application note titled, "EMI Suppression Techniques with Spread Spectrum Frequency Timing Generator (SSFTG) ICs."

How to Implement Zero Delay

Typically, Zero Delay Buffers (ZDBs) are used because a designer wants to provide multiple copies of a clock signal in phase with each other. The whole concept behind ZDBs is that the signals at the destination chips are all going HIGH at the same time as the input to the ZDB. In order to achieve this, layout must compensate for trace length between the ZDB and the target devices. The method of compensation is described below.

External feedback is the trait that allows for this compensation. Since the PLL on the ZDB will cause the feedback signal to be in phase with the reference signal. When laying out the board, match the trace lengths between the output being used for feed back and the FBIN input to the PLL.

If it is desirable to either add a little delay, or slightly precede the input signal, this may also be affected by either making the trace to the FBIN pin a little shorter or a little longer than the traces to the devices being clocked.

Inserting Other Devices in Feedback Path

Another nice feature available due to the external feedback is the ability to synchronize signals up to the signal coming from some other device. This implementation can be applied to any device (ASIC, multiple output clock buffer/driver, etc.) which is put into the feedback path.

Referring to *Figure 2*, if the traces between the ASIC/buffer and the destination of the clock signal(s) (A) are equal in length to the trace between the buffer and the FBIN pin, the signals at the destination(s) device will be driven HIGH at the same time the Reference clock provided to the ZDB goes HIGH. Synchronizing the other outputs of the ZDB to the outputs form the ASIC/Buffer is more complex however, as any propagation delay in the ASIC/Buffer must be accounted for.

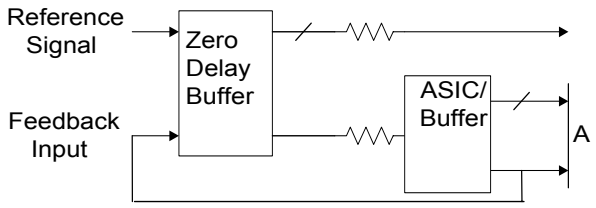


Figure 2. Six Output Buffers in the Feedback Path

Absolute Maximum Ratings [1]

Stresses greater than those listed in this table may cause permanent damage to the device. These represent a stress rating only. Operation of the device at these or any other conditions above those specified in the operating sections of this specification is not implied. Maximum conditions for extended periods may affect reliability.

Parameter	Description	Rating	Unit
V_{DD}, V_{IN}	Voltage on any pin with respect to GND	–0.5 to +7.0	V
T_{STG}	Storage Temperature	–65 to +150	°C
T_A	Operating Temperature	0 to +70	°C
T_B	Ambient Temperature under Bias	–55 to +125	°C
P_D	Power Dissipation	0.5	W

DC Electrical Characteristics: T_A =0°C to 70°C, V_{DD} = 3.3V ±10%

Parameter	Description	Test Condition	Min.	Typ.	Max.	Unit
I_{DD}	Supply Current	Unloaded, 100 MHz	–	–	200	mA
V_{IL}	Input Low Voltage		–	–	0.8	V
V_{IH}	Input High Voltage		2.0	–	V_{DD}+0.3	V
V_{OL}	Output Low Voltage	I_{OL} = 12 mA	–	–	0.8	V
V_{OH}	Output High Voltage	I_{OH} = –12 mA	2.1	–	–	V
I_{IL}	Input Low Current	V_{IN} = 0V	–	–	50	μA
I_{IH}	Input High Current	V_{IN} = V_{DD}	–	–	50	μA

AC Electrical Characteristics: T_A = 0°C to +70°C, V_{DD} = 3.3V ±10%

Parameter	Description	Test Condition	Min.	Typ.	Max.	Unit
f_{OUT}	Output Frequency	30-pF load[5]	40	–	140	MHz
t_R	Output Rise Time	0.8V to 2.0V, 30-pF load	–	–	2.1	ns
t_F	Output Fall Time	2.0V to 0.8V, 30-pF load	–	–	2.5	ns
t_{ICLKR}	Input Clock Rise Time[2]		–	–	4.5	ns
t_{ICLKF}	Input Clock Fall Time[2]		–	–	4.5	ns
t_{PEJ}	CLK to FBIN Skew Variation[3, 4]	Measured at V_{DD}/2	–350	0	350	ps
t_{SK}	Output to Output Skew	All outputs loaded equally	–100	0	100	ps
t_D	Duty Cycle	30-pF load	43	50	58	%
t_{LOCK}	PLL Lock Time	Power supply stable	–	–	1.0	ms
t_{JC}	Jitter, Cycle-to-Cycle		–	50	100	ps

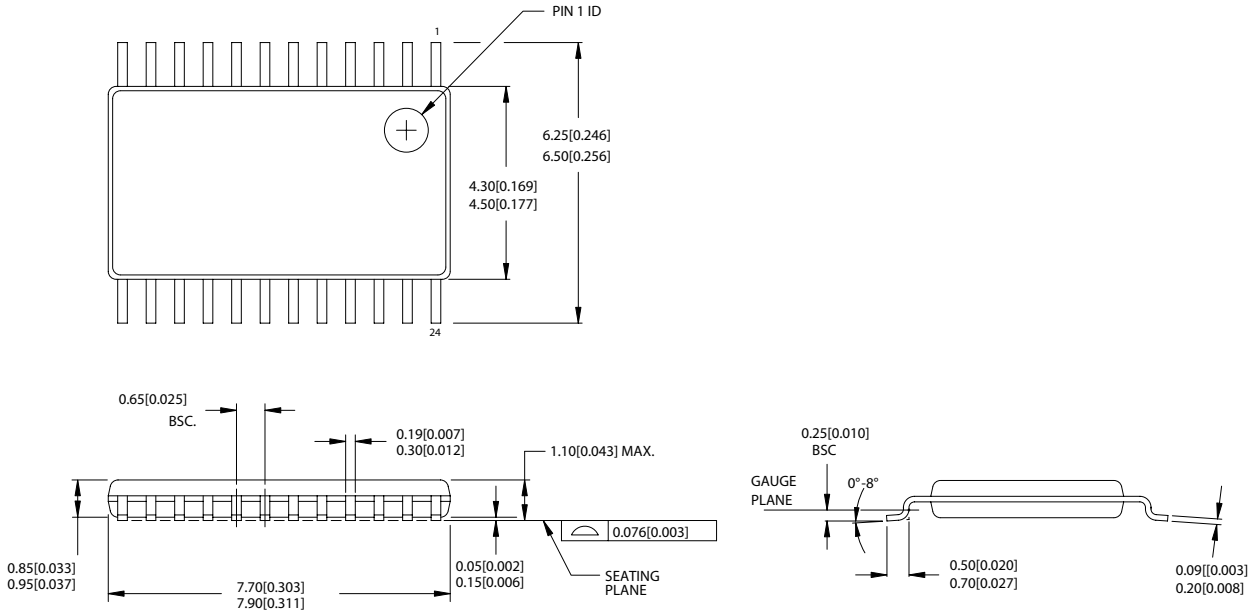
Notes:
1. **Multiple Supplies**: The voltage on any input or I/O pin cannot exceed the power pin during power-up. Power supply sequencing is NOT required.
2. Longer input rise and fall time will degrade skew and jitter performance.
3. Skew is measured at V_{DD}/2 on rising edges.
4. Duty cycle is measured at V_{DD}/2.
5. Production tests are run at 133 MHz.

Ordering Information

Ordering Code	Package Type	Temperature Range
CY2509ZC-1	24-pin TSSOP	Commercial
CY2509ZC-1T	24-pin TSSOP - Tape and Reel	Commercial
CY2510ZC-1	24-pin TSSOP	Commercial
CY2510ZC-1T	24-pin TSSOP - Tape and Reel	Commercial
Lead-free		
CY2509ZXC-1	24-pin TSSOP	Commercial
CY2509ZXC-1T	24-pin TSSOP - Tape and Reel	Commercial
CY2510ZXC-1	24-pin TSSOP	Commercial
CY2510ZXC-1T	24-pin TSSOP - Tape and Reel	Commercial

Package Drawing and Dimensions

24-Lead Thin Shrunk Small Outline Package (4.40-mm Body) Z24



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Document History Page

Document Title: CY2509/10 Spread Aware™, Ten/Eleven Output Zero Delay Buffer Document Number: 38-07230				
REV.	**ECN NO.**	**Issue Date**	**Orig. of Change**	**Description of Change**
**	110495	01/07/02	SZV	Change from Spec number: 38-00914 to 38-07230
*A	122844	12/14/02	RBI	Power up requirements added to Operating Conditions Information
*B	352015	See ECN	RGL	Added Lead-free devices Added typical jitter and max. V_{IH} numbers
*C	385383	See ECN	RGL	Minor Change: Replaced the wrong package drawing

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