Document Title

8 Bit Microcontroller

Revision History

Rev. No.	History	Issue Date	Remark
0.0	Initial issue	November 25, 1998	Preliminary

A83516 Series

Preliminary

8 Bit Microcontroller

Features

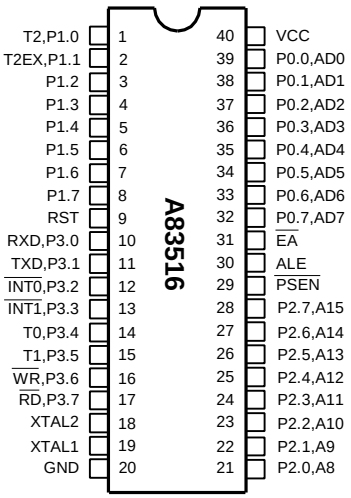
- 8-bit CMOS microcontroller
- Fully static design with power saving idle mode and power down mode
- Low standby current at full supply voltage
- Versions for 12/24/40MHz operating frequency
- On chip 256B RAM
- On chip 64KB X 8 MASK-ROM program memory
- 64K bytes external data memory space
- Four 8-bit bidirectional ports
- Three 16-bit Timers/Counters (Timer 2 with up/down counter feature)
- One full duplex serial port
- Boolean processor
- Six interrupt sources, two priority levels
- Available in 40-pin P-DIP and 44-pin PLCC packages

General Description

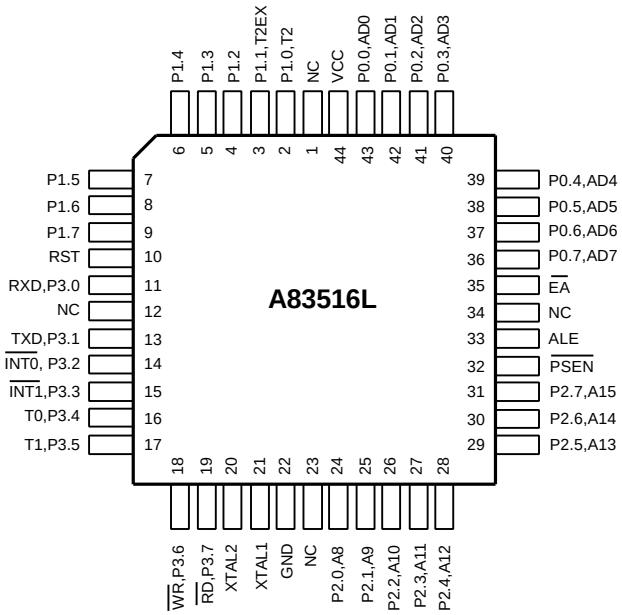
The AMIC A83516 is a high-performance 8-bit microcontroller. It is compatible with the industry standard 80C52 microcontroller series.
The A83516 contains a 256B RAM, 64KB X 8 ROM, four 8-bit bidirectional parallel ports, three 16-bit timer/counters, a serial port and six interrupt sources with two priority levels.
The A83516 has two power reduction modes, idle mode and power-down mode. It supports 64KB external data memory.

Pin Configurations

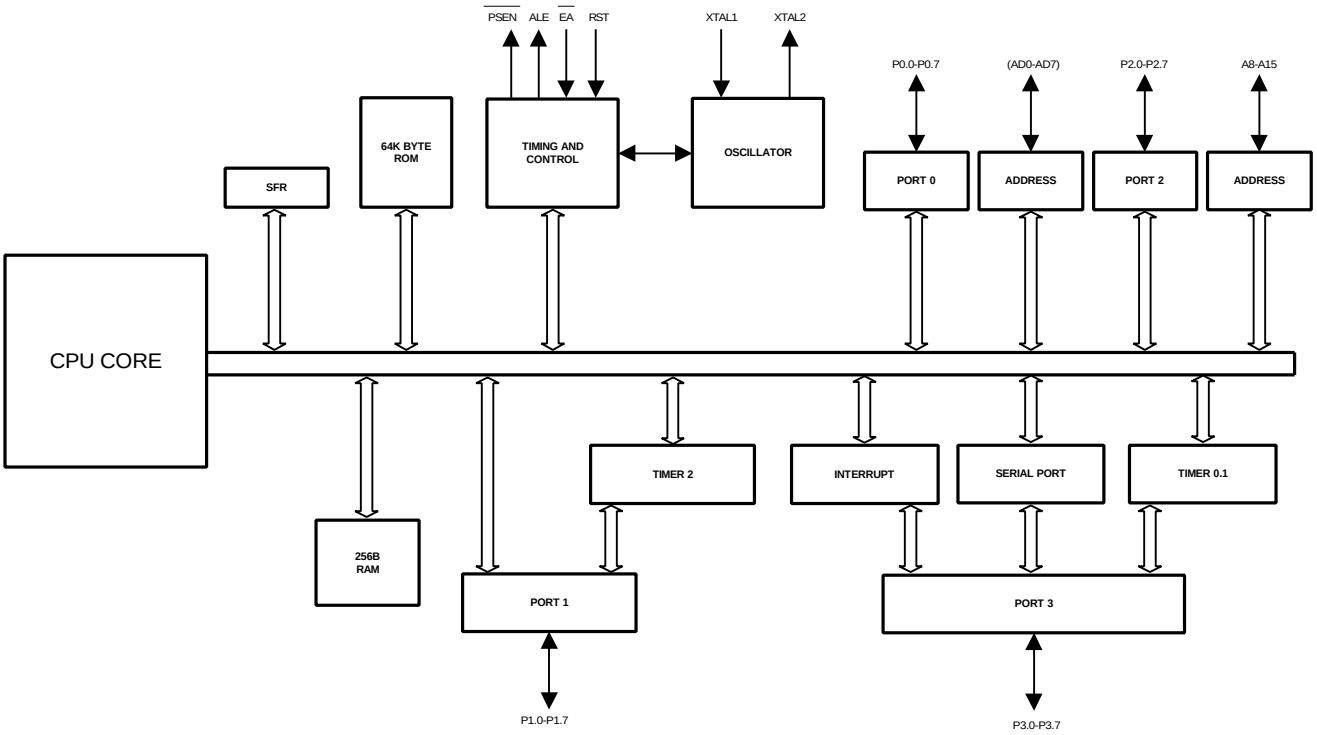
■ **P-DIP**



■ **PLCC**



Block Diagram



Pin Description

Pin No.		Symbol	Type	Description
P-DIP	PLCC			
1 - 8	2 - 9	P1.0 - P1.7	I/O	Port1. Port1 is a bidirectional I/O port with internal pull-ups. Pin P1.0 and P1.1 also provide alternate functions as follows:
			I/O	P1.0 T2 Timer/Counter2 external input/clock out
			I	P1.1 T2EX Timer/Counter2 capture/reload input
9	10	RST	I	Reset input, active high. It must be kept high for at least two machine cycles to be recognized by the processor
10 - 17	11, 13 - 19	P3.0 - P3.7	I/O	Port3. Port3 is a bidirectional I/O port with internal pull-ups. Port3 pins also serve alternate functions as follows:
			I	P3.0 $\overline{RXD}$ Serial receive port
			O	P3.1 $\overline{TXD}$ Serial transmit port
			I	P3.2 $\overline{INT0}$ External interrupt 0
			I	P3.3 $\overline{INT1}$ External interrupt 1
			I	P3.4 T0 Timer/Counter 0 input
			I	P3.5 T1 Timer/Counter 1 input
			O	P3.6 $\overline{WR}$ External data memory write strobe
			O	P3.7 $\overline{RD}$ External data memory read strobe
18	20	XTAL2	O	Crystal2. This is the output of crystal oscillator. It is the inversion of XTAL1
19	21	XTAL1	I	Crystal1. This is the input of crystal oscillator. It can be driven by an external clock
20	22	GND	I	Ground
21 - 28	24 - 31	P2.0 - P2.7	I/O	Port2. Port2 is a bidirectional I/O port with internal pull-ups. Port2 is also the multiplexed upper-order address bus during accesses to external data memory
29	32	$\overline{PSEN}$	O	Program Store Enable : active low. The read strobe to external program memory. $\overline{PSEN}$ is activated in each machine cycle when fetching external program memory
30	33	ALE	O	Address Latch Enable : active high. ALE is used to enable the address latch that separates the data on Port 0
31	35	$\overline{EA}$	I	External Access Enable : active low. It is held low to enable the device to fetch code from external program memory
32 - 39	36 - 43	P0.7 - P0.0	I/O	Port0. Port0 is an open drain, bidirectional I/O port. Port0 is also the multiplexed low-order address bus during accesses to external data memory
40	44	VCC	I	Power supply

Functional Description

The A83516 is a high speed 8-bit microcontroller. The architecture consists of a core controller, four general purposes I/O ports, 256 bytes RAM internal register, 64K bytes ROM and a serial port.
This microcontroller supports 111 opcodes and executes instructions in 12 clock/machine cycle. It can reference both a 64K program address space and a 64K data storage space.

Timer/Counter 0, 1 and 2

Timer 0,1 and 2 each consist of two 8-bit data registers. These are called TL0 and TH0 for Timer 0. TL1 and TH1 for Timer 1, and TL2 and TH2 for Timer 2. The TMOD and TCON registers support control function for Timer 0 and Timer 1. The T2CON register provides control function for Timer 2. When operating reload/capture mode, RCAP2H and RCAP2L will be used.

Interrupt

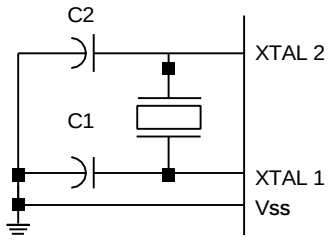
The A83516 provides 6 interrupt modes. These consist of 2 external interrupts, 3 internal interrupts and a serial port interrupt.
The enable/disable interrupt is controlled by IE register in SFR.
The priority of interrupts is controlled by IP register in SFR.

Serial Port Transfer

The A83516 provides a full duplex serial transfer function.
This function is controlled by SCON register in SFR.
And the data is storaged in SBUF register during transmitting and receiving.

Oscillator Characteristics

The oscillator connections are shown as Figure 1. And Figure 2. When quartz crystal is used, C1 and C2 are 30pF shown in Figure 1. When external clock is used, the internal clock will be gotten through a divide-by-two flip-flop. When starting up, the input loading for XTAL1 pin is 100pF. This is due to interaction between the amplifier and its feedback capacitance interaction. After the external signal meets the V_{IL} and V_{IH} specification the capacitance will not exceed 20pF.



C1,C2 = 30pF ± 10pF for Crystals
Figure 1. Oscillator Connections

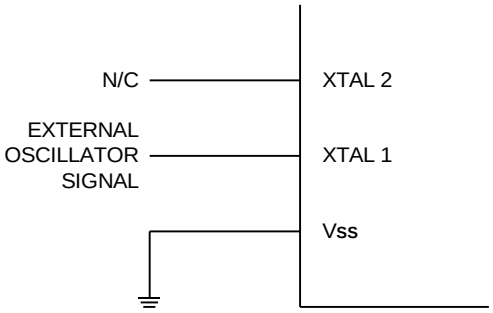


Figure 2. External Clock Drive configuration

Power Reduce Mode

IDLE Mode

It is executed by IDLE bit of PCON register in SFR. In idle mode, the clock to microcontroller core is stopped. The status in microcontroller core and I/O data are kept. The microcontroller will stop idle status when either a reset or an interrupt occurs.

POWER-DOWN Mode

It is executed by PD bit of PCON register in SFR. In power-down mode, the oscillator clock will stop. The data in RAM and status in SFR will be kept. The only way to exit power-down mode is to reset this chip.

RESET

The external reset signal must be held high for at least two machine cycles during the oscillator running.
After reset, the ports are held high, SP register to 07H, all of the other SFR registers except SBUF to 00H, and SBUF is not reset.

Recommended DC Operating Conditions (T_A = -25°C to + 85°C)

Symbol	Parameter	Min.	Typ.	Max.	Unit
VCC	Supply Voltage	4.5	5.0	5.5	V
GND	Ground	0	0	0	V
V_{IH}*	Input High Voltage	2.4	-	VCC+0.2	V
V_{IL}	Input Low Voltage	0	-	0.8	V

***** XTAL1 is a CMOS input. RESET is a Schmit trigger input.
The min. of V_{IH} is 3.5 Volts for these two pins.

Absolute Maximum Ratings*

VCC to GND . . . . . –0.3V to +7.0V
IN, IN/OUT Volt to GND . . . . . -0.5V to VCC + 0.5V
Operating Temperature, Topr . . . . . -25°C to + 85°C
Storage Temperature, Tstg . . . . . -55°C to + 125°C
Power Dissipation[1*], Pr 1W
Soldering Temperature & Time . . . . . 260°C, 10sec

1* : Operating frequency is 40MHz

*Comments

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to this device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied or intended. Exposure to the absolute maximum rating conditions for extended periods may affect device reliability.

DC Electrical Characteristics (T_A = -25°C to + 85°C, VCC = 5V ± 10%)

Symbol	Parameter	Min.	Max.	Unit	Conditions
$\lvert I_{LI} \rvert$ [1]	Input Leakage Current	-	10	μA	V_{IN} = GND to VCC
$\lvert I_{LO} \rvert$	Output Leakage Current	-	10	μA	$V_{I/O}$ = GND to VCC
I_{CC}	Operating Current	-	50	mA	foper = 40MHz External oscillator is on XTAL1 pin No load
I_{IDLE}	IDLE Mode Current	-	6	mA	foper = 40MHz V_{RST} = GND, $V_{\overline{EA}}$ = GND V_{PORT0} = VCC
I_{PD}	POWER-DOWN Mode Current	-	20	μA	No crystal oscillator input V_{RST} = GND, $V_{\overline{EA}}$ = GND V_{PORT0} = VCC
V_{OL1}	Output Low Voltage (PORT1, PORT2 and PORT3)	-	0.45	V	I_{OL} = 2mA
V_{OL2}	Output Low Voltage (ALE, $\overline{PSEN}$ and PORT0)	-	0.45	V	I_{OL} = 4mA
V_{OH1}	Output High Voltage (PORT1, PORT2 and PORT3)	2.4	-	V	I_{OH} = -100μA
V_{OH2}	Output High Voltage (ALE, $\overline{PSEN}$ and PORT0)	2.4	-	V	I_{OH} = -400μA
C_1	Input Pin Capacitance	-	10	pF	1MHz, 25°C

1. For RESET pin, the $\lvert I_{LI} \rvert$ max. is 300 μA, since it has an internal pull-low of approx. 30KΩ resistor.

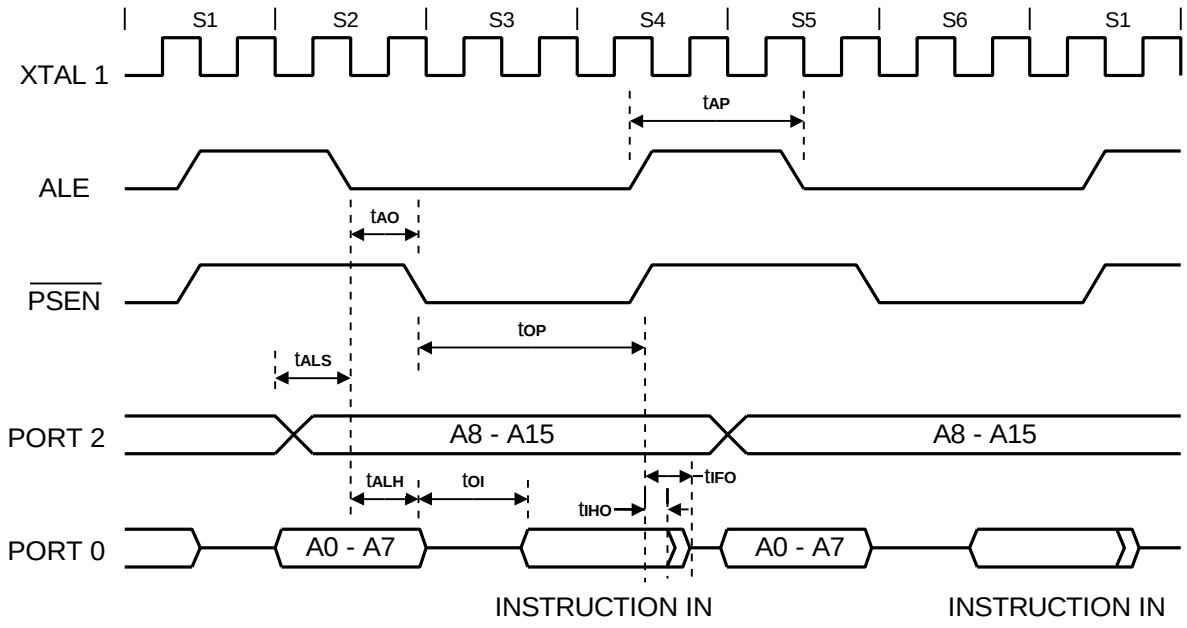
AC Characteristics (T_A = -25°C to + 85°C, VCC = 5V ± 10%)

Symbol	Parameter	Min.	Max.	Unit
Program Memory Cycle				
t_{AP}	ALE Pulse Width	$2t_{ck}$ – 20[1]	-	ns
t_{ALS}	Address Valid to ALE Low	$1t_{ck}$	-	ns
t_{ALH}	Address Hold from ALE Low	$1t_{ck}$	-	ns
t_{op}	$\overline{PSEN}$ Pulse Width	$3t_{ck}$ - 20[1]	-	ns
t_{AO}	ALE Low to $\overline{PSEN}$ Low	$1t_{ck}$	-	ns
t_{OI}[2]	$\overline{PSEN}$ Low to Valid Instruction in	-	$2t_{ck}$	ns
t_{IDO}	Input Instruction Hold after $\overline{PSEN}$ High	-	$1t_{ck}$	ns
t_{IFO}	Input Instruction Float after $\overline{PSEN}$ High	-	$1t_{ck}$	ns
External Clock				
f_{OPER}	Clock Frequency	0	40	MHz
t_{CK}[3]	Clock Period	25	-	ns
t_{CKH}[4]	Clock High Time	10	-	ns
t_{CKL}[4]	Clock Low Time	10	-	ns
Data Memory Cycle				
t_{PR}	$\overline{RD}$ Pulse Width	$6t_{ck}$ - 20[1]	-	ns
t_{PD}	$\overline{RD}$ Low to Valid Data in	-	$4t_{ck}$	ns
t_{DHR}	Data Hold from $\overline{RD}$ High	0	$2t_{ck}$	ns
t_{DFR}	Data Float from $\overline{RD}$ High	0	$2t_{ck}$	ns
t_{AR}	ALE Low to $\overline{RD}$ Low	$3t_{ck}$	$3t_{ck}$ + 20[1]	ns
t_{WP}	$\overline{WR}$ Pulse Width	$6t_{ck}$ - 20[1]	-	ns
t_{DS}	Valid Data to $\overline{WR}$ Low	$1t_{ck}$	-	ns
t_{DHW}	Data Hold from $\overline{WR}$ High	$1t_{ck}$	-	ns
t_{AW}	ALE Low to $\overline{WR}$ Low	$3t_{ck}$	$3t_{ck}$ + 20[1]	ns
Serial Port Cycle				
t_{SCK}	Serial Port Clock	$12t_{ck}$	-	ns
t_{KI}	Clock Rising Edge to Valid Input Data	-	$11t_{ck}$	ns
t_{IKH}	Input Data to Serial Clock Rising Clock Hold Time	0	-	ns
t_{OKS}	Output Data to Serial Clock Rising Edge Setup Time	$11t_{ck}$	-	ns
t_{OKH}	Output Data to Serial Clock Rising Edge Hold Time	$1t_{ck}$	-	ns

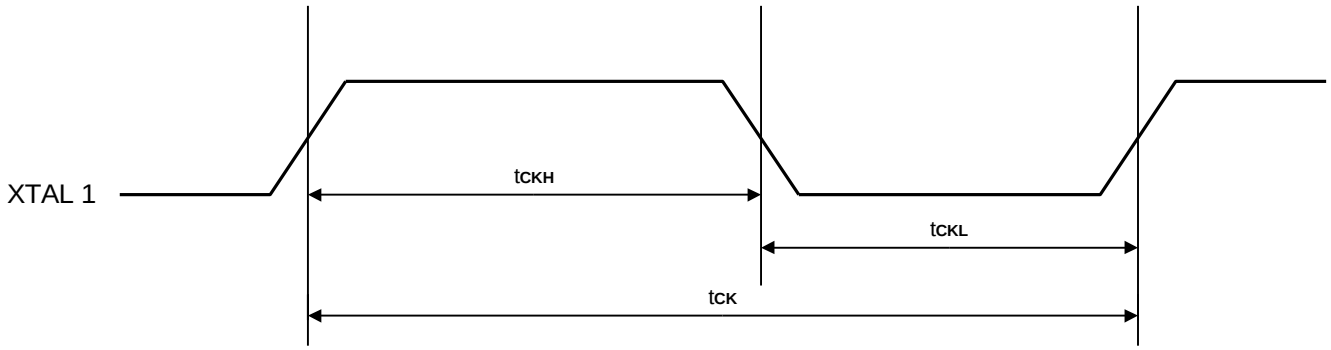
1. This 20 ns is due to buffer driving delay and wire loading.
2. Instruction cycle time is 12 t_{ck}.
3. tck = 1/ f_{oper}
4. There are no duty cycle requirements on the XTAL1 input.

Timing Waveforms

Program Memory Cycle

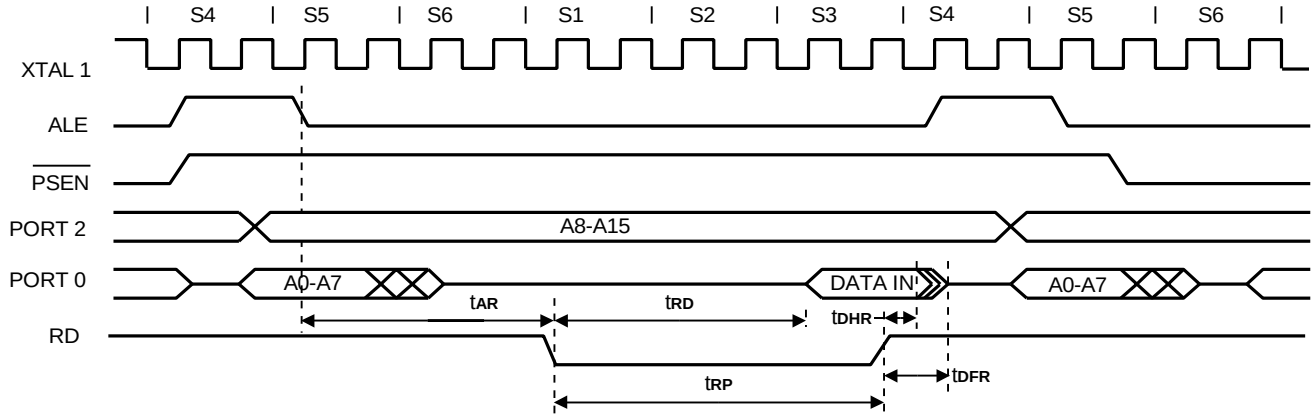


Clock Input Waveform

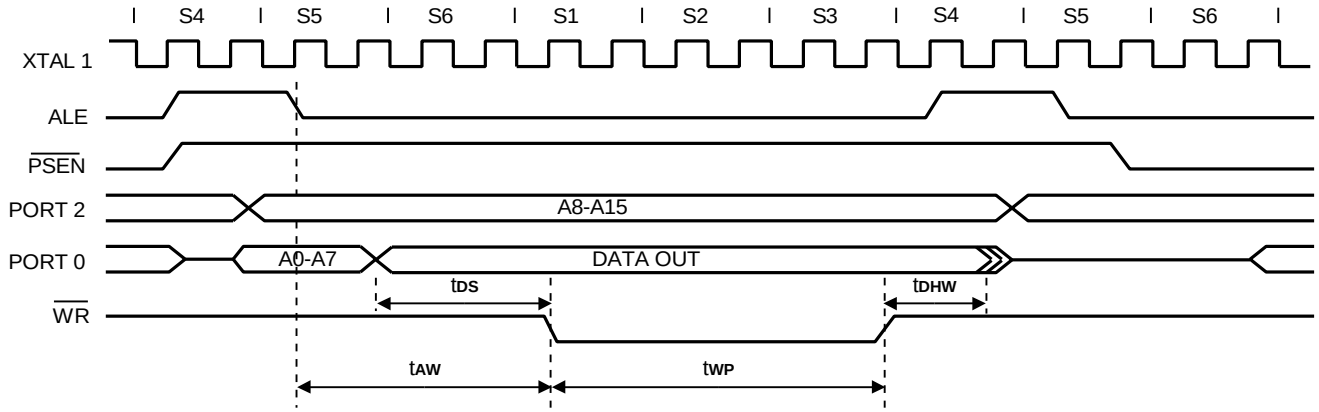


Timing Waveforms (continued)

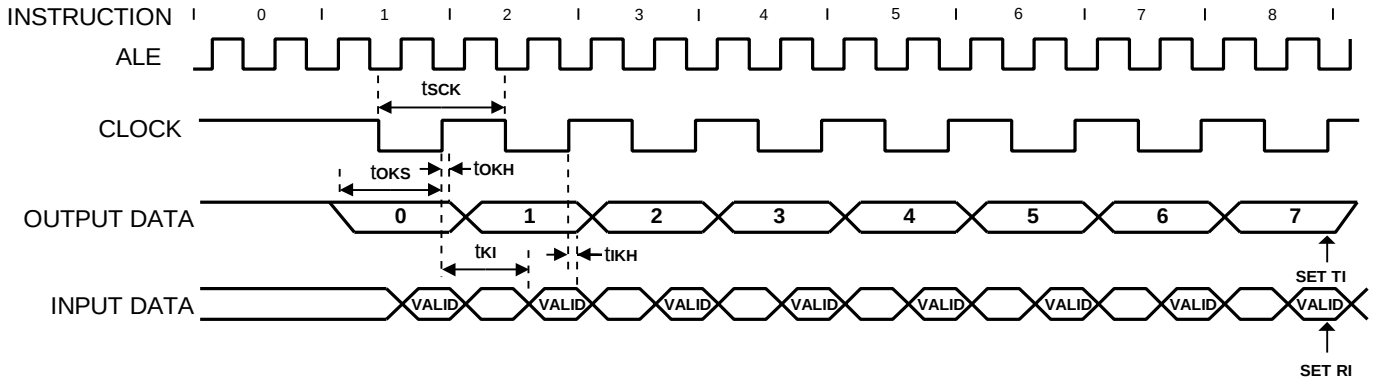
Data Memory Read Cycle



Data Memory Write Cycle



Serial Port Timing – Shift Register Mode



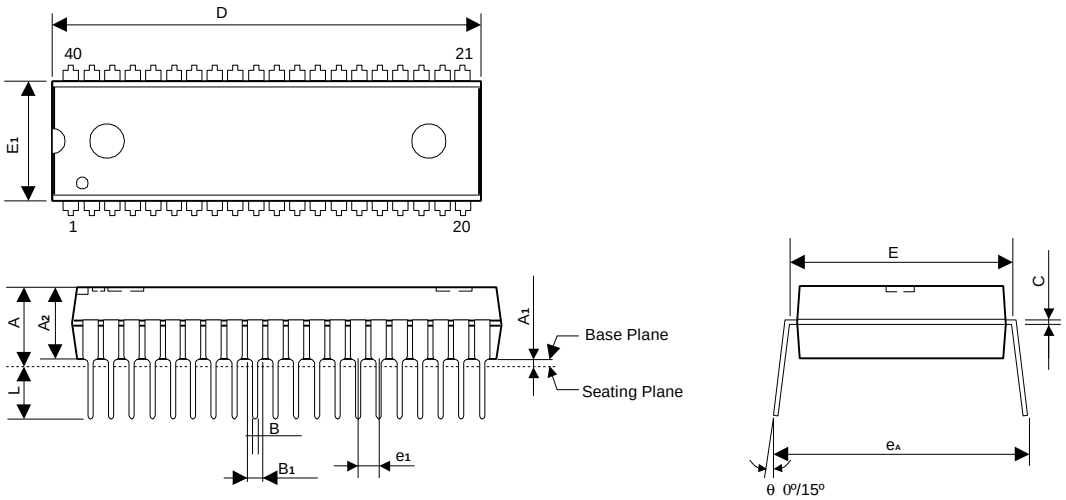
Ordering Information

Part No.	RAM	ROM	FREQ (MHz)	Package
A83516-12	256 Byte	64K Byte	12	40L P-DIP
A83516L-12	256 Byte	64K Byte	12	44L PLCC
A83516-24	256 Byte	64K Byte	24	40L P-DIP
A83516L-24	256 Byte	64K Byte	24	44L PLCC
A83516-40	256 Byte	64K Byte	40	40L P-DIP
A83516L-40	256 Byte	64K Byte	40	44L PLCC

Package Information

P-DIP 40L Outline Dimensions

unit: inches/mm



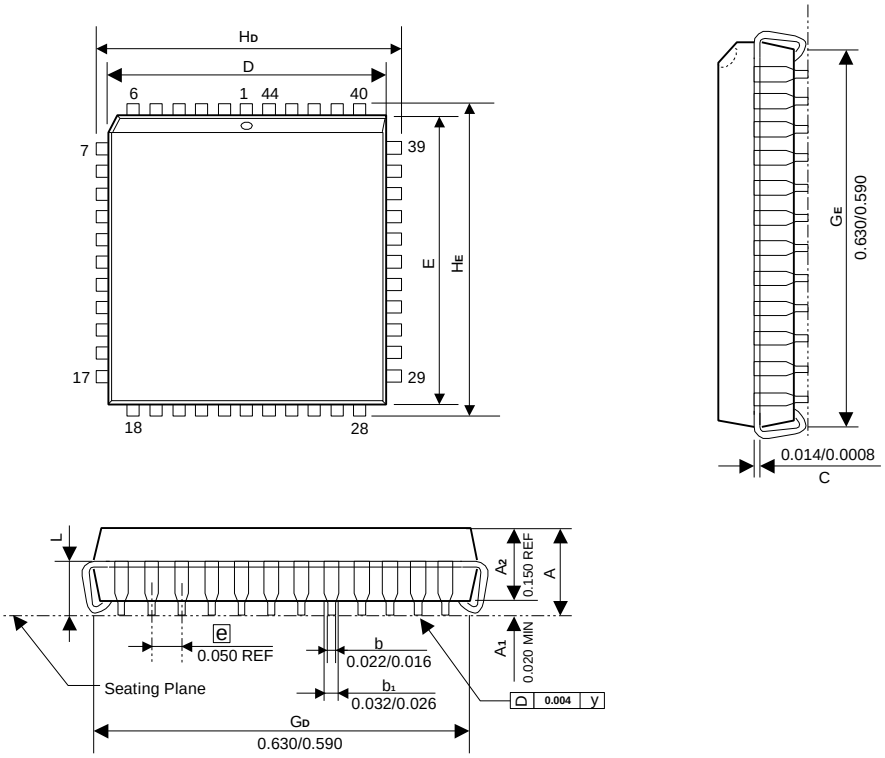
Symbol	Dimensions in inches			Dimensions in mm		
	Min	Nom	Max	Min	Nom	Max
A	-	-	0.210	-	-	5.344
A_1	0.015	-	-	0.381	-	-
A_2	0.150	0.155	0.160	3.810	3.937	4.064
B	0.018 TYP			0.457 TYP		
B_1	0.050 TYP			1.270 TYP		
C	-	0.010	-	-	0.254	-
D	2.049	2.054	2.059	52.045	52.172	52.299
E	0.590	0.600	0.610	14.986	15.240	15.494
E_1	0.542	0.547	0.552	13.767	13.894	14.021
e_1	0.100 TYP			2.540 TYP		
L	0.120	0.130	0.140	3.048	3.302	3.556
e_A	0.622	0.642	0.662	15.799	16.307	16.815

Notes:
1. The maximum value of dimension D includes end flash.
2. Dimension E_1 does not include resin fins.

Package Information

PLCC 44L Outline Dimension

unit: inches/mm



Symbol	Dimensions in inches			Dimensions in mm		
	Min	Nom	Max	Min	Nom	Max
A	-	-	0.185	-	-	4.70
D	0.648	0.653	0.658	16.46	16.59	16.71
E	0.648	0.653	0.658	16.46	16.59	16.71
H_D	0.680	0.690	0.700	17.27	17.53	17.78
H_E	0.680	0.690	0.700	17.27	17.53	17.78
L	0.090	0.100	0.110	2.29	2.54	2.79
θ	0°	-	10°	0°	-	10°

Notes:

1. Dimensions D and E do not include resin fins.
2. Dimensions G_D & G_E are for PC Board surface mount pad pitch design reference only.

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