



# 128K x 8 Static RAM

## Features

- **High Speed**  
— 55ns and 70ns availability
- **Voltage range**  
— 2.7V–3.6V
- **Ultra low active power**  
— Typical active current: 20 mA @  $f = f_{max}$  (70ns speed)
- **Low standby power**
- **Easy memory expansion with  $\overline{CE}$  and  $\overline{OE}$  features**
- **Automatic power-down when deselected**
- **CMOS for optimum speed/power**

## Functional Description

The WCMA1008U1X is a high-performance CMOS static RAM organized as 128K words by 8 bits. Easy memory expansion is provided by an active LOW Chip Enable ( $\overline{CE}_1$ ), an active HIGH Chip Enable ( $CE_2$ ), an active LOW Output Enable ( $\overline{OE}$ ) and three-state drivers. These devices have an automat-

ic power-down feature, reducing the power consumption by over 99% when deselected.

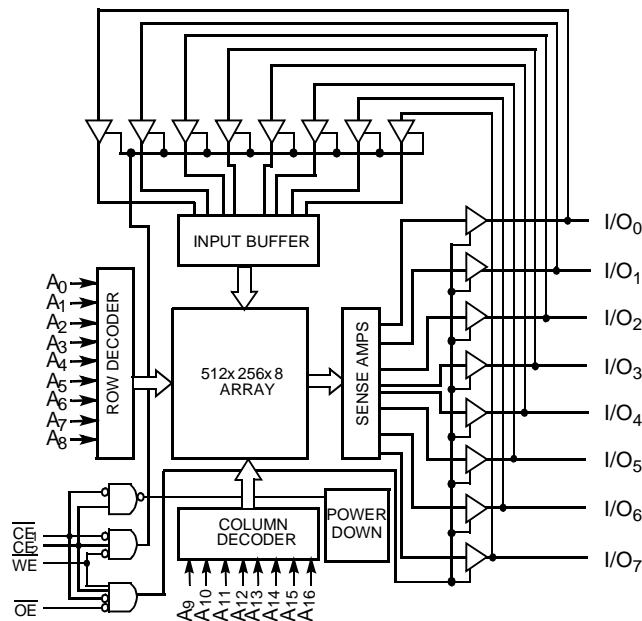
Writing to the device is accomplished by taking Chip Enable one ( $\overline{CE}_1$ ) and Write Enable ( $\overline{WE}$ ) inputs LOW and the Chip Enable two ( $CE_2$ ) input HIGH. Data on the eight I/O pins ( $I/O_0$  through  $I/O_7$ ) is then written into the location specified on the address pins ( $A_0$  through  $A_{16}$ ).

Reading from the device is accomplished by taking Chip Enable one ( $\overline{CE}_1$ ) and Output Enable ( $\overline{OE}$ ) LOW while forcing Write Enable ( $\overline{WE}$ ) and Chip Enable two ( $CE_2$ ) HIGH. Under these conditions, the contents of the memory location specified by the address pins will appear on the I/O pins.

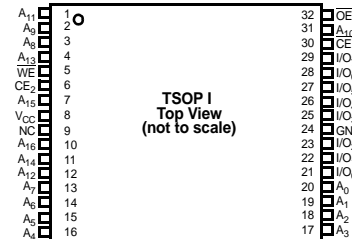
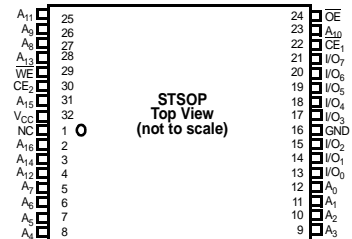
The eight input/output pins ( $I/O_0$  through  $I/O_7$ ) are placed in a high-impedance state when the device is deselected ( $\overline{CE}_1$  HIGH or  $CE_2$  LOW), the outputs are disabled ( $\overline{OE}$  HIGH), or during a write operation ( $\overline{CE}_1$  LOW,  $CE_2$  HIGH, and  $\overline{WE}$  LOW).

The WCMA1008U1X is available in a 32 Lead TSOP and STSOP packages.

## Logic Block Diagram



## Pin Configurations





**Maximum Ratings**

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature .....-65°C to +150°C  
 Ambient Temperature with  
 Power Applied.....55°C to +125°C  
 Supply Voltage to Ground Potential.....-0.5V to +4.6V

DC Voltage Applied to Outputs  
 in High Z State<sup>[1]</sup>.....0.5V to  $V_{CC} + 0.5V$   
 DC Input Voltage<sup>[1]</sup>.....-0.5V to  $V_{CC} + 0.5V$   
 Output Current into Outputs (LOW).....20 mA  
 Static Discharge Voltage .....>2001V  
 (per MIL-STD-883, Method 3015)  
 Latch-Up Current .....>200 mA

**Operating Range**

Product	Range	Ambient Temperature	$V_{CC}$
WCMA1008U1X	Industrial	-40°C to +85°C	2.7V to 3.6V

**Product Portfolio**

Product	$V_{CC}$ Range			Speed	Power Dissipation (Industrial)			
					Operating, $I_{CC}$		Standby ( $I_{SB2}$ )	
					$f = f_{max}$		Typ. <sup>[2]</sup>	Max.
	Min.	Typ. <sup>[2]</sup>	Max.		Typ. <sup>[2]</sup>	Max.		
WCMA1008U1X	2.7V	3.0V	3.6V	70 ns	20 mA	40 mA	0.4 $\mu A$	30 $\mu A$
				55 ns				

**Notes:**

- $V_{IL(min.)} = -2.0V$  for pulse durations less than 20 ns.
- Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at  $V_{CC} = V_{CC(typ.)}$ ,  $T_A = 25^\circ C$ .

**Electrical Characteristics Over the Operating Range**

Parameter	Description	Test Conditions		WCMA1008U1X-70/55			Unit
				Min.	Typ. <sup>[2]</sup>	Max.	
V <sub>OH</sub>	Output HIGH Voltage	I <sub>OH</sub> = -1.0 mA	V <sub>CC</sub> = 2.7V	2.4			V
V <sub>OL</sub>	Output LOW Voltage	I <sub>OL</sub> = 2.1 mA	V <sub>CC</sub> = 2.7V			0.4	V
V <sub>IH</sub>	Input HIGH Voltage			2		V <sub>CC</sub> + 0.5V	V
V <sub>IL</sub>	Input LOW Voltage			-0.5		0.8	V
I <sub>IX</sub>	Input Leakage Current	GND ≤ V <sub>I</sub> ≤ V <sub>CC</sub>		-1		+1	μA
I <sub>OZ</sub>	Output Leakage Current	GND ≤ V <sub>O</sub> ≤ V <sub>CC</sub> , Output Disabled		-1		+1	μA
I <sub>CC</sub>	V <sub>CC</sub> Operating Supply Current	f = f <sub>MAX</sub> = 1/t <sub>RC</sub>	V <sub>CC</sub> = 3.6V I <sub>OUT</sub> = 0 mA CMOS Levels	70ns	20	40	mA
				55ns	23	50	
I <sub>SB1</sub>	Automatic CE Power-Down Current— TTL Inputs	Max. V <sub>CC</sub> , $\overline{CE}_1 \geq V_{IH}$ , CE <sub>2</sub> < V <sub>IH</sub> V <sub>IN</sub> ≥ V <sub>IH</sub> or V <sub>IN</sub> ≤ V <sub>IL</sub> , f = f <sub>MAX</sub>		70ns	15	300	μA
				55ns	17	350	
I <sub>SB2</sub>	Automatic CE Power-Down Current— CMOS Inputs	Max. V <sub>CC</sub> , $\overline{CE}_1 \geq V_{CC} - 0.3V$ , CE <sub>2</sub> < 0.3 V <sub>IN</sub> ≥ V <sub>CC</sub> - 0.3V or V <sub>IN</sub> ≤ 0.3V, f = 0			0.4	30	

**Capacitance<sup>[3]</sup>**

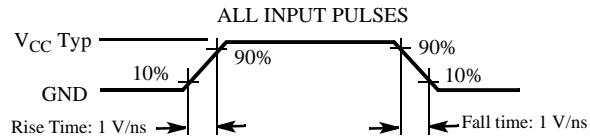
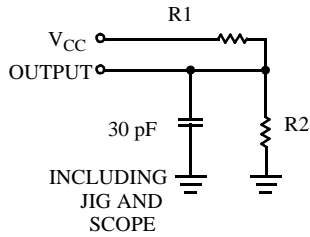
Parameter	Description	Test Conditions	Max.	Unit
C <sub>IN</sub>	Input Capacitance	T <sub>A</sub> = 25°C, f = 1 MHz, V <sub>CC</sub> = V <sub>CC(typ)</sub>	6	pF
C <sub>OUT</sub>	Output Capacitance		8	pF

**Thermal Resistance**

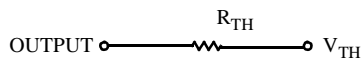
Description	Test Conditions	Symbol	BGA	Unit
Thermal Resistance <sup>[3]</sup> (Junction to Ambient)	Still Air, soldered on a 4.25 x 1.125 inch, 4-layer printed circuit board	Θ <sub>JA</sub>	55	°C/W
Thermal Resistance <sup>[3]</sup> (Junction to Case)		Θ <sub>JC</sub>	16	°C/W

**Note:**

3. Tested initially and after any design or process changes that may affect these parameters.

**AC Test Loads and Waveforms**


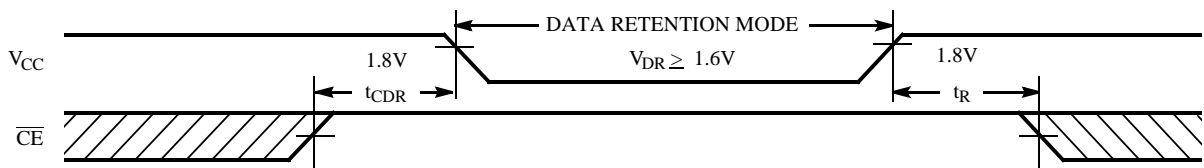
Equivalent to: THÉVENIN EQUIVALENT



Parameters	3.3V	Unit
R1	1213	Ohms
R2	1378	Ohms
R <sub>TH</sub>	645	Ohms
V <sub>TH</sub>	1.75	Volts

**Data Retention Characteristics (Over the Operating Range)**

Parameter	Description	Conditions	Min.	Typ. <sup>[2]</sup>	Max.	Unit
V <sub>DR</sub>	V <sub>CC</sub> for Data Retention		1.6			V
I <sub>CCDR</sub>	Data Retention Current	V <sub>CC</sub> = 2V, $\overline{CE}_1 \geq V_{CC} - 0.3V$ , CE <sub>2</sub> < 0.3V V <sub>IN</sub> ≥ V <sub>CC</sub> - 0.3V or V <sub>IN</sub> ≤ 0.3V		0.4	20	μA
t <sub>CDR</sub> <sup>[3]</sup>	Chip Deselect to Data Retention Time		0			ns
t <sub>R</sub> <sup>[4]</sup>	Operation Recovery Time		t <sub>RC</sub>			ns

**Data Retention Waveform**

**Note:**

4. Full Device AC operation requires linear V<sub>CC</sub> ramp from V<sub>DR</sub> to V<sub>CC(min.)</sub> ≥ 100 μs or stable at V<sub>CC(min.)</sub> ≥ 100 μs.

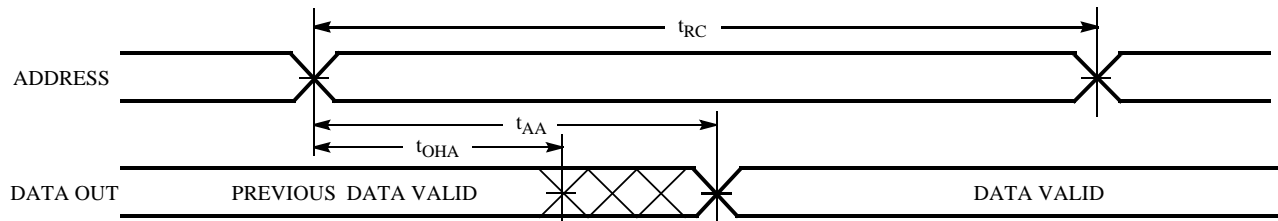
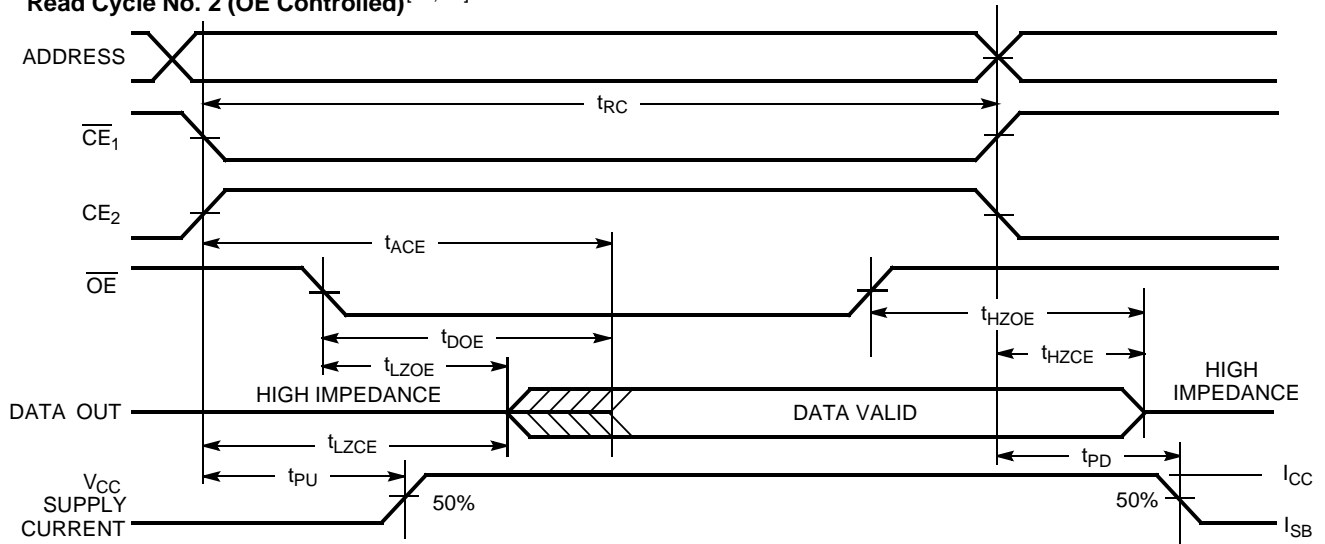


Switching Characteristics Over the Operating Range<sup>[5]</sup>

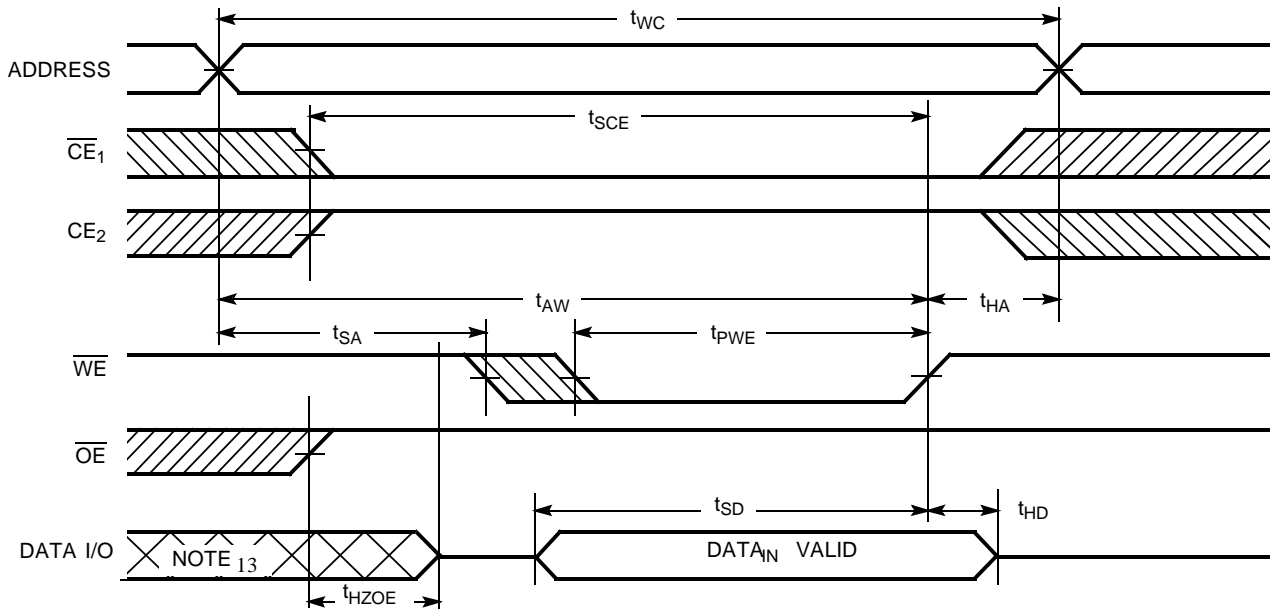
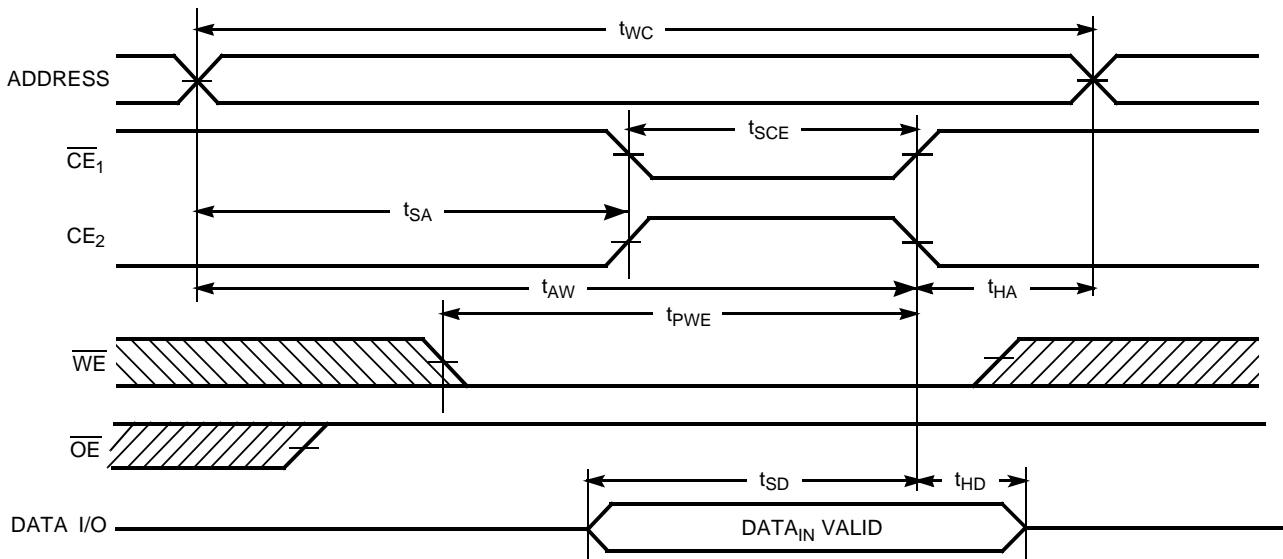
Parameter	Description	WCMA1008U1X-55		WCMA1008U1X-70		Unit
		Min.	Max.	Min.	Max.	
<b>READ CYCLE</b>						
t <sub>RC</sub>	Read Cycle Time	55		70		ns
t <sub>AA</sub>	Address to Data Valid		55		70	ns
t <sub>OHA</sub>	Data Hold from Address Change	5		10		ns
t <sub>ACE</sub>	$\overline{CE}_1$ LOW and CE <sub>2</sub> HIGH to Data Valid		55		70	ns
t <sub>DOE</sub>	$\overline{OE}$ LOW to Data Valid		20		35	ns
t <sub>LZOE</sub>	$\overline{OE}$ LOW to Low Z <sup>[6]</sup>	10		10		ns
t <sub>HZOE</sub>	$\overline{OE}$ HIGH to High Z <sup>[6, 7]</sup>		20		25	ns
t <sub>LZCE</sub>	$\overline{CE}_1$ LOW and CE <sub>2</sub> HIGH to Low Z <sup>[6]</sup>	10		10		ns
t <sub>HZCE</sub>	$\overline{CE}_1$ HIGH or CE <sub>2</sub> LOW to High Z <sup>[6, 7]</sup>		20		25	ns
t <sub>PU</sub>	$\overline{CE}_1$ LOW and CE <sub>2</sub> HIGH to Power-Up	0		0		ns
t <sub>PD</sub>	$\overline{CE}_1$ HIGH or CE <sub>2</sub> LOW to Power-Down		55		70	ns
<b>WRITE CYCLE<sup>[8,]</sup></b>						
t <sub>WC</sub>	Write Cycle Time	55		70		ns
t <sub>SCE</sub>	$\overline{CE}_1$ LOW and CE <sub>2</sub> HIGH to Write End	45		60		ns
t <sub>AW</sub>	Address Set-Up to Write End	45		60		ns
t <sub>HA</sub>	Address Hold from Write End	0		0		ns
t <sub>SA</sub>	Address Set-Up to Write Start	0		0		ns
t <sub>PWE</sub>	$\overline{WE}$ Pulse Width	45		55		ns
t <sub>SD</sub>	Data Set-Up to Write End	25		30		ns
t <sub>HD</sub>	Data Hold from Write End	0		0		ns
t <sub>HZWE</sub>	$\overline{WE}$ LOW to High Z <sup>[6, 7]</sup>		20		25	ns
t <sub>LZWE</sub>	$\overline{WE}$ HIGH to Low Z <sup>[6]</sup>	5		5		ns

Notes:

- Test conditions assume signal transition time of 5 ns or less, timing reference levels of  $V_{CC(typ.)}/2$ , input pulse levels of 0 to  $V_{CC(typ.)}$ , and output loading of the specified  $I_{OL}/I_{OH}$  and 30 pF load capacitance.
- At any given temperature and voltage condition, t<sub>HZCE</sub> is less than t<sub>LZCE</sub>, t<sub>HZOE</sub> is less than t<sub>LZOE</sub>, and t<sub>HZWE</sub> is less than t<sub>LZWE</sub> for any given device.
- t<sub>HZOE</sub>, t<sub>HZCE</sub>, and t<sub>HZWE</sub> transitions are measured when the outputs enter a high impedance state.
- The internal write time of the memory is defined by the overlap of  $\overline{WE}$ ,  $CE_1 = V_{IL}$  and  $CE_2 = V_{IH}$ . All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input set-up and hold timing should be referenced to the edge of the signal that terminates the write.

**Switching Waveforms**
**Read Cycle No. 1 (Address Transition Controlled) [9, 10]**

**Read Cycle No. 2 ( $\overline{OE}$  Controlled) [10, 11]**

**Notes:**

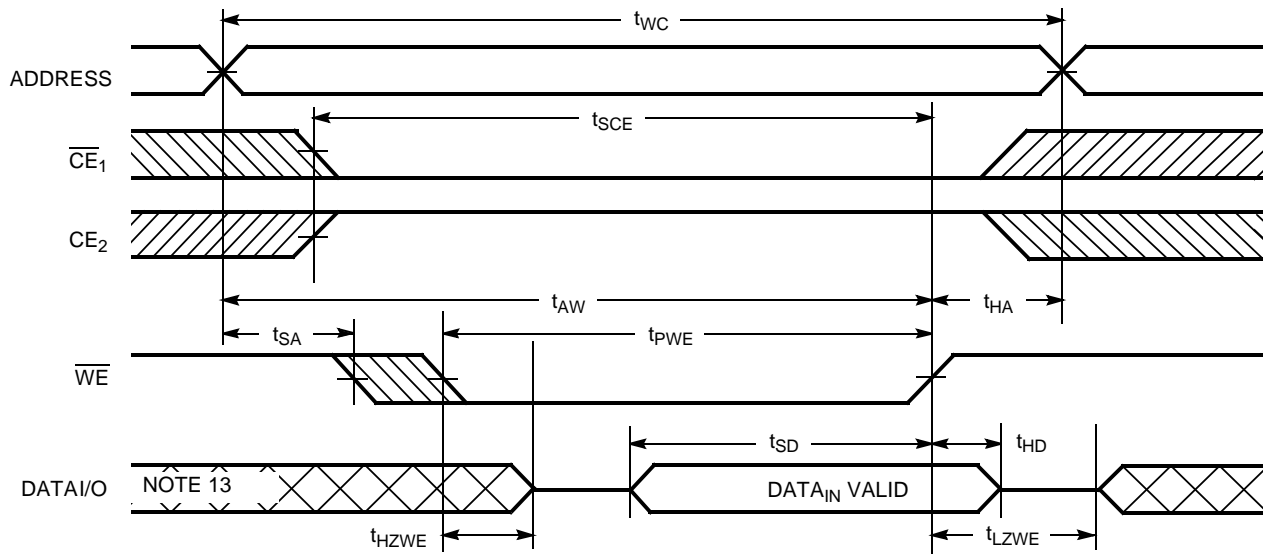
9. Device is continuously selected.  $\overline{OE}$ ,  $\overline{CE}_1 = V_{IL}$ ,  $CE_2 = V_{IH}$ .
10.  $\overline{WE}$  is HIGH for read cycle.
11. Address valid prior to or coincident with  $\overline{CE}_1$  transition LOW and  $CE_2$  transition HIGH.

**Switching Waveforms (continued)**
**Write Cycle No. 1 ( $\overline{\text{WE}}$  Controlled)** <sup>[8, 12, 14]</sup>

**Write Cycle No. 2 ( $\overline{\text{CE}}_1$  or  $\text{CE}_2$  Controlled)** <sup>[8, 12, 14]</sup>

**Notes:**

12. Data I/O is high impedance if  $\overline{\text{OE}} = V_{IH}$ .
13. During this period, the I/Os are in output state and input signals should not be applied.
14. If  $\overline{\text{CE}}_1$  goes HIGH and  $\text{CE}_2$  goes LOW simultaneously with WE HIGH, the output remains in a high-impedance state.

Switching Waveforms (continued)

Write Cycle No. 3 ( $\overline{WE}$  Controlled,  $\overline{OE}$  LOW)<sup>[14]</sup>







**Truth Table**

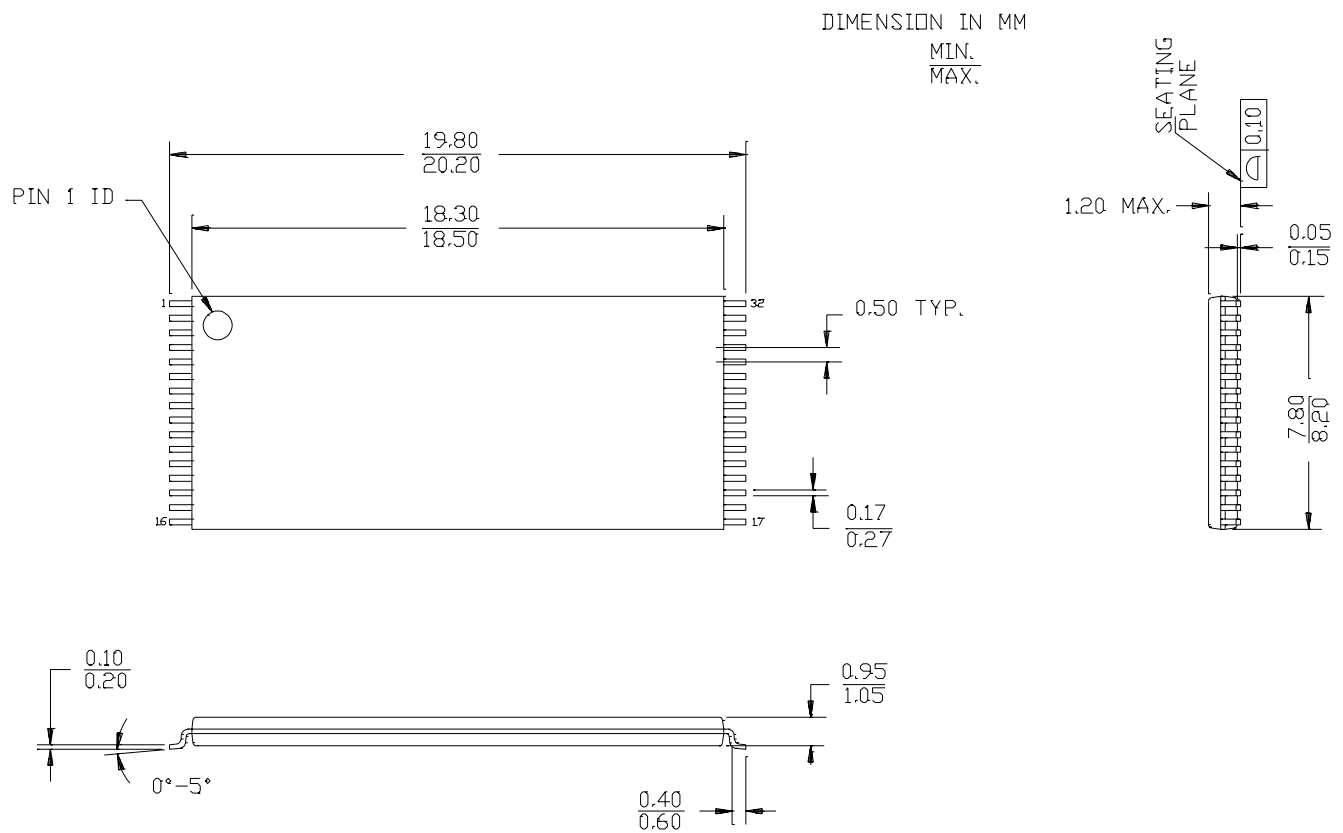
<b>CE<sub>1</sub></b>	<b>CE<sub>2</sub></b>	<b>WE</b>	<b>OE</b>	<b>Inputs/Outputs</b>	<b>Mode</b>	<b>Power</b>
H	X	X	X	High Z	Deselect/Power-Down	Standby (I <sub>SB</sub> )
X	L	X	X	High Z	Deselect/Power-Down	Standby (I <sub>SB</sub> )
L	H	H	L	Data Out	Read	Active (I <sub>CC</sub> )
L	H	L	X	Data In	Write	Active (I <sub>CC</sub> )
L	H	H	H	High Z	Output Disabled	Active (I <sub>CC</sub> )

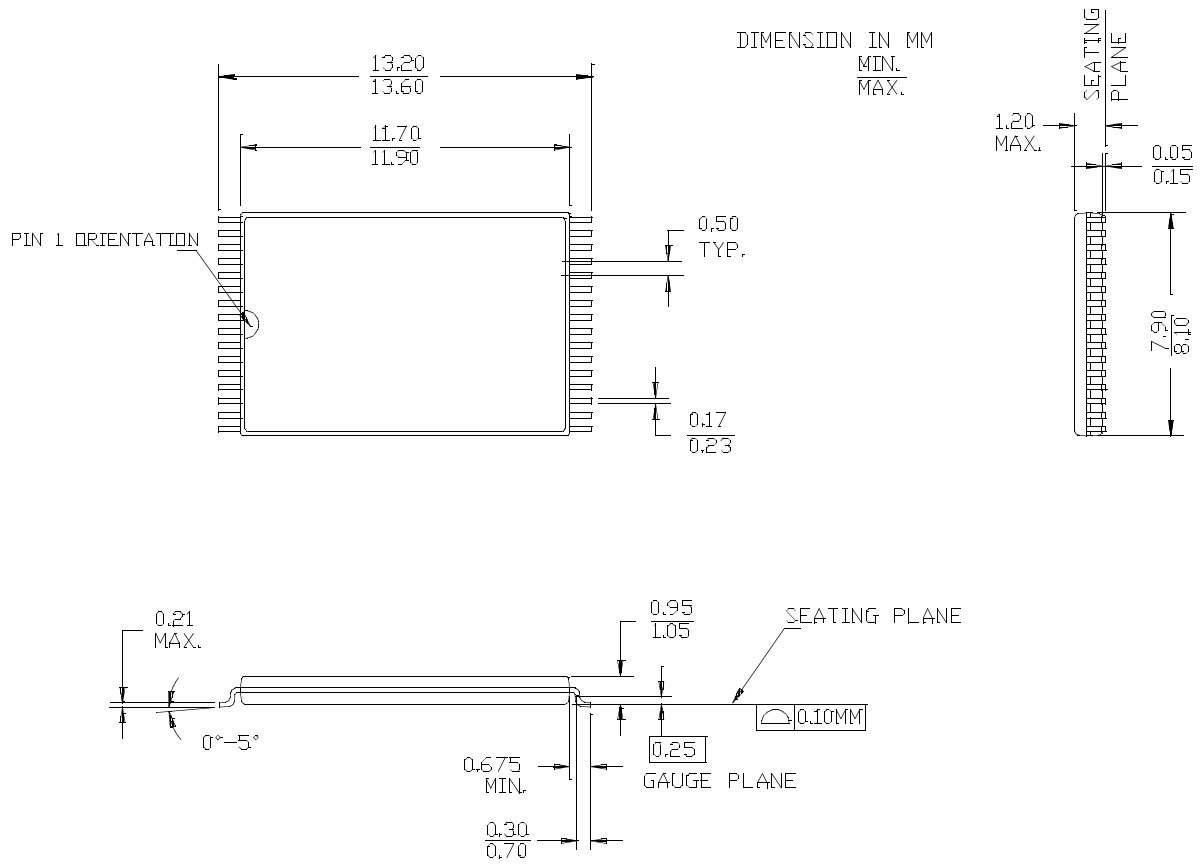
## Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
70	WCMA1008U1X-TF70	T32	32-Lead TSOP	Industrial
	WCMA1008U1X-SF70	S32	32-Lead STSOP	
55	WCMA1008U1X-TF55	T32	32-Lead TSOP	
	WCMA1008U1X-SF55	S32	32-Lead STSOP	

## Package Diagrams

### 32-Lead Thin Small Outline Package, T32



**Package Diagrams (continued)**
**32-Lead Shrunken Thin Small Outline Package, S32**




<b>Document Title: WCMA1008U1X, 128K x 8 Static RAM</b>					
<b>REV.</b>	<b>Spec #</b>	<b>ECN #</b>	<b>Issue Date</b>	<b>Orig. of Change</b>	<b>Description of Change</b>
**	38-14023	115246	4/24/2002	MGN	New Data Sheet

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С уважением,

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