

AT91SAM9261-EK Evaluation Board

User Guide





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Section 1

Overview

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|------------|--|---|
| 1.1 | Scope | <p>The AT91SAM9261-EK evaluation kit is an effective platform for evaluating chip performance and developing code for applications based on the AT91SAM9261.</p> <p>This guide is a description of the hardware included in the AT91SAM9261-EK evaluation kit. Software files are available on the DVD-ROM included in the kit and described in “Deliverables” below.</p> |
| <hr/> | | |
| 1.2 | Deliverables | <p>The AT91SAM9261-EK package contains the following items:</p> <ul style="list-style-type: none">■ an AT91SAM9261-EK board■ one A/B-type USB cable■ one serial RS232 cable■ one RJ45 crossed Ethernet cable■ universal input AC/DC power supply with US and EU plug adapter■ one DVD-ROM containing summary and full datasheets, datasheets with electrical and mechanical characteristics, application notes and getting started documents for all development boards and AT91 microcontrollers. An AT91 software package with C and assembly listings is also provided. This allows the user to begin evaluating the AT91 ARM® Thumb® 32-bit microcontroller quickly. |
| <hr/> | | |
| 1.3 | The AT91SAM9261-EK Evaluation Board | <p>The board is equipped with an AT91SAM9261 (217-ball LFBGA package) together with the following:</p> <ul style="list-style-type: none">■ 64 Mbytes of SDRAM memory■ 256 Mbytes of NAND Flash memory■ one Atmel® serial DataFlash®■ one USB device port interface■ two USB host port interfaces■ one DBGU serial communication port■ JTAG/ICE debug interface |

- one Ethernet 100-base TX with three status LEDs
- one Atmel AT73C213 Audio DAC
- one 3.5" 1/4 VGA TFT LCD Module with TouchScreen and backlight
- one Power LED and two general-purpose LEDs
- four user input pushbuttons
- one wakeup input pushbutton
- one reset pushbutton
- one DataFlash SD/MMC card slot
- two expansion footprint connectors (solder side)
- one Lithium Coin Cell Battery Retainer for 12 mm cell size
- dual pitch prototyping area

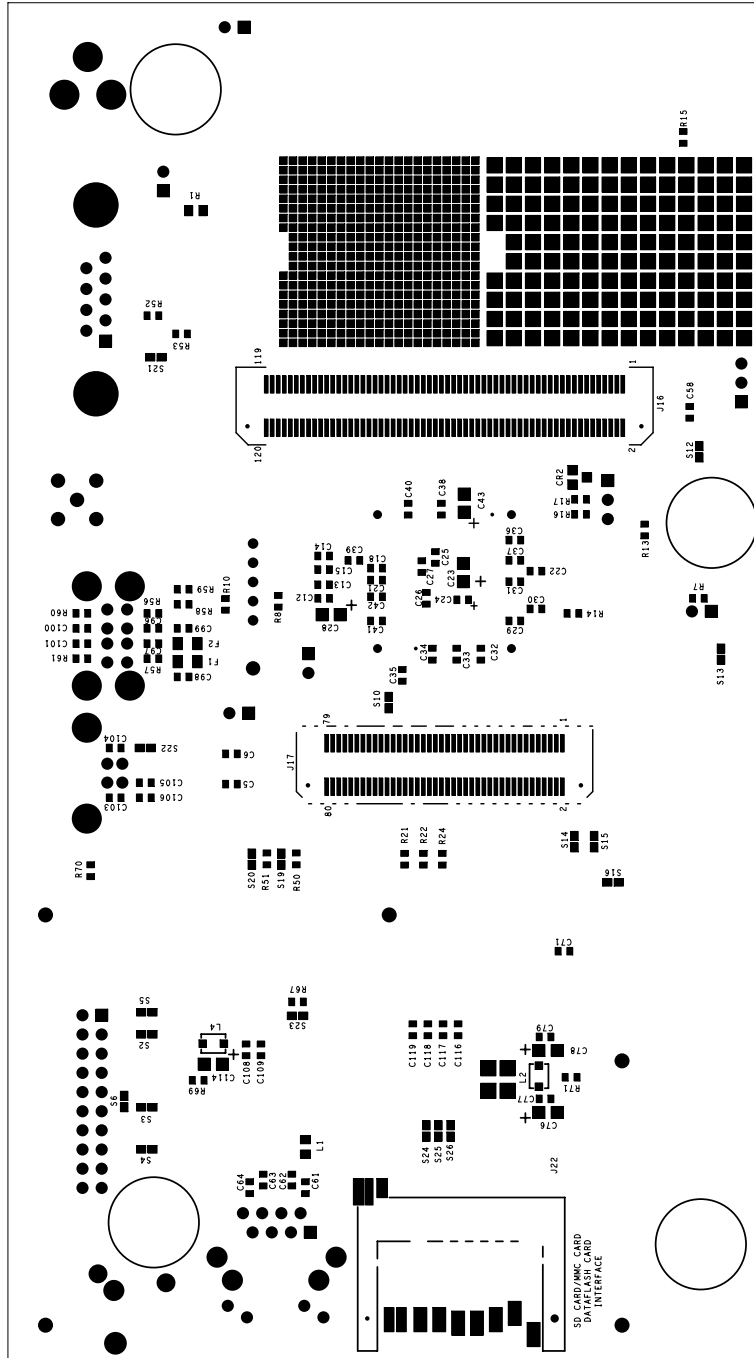


Section 2

Setting Up the AT91SAM9261-EK Evaluation Board

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|------------|------------------------------|---|
| 2.1 | Electrostatic Warning | The AT91SAM9261-EK evaluation board is shipped in a protective anti-static package. The board must not be subjected to high electrostatic potentials. A grounding strap or similar protective device should be worn when handling the board. Avoid touching the component pins or any other metallic element. |
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| 2.2 | Requirements | <p>In order to set up the AT91SAM9261-EK evaluation board, the following items are required:</p> <ul style="list-style-type: none">■ the AT91SAM9261-EK evaluation board itself■ AC/DC power adapter (5V at 2A), 2.1 mm by 5.5 mm |
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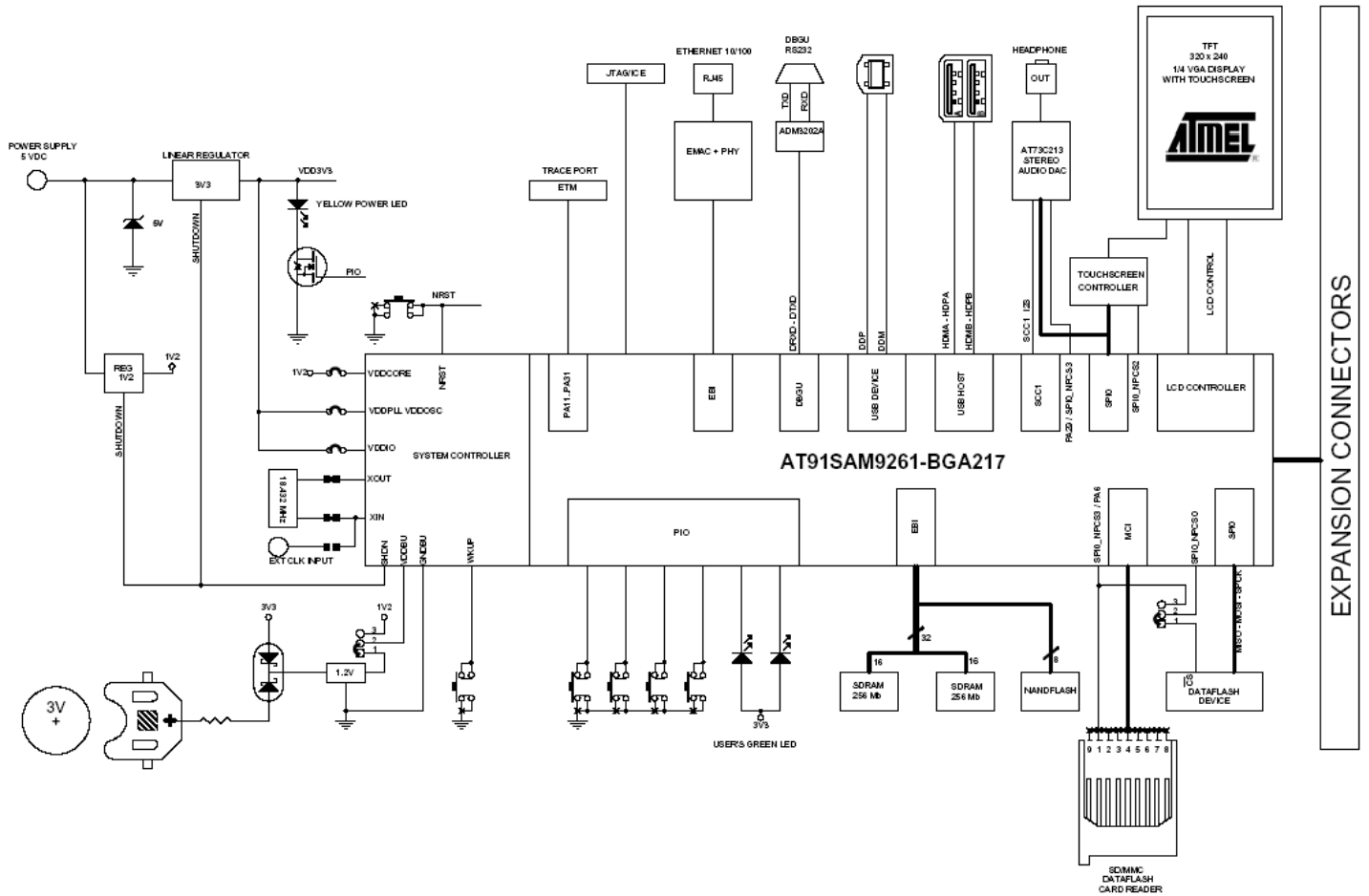
Figure 2-2. AT91SAM9261-EK Layout - Bottom View



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| 2.4 | Powering Up the Board | AT91SAM9261-EK requires 5V DC ($\pm 5\%$). DC power is supplied to the board via the 2.1 mm by 5.5 mm socket (J1). The coaxial power plug center pin is positive polarity . |
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| 2.5 | Backup Power Supply | <p>The user has the possibility to add a battery (3V Lithium Battery CR1225 or equivalent) in order to permanently power the backup part of the device. In this case, J9 configuration must to be set in position 1, 2.</p> <p>Refer to Table 4-1, "Configuration Jumpers and Straps".</p> |
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| 2.6 | Getting Started | The AT91SAM9261-EK evaluation board is delivered with one CD-ROM allowing the user to begin evaluating the AT91 ARM Thumb 32-bit microcontroller quickly. Please refer to the AT91 web site, www.atmel.com/products/AT91/ , for the most up-to-date information on getting started with the AT91SAM9261-EK. |
|------------|------------------------|---|
-

2.7 AT91SAM9261-EK Block Diagram

Figure 2-3. Block Diagram





Section 3

Board Description

- 3.1 AT91SAM9261 Microcontroller**
- Incorporates the ARM926EJ-S™ ARM Thumb Processor
 - DSP Instruction Extensions
 - ARM Jazelle® Technology for Java® Acceleration
 - 16-KByte Data Cache, 16-KByte Instruction Cache, Write Buffer
 - 200 MIPS at 180 MHz
 - Memory Management Unit
 - EmbeddedICE™ In-circuit Emulation, Debug Communication Channel Support
 - Mid-level implementation Embedded Trace Macrocell™
 - Additional Embedded Memories
 - 32K Bytes of Internal ROM, Single-cycle Access at Maximum Bus Speed
 - 160K Bytes of Internal SRAM, Single-cycle Access at Maximum Processor or Bus Speed
 - External Bus Interface (EBI)
 - Supports SDRAM, Static Memory, NAND Flash and CompactFlash®
 - LCD Controller
 - Supports Passive or Active Displays
 - Up to 16-bits per Pixel in STN Color Mode
 - Up to 16M Colors in TFT Mode (24-bit per Pixel), Resolution up to 2048 x 2048
 - USB
 - USB 2.0 Full Speed (12 Mbits per second) Host Double Port
 - Dual On-chip Transceivers
 - Integrated FIFOs and Dedicated DMA Channels
 - USB 2.0 Full Speed (12 Mbits per second) Device Port
 - On-chip Transceiver, 2-Kbyte Configurable Integrated FIFOs
 - Bus Matrix
 - Handles Five Masters and Five Slaves
 - Boot Mode Select Option

- Remap Command
- Fully Featured System Controller (SYSC) for Efficient System Management, including
 - Reset Controller, Shutdown Controller, Four 32-bit Battery Backup Registers for a Total of 16 Bytes
 - Clock Generator and Power Management Controller
 - Advanced Interrupt Controller and Debug Unit
 - Periodic Interval Timer, Watchdog Timer and Real-time Timer
 - Three 32-bit PIO Controllers
- Reset Controller (RSTC)
 - Based on Power-on Reset Cells, Reset Source Identification and Reset Output Control
- Shutdown Controller (SHDWC)
 - Programmable Shutdown Pin Control and Wake-up Circuitry
- Clock Generator (CKGR)
 - 32.768 kHz Low-power Oscillator on Battery Backup Power Supply, Providing a Permanent Slow Clock
 - 3 to 20 MHz On-chip Oscillator and two PLLs
- Power Management Controller (PMC)
 - Very Slow Clock Operating Mode, Software Programmable Power Optimization Capabilities
 - Four Programmable External Clock Signals
- Advanced Interrupt Controller (AIC)
 - Individually Maskable, Eight-level Priority, Vectored Interrupt Sources
 - Three External Interrupt Sources and One Fast Interrupt Source, Spurious Interrupt Protected
- Debug Unit (DBGU)
 - 2-wire USART and Support for Debug Communication Channel, Programmable ICE Access Prevention
- Periodic Interval Timer (PIT)
 - 20-bit Interval Timer plus 12-bit Interval Counter
- Watchdog Timer (WDT)
 - Key Protected, Programmable Only Once, Windowed 12-bit Counter, Running at Slow Clock
- Real-Time Timer (RTT)
 - 32-bit Free-running Backup Counter Running at Slow Clock
- Three 32-bit Parallel Input/Output Controllers (PIO) PIOA, PIOB and PIOC
 - 96 Programmable I/O Lines Multiplexed with up to Two Peripheral I/Os
 - Input Change Interrupt Capability on Each I/O Line
 - Individually Programmable Open-drain, Pull-up Resistor and Synchronous Output
- Nineteen Peripheral DMA (PDC) Channels

- Multimedia Card Interface (MCI)
 - Compliant with Multimedia Cards and SDCards
 - Automatic Protocol Control and Fast Automatic Data Transfers with PDC, MMC and SDCard Compliant
- Three Synchronous Serial Controllers (SSC)
 - Independent Clock and Frame Sync Signals for Each Receiver and Transmitter
 - I²S Analog Interface Support, Time Division Multiplex Support
 - High-speed Continuous Data Stream Capabilities with 32-bit Data Transfer
- Three Universal Synchronous/Asynchronous Receiver Transmitters (USART)
 - Individual Baud Rate Generator, IrDA[®] Infrared Modulation/Demodulation
 - Support for ISO7816 T0/T1 Smart Card, Hardware and Software Handshaking, RS485 Support
- Two Master/Slave Serial Peripheral Interface (SPI)
 - 8- to 16-bit Programmable Data Length, Four External Peripheral Chip Selects
- One Three-channel 16-bit Timer/Counters (TC)
 - Three External Clock Inputs, Two multi-purpose I/O Pins per Channel
 - Double PWM Generation, Capture/Waveform Mode, Up/Down Capability
- Two-wire Interface (TWI)
 - Master Mode Support, All Two-wire Atmel EEPROMs Supported
- IEEE[®] 1149.1 JTAG Boundary Scan on All Digital Pins
- Required Power Supplies:
 - 1.08V to 1.32V for VDDCORE and VDDBU
 - 3.0V to 3.6V for VDDOSC and for VDDPLL
 - 2.7V to 3.6V for VDDIOP (Peripheral I/Os)
 - 1.65V to 1.95V and 3.0V to 3.6V for VDDIOM (Memory I/Os)
- Available in a 217-ball LFBGA RoHS-compliant Package

Figure 3-1. Block Diagram



3.3	Memory	■ 32 Kbytes of Internal ROM ■ 160 Kbytes of Internal High-speed SRAM ■ Atmel serial DataFlash ■ 64 Mbytes of SDRAM memory ■ 256 Mbytes of NAND Flash memory
3.4	Clock Circuitry	■ 18.432 MHz standard crystal for the embedded oscillator ■ 32.768 kHz standard crystal for the slow clock oscillator
3.5	Reset Circuitry	■ Internal reset controller with a bi-directional reset pin ■ External reset push button
3.6	Shutdown Controller	■ Programmable shutdown and Wake-Up ■ Wake-up push button
3.7	Power Supply Circuitry	■ For dynamic power consumption, the AT91SAM9261 consumes a maximum of 50 mA on VDDCORE at maximum speed in typical conditions (1.2V, 25°C), processor running full-performance algorithm ■ On-board 1.2V high efficiency step-down charge pump regulator with shutdown control ■ On-board 3.3V linear regulator with shutdown control
3.8	Remote Communication	■ One Serial interface (DBGU COM Port) via RS-232 DB9 male socket ■ USB V2.0 Full-speed Compliant, 12 Mbits per second (UDP) ■ Two USB Host port V2.0 Full-speed Compliant, 12 Mbits per second (UHP) ■ One Ethernet 100-base TX with three status LEDs
3.9	Audio Stereo Interface	■ One Atmel stereo audio DAC AT73C213 ■ One 32 Ohm/20 mW Stereo Headset output (J20) with Master Volume and Mute Controls
3.10	User Interface	■ Four user input pushbuttons ■ Two user green LEDs ■ One yellow power LED (can be also software controlled)

- One ¼ VGA display LCD with Touchscreen and white LED backlight

3.11 Debug Interface

- 20-pin JTAG/ICE interface connector
- DBGU COM Port

3.12 Expansion Slot

- One DataFlash, SD/MMC card slot
- All I/Os of the AT91SAM9261 are routed to peripheral extension footprint connectors (J16 and J17). This allows the developer to check the integrity of the components and to extend the features of the board by adding external hardware components or boards.

3.13 PIO Usage

Table 3-1. PIO Controller A

I/O Line	Peripheral A	Peripheral B	Comments	
PA0	SPI0_MISO	MCDA0	SD/MMC/DATAFLASH SOCKET (J9) & DATAFLASH DEVICE & TOUCH SCREEN CONTROLLER & AUDIO DAC	SPI0_MISO or MCI0_DA0
PA1	SPI0_MOSI	MCCDA	SD/MMC/DATAFLASH SOCKET (J9) & DATAFLASH DEVICE & TOUCH SCREEN CONTROLLER & AUDIO DAC	SPI0_MOSI or MCI0_CDA
PA2	SPI0_SPCK	MCCK	SD/MMC/DATAFLASH SOCKET (J9) & DATAFLASH DEVICE & TOUCH SCREEN CONTROLLER & AUDIO DAC	SPI0_SPCK or MCCK
PA3	SPI0_NPCS0		DATAFLASH DEVICE or DATAFLASH SOCKET (J9)	SPI0_NPCS0
PA4	SPI0_NPCS1	MCDA1	SD/MMC/DATAFLASH SOCKET (J9)	MCDA1
PA5	SPI0_NPCS2	MCDA2	SD/MMC/DATAFLASH SOCKET (J9)	MCDA2
PA6	SPI0_NPCS3	MCDA3	SD/MMC/DATAFLASH SOCKET (J9)	SPI0_NPCS3 or MCDA3
PA7	TWD	PCK0		
PA8	TWCK	PCK1		
PA9	DRXD	PCK2	SERIAL DEBUG PORT (J15)	DRXD
PA10	DTXD	PCK3	SERIAL DEBUG PORT (J15)	DTXD
PA11	TSYNC	SCK1	TOUCH SCREEN CONTROLLER (MN16) BUSY	PA11
PA12	TCLK	RTS1	TFT PANEL CONTROL (J23) POWER CONTROL IN	PA12
PA13	TPS0	CTS1	GREEN USER'S LED 1 (DS8)	PA13
PA14	TPS1	SCK2	GREEN USER'S LED 2 (DS7)	PA14
PA15	TPS2	RTS2		
PA16	TPK0	CTS2		
PA17	TPK1	TF1	I2S AUDIO DAC AT73C213 (MN15) LRFS	TF1
PA18	TPK2	TK1	I2S AUDIO DAC AT73C213 (MN15) BCLK	TK1
PA19	TPK3	TD1	I2S AUDIO DAC AT73C213 (MN15) SDIN	TD1
PA20	TPK4	RD1		
PA21	TPK5	RK1		
PA22	TPK6	RF1		
PA23	TPK7	RTS0	YELLOW POWER LED CONTROL (DS1)	PA23
PA24	TPK8	SPI1_NPCS1	USER'S PUSH BUTTON INPUT (BP6)	PA24
PA25	TPK9	SPI1_NPCS2	USER'S PUSH BUTTON INPUT (BP5)	PA25
PA26	TPK10	SPI1_NPCS3	USER'S PUSH BUTTON INPUT (BP4)	PA26
PA27	TPK11	SPI0_NPCS1	USER'S PUSH BUTTON INPUT (BP3)	PA27
PA28	TPK12	SPI0_NPCS2	TOUCH SCREEN CONTROLLER (MN16)	SPI0_NPCS2
PA29	TPK13	SPI0_NPCS3	I2S AUDIO DAC AT73C213 (MN15)	SPI0_NPCS3
PA30	TPK14	A23		
PA31	TPK15	A24		

Table 3-2. PIO Controller B

I/O Line	Peripheral A	Peripheral B	Comments		
PB0	LCDVSYNC				
PB1	LCDHSYNC		TFT PANEL CONTROL (J23)	LCDHSYNC	
PB2	LCDDOTCK	PCK0	TFT PANEL CONTROL (J23)	LCDDOTCK	
PB3	LCDDEN		TFT PANEL CONTROL (J23)	LCDDEN	
PB4	LCDDCC	LCDD2	TFT PANEL CONTROL (J23) BACKLIGHT	LCDDCC	
PB5	LCDD0	LCDD3			
PB6	LCDD1	LCDD4			
PB7	LCDD2	LCDD5	TFT PANEL CONTROL (J23)	LCDD2	RED
PB8	LCDD3	LCDD6	TFT PANEL CONTROL (J23)	LCDD3	RED
PB9	LCDD4	LCDD7	TFT PANEL CONTROL (J23)	LCDD4	RED
PB10	LCDD5	LCDD10	TFT PANEL CONTROL (J23)	LCDD5	RED
PB11	LCDD6	LCDD11	TFT PANEL CONTROL (J23)	LCDD6	RED
PB12	LCDD7	LCDD12	TFT PANEL CONTROL (J23)	LCDD7	RED
PB13	LCDD8	LCDD13			
PB14	LCDD9	LCDD14			
PB15	LCDD10	LCDD15	TFT PANEL CONTROL (J23)	LCDD10	GREEN
PB16	LCDD11	LCDD19	TFT PANEL CONTROL (J23)	LCDD11	GREEN
PB17	LCDD12	LCDD20	TFT PANEL CONTROL (J23)	LCDD12	GREEN
PB18	LCDD13	LCDD21	TFT PANEL CONTROL (J23)	LCDD13	GREEN
PB19	LCDD14	LCDD22	TFT PANEL CONTROL (J23)	LCDD14	GREEN
PB20	LCDD15	LCDD23	TFT PANEL CONTROL (J23)	LCDD15	GREEN
PB21	TF0	LCDD16			
PB22	TK0	LCDD17			
PB23	TD0	LCDD18	TFT PANEL CONTROL (J23)	LCDD18	BLUE
PB24	RD0	LCDD19	TFT PANEL CONTROL (J23)	LCDD19	BLUE
PB25	RK0	LCDD20	TFT PANEL CONTROL (J23)	LCDD20	BLUE
PB26	RF0	LCDD21	TFT PANEL CONTROL (J23)	LCDD21	BLUE
PB27	SPI1_NPCS1	LCDD22	TFT PANEL CONTROL (J23)	LCDD22	BLUE
PB28	SPI1_NPCS0	LCDD23	TFT PANEL CONTROL (J23)	LCDD23	BLUE
PB29	SPI1_SPCK	IRQ2	USB DEVICE INTERFACE (J19) USB_CNX	PB29	
PB30	SPI1_MISO	IRQ1			
PB31	SPI1_MOSI	PCK2	I2S AUDIO DAC AT73C213 (MN15) MCLK	PCK2	

Table 3-3. PIO Controller C

I/O Line	Peripheral A	Peripheral B	Comments	
PC0	NANDOE	NCS6	NAND FLASH DEVICE (MN6x)	NANDOE
PC1	NANDWE	NCS7	NAND FLASH DEVICE (MN6x)	NANDWE
PC2	NWAIT	IRQ0	TOUCH SCREEN CONTROLLER (MN16) PENIRQ	IRQ0
PC3	A25/CFRNW			
PC4	NCS4/CFCS0			
PC5	NCS5/CFCS1			
PC6	CFCE1			
PC7	CFCE2			
PC8	TXD0	PCK2		
PC9	RXD0	PCK3		
PC10	RTS0	SCK0	ETHERNET CONTROLLER (MN8) RST	PC10
PC11	CTS0	FIQ	ETHERNET CONTROLLER (MN8) IRQ	PC11
PC12	TXD1	NCS6		
PC13	RXD1	NCS7		
PC14	TXD2	SPI1_NPCS2	NAND FLASH DEVICE (MN6x) CHIP ENABLE (CE)	PC14
PC15	RXD2	SPI1_NPCS3	NAND FLASH DEVICE (MN6x) READY/BUSY (R/B)	PC15
PC16	D16	TCLK0	EBI DATA BUS D16	D16
PC17	D17	TCLK1	EBI DATA BUS D17	D17
PC18	D18	TCLK2	EBI DATA BUS D18	D18
PC19	D19	TIOA0	EBI DATA BUS D19	D19
PC20	D20	TIOB0	EBI DATA BUS D20	D20
PC21	D21	TIOA1	EBI DATA BUS D21	D21
PC22	D22	TIOB1	EBI DATA BUS D22	D22
PC23	D23	TIOA2	EBI DATA BUS D23	D23
PC24	D24	TIOB2	EBI DATA BUS D24	D24
PC25	D25	TF2	EBI DATA BUS D25	D25
PC26	D26	TK2	EBI DATA BUS D26	D26
PC27	D27	TD2	EBI DATA BUS D27	D27
PC28	D28	RD2	EBI DATA BUS D28	D28
PC29	D29	RK2	EBI DATA BUS D29	D29
PC30	D30	RF2	EBI DATA BUS D30	D30
PC31	D31	PCK1	EBI DATA BUS D31	D31



Section 4

Configuration Straps

4.1 Configuration Straps

Table 4-1 gives details on configuration straps on the AT91SAM9261-EK evaluation board and their default settings.

Table 4-1. Configuration Jumpers and Straps

Designation	Default Setting	Feature
J2	Closed	3.3V Jumper ⁽¹⁾ This jumper footprint is provided for 3.3V power consumption measurement use. By default, it is closed. To use this feature, the user has to open the strap by cutting it before soldering a jumper.
J3	Closed	Forces power on. To use the software shutdown control, J3 must be opened.
J4	Opened	Enables Boot on the internal ROM
	Closed	Enables Boot on the NCS0
J8	Closed	VDDPLL Jumper ⁽¹⁾
J9	2-3	VDDBU Jumper select ⁽¹⁾ 1-2 : Lithium 3V Battery 2-3 : 1.2V from VDDCORE
J12	Closed	VDDCORE Jumper ⁽¹⁾
J21	1-2	NPCS0 select 1-2: DataFlash device (MN7) 2-3: DataFlash card interface (J22) Warning: In this case NPCS03 must be configured as input.
S2	Opened	Disables the ICE NTRST input
S3	Closed	Enables the ICE RTCK return. S6 must be opened
S4	Closed	Enables the ICE NRST input
S5	Opened	Selects ICE mode or JTAG mode (See Section 6, Errata)
S6	Opened	Disables TCK <-> RTCK local loop. If S6 is closed, S3 must be opened.

Table 4-1. Configuration Jumpers and Straps

Designation	Default Setting	Feature
S7-S8 S9	Closed	Enables the use of 18.432 MHz crystal. If external clock used, S7-S8 must be opened and S9 closed.
	Opened	
S10	Closed	Enables the use of SDRAM (NCS1_SDCS)
S12	Opened	Disables Serial DataFlash write protect.
S13	Closed	Disables NAND FLASH write protect.
S14	Closed	Enables the use of interrupt ETHERNET MAC (PC11_FIQ).
S15	Closed	Enables the use of ETHERNET MAC (NCS2).
S16	Opened	Disables the use of NWAIT ETHERNET MAC signal (PC2_NWAIT)
S19	Closed	Enables the use of the User LED DS7 (PA14)
S20	Closed	Enables the use of the User LED DS8 (PA13)
S21	Closed	Enables the use of the DBGU RXD signal (PA9)
S22	Closed	Enables the use of the USB CNX detection (PB29)
S23	Closed	Enables the use of AUDIO DAC INTERFACE (NPCS03)
S24	Closed	Enables the use of TOUCH SCEEN CONTROLLER (NPCS02)
S25	Closed	Enables the use of TOUCH SCEEN CONTROLLER BUSY signal (PA11)
S26	Closed	Enables the use of TOUCH SCEEN CONTROLLER PENIRQ (PC2_IRQ0)
TP1	N.A	3.3V Test point.
TP2	N.A	GND Test point.
TP3	N.A	1.2V Test point.
TP4	N.A	GND Test point.
TP63	N.A	0 to 3.3V analog user's input
TP64	N.A	0 to 3.3V analog user's input
TP65	N.A	AGND of TP63
TP66	N.A	AGND of TP64

Note: 1. These jumpers are provided for measuring power consumption. By default, they are closed. To use this feature, the user has to open the strap and insert an ammeter.



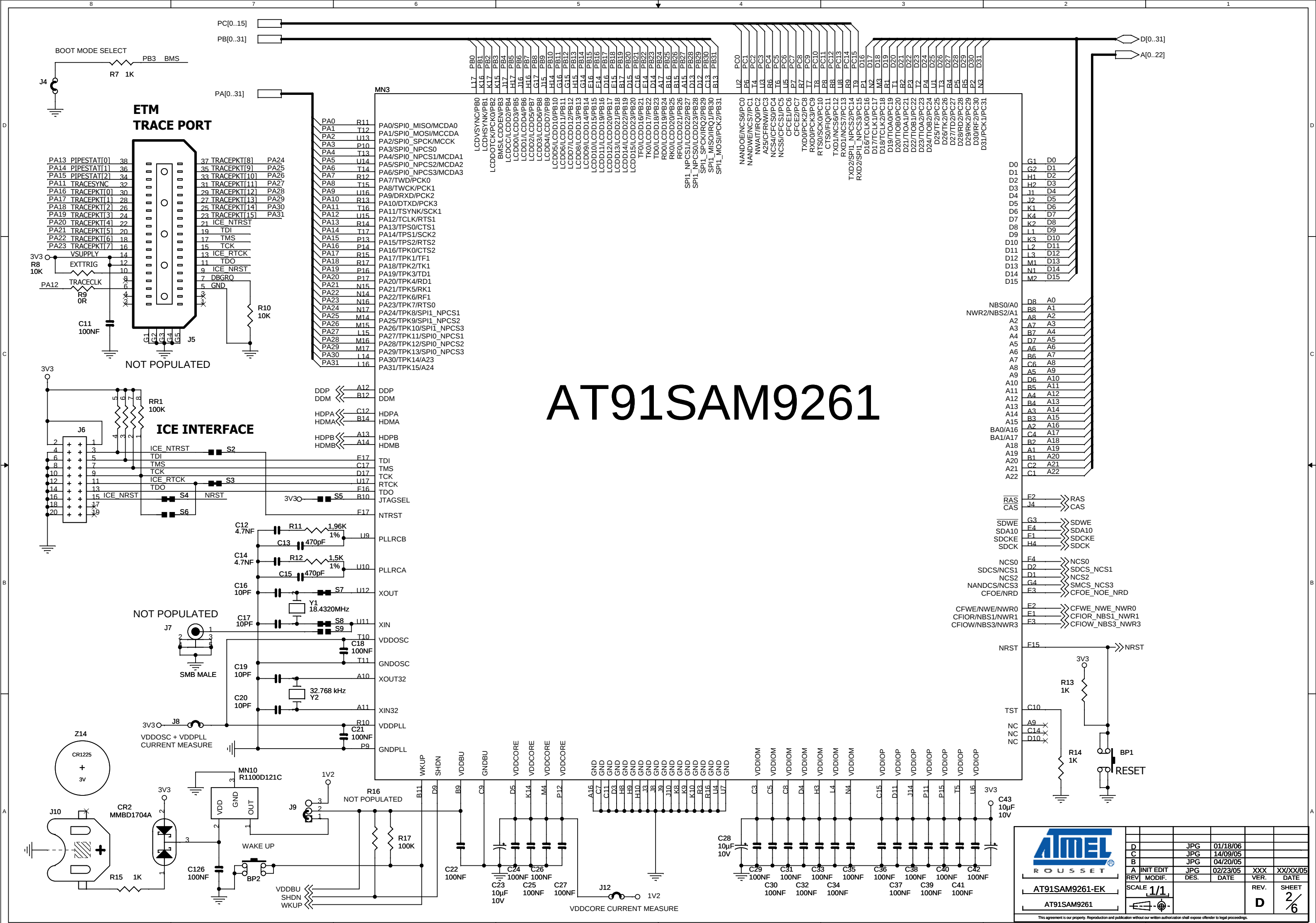
Section 5

Schematics

5.1 Schematics

This section contains the following schematics:

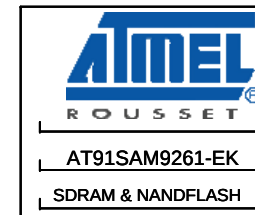
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- AT91SAM9261
- SDRAM and NAND Flash
- Ethernet
- LCD and User Interface
- Serial and I/O Expansion



EBI SDRAM INTERFACE

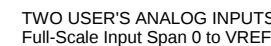
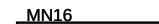
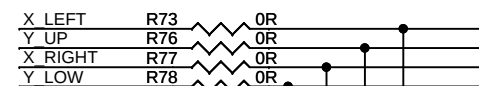
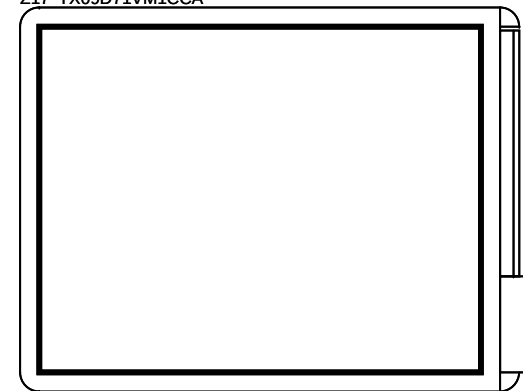
The diagram illustrates the EBI SDRAM Interface signals. It features a dashed rectangular frame. Inside, the signals are listed on the left, and their connections are shown on the right. The signals and their connections are as follows:

- A[0..22]**: Connected to a single horizontal line with a right-pointing arrowhead.
- D[0..31]**: Connected to a single horizontal line with a left-pointing arrowhead.
- RAS**: Connected to a horizontal line with a double left-pointing arrowhead.
- CAS**: Connected to a horizontal line with a double left-pointing arrowhead.
- SDWE**: Connected to a horizontal line with a double left-pointing arrowhead.
- SDA10**: Connected to a horizontal line with a double left-pointing arrowhead.
- SDCKE**: Connected to a horizontal line with a double left-pointing arrowhead.
- SDCK**: Connected to a horizontal line with a double left-pointing arrowhead.
- CFIOR_NBS1_NWR1**: Connected to a horizontal line with a double left-pointing arrowhead.
- CFIOW_NBS3_NWR3**: Connected to a horizontal line with a double left-pointing arrowhead.
- SDCS_NCS1**: Connected to a horizontal line with a double left-pointing arrowhead.



D	JPG	01/18/06			
C	JPG	14/09/05			
B	JPG	04/20/05			
A	INIT EDIT	JPG	02/23/05	XXX	XX/XX/05
REV	MODIF.	DES.	DATE	VER.	DATE
SCALE	<u>1/1</u>			REV.	SHEET 3 / 6
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The diagram shows the pinout for the AERA module, which is a 128-pin module. The pins are organized into four groups: PA[0..31], PB[0..31], PC[0..15], and D[0..31]. The module is connected to a 128-pin connector (J16) and a 128-pin connector (J17). The pinout for J16 is as follows:

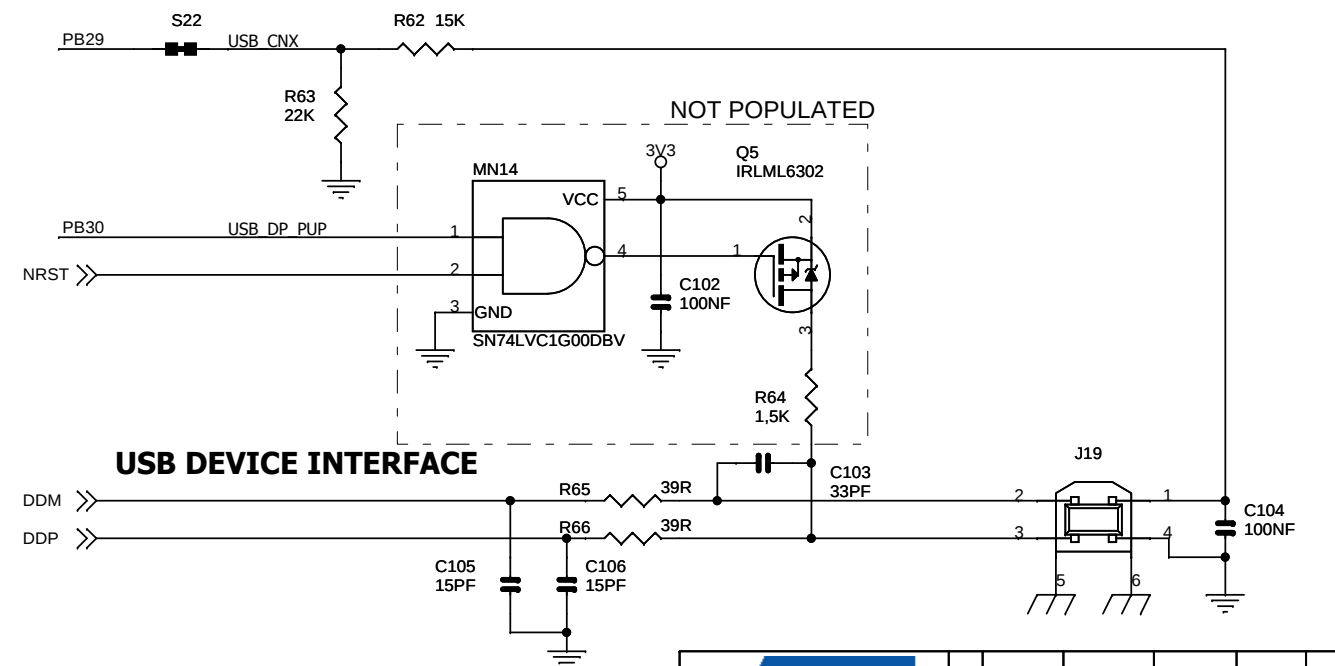
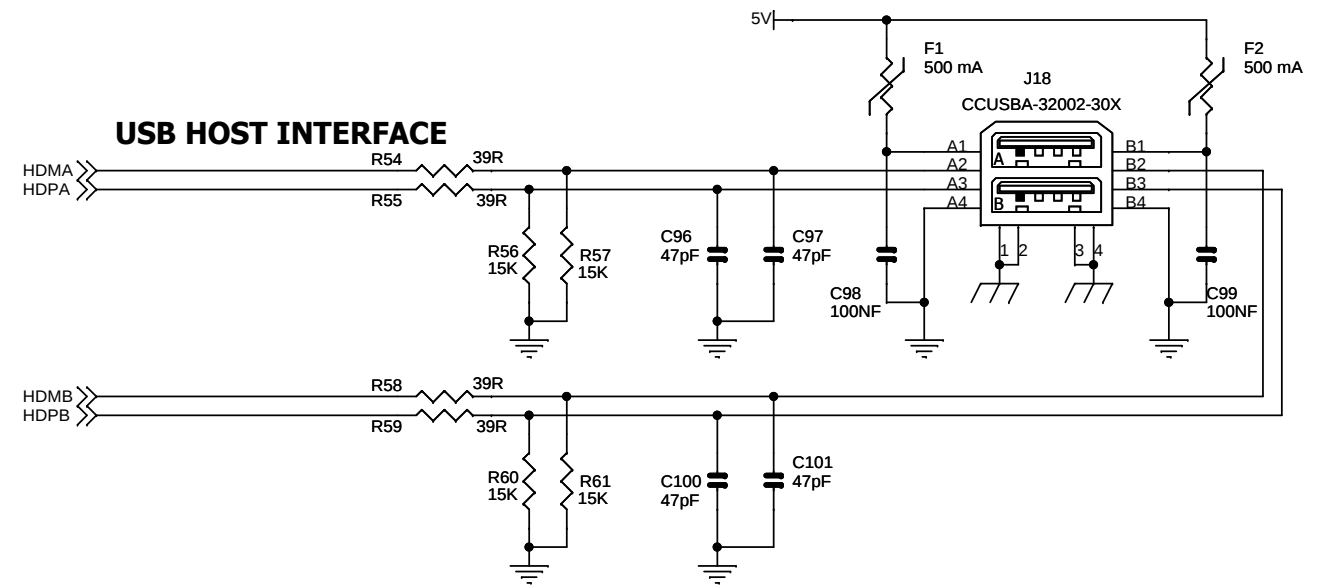
Pin	Signal	Pin	Signal
1	PA0	65	PA28
2	PA1	66	PA29
3	PA2	67	PA30
4	PA3	68	PA31
5	PA4	69	PC0
6	PA5	70	PC1
7	PA6	71	PC2
8	PA7	72	PC3
9	PA8	73	PC4
10	PA9	74	PC5
11	PA10	75	PC6
12	PA11	76	PC7
13	PA12	77	PC8
14	PA13	78	PC9
15	PA14	79	PC10
16	PA15	80	PC11
17	PA16	81	PC12
18	PA17	82	PC13
19	PA18	83	PC14
20	PA19	84	PC15
21	PA20	85	D16
22	PA21	86	D17
23	PA22	87	D18
24	PA23	88	D19
25	PA24	89	D20
26	PA25	90	D21
27	PA26	91	D22
28	PA27	92	D23
29	PA28	93	D24
30	PA29	94	D25
31	PA30	95	D26
32	PA31	96	D27
33	PC0	97	D28
34	PC1	98	D29
35	PC2	99	D30
36	PC3	100	D31
37	PC4	101	
38	PC5	102	
39	PC6	103	
40	PC7	104	
41	PC8	105	
42	PC9	106	
43	PC10	107	
44	PC11	108	
45	PC12	109	
46	PC13	110	
47	PC14	111	
48	PC15	112	
49		113	
50		114	
51		115	
52		116	
53		117	
54		118	
55		119	
56		120	

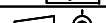
The pinout for J17 is as follows:

Pin	Signal	Pin	Signal
1	A1	65	PA28
2	A2	66	PA29
3	A3	67	PA30
4	A4	68	PA31
5	A5	69	PC0
6	A6	70	PC1
7	A7	71	PC2
8	A8	72	PC3
9	A9	73	PC4
10	A10	74	PC5
11	A11	75	PC6
12	A12	76	PC7
13	A13	77	PC8
14	A14	78	PC9
15	A15	79	PC10
16	A16	80	PC11
17	A17	81	PC12
18	A18	82	PC13
19	A19	83	PC14
20	A20	84	PC15
21	A21	85	D16
22	A22	86	D17
23		87	D18
24		88	D19
25		89	D20
26		90	D21
27		91	D22
28		92	D23
29		93	D24
30		94	D25
31		95	D26
32		96	D27
33		97	D28
34		98	D29
35		99	D30
36		100	D31
37		101	
38		102	
39		103	
40		104	
41		105	
42		106	
43		107	
44		108	
45		109	
46		110	
47		111	
48		112	
49		113	
50		114	
51		115	
52		116	
53		117	
54		118	
55		119	
56		120	

The USER'S GRID AERA is a 128-pin module. The pinout is as follows:

Pin	Signal	Pin	Signal
1	PA0	65	PA28
2	PA1	66	PA29
3	PA2	67	PA30
4	PA3	68	PA31
5	PA4	69	PC0
6	PA5	70	PC1
7	PA6	71	PC2
8			



	D	JPG	01/18/06			
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	B	JPG	04/20/05			
	A	INIT EDIT	JPG	02/23/05	XXX	XX/XX/05
	REV	MODIF.	DES.	DATE	VER.	DATE
	SCALE	1/1			REV.	SHEET
SERIAL & I/O EXPANSION				D	6/6	
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Section 6

Errata

-
- | | | |
|------------|--|--|
| 6.1 | JTAGSEL S5
Footprint
Selector | <p>For JTAG selection, the S5 footprint must never be soldered, else the chip can be damaged.</p> <p>By default, the JTAGSEL input pin integrates a pull-down resistor (ICE mode).</p> <p>To select JTAG mode, the designer should connect the JTAGSEL input pin to VDDBU power.</p> |
|------------|--|--|



Section 7

Revision History

7.1 Revision History

Table 7-1.

Document	Comments	Change Request Ref.
6198A	First issue.	
6198B	Removed DataFlash card from list in Section 1.2 "Deliverables" .	
	Removed references to 32-bit serial DataFlash, ref. AT45DB321C in Section 1.3 "The AT91SAM9261-EK Evaluation Board" , Figure 2-3 on page 5 "Block Diagram", Section 3.3 "Memory" , Table 4-1 "Configuration Jumpers and Straps" and in schematic 3/6 "SDRAM and NANDFLASH". In Figure 2-3 on page 5 "Block Diagram" changed size of NANDFlash to 2 Gb.	2733
	Specified TRACE PORT as NOT POPULATED in Figure 2-3 on page 5 "Block Diagram". Changed all instances of DNP to NOT POPULATED in Schematics 2/6 "AT91SAM9261", 4/6 "Ethernet" and 5/6 "LCD and User Interface".	2736
6198C	New Figure 2-1 "AT91SAM9261-EK Layout - Top View" and new Figure 2-2 "AT91SAM9261-EK Layout - Bottom View"	3542
	Updated Section 2.6 "Getting Started" .	
	In Section 2.3 "Layout" , updated Figure 2-3, "Block Diagram".	
	Added Section 3.13 "PIO Usage" .	
	In Section 4.1 "Configuration Straps" , updated Table 4-1, S5, with reference to Errata section.	
	Updated all schematics in Section 5.1 "Schematics" .	
	Added Section 6, Errata.	



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