EMBEDDED WRITE-BACK ENHANCED IntelDX4™ PROCESSOR

- **Up to 100 MHz Operation**
- **Integrated Floating-Point Unit**
- **Speed-Multiplying Technology**
- **32-Bit RISC Technology Core**
- **16-Kbyte Write-Back Cache**
- **3.3 V Core Operation with 5 V Tolerant I/O Buffers**
- **Burst Bus Cycles**
- **Dynamic Bus Sizing for 8- and 16-bit Data Bus Devices**
- **SL Technology**
- **Data Bus Parity Generation and Checking**
- **Boundary Scan (JTAG)**
- **3.3-Volt Processor, 75 MHz, 25 MHz CLK**
  - **208-Lead Shrink Quad Flat Pack (SQFP)**
- **3.3-Volt Processor, 100 MHz, 33 MHz CLK**
  - **208-Lead Shrink Quad Flat Pack (SQFP)**
  - **168-Pin Pin Grid Array (PGA)**
- **Binary Compatible with Large Software Base**

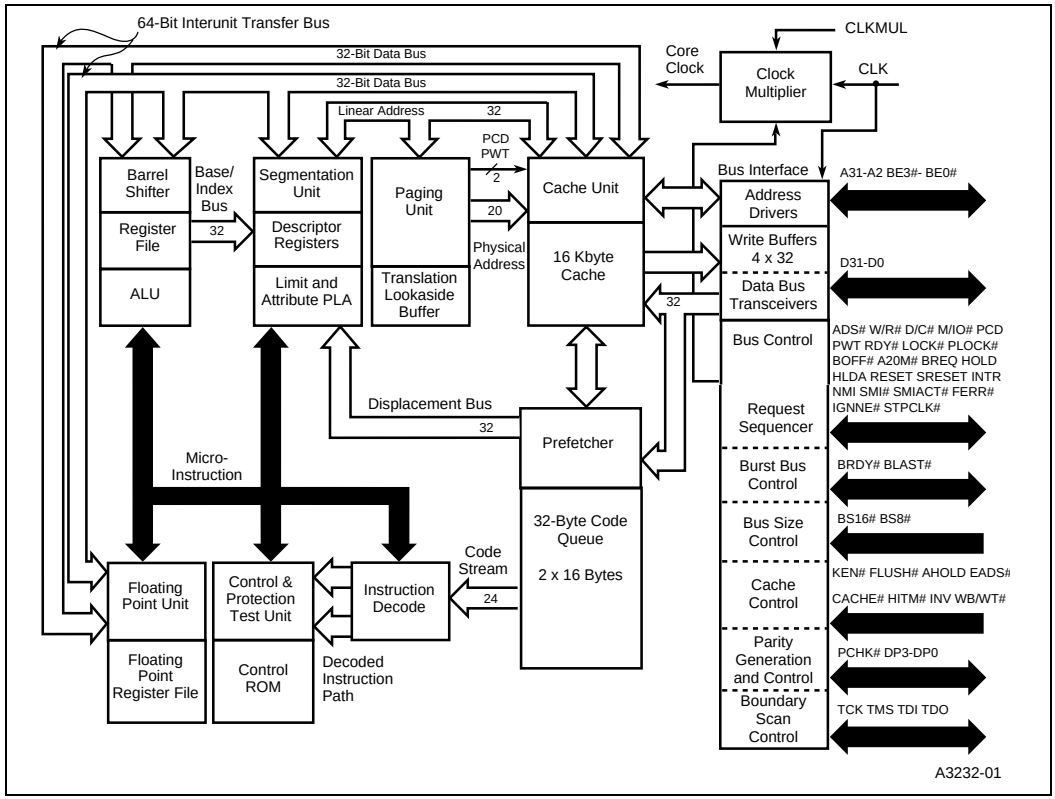


Figure 1. Embedded Write-Back Enhanced IntelDX4™ Processor Block Diagram

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Contact your local Intel sales office or your distributor to obtain the latest specifications and before placing your product order.

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EMBEDDED WRITE-BACK ENHANCED IntelDX4™ PROCESSOR

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1.0 INTRODUCTION

The embedded Write-Back Enhanced IntelDX4™ processor provides high performance to 32-bit, embedded applications. Designed for applications that need a floating-point unit, the processor is ideal for embedded designs running DOS*, Microsoft Windows*, OS/2*, or UNIX* applications written for the Intel architecture. Projects can be completed quickly using the wide range of software tools, utilities, assemblers and compilers that are available for desktop computer systems. Also, developers can find advantages in using existing chipsets and peripheral components in their embedded designs.

The Embedded Write-Back Enhanced IntelDX4 processor is binary compatible with the Intel386™ and earlier Intel processors. Compared with the Intel386 processor, it provides faster execution of many commonly-used instructions. It also provides the benefits of an integrated, 16-Kbyte, write-back cache for code and data. Its data bus can operate in burst mode which provides up to 106-Mbyte-per-second transfers for cache-line fills and instruction prefetches.

Intel's SL technology is incorporated in the Embedded Write-Back Enhanced IntelDX4 processor. Utilizing Intel's System Management Mode (SMM) enables designers to develop energy-efficient systems.

Two component packages are available:

- 168-pin Pin Grid Array (PGA)
- 208-lead Shrink Quad Flat Pack (SQFP)

The processor operates at either two or three times the external bus frequency. At two times the external bus frequency the processor operates up to 66 MHz, (33-MHz CLK). At three times the external bus frequency the processor operates up to 100 MHz (33-MHz CLK).

1.1 Features

The Embedded Write-Back Enhanced IntelDX4 processor offers these features:

- **32-bit RISC-Technology Core** — The Embedded Write-Back Enhanced IntelDX4 processor performs a complete set of arithmetic and logical operations on 8-, 16-, and 32-bit data types using a full-width ALU and eight general purpose registers.
- **Single Cycle Execution** — Many instructions execute in a single clock cycle.
- **Instruction Pipelining** — Overlapped instruction fetching, decoding, address translation and execution.
- **On-Chip Floating-Point Unit** — Intel486™ processors support the 32-, 64-, and 80-bit formats specified in IEEE standard 754. The unit is binary compatible with the 8087, Intel287™, Intel387™ coprocessors, and Intel OverDrive® processor.
- **On-Chip Cache with Cache Consistency Support** — A 16-Kbyte internal cache is used for both data and instructions. It is configurable to be write-back or write-through on a line-by-line basis. The internal cache implements a modified MESI protocol, which is applicable to uniprocessor systems. Cache hits provide zero wait-state access times for data within the cache. Bus activity is tracked to detect alterations in the memory represented by the internal cache. The internal cache can be invalidated or flushed so that an external cache controller can maintain cache consistency.
- **External Cache Control** — Write-back and flush controls for an external cache are provided so the processor can maintain cache consistency.
- **On-Chip Memory Management Unit** — Address management and memory space protection mechanisms maintain the integrity of memory in a multitasking and virtual memory environment. Both memory segmentation and paging are supported.
- **Burst Cycles** — Burst transfers allow a new double-word to be read from memory on each bus clock cycle. This capability is especially useful for instruction prefetch and for filling the internal cache. Data written from the processor to memory can also be burst transfers.
- **Write Buffers** — The processor contains four write buffers to enhance the performance of consecutive writes to memory. The processor can continue internal operations after a write to these buffers, without waiting for the write to be completed on the external bus.

- **Bus Backoff** — When another bus master needs control of the bus during a processor initiated bus cycle, the Embedded Write-Back Enhanced IntelDX4 processor floats its bus signals, then restarts the cycle when the bus becomes available again.
- **Instruction Restart** — Programs can continue execution following an exception generated by an unsuccessful attempt to access memory. This feature is important for supporting demand-paged virtual memory applications.
- **Dynamic Bus Sizing** — External controllers can dynamically alter the effective width of the data bus. Bus widths of 8, 16, or 32 bits can be used.
- **Boundary Scan (JTAG)** — Boundary Scan provides in-circuit testing of components on printed circuit boards. The Intel Boundary Scan implementation conforms with the IEEE Standard Test Access Port and Boundary Scan Architecture.
- **Enhanced Bus Mode** — The definitions of some signals have been changed to support write-back cache mode.

Intel's SL technology provides these features:

- **Intel System Management Mode (SMM)** — A unique Intel architecture operating mode provides a dedicated special purpose interrupt and address space that can be used to implement intelligent power management and other enhanced functions in a manner that is completely transparent to the operating system and applications software.
- **I/O Restart** — An I/O instruction interrupted by a System Management Interrupt (SMI#) can automatically be restarted following the execution of the RSM instruction.
- **Stop Clock** — The Embedded Write-Back Enhanced IntelDX4 processor has a stop clock control mechanism that provides two low-power states: a Stop Grant state (20–50 mA typical, depending on input clock frequency) and a Stop Clock state (~600 μA typical, with input clock frequency of 0 MHz).
- **Auto HALT Power Down** — After the execution of a HALT instruction, the Embedded Write-Back Enhanced IntelDX4 processor issues a normal Halt bus cycle and the clock input to the processor core is automatically stopped, causing the processor to enter the Auto HALT Power Down state (20–50 mA typical, depending on input clock frequency).
- **Auto Idle Power Down** — This function allows the processor to reduce the core frequency to the bus frequency when both the core and bus are idle. Auto Idle Power Down is software transparent and does not affect processor performance. Auto Idle Power Down provides an average power savings of 10% and is only applicable to clock multiplied processors.

1.2 Family Members

Table 1 shows the Embedded Write-Back Enhanced IntelDX4 processors and briefly describes their characteristics.

Table 1. The Embedded Write-Back Enhanced IntelDX4™ Processor Family

Product	Supply Voltage V_{CC}	Maximum Processor Frequency	Maximum External Bus Frequency	Package
x80486DX4WB75	3.3 V	75 MHz	25 MHz	208-Lead SQFP
x80486DX4WB100	3.3 V	100 MHz	33 MHz	208-Lead SQFP
x80486DX4WB100	3.3 V	100 MHz	33 MHz	168-Pin PGA

NOTE: To address the fact that many of the package prefix variables have changed, all package prefix variables in this document are now indicated with an "x".

2.0 HOW TO USE THIS DOCUMENT

For a complete set of documentation related to the Embedded Write-Back Enhanced IntelDX4 processor, use this document in conjunction with the following reference documents:

- *Embedded Intel486™ Processor Family Developer's Manual* — Order No. 273021
- *Embedded Intel486™ Processor Hardware Reference Manual* — Order No. 273025
- *Intel486 Microprocessor Family Programmer's Reference Manual* — Order No. 240486
- Intel Application Note AP-485 — *Intel Processor Identification with the CPUID Instruction* — Order No. 241618

The information in the reference documents for the IntelDX4 processor applies to the Embedded Write-Back Enhanced IntelDX4 processor. Some of the IntelDX4 processor information is duplicated in this document to minimize the dependence on the reference documents.

3.0 PIN DESCRIPTIONS

3.1 Pin Assignments

The following figures and tables show the pin assignments of each package type for the Embedded Write-Back Enhanced IntelDX4 processor. Tables are provided showing the pin differences between the Embedded Write-Back Enhanced IntelDX4 processor and other embedded Intel486 processor products.

208-Lead SQFP - Quad Flat Pack

- Figure 2, Package Diagram for 208-Lead SQFP Embedded Write-Back Enhanced IntelDX4™ Processor (pg. 4)
- Table 2, Pinout Differences for 208-Lead SQFP Package (pg. 5)
- Table 3, Pin Assignment for 208-Lead SQFP Package (pg. 6)
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168-Pin PGA - Pin Grid Array

- Figure 3, Package Diagram for 168-Pin PGA Embedded Write-Back Enhanced IntelDX4™ Processor (pg. 10)
- Table 5, Pinout Differences for 168-Pin PGA Package (pg. 11)
- Table 6, Pin Assignment for 168-Pin PGA Package (pg. 12)
- Table 7, Pin Cross Reference for 168-Pin PGA Package (pg. 14)

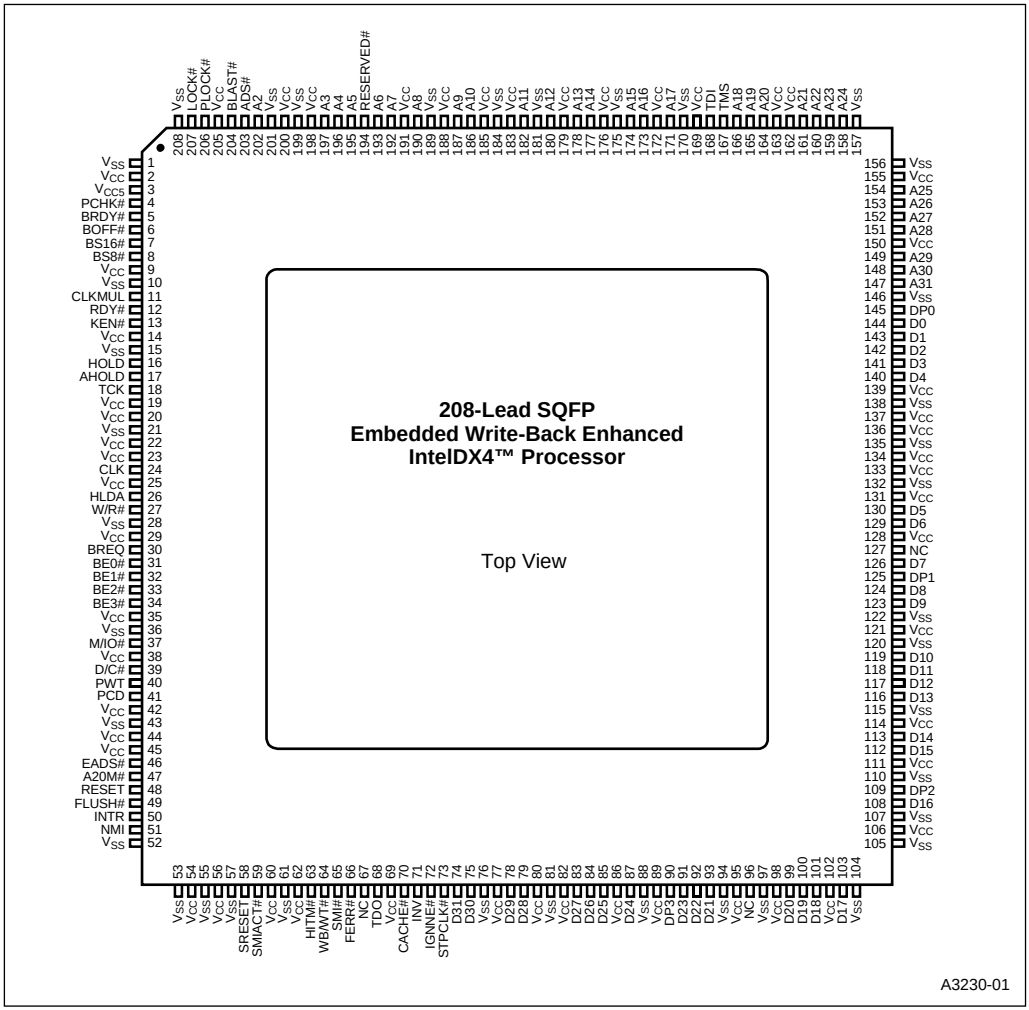


Figure 2. Package Diagram for 208-Lead SQFP Embedded Write-Back Enhanced IntelDX4™ Processor

Table 2. Pinout Differences for 208-Lead SQFP Package

Pin #	Embedded Intel486™ SX Processor	Embedded IntelDX2™ Processor	Embedded Write-Back Enhanced IntelDX4™ Processor
3	V_{CC}[1]	V_{CC}	V_{CC5}
11	INC[2]	INC	CLKMUL
63	INC	INC	HITM#
64	INC	INC	WB/WT#
66	INC	FERR#	FERR#
70	INC	INC	CACHE#
71	INC	INC	INV
72	INC	IGNNE#	IGNNE#

NOTES:

1. This pin location is for the V_{CC5} pin on the embedded IntelDX4 processor. For compatibility with 3.3V processors that have 5V-tolerant input buffers (i.e., embedded IntelDX4 processors), this pin should be connected to a V_{CC} trace, not to the V_{CC} plane.
2. INC. Internal No Connect. These pins are not connected to any internal pad. However, signals are defined for the location of the INC pins in the embedded IntelDX4 processor. One system design can accommodate any one of these processors provided the purpose of each INC pin is understood before it is used.

Table 3. Pin Assignment for 208-Lead SQFP Package (Sheet 1 of 2)

Pin#	Description	Pin#	Description	Pin#	Description	Pin#	Description
1	V_{SS}	53	V_{SS}	105	V_{SS}	157	V_{SS}
2	V_{CC}	54	V_{CC}	106	V_{CC}	158	A24
3	V_{CC5}	55	V_{SS}	107	V_{SS}	159	A23
4	PCHK#	56	V_{CC}	108	D16	160	A22
5	BRDY#	57	V_{SS}	109	DP2	161	A21
6	BOFF#	58	SRESET	110	V_{SS}	162	V_{CC}
7	BS16#	59	SMIACT#	111	V_{CC}	163	V_{CC}
8	BS8#	60	V_{CC}	112	D15	164	A20
9	V_{CC}	61	V_{SS}	113	D14	165	A19
10	V_{SS}	62	V_{CC}	114	V_{CC}	166	A18
11	CLKMUL	63	HITM#	115	V_{SS}	167	TMS
12	RDY#	64	WB/WT#	116	D13	168	TDI
13	KEN#	65	SMI#	117	D12	169	V_{CC}
14	V_{CC}	66	FERR#	118	D11	170	V_{SS}
15	V_{SS}	67	NC[1]	119	D10	171	A17
16	HOLD	68	TDO	120	V_{SS}	172	V_{CC}
17	AHOLD	69	V_{CC}	121	V_{CC}	173	A16
18	TCK	70	CACHE#	122	V_{SS}	174	A15
19	V_{CC}	71	INV	123	D9	175	V_{SS}
20	V_{CC}	72	IGNNE#	124	D8	176	V_{CC}
21	V_{SS}	73	STPCLK#	125	DP1	177	A14
22	V_{CC}	74	D31	126	D7	178	A13
23	V_{CC}	75	D30	127	NC[1]	179	V_{CC}
24	CLK	76	V_{SS}	128	V_{CC}	180	A12
25	V_{CC}	77	V_{CC}	129	D6	181	V_{SS}
26	HLDA	78	D29	130	D5	182	A11
27	W/R#	79	D28	131	V_{CC}	183	V_{CC}
28	V_{SS}	80	V_{CC}	132	V_{SS}	184	V_{SS}
29	V_{CC}	81	V_{SS}	133	V_{CC}	185	V_{CC}
30	BREQ	82	V_{CC}	134	V_{CC}	186	A10
31	BE0#	83	D27	135	V_{SS}	187	A9
32	BE1#	84	D26	136	V_{CC}	188	V_{CC}
33	BE2#	85	D25	137	V_{CC}	189	V_{SS}
34	BE3#	86	V_{CC}	138	V_{SS}	190	A8
35	V_{CC}	87	D24	139	V_{CC}	191	V_{CC}

Table 3. Pin Assignment for 208-Lead SQFP Package (Sheet 2 of 2)

Pin#	Description	Pin#	Description	Pin#	Description	Pin#	Description
36	V_{SS}	88	V_{SS}	140	D4	192	A7
37	M/IO#	89	V_{CC}	141	D3	193	A6
38	V_{CC}	90	DP3	142	D2	194	RESERVED#
39	D/C#	91	D23	143	D1	195	A5
40	PWT	92	D22	144	D0	196	A4
41	PCD	93	D21	145	DP0	197	A3
42	V_{CC}	94	V_{SS}	146	V_{SS}	198	V_{CC}
43	V_{SS}	95	V_{CC}	147	A31	199	V_{SS}
44	V_{CC}	96	NC[1]	148	A30	200	V_{CC}
45	V_{CC}	97	V_{SS}	149	A29	201	V_{SS}
46	EADS#	98	V_{CC}	150	V_{CC}	202	A2
47	A20M#	99	D20	151	A28	203	ADS#
48	RESET	100	D19	152	A27	204	BLAST#
49	FLUSH#	101	D18	153	A26	205	V_{CC}
50	INTR	102	V_{CC}	154	A25	206	PLOCK#
51	NMI	103	D17	155	V_{CC}	207	LOCK#
52	V_{SS}	104	V_{SS}	156	V_{SS}	208	V_{SS}

NOTE:

1. NC. Do Not Connect. These pins should always remain unconnected. Connection of NC pins to V_{CC}, or V_{SS} or to any other signal can result in component malfunction or incompatibility with future steppings of the Intel486 processors.

Table 4. Pin Cross Reference for 208-Lead SQFP Package (Sheet 1 of 2)

Address	Pin #	Data	Pin #	Control	Pin #	NC	V_{CC5}	V_{CC}	V_{SS}
A2	202	D0	144	A20M#	47	67	3	2	1
A3	197	D1	143	ADS#	203	96		9	10
A4	196	D2	142	AHOLD	17	127		14	15
A5	195	D3	141	BE0#	31			19	21
A6	193	D4	140	BE1#	32			20	28
A7	192	D5	130	BE2#	33			22	36
A8	190	D6	129	BE3#	34			23	43
A9	187	D7	126	BLAST#	204			25	52
A10	186	D8	124	BOFF#	6			29	53
A11	182	D9	123	BRDY#	5			35	55
A12	180	D10	119	BREQ	30			38	57
A13	178	D11	118	BS16#	7			42	61
A14	177	D12	117	BS8#	8			44	76
A15	174	D13	116	CACHE#	70			45	81
A16	173	D14	113	CLK	24			54	88
A17	171	D15	112	CLKMUL	11			56	94
A18	166	D16	108	D/C#	39			60	97
A19	165	D17	103	DP0	145			62	104
A20	164	D18	101	DP1	125			69	105
A21	161	D19	100	DP2	109			77	107
A22	160	D20	99	DP3	90			80	110
A23	159	D21	93	EADS#	46			82	115
A24	158	D22	92	FERR#	66			86	120
A25	154	D23	91	FLUSH#	49			89	122
A26	153	D24	87	HITM#	63			95	132
A27	152	D25	85	HLDA	26			98	135
A28	151	D26	84	HOLD	16			102	138
A29	149	D27	83	IGNNE#	72			106	146
A30	148	D28	79	INTR	50			111	156
A31	147	D29	78	INV	71			114	157
		D30	75	KEN#	13			121	170
		D31	74	LOCK#	207			128	175
				M/IO#	37			131	181

Table 4. Pin Cross Reference for 208-Lead SQFP Package (Sheet 2 of 2)

Address	Pin #	Data	Pin #	Control	Pin #	NC	V_{CC5}	V_{CC}	V_{SS}
				NMI	51			133	184
				PCD	41			134	189
				PCHK#	4			136	199
				PLOCK#	206			137	201
				PWT	40			139	208
				RDY#	12			150	
				RESERVED#	194			155	
				RESET	48			162	
				SMI#	65			163	
				SMIACT#	59			169	
				SRESET	58			172	
				STPCLK#	73			176	
				TCK	18			179	
				TDI	168			183	
				TDO	68			185	
				TMS	167			188	
				WB/WT#	64			191	
				W/R#	27			198	
								200	
								205	

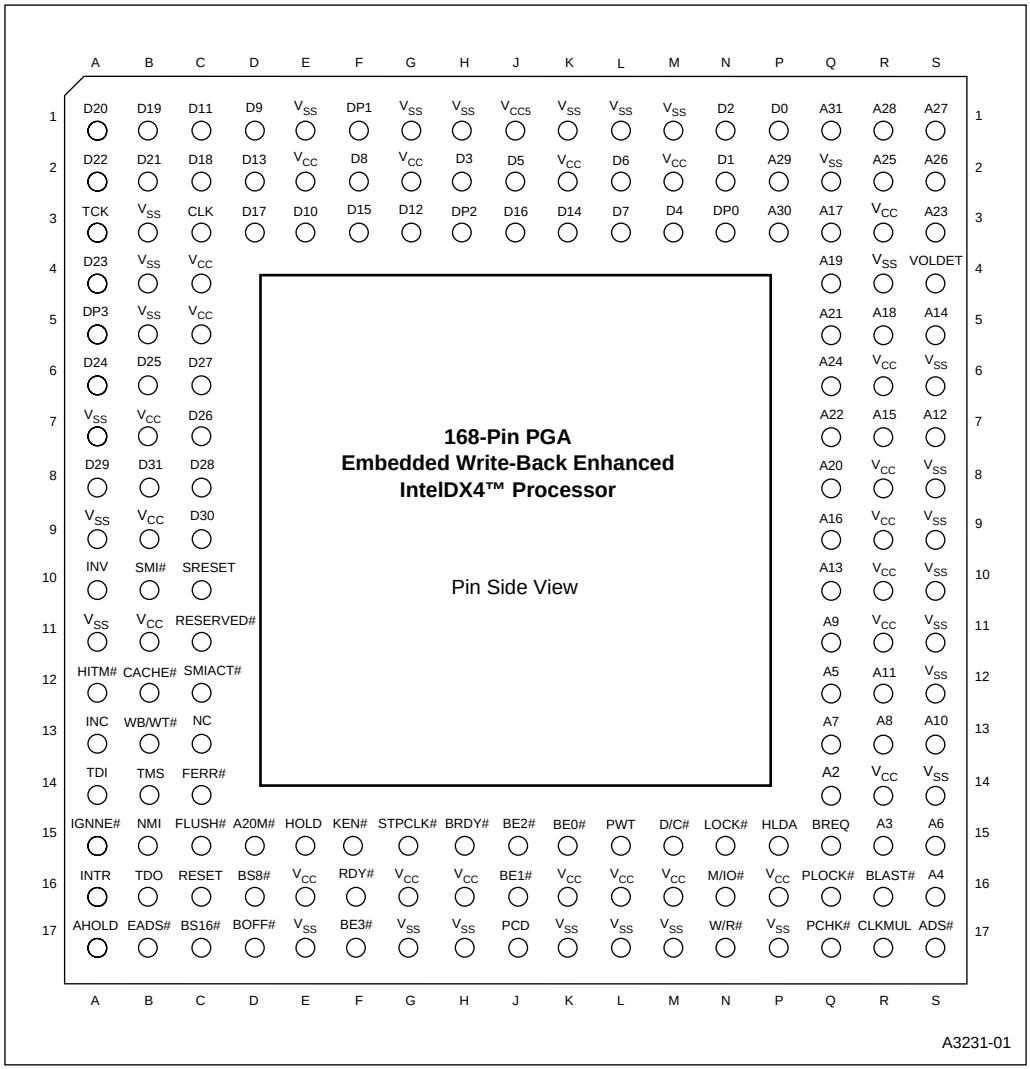


Figure 3. Package Diagram for 168-Pin PGA Embedded Write-Back Enhanced IntelDX4™ Processor

Table 5. Pinout Differences for 168-Pin PGA Package

Pin #	Embedded IntelDX2™ Processor	Embedded Write-Back Enhanced IntelDX4™ Processor
A10	INC	INV
A12	INC	HITM#
B12	INC	CACHE#
B13	INC	WB/WT#
J1	V_{CC}	V_{CC5}
R17	INC	CLKMUL
S4	NC	VOLDET

Table 6. Pin Assignment for 168-Pin PGA Package (Sheet 1 of 2)

Pin #	Description	Pin #	Description	Pin #	Description
A1	D20	D17	BOFF#	P2	A29
A2	D22	E1	V_{SS}	P3	A30
A3	TCK	E2	V_{CC}	P15	HLDA
A4	D23	E3	D10	P16	V_{CC}
A5	DP3	E15	HOLD	P17	V_{SS}
A6	D24	E16	V_{CC}	Q1	A31
A7	V_{SS}	E17	V_{SS}	Q2	V_{SS}
A8	D29	F1	DP1	Q3	A17
A9	V_{SS}	F2	D8	Q4	A19
A10	INV	F3	D15	Q5	A21
A11	V_{SS}	F15	KEN#	Q6	A24
A12	HITM#	F16	RDY#	Q7	A22
A13	INC	F17	BE3#	Q8	A20
A14	TDI	G1	V_{SS}	Q9	A16
A15	IGNNE#	G2	V_{CC}	Q10	A13
A16	INTR	G3	D12	Q11	A9
A17	AHOLD	G15	STPCLK#	Q12	A5
B1	D19	G16	V_{CC}	Q13	A7
B2	D21	G17	V_{SS}	Q14	A2
B3	V_{SS}	H1	V_{SS}	Q15	BREQ
B4	V_{SS}	H2	D3	Q16	PLOCK#
B5	V_{SS}	H3	DP2	Q17	PCHK#
B6	D25	H15	BRDY#	R1	A28
B7	V_{CC}	H16	V_{CC}	R2	A25
B8	D31	H17	V_{SS}	R3	V_{CC}
B9	V_{CC}	J1	V_{CC5}	R4	V_{SS}
B10	SMI#	J2	D5	R5	A18
B11	V_{CC}	J3	D16	R6	V_{CC}
B12	CACHE#	J15	BE2#	R7	A15
B13	WB/WT#	J16	BE1#	R8	V_{CC}
B14	TMS	J17	PCD	R9	V_{CC}
B15	NMI	K1	V_{SS}	R10	V_{CC}
B16	TDO	K2	V_{CC}	R11	V_{CC}
B17	EADS#	K3	D14	R12	A11
C1	D11	K15	BE0#	R13	A8
C2	D18	K16	V_{CC}	R14	V_{CC}
C3	CLK	K17	V_{SS}	R15	A3
C4	V_{CC}	L1	V_{SS}	R16	BLAST#
C5	V_{CC}	L2	D6	R17	CLKMUL

Table 6. Pin Assignment for 168-Pin PGA Package (Sheet 2 of 2)

Pin #	Description	Pin #	Description	Pin #	Description
C6	D27	L3	D7	S1	A27
C7	D26	L15	PWT	S2	A26
C8	D28	L16	V_{CC}	S3	A23
C9	D30	L17	V_{SS}	S4	VOLDET
C10	SRESET	M1	V_{SS}	S5	A14
C11	RESERVED#	M2	V_{CC}	S6	V_{SS}
C12	SMIACT#	M3	D4	S7	A12
C13	NC	M15	D/C#	S8	V_{SS}
C14	FERR#	M16	V_{CC}	S9	V_{SS}
C15	FLUSH#	M17	V_{SS}	S10	V_{SS}
C16	RESET	N1	D2	S11	V_{SS}
C17	BS16#	N2	D1	S12	V_{SS}
D1	D9	N3	DP0	S13	A10
D2	D13	N15	LOCK#	S14	V_{SS}
D3	D17	N16	M/IO#	S15	A6
D15	A20M#	N17	W/R#	S16	A4
D16	BS8#	P1	D0	S17	ADS#

Table 7. Pin Cross Reference for 168-Pin PGA Package (Sheet 1 of 2)

Address	Pin #	Data	Pin #	Control	Pin #	NC	INC	Vcc5	Vcc	Vss
A2	Q14	D0	P1	A20M#	D15	C13	A13	J1	B7	A7
A3	R15	D1	N2	ADS#	S17				B9	A9
A4	S16	D2	N1	AHOLD	A17				B11	A11
A5	Q12	D3	H2	BE0#	K15				C4	B3
A6	S15	D4	M3	BE1#	J16				C5	B4
A7	Q13	D5	J2	BE2#	J15				E2	B5
A8	R13	D6	L2	BE3#	F17				E16	E1
A9	Q11	D7	L3	BLAST#	R16				G2	E17
A10	S13	D8	F2	BOFF#	D17				G16	G1
A11	R12	D9	D1	BRDY#	H15				H16	G17
A12	S7	D10	E3	BREQ	Q15				K2	H1
A13	Q10	D11	C1	BS16#	C17				K16	H17
A14	S5	D12	G3	BS8#	D16				L16	K1
A15	R7	D13	D2	CLK	C3				M2	K17
A16	Q9	D14	K3	CLKMUL	R17				M16	L1
A17	Q3	D15	F3	CACHE#	B12				P16	L17
A18	R5	D16	J3	D/C#	M15				R3	M1
A19	Q4	D17	D3	DP0	N3				R6	M17
A20	Q8	D18	C2	DP1	F1				R8	P17
A21	Q5	D19	B1	DP2	H3				R9	Q2
A22	Q7	D20	A1	DP3	A5				R10	R4
A23	S3	D21	B2	EADS#	B17				R11	S6
A24	Q6	D22	A2	FERR#	C14				R14	S8
A25	R2	D23	A4	FLUSH#	C15					S9
A26	S2	D24	A6	HITM#	A12					S10
A27	S1	D25	B6	HLDA	P15					S11
A28	R1	D26	C7	HOLD	E15					S12
A29	P2	D27	C6	IGNNE#	A15					S14
A30	P3	D28	C8	INTR	A16					
A31	Q1	D29	A8	INV	A10					
		D30	C9	KEN#	F15					
		D31	B8	LOCK#	N15					
				M/IO#	N16					

Table 7. Pin Cross Reference for 168-Pin PGA Package (Sheet 2 of 2)

Address	Pin #	Data	Pin #	Control	Pin #	NC	INC	Vcc5	Vcc	Vss
				NMI	B15					
				PCD	J17					
				PCHK#	Q17					
				PLOCK#	Q16					
				PWT	L15					
				RDY#	F16					
				RESERVED#	C11					
				RESET	C16					
				SMI#	B10					
				SMIACT#	C12					
				SRESET	C10					
				STPCLK#	G15					
				TCK	A3					
				TDI	A14					
				TDO	B16					
				TMS	B14					
				VOLDET	S4					
				WB/WT#	B13					
				W/R#	N17					

3.2 Pin Quick Reference

The following is a brief pin description. For detailed signal descriptions refer to Appendix A, “Signal Descriptions,” in the *Embedded Intel486™ Processor Family Developer’s Manual,* order No. 273021.

Table 8. Embedded Write-Back Enhanced IntelDX4™ Processor Pin Descriptions (Sheet 1 of 8)

Symbol	Type	Name and Function
CLK	I	**Clock** provides the fundamental timing and internal operating frequency for the Embedded Write-Back Enhanced IntelDX4 processor. All external timing parameters are specified with respect to the rising edge of CLK.
ADDRESS BUS		
A31-A4 **A3–A2**	I/O O	**Address Lines** A31–A2, together with the byte enable signals, BE3#–BE0#, define the physical area of memory or input/output space accessed. Address lines A31–A4 are used to drive addresses into the Embedded Write-Back Enhanced IntelDX4 processor to perform cache line invalidation. Input signals must meet setup and hold times t_{22} and t_{23}. A31–A2 are not driven during bus or address hold.
BE3# **BE2#** **BE1#** **BE0#**	O O O O	**Byte Enable** signals indicate active bytes during read and write cycles. During the first cycle of a cache fill, the external system should assume that all byte enables are active. BE3#–BE0# are active LOW and are not driven during bus hold. BE3# applies to D31–D24 BE2# applies to D23–D16 BE1# applies to D15–D8 BE0# applies to D7–D0
DATA BUS		
D31–D0	I/O	**Data Lines.** D7–D0 define the least significant byte of the data bus; D31–D24 define the most significant byte of the data bus. These signals must meet setup and hold times t_{22} and t_{23} for proper operation on reads. These pins are driven during the second and subsequent clocks of write cycles.
DATA PARITY		
DP3–DP0	I/O	There is one **Data Parity** pin for each byte of the data bus. Data parity is generated on all write data cycles with the same timing as the data driven by the Embedded Write-Back Enhanced IntelDX4 processor. Even parity information must be driven back into the processor on the data parity pins with the same timing as read information to ensure that the correct parity check status is indicated by the Embedded Write-Back Enhanced IntelDX4 processor. The signals read on these pins do not affect program execution. Input signals must meet setup and hold times t_{22} and t_{23}. DP3–DP0 must be connected to V_{CC} through a pull-up resistor in systems that do not use parity. DP3–DP0 are active HIGH and are driven during the second and subsequent clocks of write cycles.
PCHK#	O	**Parity Status** is driven on the PCHK# pin the clock after ready for read operations. The parity status is for data sampled at the end of the previous clock. A parity error is indicated by PCHK# being LOW. Parity status is only checked for enabled bytes as indicated by the byte enable and bus size signals. PCHK# is valid only in the clock immediately after read data is returned to the processor. At all other times PCHK# is inactive (HIGH). PCHK# is never floated.

Table 8. Embedded Write-Back Enhanced IntelDX4™ Processor Pin Descriptions (Sheet 2 of 8)

Symbol	Type	Name and Function
BUS CYCLE DEFINITION		
M/IO# **D/C#** **W/R#**	O O O	**Memory/Input-Output**, **Data/Control** and **Write/Read** lines are the primary bus definition signals. These signals are driven valid as the ADS# signal is asserted. **M/IO# D/C# W/R# Bus Cycle Initiated** 0 0 0 Interrupt Acknowledge 0 0 1 HALT/Special Cycle (see details below) 0 1 0 I/O Read 0 1 1 I/O Write 1 0 0 Code Read 1 0 1 Reserved 1 1 0 Memory Read 1 1 1 Memory Write **HALT/Special Cycle** **Cycle Name — BE3# - BE0# — A4-A2** Shutdown — 1110 — 000 HALT — 1011 — 000 Stop Grant bus cycle — 1011 — 100
LOCK#	O	**Bus Lock** indicates that the current bus cycle is locked. The Embedded Write-Back Enhanced IntelDX4 processor does not allow a bus hold when LOCK# is asserted (address holds are allowed). LOCK# goes active in the first clock of the first locked bus cycle and goes inactive after the last clock of the last locked bus cycle. The last locked cycle ends when Ready is returned. LOCK# is active LOW and not driven during bus hold. Locked read cycles are not transformed into cache fill cycles when KEN# is returned active.
PLOCK#	O	**Pseudo-Lock** indicates that the current bus transaction requires more than one bus cycle to complete. For the Embedded Write-Back Enhanced IntelDX4 processor, examples of such operations are segment table descriptor reads (64 bits) and cache line fills (128 bits). For Intel486 processors with on-chip Floating-Point Unit, floating-point long reads and writes (64 bits) also require more than one bus cycle to complete. The Embedded Write-Back Enhanced IntelDX4 processor drives PLOCK# active until the addresses for the last bus cycle of the transaction are driven, regardless of whether RDY# or BRDY# have been returned. Normally PLOCK# and BLAST# are inverse of each other. However, during the first bus cycle of a 64-bit floating-point write (for Intel486 processors with on-chip Floating-Point Unit) both PLOCK# and BLAST# are asserted. PLOCK# is a function of the BS8#, BS16# and KEN# inputs. PLOCK# should be sampled only in the clock in which Ready is returned. PLOCK# is active LOW and is not driven during bus hold.
BUS CONTROL		
ADS#	O	**Address Status** output indicates that a valid bus cycle definition and address are available on the cycle definition lines and address bus. ADS# is driven active in the same clock in which the addresses are driven. ADS# is active LOW and not driven during bus hold.

Table 8. Embedded Write-Back Enhanced IntelDX4™ Processor Pin Descriptions (Sheet 3 of 8)

Symbol	Type	Name and Function
RDY#	I	**Non-burst Ready** input indicates that the current bus cycle is complete. RDY# indicates that the external system has presented valid data on the data pins in response to a read or that the external system has accepted data from the Embedded Write-Back Enhanced IntelDX4 processor in response to a write. RDY# is ignored when the bus is idle and at the end of the first clock of the bus cycle. RDY# is active during address hold. Data can be returned to the Embedded Write-Back Enhanced IntelDX4 processor while AHOLD is active. RDY# is active LOW and is not provided with an internal pull-up resistor. RDY# must satisfy setup and hold times t_{16} and t_{17} for proper chip operation.
BURST CONTROL		
BRDY#	I	**Burst Ready** input performs the same function during a burst cycle that RDY# performs during a non-burst cycle. BRDY# indicates that the external system has presented valid data in response to a read or that the external system has accepted data in response to a write. BRDY# is ignored when the bus is idle and at the end of the first clock in a bus cycle. BRDY# is sampled in the second and subsequent clocks of a burst cycle. Data presented on the data bus is strobed into the Embedded Write-Back Enhanced IntelDX4 processor when BRDY# is sampled active. If RDY# is returned simultaneously with BRDY#, BRDY# is ignored and the burst cycle is prematurely aborted. BRDY# is active LOW and is provided with a small pull-up resistor. BRDY# must satisfy the setup and hold times t_{16} and t_{17}.
BLAST#	O	**Burst Last** signal indicates that the next time BRDY# is returned, the burst bus cycle is complete. BLAST# is active for both burst and non-burst bus cycles. BLAST# is active LOW and is not driven during bus hold.
INTERRUPTS		
RESET	I	**Reset** input forces the Embedded Write-Back Enhanced IntelDX4 processorto begin execution at a known state. The processor cannot begin executing instructions until at least 1 ms after V_{CC}, and CLK have reached their proper DC and AC specifications. The RESET pin must remain active during this time to ensure proper processor operation. However, for warm resets, RESET should remain active for at least 15 CLK periods. RESET is active HIGH. RESET is asynchronous but must meet setup and hold times t_{20} and t_{21} for recognition in any specific clock.
INTR	I	**Maskable Interrupt** indicates that an external interrupt has been generated. When the internal interrupt flag is set in EFLAGS, active interrupt processing is initiated. The Embedded Write-Back Enhanced IntelDX4 processorgenerates two locked interrupt acknowledge bus cycles in response to the INTR pin going active. INTR must remain active until the interrupt acknowledges have been performed to ensure processor recognition of the interrupt. INTR is active HIGH and is not provided with an internal pull-down resistor. INTR is asynchronous, but must meet setup and hold times t_{20} and t_{21} for recognition in any specific clock.
NMI	I	**Non-Maskable Interrupt** request signal indicates that an external non-maskable interrupt has been generated. NMI is rising-edge sensitive and must be held LOW for at least four CLK periods before this rising edge. NMI is not provided with an internal pull-down resistor. NMI is asynchronous, but must meet setup and hold times t_{20} and t_{21} for recognition in any specific clock.

Table 8. Embedded Write-Back Enhanced IntelDX4™ Processor Pin Descriptions (Sheet 4 of 8)

Symbol	Type	Name and Function
SRESET	I	**Soft Reset** pin duplicates all functionality of the RESET pin except that the SMBASE register retains its previous value. For soft resets, SRESET must remain active for at least 15 CLK periods. SRESET is active HIGH. SRESET is asynchronous but must meet setup and hold times t_{20} and t_{21} for recognition in any specific clock.
SMI#	I	**System Management Interrupt** input invokes System Management Mode (SMM). SMI# is a falling-edge triggered signal which forces the Embedded Write-Back Enhanced IntelDX4 processorinto SMM at the completion of the current instruction. SMI# is recognized on an instruction boundary and at each iteration for repeat string instructions. SMI# does not break LOCKed bus cycles and cannot interrupt a currently executing SMM. The Embedded Write-Back Enhanced IntelDX4 proces-sorlatches the falling edge of one pending SMI# signal while it is executing an existing SMI#. The nested SMI# is not recognized until after the execution of a Resume (RSM) instruction.
SMIACT#	O	**System Management Interrupt Active**, an active LOW output, indicates that the Embedded Write-Back Enhanced IntelDX4 processoris operating in SMM. It is asserted when the processor begins to execute the SMI# state save sequence and remains active LOW until the processor executes the last state restore cycle out of SMRAM.
STPCLK#	I	**Stop Clock Request** input signal indicates a request was made to turn off or change the CLK input frequency. When the Embedded Write-Back Enhanced IntelDX4 processorrecognizes a STPCLK#, it stops execution on the next instruction boundary (unless superseded by a higher priority interrupt), empties all internal pipelines and write buffers, and generates a Stop Grant bus cycle. STPCLK# is active LOW. STPCLK# must be pulled high via a 10-KW pullup resistor. **STPCLK# is an asynchronous signal, but must remain active until the Embedded Write-Back Enhanced IntelDX4 processor issues the Stop Grant bus cycle. STPCLK# may be de-asserted at any time after the processor has issued the Stop Grant bus cycle.**
BUS ARBITRATION		
BREQ	O	**Bus Request** signal indicates that the Embedded Write-Back Enhanced IntelDX4 processorhas internally generated a bus request. BREQ is generated whether or not the processor is driving the bus. BREQ is active HIGH and is never floated.
HOLD	I	**Bus Hold Request** allows another bus master complete control of the Embedded Write-Back Enhanced IntelDX4 processorbus. In response to HOLD going active, the processor floats most of its output and input/output pins. HLDA is asserted after completing the current bus cycle, burst cycle or sequence of locked cycles. The Embedded Write-Back Enhanced IntelDX4 processorremains in this state until HOLD is de-asserted. HOLD is active HIGH and is not provided with an internal pull-down resistor. HOLD must satisfy setup and hold times t_{18} and t_{19} for proper operation.
HLDA	O	**Hold Acknowledge** goes active in response to a hold request presented on the HOLD pin. HLDA indicates that the Embedded Write-Back Enhanced IntelDX4 processor has given the bus to another local bus master. HLDA is driven active in the same clock that the processor floats its bus. HLDA is driven inactive when leaving bus hold. HLDA is active HIGH and remains driven during bus hold.

Table 8. Embedded Write-Back Enhanced IntelDX4™ Processor Pin Descriptions (Sheet 5 of 8)

Symbol	Type	Name and Function
BOFF#	I	**Backoff** input forces the Embedded Write-Back Enhanced IntelDX4 processor to float its bus in the next clock. The processor floats all pins normally floated during bus hold but HLDA is not asserted in response to BOFF#. BOFF# has higher priority than RDY# or BRDY#; if both are returned in the same clock, BOFF# takes effect. The Embedded Write-Back Enhanced IntelDX4 processor remains in bus hold until BOFF# is negated. If a bus cycle is in progress when BOFF# is asserted the cycle is restarted. BOFF# is active LOW and must meet setup and hold times t_{18} and t_{19} for proper operation.
CACHE INVALIDATION		
AHOLD	I	**Address Hold** request allows another bus master access to the Embedded Write-Back Enhanced IntelDX4 processor's address bus for a cache invalidation cycle. The processor stops driving its address bus in the clock following AHOLD going active. Only the address bus is floated during address hold, the remainder of the bus remains active. AHOLD is active HIGH and is provided with a small internal pull-down resistor. For proper operation, AHOLD must meet setup and hold times t_{18} and t_{19}.
EADS#	I	**External Address** - This signal indicates that a *valid* external address has been driven onto the Embedded Write-Back Enhanced IntelDX4 processor address pins. This address is used to perform an internal cache invalidation cycle. EADS# is active LOW and is provided with an internal pull-up resistor. EADS# must satisfy setup and hold times t_{12} and t_{13} for proper operation.
CACHE CONTROL		
KEN#	I	**Cache Enable** pin is used to determine whether the current cycle is cacheable. When the Embedded Write-Back Enhanced IntelDX4 processorgenerates a cycle that can be cached and KEN# is active one clock before RDY# or BRDY# during the first transfer of the cycle, the cycle becomes a cache line fill cycle. Returning KEN# active one clock before RDY# during the last read in the cache line fill causes the line to be placed in the on-chip cache. KEN# is active LOW and is provided with a small internal pull-up resistor. KEN# must satisfy setup and hold times t_{14} and t_{15} for proper operation.
FLUSH#	I	**Cache Flush** input forces the Embedded Write-Back Enhanced IntelDX4 processorto flush its entire internal cache. FLUSH# is active LOW and need only be asserted for one clock. FLUSH# is asynchronous but setup and hold times t_{20} and t_{21} must be met for recognition in any specific clock.
PAGE CACHEABILITY		
PWT **PCD**	O O	**Page Write-Through** and **Page Cache Disable** pins reflect the state of the page attribute bits, PWT and PCD, in the page table entry, page directory entry or control register 3 (CR3) when paging is enabled. When paging is disabled, the Embedded Write-Back Enhanced IntelDX4 processorignores the PCD and PWT bits and assumes they are zero for the purpose of caching and driving PCD and PWT pins. PWT and PCD have the same timing as the cycle definition pins (M/IO#, D/C#, and W/R#). PWT and PCD are active HIGH and are not driven during bus hold. PCD is masked by the cache disable bit (CD) in Control Register 0.

Table 8. Embedded Write-Back Enhanced IntelDX4™ Processor Pin Descriptions (Sheet 6 of 8)

Symbol	Type	Name and Function
BUS SIZE CONTROL		
BS16# **BS8#**	I I	**Bus Size 16** and **Bus Size 8** pins (bus sizing pins) cause the Embedded Write-Back Enhanced IntelDX4 processor to run multiple bus cycles to complete a request from devices that cannot provide or accept 32 bits of data in a single cycle. The bus sizing pins are sampled every clock. The processor uses the state of these pins in the clock before Ready to determine bus size. These signals are active LOW and are provided with internal pull-up resistors. These inputs must satisfy setup and hold times t_{14} and t_{15} for proper operation.
ADDRESS MASK		
A20M#	I	**Address Bit 20 Mask** pin, when asserted, causes the Embedded Write-Back Enhanced IntelDX4 processorto mask physical address bit 20 (A20) before performing a lookup to the internal cache or driving a memory cycle on the bus. A20M# emulates the address wraparound at 1 Mbyte, which occurs on the 8086 processor. A20M# is active LOW and should be asserted only when the Embedded Write-Back Enhanced IntelDX4 processoris in real mode. This pin is asynchronous but should meet setup and hold times t_{20} and t_{21} for recognition in any specific clock. For proper operation, A20M# should be sampled HIGH at the falling edge of RESET.
TEST ACCESS PORT		
TCK	I	**Test Clock**, an input to the Embedded Write-Back Enhanced IntelDX4 processor, provides the clocking function required by the JTAG Boundary scan feature. TCK is used to clock state information (via TMS) and data (via TDI) into the component on the rising edge of TCK. Data is clocked out of the component (via TDO) on the falling edge of TCK. TCK is provided with an internal pull-up resistor.
TDI	I	**Test Data Input** is the serial input used to shift JTAG instructions and data into the processor. TDI is sampled on the rising edge of TCK, during the SHIFT-IR and SHIFT-DR Test Access Port (TAP) controller states. During all other TAP controller states, TDI is a “don’t care.” TDI is provided with an internal pull-up resistor.
TDO	O	**Test Data Output** is the serial output used to shift JTAG instructions and data out of the component. TDO is driven on the falling edge of TCK during the SHIFT-IR and SHIFT-DR TAP controller states. At all other times TDO is driven to the high impedance state.
TMS	I	**Test Mode Select** is decoded by the JTAG TAP to select test logic operation. TMS is sampled on the rising edge of TCK. To guarantee deterministic behavior of the TAP controller, TMS is provided with an internal pull-up resistor.
NUMERIC ERROR REPORTING		
FERR#	O	The **Floating Point Error** pin is driven active when a floating point error occurs. FERR# is similar to the ERROR# pin on the Intel387™ Math CoProcessor. FERR# is included for compatibility with systems using DOS type floating point error reporting. FERR# will not go active if FP errors are masked in FPU register. FERR# is active LOW, and is not floated during bus hold.

Table 8. Embedded Write-Back Enhanced IntelDX4™ Processor Pin Descriptions (Sheet 7 of 8)

Symbol	Type	Name and Function
IGNNE#	I	When the **Ignore Numeric Error** pin is asserted the processor will ignore a numeric error and continue executing non-control floating point instructions, but FERR# will still be activated by the processor. When IGNNE# is de-asserted the processor will freeze on a non-control floating point instruction, if a previous floating point instruction caused an error. IGNNE# has no effect when the NE bit in control register 0 is set. IGNNE# is active LOW and is provided with a small internal pull-up resistor. IGNNE# is asynchronous but setup and hold times t_{20} and t_{21} must be met to ensure recognition on any specific clock.
WRITE-BACK ENHANCED MODE		
CACHE#	O	The **CACHE#** output indicates internal cacheability on read cycles and burst write-back on write cycles. CACHE# is asserted for cacheable reads, cacheable code fetches and write-backs. It is driven inactive for non-cacheable reads, I/O cycles, special cycles, and write-through cycles.
FLUSH#	I	**Cache FLUSH#** is an existing pin that operates differently if the processor is configured as Enhanced Bus mode (write-back). FLUSH# causes the processor to write back all modified lines and flush (invalidate) the cache. FLUSH# is asynchronous, but must meet setup and hold times t_{20} and t_{21} for recognition in any specific clock.
HITM#	O	The **Hit/Miss to a Modified Line** pin is a cache coherency protocol pin that is driven only in Enhanced Bus mode. When a snoop cycle is run, HITM# indicates that the processor contains the snooped line and that the line has been modified. Assertion of HITM# implies that the line will be written back in its entirety, unless the processor is already in the process of doing a replacement write-back of the same line.
INV	I	The **Invalidation Request** pin is a cache coherency protocol pin that is used only in the Enhanced Bus mode. It is sampled by the processor on EADS#-driven snoop cycles. It is necessary to assert this pin to get the effect of the processor invalidate cycle on write-through-only lines**.** INV also invalidates the write-back lines. However, if the snooped line is modified, the line will be written back and then invalidated. INV must satisfy setup and hold times t_{12} and t_{13} for proper operation.
PLOCK#	O	In the Enhanced bus mode, **Pseudo-Lock Output** is always driven inactive. In this mode, a 64-bit data read (caused by an FP operand access or a segment descriptor read) is treated as a multiple cycle read request, which may be a burst or a non-burst access based on whether BRDY# or RDY# is returned by the system. Because only write-back cycles (caused by snoop write-back or replacement write-back) are write burstable, a 64-bit write will be driven out as two non-burst bus cycles. BLAST# is asserted during both writes.
SRESET	I	For the Embedded Write-Back Enhanced IntelDX4 processor, **Soft RESET** operates similar to other the Intel486 processors. On SRESET, the internal SMRAM base register retains its previous value, does not flush, write-back or disable the internal cache. Because SRESET is treated as an interrupt, it is possible to have a bus cycle while SRESET is asserted. SRESET is serviced only on an instruction boundary. SRESET is asynchronous but must meet setup and hold times t_{20} and t_{21} for recognition in any specific clock.

Table 8. Embedded Write-Back Enhanced IntelDX4™ Processor Pin Descriptions (Sheet 8 of 8)

Symbol	Type	Name and Function
WB/WT#	I	The **Write-Back/Write-Through** pin enables Enhanced Bus mode (write-back cache). It also defines a cached line as write-through or write-back. For cache configuration, WB/WT# must be valid during RESET and be active for at least two clocks before and two clocks after RESET is de-asserted. To define write-back or write-through configuration of a line, WB/WT# is sampled in the same clock as the first RDY# or BRDY# is returned during a line fill (allocation) cycle.
CLKMUL, VCC5, AND VOLDET		
CLKMUL	I	The **Clock Multiplier** input, defined during device RESET, defines the ratio of internal core frequency to external bus frequency. If sampled low, the core frequency operates at twice the external bus frequency (speed doubled mode). If driven high, speed triple mode is selected. CLKMUL has an internal pull-up speed to V_{CC}. A 10-KΩ pullup resistor is recommended when the pin is tied high.
V_{CC5}	I	The **5V reference voltage** input is the reference voltage for the 5V-tolerant I/O buffers. This signal should be connected to +5V ±5% for use with 5V logic. If all inputs are from 3V logic, this pin should be connected to 3.3V.
VOLDET	O	A **Voltage Detect** signal allows external system logic to distinguish between a 5V Intel486 processor and the 3.3V IntelDX4 processor. This signal is active LOW for a 3.3V IntelDX4 processor. This pin is available only on the PGA version of the Embedded Write-Back Enhanced IntelDX4 processor.
RESERVED PINS		
RESERVED#	I	**Reserved** is reserved for future use. This pin MUST be connected to an external pull-up resistor circuit. The recommended resistor value is 10 kOhms. The pull-up resistor must be connected only to the RESERVED# pin. **Do not share this resistor with other pins requiring pull-ups.**

Table 9. Output Pins

Name	Active Level	Output Signal		
		Floated During Address Hold	Floated During Bus Hold	During Stop Grant and Stop Clock States
BREQ	HIGH			Previous State[1]
HLDA	HIGH			As per HOLD
BE3#-BE0#	LOW		•	Previous State
PWT, PCD	HIGH		•	Previous State
W/R#, M/IO#, D/C#	HIGH/LOW		•	Previous State
LOCK#	LOW		•	HIGH (inactive)
PLOCK#	LOW		•	HIGH (inactive)
ADS#	LOW		•	HIGH (inactive)
BLAST#	LOW		•	Previous State
PCHK#	LOW			Previous State
FERR#	LOW			Previous State
A3-A2	HIGH	•	•	Previous State
SMIACT#	LOW			Previous State
CACHE#	LOW	•	•	HIGH[2]
HITM#	LOW	•	•	HIGH[2]
VOLDET	LOW			LOW

NOTES:

1. The term “Previous State” means that the processor maintains the logic level applied to the signal pin just before the processor entered the Stop Grant state. This conserves power by preventing the signal pin from floating.
2. For the case of snoop cycles (via EADS#) during Stop Grant state, CACHE# and HITM# can go active depending on the snoop hit in the internal cache.

Table 10. Input/Output Pins

Name	Active Level	Output Signal		
		Floated During Address Hold	Floated During Bus Hold	During Stop Grant and Stop Clock States
D31-D0	HIGH		•	Floated
DP3–DP0	HIGH		•	Floated
A31-A4	HIGH	•	•	Previous State

NOTE: The term “Previous State” means that the processor maintains the logic level applied to the signal pin just before the processor entered the Stop Grant state. This conserves power by preventing the signal pin from floating.

Table 11. Test Pins

Name	Input or Output	Sampled/ Driven On
TCK	Input	N/A
TDI	Input	Rising Edge of TCK
TDO	Output	Failing Edge of TCK
TMS	Input	Rising Edge of TCK

Table 12. Input Pins (Sheet 1 of 2)

Name	Active Level	Synchronous/ Asynchronous	Internal Pull-Up/ Pull-Down
CLK			
RESET	HIGH	Asynchronous	
SRESET	HIGH	Asynchronous	Pull-Down
HOLD	HIGH	Synchronous	
AHOLD	HIGH	Synchronous	Pull-Down
EADS#	LOW	Synchronous	Pull-Up
BOFF#	LOW	Synchronous	Pull-Up
FLUSH#	LOW	Asynchronous	Pull-Up
A20M#	LOW	Asynchronous	Pull-Up
BS16#, BS8#	LOW	Synchronous	Pull-Up
KEN#	LOW	Synchronous	Pull-Up
RDY#	LOW	Synchronous	
BRDY#	LOW	Synchronous	Pull-Up
INTR	HIGH	Asynchronous	
NMI	HIGH	Asynchronous	
IGNNE#	LOW	Asynchronous	Pull-Up
RESERVED#	LOW	Asynchronous	Pull-Up
SMI#	LOW	Asynchronous	Pull-Up
STPCLK#	LOW	Asynchronous	Pull-Up[1]
INV	HIGH	Synchronous	Pull-Up

NOTE:

1. Even though STPCLK# and CLKMUL have internal pull-up resistors, they cannot be left floating. An external 10-KΩ pull-up resistor is needed if the STPCLK# pin is unused. CLKMUL must be driven to a valid logic level. If tied HIGH, an external 10-KΩ pull-up resistor is recommended.

Table 12. Input Pins (Sheet 2 of 2)

Name	Active Level	Synchronous/ Asynchronous	Internal Pull-Up/ Pull-Down
WB/WT#	HIGH/LOW	Synchronous	Pull-Down
CLKMUL	HIGH		Pull-Up[1]
TCK	HIGH		Pull-Up
TDI	HIGH		Pull-Up
TMS	HIGH		Pull-Up

NOTE:

1. Even though STPCLK# and CLKMUL have internal pull-up resistors, they cannot be left floating. An external 10-KΩ pull-up resistor is needed if the STPCLK# pin is unused. CLKMUL must be driven to a valid logic level. If tied HIGH, an external 10-KΩ pull-up resistor is recommended.

4.0 ARCHITECTURAL AND FUNCTIONAL OVERVIEW

The Embedded Write-Back Enhanced IntelDX4 processor architecture is essentially the same as the IntelDX4 processor. Refer to the *Embedded Intel486™ Processor Family Developer's Manual* (273021)

The Embedded Write-Back Enhanced IntelDX4 processor has one pin reserved for possible future use. This pin, an input signal, is called RESERVED# and must be connected to a 10-KΩ pull-up resistor. The pull-up resistor must be connected only to the RESERVED# pin. **Do not share this resistor with other pins requiring pull-ups.**

4.1 CPUID Instruction

The Embedded Write-Back Enhanced IntelDX4 processor supports the CPUID instruction (see Table 13). Because not all Intel processors support the CPUID instruction, a simple test can determine if the instruction is supported. The test involves the processor's ID Flag, which is bit 21 of the EFLAGS register. If software can change the value of this flag, the CPUID instruction is available. The actual state of the ID Flag bit is irrelevant and provides no significance to the hardware. This bit is cleared (reset to zero) upon device reset (RESET or SRESET) for compatibility with Intel486 processor designs that do not support the CPUID instruction.

CPUID-instruction details are provided here for the Embedded Write-Back Enhanced IntelDX4 processor. Refer to Intel Application Note AP-485 *Intel Processor Identification with the CPUID Instruction* (Order No. 241618) for a description that covers all aspects of the CPUID instruction and how it pertains to other Intel processors.

4.1.1 Operation of the CPUID Instruction

The CPUID instruction requires the software developer to pass an input parameter to the processor in the EAX register. The processor response is returned in registers EAX, EBX, EDX, and ECX.

Table 13. CPUID Instruction Description

OP CODE	Instruction	Processor Core Clocks	Parameter passed in EAX (Input Value)	Description
0F A2	CPUID	9	0	Vendor (Intel) ID String
		14	1	Processor Identification
		9	> 1	Undefined (Do Not Use)

Vendor ID String - When the parameter passed in EAX is 0 (zero), the register values returned upon instruction execution are shown in the following table.

		31----------24	23----------16	15----------8	7----------0
High Value (= 1)	**EAX**	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 1
Vendor ID String	**EBX**	u (75)	n (6E)	e (65)	G (47)
(ASCII	**EDX**	I (49)	e (65)	n (6E)	i (69)
Characters)	**ECX**	l (6C)	e (65)	t (74)	n (6E)

The values in EBX, EDX and ECX indicate an Intel processor. When taken in the proper order, they decode to the string "GenuineIntel."

The state of the WB/WT# input pin is sampled by the processor on the falling edge of the RESET signal. If WB/WT# is LOW, the processor is configured to operate in Write-Through/Standard Bus mode. If HIGH, it is configured to operate in Write-Back/Enhanced Bus mode. The value of the "Model" field of the processor signature register depends on the bus mode for which the processor is configured.

Processor Identification - When the parameter passed to EAX is 1 (one), the register values returned upon instruction execution are:

		31----------14	13,12	11----8	7----4	3----0
Processor Signature for Write-Through/Standard Bus mode	**EAX**	(Do Not Use) Intel Reserved	0 0 Processor Type	0 1 0 0 Family	1 0 0 0 Model	XXXX Stepping
Processor Signature for Write-Back/Enhanced Bus mode		(Do Not Use) Intel Reserved	0 0 Processor Type	0 1 0 0 Family	1 0 0 1 Model	XXXX Stepping

(Intel releases information about stepping numbers as needed)

		31----------0
Intel Reserved	**EBX**	Intel Reserved
(Do Not Use)	**ECX**	Intel Reserved

		31----------2	1	0
Feature Flags	**EDX**	0----------0	1 VME	0 FPU

4.2 Identification After Reset

Processor Identification - Upon reset, the EDX register contains the processor signature:

		31----------14	13,12	11----8	7----4	3----0
Processor Signature for Write-Through/Standard Bus mode	**EDX**	(Do Not Use) Intel Reserved	0 0 Processor Type	0 1 0 0 Family	1 0 0 0 Model	XXXX Stepping
Processor Signature for Write-Back/Enhanced Bus mode		(Do Not Use) Intel Reserved	0 0 Processor Type	0 1 0 0 Family	1 0 0 1 Model	XXXX Stepping

(Intel releases information about stepping numbers as needed)

4.3 Boundary Scan (JTAG)

4.3.1 Device Identification

Tables 14 and 15 show the 32-bit code for the Embedded Write-Back Enhanced IntelDX4 processor. This code is loaded into the Device Identification Register.

Table 14. Boundary Scan Component Identification Code (Write-Through/Standard Bus Mode)

Version	**Part Number**				**Mfg ID**	**1**
	V_{CC} 1=3.3 V	**Intel Architecture Type**	**Family** 0100 = Intel486 CPU Family	**Model** 01000 = Embedded Write-Back Enhanced IntelDX4 processor	009H = Intel	
31----28	27	26----------21	20----17	16--------12	11----------1	0
XXXX	1	000001	0100	01000	00000001001	1

(Intel releases information about version numbers as needed)
Boundary Scan Component Identification Code = x828 8013 (Hex)

Table 15. Boundary Scan Component Identification Code (Write-Back/Enhanced Bus Mode)

Version	Part Number				Mfg ID	1
	V_{CC} 1=3.3 V	Intel Architecture Type	Family 0100 = Intel486 CPU Family	Model 01001 = Embedded Write-Back Enhanced IntelDX4 processor	009H = Intel	
31----28	27	26----------21	20----17	16--------12	11----------1	0
XXXX	1	000001	0100	01001	00000001001	1

(Intel releases information about version numbers as needed)
Boundary Scan Component Identification Code = x828 9013 (Hex)

4.3.2 Boundary Scan Register Bits and Bit Order

The boundary scan register contains a cell for each pin as well as cells for control of bidirectional and three-state pins. There are “Reserved” bits which correspond to no-connect (N/C) signals of the Embedded Write-Back Enhanced IntelDX4 processor. Control registers WRCTL, ABUSCTL, BUSCTL, and MISCCTL are used to select the direction of bidirectional or three-state output signal pins. A “1” in these cells designates that the associated bus or bits are floated if the pins are three-state, or selected as input if they are bidirectional.

- WRCTL controls D31-D0 and DP3–DP0
- ABUSCTL controls A31-A2
- BUSCTL controls ADS#, BLAST#, PLOCK#, LOCK#, W/R#, BE0#, BE1#, BE2#, BE3#, M/IO#, D/C#, PWT, PCD, and CACHE#
- MISCCTL controls PCHK#, HLDA, BREQ, and HITM#

The following is the bit order of the Embedded Write-Back Enhanced IntelDX4 processor boundary scan register:

TDO ← A2, A3, A4, A5, RESERVED#, A6, A7, A8, A9, A10, A11, A12, A13, A14, A15, A16, A17, A18, A19, A20, A21, A22, A23, A24, A25, A26, A27, A28, A29, A30, A31, DP0, D0, D1, D2, D3, D4, D5, D6, D7, DP1, D8, D9, D10, D11, D12, D13, D14, D15, DP2, D16, D17, D18, D19, D20, D21, D22, D23, DP3, D24, D25, D26, D27, D28, D29, D30, D31, STPCLK#, IGNNE#, INV, CACHE#, FERR#, SMI#, WB/WT#, HITM#, SMIACT#, SRESET, NMI, INTR, FLUSH#, RESET, A20M#, EADS#, PCD, PWT, D/C#, M/IO#, BE3#, BE2#, BE1#, BE0#, BREQ, W/R#, HLDA, CLK, AHOLD, HOLD, KEN#, RDY#, CLKMUL, BS8#, BS16#, BOFF#, BRDY#, PCHK#, LOCK#, PLOCK#, BLAST#, ADS#, MISCCTL, BUSCTL, ABUSCTL, WRCTL ← **TDI**

5.0 ELECTRICAL SPECIFICATIONS

5.1 Maximum Ratings

Table 16 is a stress rating only. Extended exposure to the Maximum Ratings may affect device reliability.

Furthermore, although the Embedded Write-Back Enhanced IntelDX4 processorcontains protective circuitry to resist damage from electrostatic discharge, always take precautions to avoid high static voltages or electric fields.

Functional operating conditions are given in **Section 5.2, DC Specifications** and **Section 5.3, AC Specifications**.

Table 16. Absolute Maximum Ratings

Case Temperature under Bias	-65 °C to +110 °C
Storage Temperature	-65 °C to +150 °C
DC Voltage on Any Pin with Respect to Ground	-0.5 V to V_{CC5} + 0.5 V
Supply Voltage V_{CC} with Respect to V_{SS}	-0.5 V to +4.6 V
Reference Voltage V_{CC5} with Respect to V_{SS}	-0.5 V to +6.5 V
Transient Voltage on any Input	The lesser of: V_{CC5} + 1.6 V or 6.5 V
Current Sink on V_{CC5}	55 mA

5.2 DC Specifications

The following tables show the operating supply voltages, DC I/O specifications, and component power consumption for the Embedded Write-Back Enhanced IntelDX4 processor.

Table 17. Operating Supply Voltages

Product	V_{CC}
x80486DX4WB75	3.3 V ± 0.3 V
x80486DX4WB100	3.3 V ± 0.3 V
x0486DX4WB100	3.3 V ± 0.3 V

NOTE: To address the fact that many of the package prefix variables have changed, all package prefix variables in this document are now indicated with an "x".

Table 18. DC Specifications

Functional Operating Range: V_{CC} = 3.3 V ± 0.3 V; V_{CC5} = 5 V ± 0.25 V (Note 1); T_{CASE}=0 °C to +85 °C

Symbol	Parameter	Min.	Typ.	Max.	Unit	Notes
V_{IL}	Input LOW Voltage	-0.3		+0.8	V	
V_{IH}	Input HIGH Voltage	2.0		V_{CC5} +0.3	V	Note 2
V_{IHC}	Input HIGH Voltage of CLK	V_{CC5} -0.6		V_{CC5} +0.3	V	
V_{OL}	Output LOW Voltage					
	I_{OL} = 4.0 mA (Address, Data, BE*n*)			0.45	V	
	I_{OL} = 5.0 mA (Definition, Control)			0.45	V	
	I_{OL} = 2.0 mA			0.40	V	
	I_{OL} = 100 µA			0.20	V	
V_{OH}	Output HIGH Voltage					
	I_{OH} = -2.0 mA	2.4			V	
I_{CC5}	V_{CC5} Leakage Current		15	300	µA	Note 3
I_{LI}	Input Leakage Current			15	µA	Note 4
I_{IH}	Input Leakage Current			200	µA	Note 5
	SRESET			300	µA	Note 5
I_{IL}	Input Leakage Current			400	µA	Note 6
I_{LO}	Output Leakage Current			15	µA	
C_{IN}	Input Capacitance			10	pF	Note 7
C_{OUT}	I/O or Output Capacitance			14	pF	Note 7
C_{CLK}	CLK Capacitance			12	pF	Note 7

NOTES:

1. V_{CC5} should be connected to 3.3 V ± 0.3 V in 3.3 V-only systems.
2. All inputs except CLK.
3. This parameter is for inputs without pull-up or pull-down resistors and $0V \le V_{IN} \le V_{CC}$.
4. This parameter is for $V_{CC5} - V_{CC} \le 2.25$ V. Typical value is not 100% tested.
5. This parameter is for inputs with pull-down resistors and V_{IH} = 2.4V.
6. This parameter is for inputs with pull-up resistors and V_{IL} = 0.4V.
7. F_C=1 MHz. Not 100% tested.

Table 19. I_{CC} Values

Functional Operating Range: V_{CC} = 3.3 V ±0.3 V; V_{CC5} = 5 V ± 0.25 V (Note 1); T_{CASE} = 0°C to +85°C

Parameter	Operating Frequency	Typ.	Maximum	Notes
I_{CC} Active (Power Supply)	75 MHz 100 MHz		1100 mA 1450 mA	Note 2
I_{CC} Active (Thermal Design)	75 MHz 100 MHz	825 mA 1075 mA	975 mA 1300 mA	Notes 3, 4, 5
I_{CC} Stop Grant	75 MHz 100 MHz	20 mA 50 mA	75 mA 100 mA	Note 6
I_{CC} Stop Clock	0 MHz	600 µA	2 mA	Note 7

NOTES:

1. V_{CC5} should be connected to 3.3 V ± 0.3 V in 3.3 V-only systems.
2. This parameter is for proper power supply selection. It is measured using the worst case instruction mix at V_{CC} = 3.6V.
3. The maximum current column is for thermal design power dissipation. It is measured using the worst case instruction mix at V_{CC} = 3.3V.
4. The typical current column is the typical operating current in a system. This value is measured in a system using a typical device at V_{CC} = 3.3V, running Microsoft Windows 3.1 at an idle condition. This typical value is dependent upon the specific system configuration.
5. Typical values are not 100% tested.
6. The I_{CC} Stop Grant specification refers to the I_{CC} value once the Embedded Write-Back Enhanced IntelDX4 processor enters the Stop Grant or Auto HALT Power Down state.
7. The I_{CC} Stop Clock specification refers to the I_{CC} value once the Embedded Write-Back Enhanced IntelDX4 processor enters the Stop Clock state. The V_{IH} and V_{IL} levels must be equal to V_{CC} and 0 V, respectively, in order to meet the I_{CC} Stop Clock specifications.

5.3 AC Specifications

The AC specifications for the Embedded Write-Back Enhanced IntelDX4 processor are given in this section.

Table 20. AC Characteristics
V_{CC} = 3.3 V ± 0.3 V; V_{CC5} = 5 V ± 0.25 V (Note 1)
T_{CASE} = 0°C to +85°C; C_L = 50pF, unless otherwise specified. (Sheet 1 of 2)

Symbol	Parameter	Product						
		WB75		WB100				
		Min	Max	Min	Max	Unit	Figure	Notes
	CLK Frequency	8	25	8	33	MHz		Note 2
t_1	CLK Period	40	125	30	125	ns	4	
t_{1a}	CLK Period Stability		±250		±250	ps	4	Adjacent clocks Note 3
t_2	CLK High Time	14		11		ns	4	at 2V
t_3	CLK Low Time	14		11		ns	4	at 0.8V
t_4	CLK Fall Time		4		3	ns	4	2V to 0.8V
t_5	CLK Rise Time		4		3	ns	4	0.8V to 2V
t_6	A31–A2, PWT, PCD, BE3–BE0#, M/IO#, D/C#, W/R#, ADS#, LOCK#, FERR#, CACHE#, HITM#, BREQ, HLDA Valid Delay	3	19	3	14	ns	8	
t_7	A31–A2, PWT, PCD, BE3–BE0#, M/IO#, D/C#, W/R#, ADS#, LOCK#, CACHE# Float Delay		28		20	ns	9	Note 3
t_8	PCHK# Valid Delay	3	24	3	14	ns	7	
t_{8a}	BLAST#, PLOCK#, SMIACT# Valid Delay	3	24	3	14	ns	8	
t_9	BLAST#, PLOCK# Float Delay		28		20	ns	9	Note 3
t_{10}	D31–D0, DP3–DP0 Write Data Valid Delay	3	20	3	14	ns	8	
t_{11}	D31–D0, DP3–DP0 Write Data Float Delay		28		20	ns	9	Note 3
t_{12}	EADS#, INV Setup Time	8		5		ns	5	
t_{13}	EADS#, INV Hold Time	3		3		ns	5	
t_{14}	KEN#, BS16#, BS8#, WB/WT# Setup Time	8		5		ns	5	
t_{15}	KEN#, BS16#, BS8#, WB/WT# Hold Time	3		3		ns	5	
t_{16}	RDY#, BRDY# Setup Time	8		5		ns	6	
t_{17}	RDY#, BRDY# Hold Time	3		3		ns	6	

Table 20. AC Characteristics
V_{CC} = 3.3 V ± 0.3 V; V_{CC5} = 5 V ± 0.25 V (Note 1)
T_{CASE} = 0°C to +85°C; C_L = 50pF, unless otherwise specified. (Sheet 2 of 2)

Symbol	Parameter	Product						
		WB75		WB100				
		Min	Max	Min	Max	Unit	Figure	Notes
t_{18}	HOLD, AHOLD Setup Time	8		6		ns	5	
t_{18a}	BOFF# Setup Time	8		7		ns	5	
t_{19}	HOLD, AHOLD, BOFF# Hold Time	3		3		ns	5	
t_{20}	FLUSH#, A20M#, NMI, INTR, SMI#, STPCLK#, SRESET, RESET, IGNNE# Setup Time	8		5		ns	5	Note 4
t_{21}	FLUSH#, A20M#, NMI, INTR, SMI#, STPCLK#, SRESET, RESET, IGNNE# Hold Time	3		3		ns	5	Note 4
t_{22}	D31–D0, DP3–DP0, A31–A4 Read Setup Time	5		5		ns	6 5	
t_{23}	D31–D0, DP3–DP0, A31–A4 Read Hold Time	3		3		ns	6 5	

NOTES:

1. V_{CC5} should be connected to 3.3 V ± 0.3 V in 3.3 V-only systems.
2. 0-MHz operation is guaranteed when the STPCLK# and Stop Grant bus cycle protocol is used.
3. Not 100% tested, guaranteed by design characterization.
4. A reset pulse width of 15 CLK cycles is required for warm resets (RESET or SRESET). Power-up resets (cold resets) require RESET to be asserted for at least 1 ms after V_{CC} and CLK are stable.

Table 21. AC Specifications for the Test Access Port
V_{CC} = 3.3 V ±0.3 V; V_{CC5} = 5 V ±0.25 V (Note 1)
T_{CASE} = 0°C to +85°C; C_L = 50 pF

Symbol	Parameter	Min	Max	Unit	Figure	Notes
t_{24}	TCK Frequency		25	MHz		Note 2
t_{25}	TCK Period	40		ns	10	
t_{26}	TCK High Time	10		ns	10	@ 2.0V
t_{27}	TCK Low Time	10		ns	10	@ 0.8V
t_{28}	TCK Rise Time		4	ns	10	Note 3
t_{29}	TCK Fall Time		4	ns	10	Note 3
t_{30}	TDI, TMS Setup Time	8		ns	11	Note 4
t_{31}	TDI, TMS Hold Time	7		ns	11	Note 4
t_{32}	TDO Valid Delay	3	25	ns	11	Note 4
t_{33}	TDO Float Delay		30	ns	11	Note 4
t_{34}	All Outputs (except TDO) Valid Delay	3	25	ns	11	Note 4
t_{35}	All Outputs (except TDO) Float Delay		36	ns	11	Note 4
t_{36}	All Inputs (except TDI, TMS, TCK) Setup Time	8		ns	11	Note 4
t_{37}	All Inputs (except TDI, TMS, TCK) Hold Time	7		ns	11	Note 4

NOTES:

1. V_{CC5} should be connected to 3.3 V ±0.3 V in 3.3 V-only systems. All inputs and outputs are TTL level.
2. TCK period ≤ CLK period.
3. Rise/Fall times are measured between 0.8V and 2.0V. Rise/Fall times can be relaxed by 1 ns per 10-ns increase in TCK period.
4. Parameters t_{30} – t_{37} are measured from TCK.

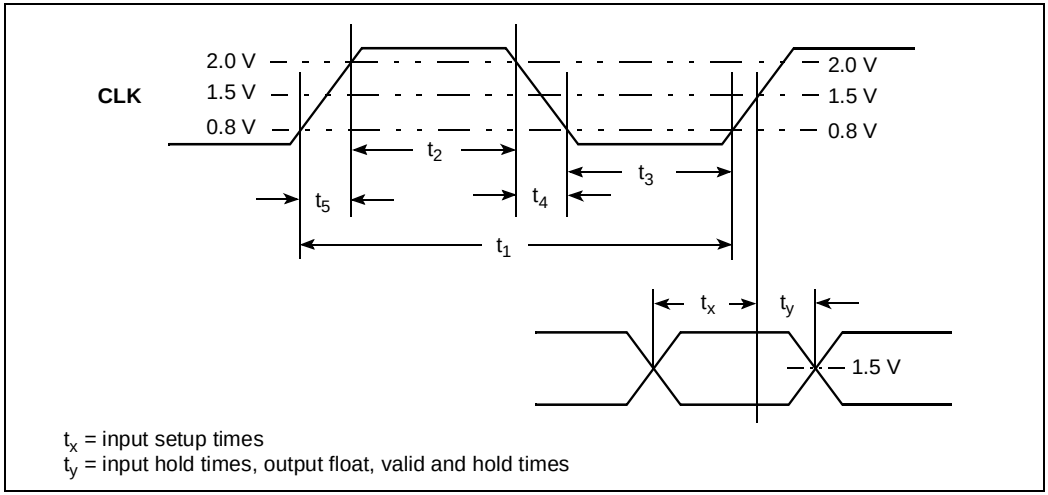


Figure 4. CLK Waveform

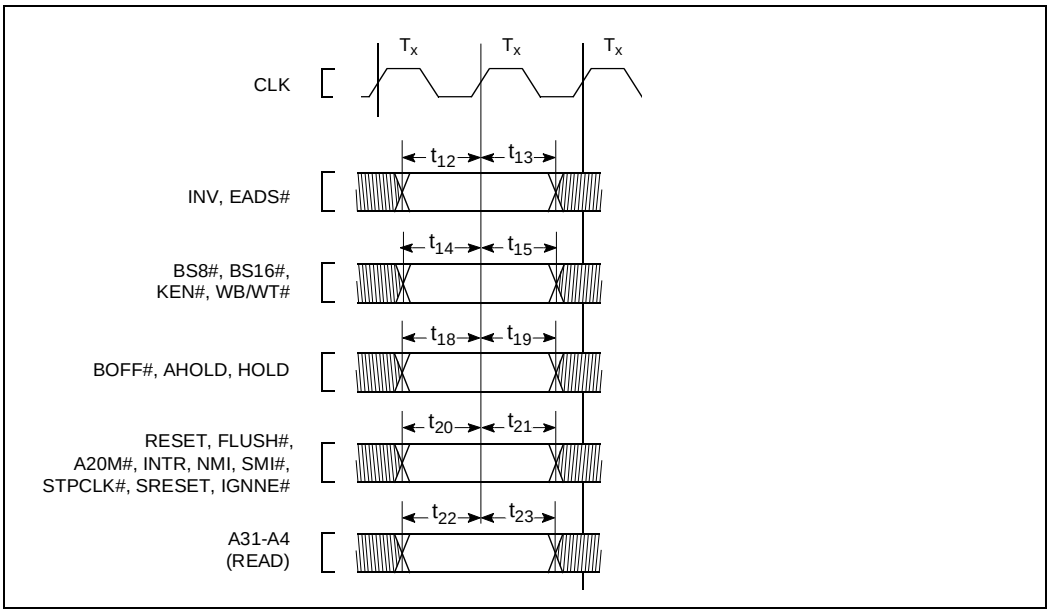


Figure 5. Input Setup and Hold Timing

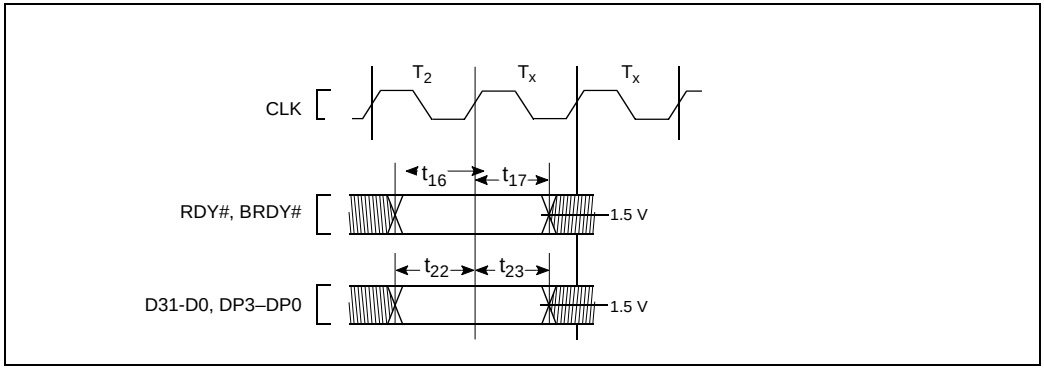


Figure 6. Input Setup and Hold Timing

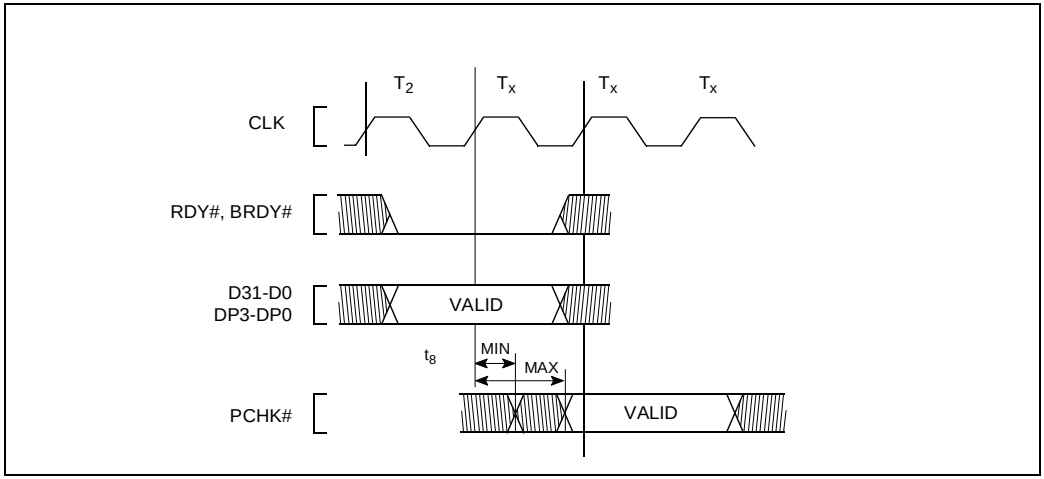


Figure 7. PCHK# Valid Delay Timing

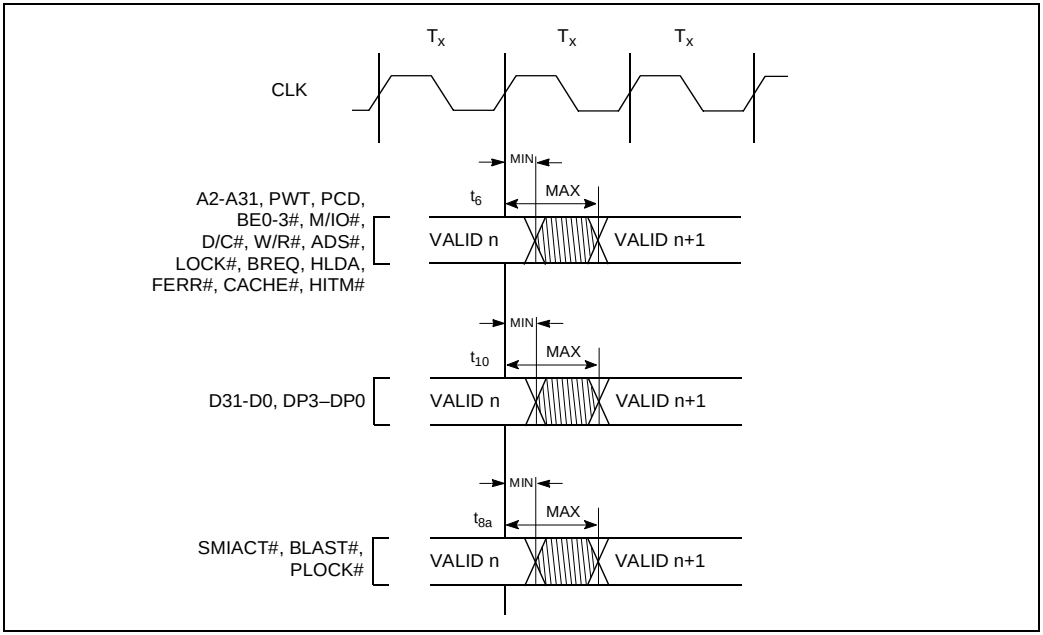


Figure 8. Output Valid Delay Timing

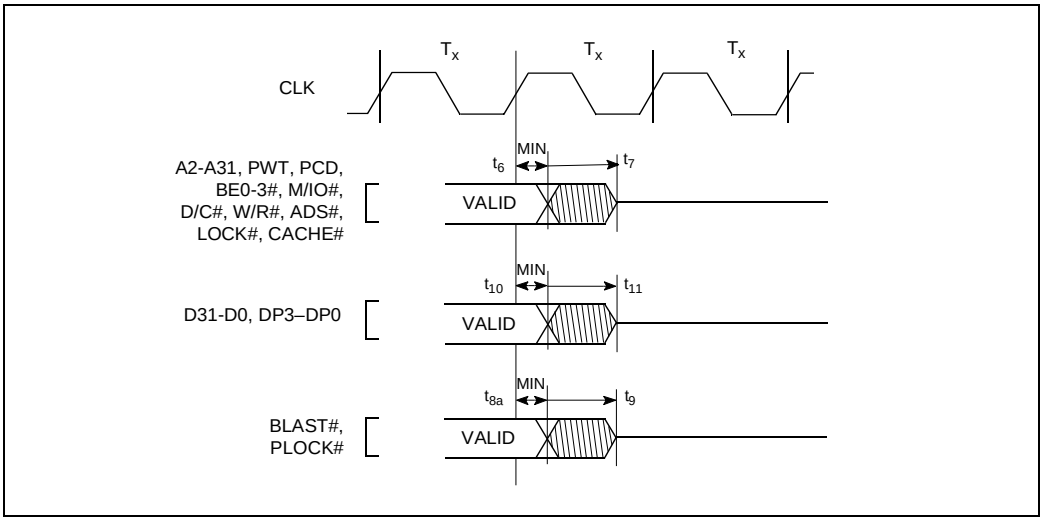


Figure 9. Maximum Float Delay Timing

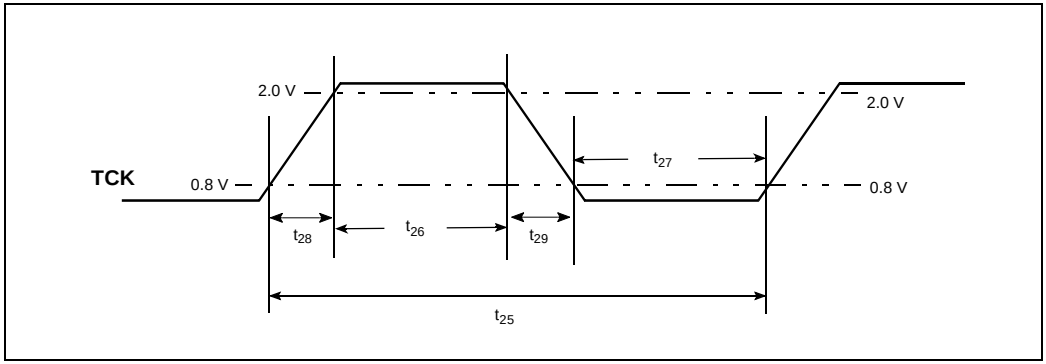


Figure 10. TCK Waveform

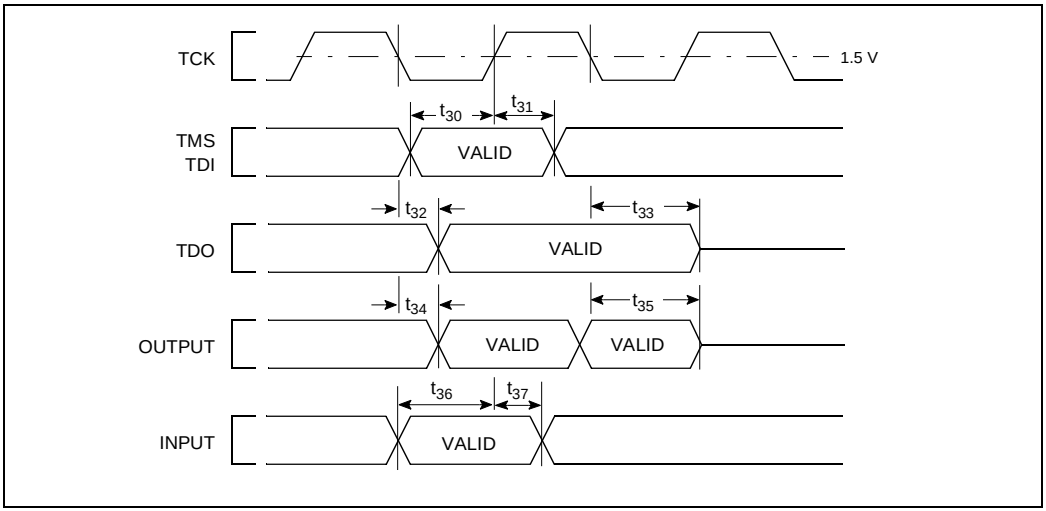
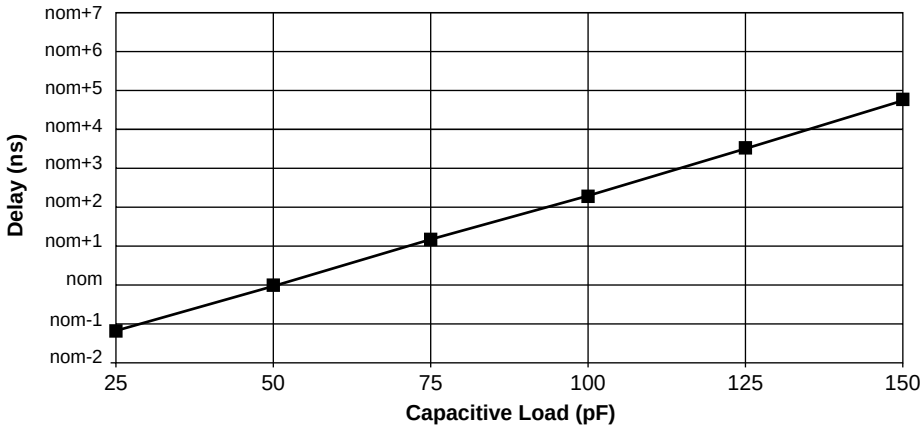


Figure 11. Test Signal Timing Diagram

5.4 Capacitive Derating Curves

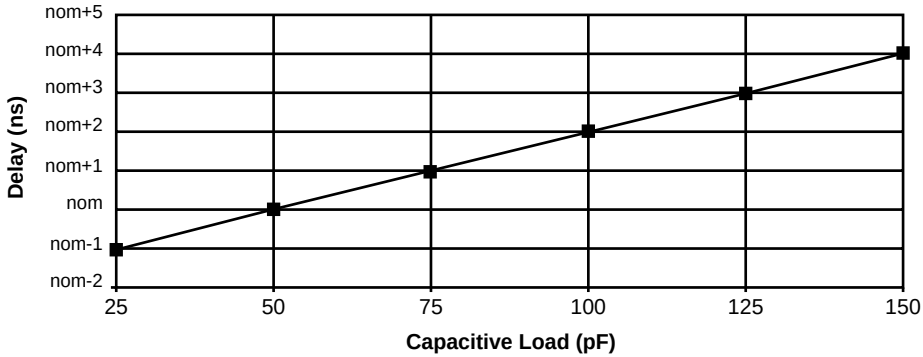
These graphs are the capacitive derating curves for the Embedded Write-Back Enhanced IntelDX4 processor.



Note: This graph will not be linear outside of the capacitive range shown.
nom = nominal value from the AC Characteristics table.

A3238-01

Figure 12. Typical Loading Delay versus Load Capacitance under Worst-Case Conditions for a Low-to-High Transition



Note: This graph will not be linear outside of the capacitive range shown.
nom = nominal value from the AC Characteristics table.

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Figure 13. Typical Loading Delay versus Load Capacitance under Worst-Case Conditions for a High-to-Low Transition

In a mixed voltage system (processors at 3 volts, peripherals at 5 volts), the bus is driven to 5 volts by the peripheral logic. Therefore, the processor must discharge the capacitance on the bus from 5 volts to 0 volts, which takes more time than the 3 volts to 0 volts transition. Inaccurate capacitive derating impacts timing margins and may result in system failures under certain load conditions.

When designing for higher loads in mixed voltage systems, timing margins should be evaluated based on the derating curves shown in Figure 14. For more accurate delay prediction, use I/O buffer models.

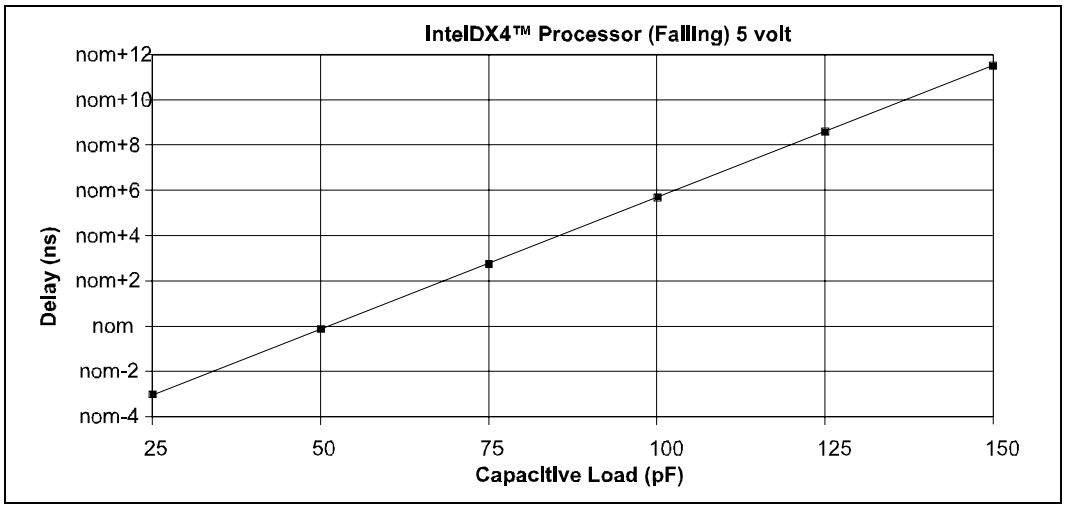


Figure 14. Typical Loading Delay versus Load Capacitance in Mixed Voltage System

6.0 MECHANICAL DATA

This section describes the packaging dimensions and thermal specifications for the Embedded Write-Back Enhanced IntelDX4 processor.

6.1 Package Dimensions

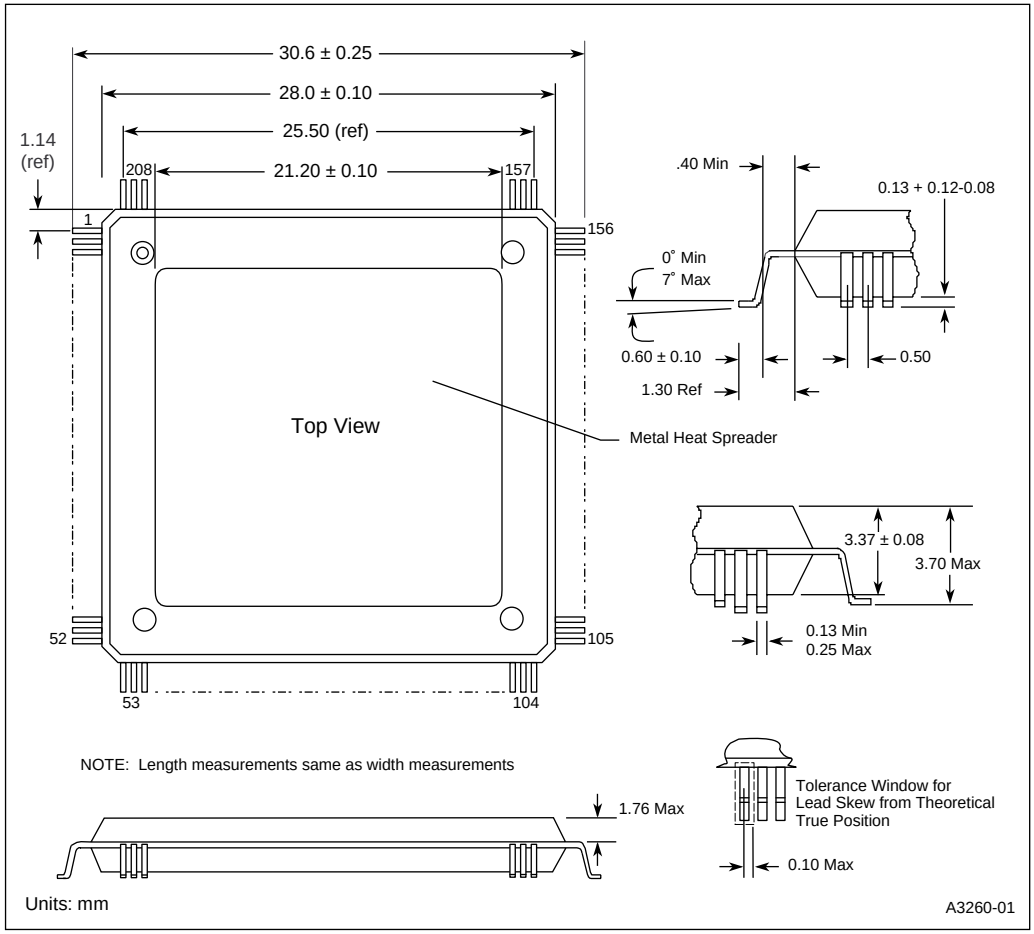


Figure 15. 208-Lead SQFP Package Dimensions

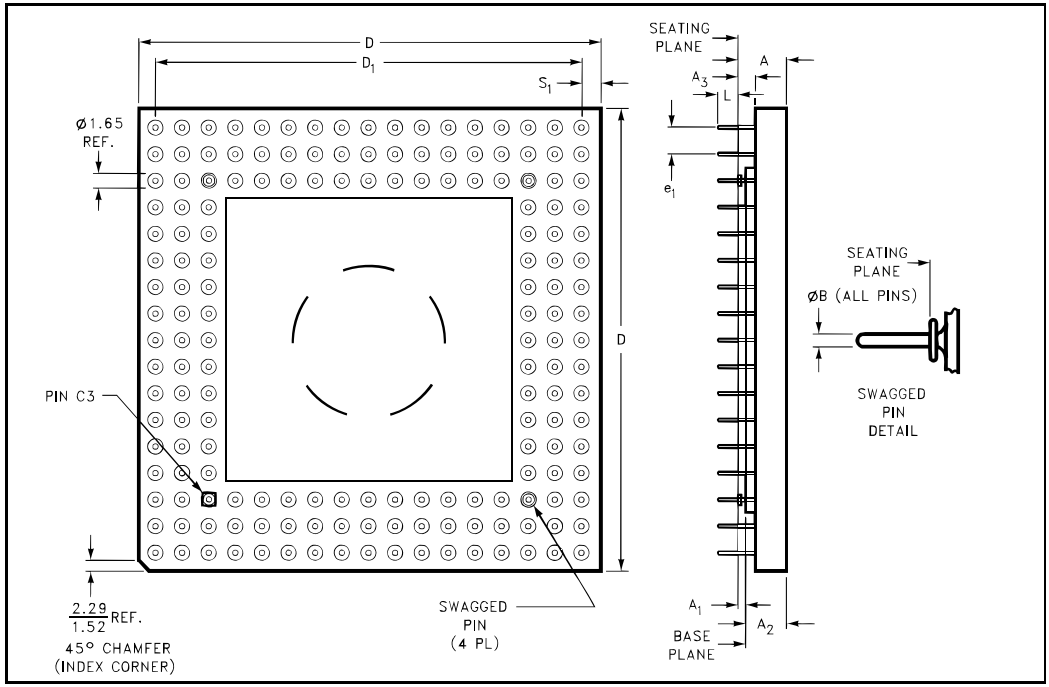


Figure 16. Principal Dimensions and Data for 168-Pin Grid Array Package

Table 22. 168-Pin Ceramic PGA Package Dimensions

Symbol	Millimeters			Inches		
	Min	Max	Notes	Min	Max	Notes
A	3.56	4.57		0.140	0.180	
A_1	0.64	1.14	SOLID LID	0.025	0.045	SOLID LID
A_2	2.8	3.5	SOLID LID	0.110	0.140	SOLID LID
A_3	1.14	1.40		0.045	0.055	
B	0.43	0.51		0.017	0.020	
D	44.07	44.83		1.735	1.765	
D_1	40.51	40.77		1.595	1.605	
e_1	2.29	2.79		0.090	0.110	
L	2.54	3.30		0.100	0.130	
N	168			168		
S_1	1.52	2.54		0.060	0.100	

Table 23. Ceramic PGA Package Dimension Symbols

Letter or Symbol	Description of Dimensions
A	Distance from seating plane to highest point of body
A_1	Distance between seating plane and base plane (lid)
A_2	Distance from base plane to highest point of body
A_3	Distance from seating plane to bottom of body
B	Diameter of terminal lead pin
D	Largest overall package dimension of length
D_1	A body length dimension, outer lead center to outer lead center
e_1	Linear spacing between true lead position centerlines
L	Distance from seating plane to end of lead
S_1	Other body dimension, outer lead center to edge of body

NOTES:

1. Controlling dimension: millimeter.
2. Dimension "e_1" ("e") is non-cumulative.
3. Seating plane (standoff) is defined by P.C. board hole size: 0.0415–0.0430 inch.
4. Dimensions "B", "B_1" and "C" are nominal.
5. Details of Pin 1 identifier are optional.

6.2 Package Thermal Specifications

The Embedded Write-Back Enhanced IntelDX4 processoris specified for operation when the case temperature (T_C) is within the range of 0°C to 85°C. T_C may be measured in any environment to determine whether the processor is within the specified operating range.

The ambient temperature (T_A) can be calculated from θ_{JC} and θ_{JA} from the following equations:

$$T_J = T_C + P * \theta_{JC}$$
$$T_A = T_J - P * \theta_{JA}$$
$$T_C = T_A + P * [\theta_{JA} - \theta_{JC}]$$
$$T_A = T_C - P * [\theta_{JA} - \theta_{JC}]$$

Where T_J, T_A, T_C equals Junction, Ambient and Case Temperature respectively. θ_{JC}, θ_{JA} equals Junction-to-Case and Junction-to-Ambient thermal Resistance, respectively. P is defined as Maximum Power Consumption.

Values for θ_{JA} and θ_{JC} are given in the following tables for each product at its maximum operating frequencies. Maximum T_A is shown for each product operating at its maximum processor frequency (three times the CLK frequency). Refer to the *Embedded Intel486™ Processor Family Developer's Manual* (273021) for a description of the methods used to measure these characteristics.

Table 24. Thermal Resistance, θ_{JA} (°C/W)

Package	Heat Sink	θ_{JA} vs. Airflow — ft/min. (m/sec)					
		0 (0)	200 (1.01)	400 (2.03)	600 (3.04)	800 (4.06)	1000 (5.07)
168-Pin PGA	No	17.5	15.0	13.0	11.5	10.0	9.5
168-Pin PGA	Yes	13.5	8.5	6.5	5.5	4.5	4.25
208-Lead SQFP	No	12.5	10.0	9.0	8.5		
208-Lead SQFP	Yes	10.5	6.5	5.0	4.0		

Table 25. Thermal Resistance, θ_{JC} (°C/W)

Package	Heat Sink	θ_{JC}
168-Pin PGA	No	2.0
168-Pin PGA	Yes	2.0
208-Lead SQFP	No	1.2
208-Lead SQFP	Yes	0.8

Table 26. Maximum $T_{ambient}$, T_A max (°C)

Package	Heat Sink	Airflow — ft/min. (m/sec)				
		Freq. (MHz)	0 (0)	200 (1.01)	400 (2.03)	600 (3.04)
168-Pin PGA	No	100	18.5	29.0	37.5	44.0
168-Pin PGA	Yes	100	35.5	57.0	65.5	70.0
208-Lead SQFP	No	100	36.5	46.0	50.0	52.5
208-Lead SQFP	Yes	100	43.5	60.5	67.0	71.0
208-Lead SQFP	No	75				
208-Lead SQFP	Yes	75				

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