Multichannel, 24-Bit, 192 kHz, Σ-Δ DAC

AD1833A

FEATURES

- 5 V Stereo Audio System with 3.3 V Tolerant Digital Interface
- Supports 96 kHz Sample Rates on 6 Channels and 192 kHz on 2 Channels
- Supports 16-/20-/24-Bit Word Lengths
- Multibit Σ-Δ Modulators with Perfect Differential Linearity Restoration for Reduced Idle Tones and Noise Floor
- Data Directed Scrambling DACs—Least Sensitive to Jitter
- Differential Output for Optimum Performance
- DACs Signal-to-Noise and Dynamic Range: 110 dB
- –94 dB THD + N—6-Channel Mode
- –95 dB THD + N—2-Channel Mode
- On-Chip Volume Control per Channel with 1024-Step Linear Scale
- Software Controllable Clickless Mute
- Digital De-emphasis Processing
- Supports 256 × f_S, 512 × f_S, and 768 × f_S Master Clock Modes
- Power-Down Mode Plus Soft Power-Down Mode
- Flexible Serial Data Port with Right-Justified, Left-Justified, I^2S Compatible, and DSP Serial Port Modes
- Supports Packed Data Mode and TDM Mode
- 48-Lead LQFP Plastic Package

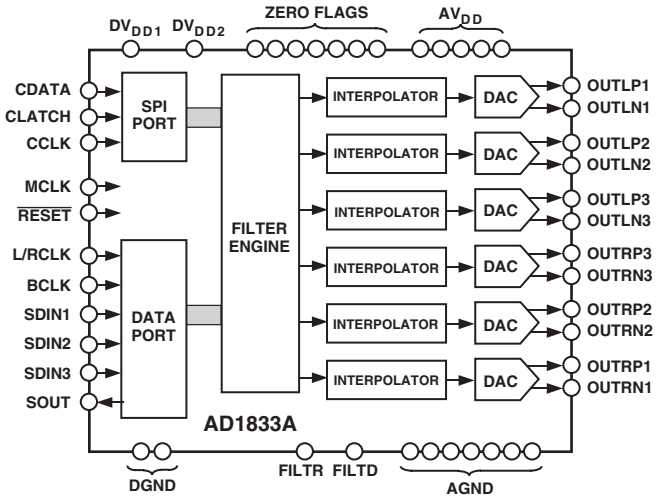
APPLICATIONS

- DVD Video and Audio Players
- Home Theater Systems
- Automotive Audio Systems
- Set-Top Boxes
- Digital Audio Effects Processors

GENERAL DESCRIPTION

The AD1833A is a complete, high performance, single-chip, multichannel, digital audio playback system. It features six audio playback channels, each comprising a high performance digital interpolation filter, a multibit Σ-Δ modulator featuring Analog Devices' patented technology, and a continuous-time voltage-out analog DAC section. Other features include an on-chip clickless attenuator and mute capability for each channel, programmed through an SPI compatible serial control port.

FUNCTIONAL BLOCK DIAGRAM



The AD1833A is fully compatible with all known DVD formats, accommodating word lengths of up to 24 bits at sample rates of 48 kHz and 96 kHz on all six channels while supporting a 192 kHz sample rate on two channels. It also provides the Redbook standard 50 µs/15 µs digital de-emphasis filters at sample rates of 32 kHz, 44.1 kHz, and 48 kHz.

The AD1833A has a very flexible serial data input port that allows glueless interconnection to a variety of ADCs, DSP chips, AES/EBU receivers, and sample rate converters. It can be configured in right-justified, left-justified, I^2S, or DSP serial port compatible modes. The AD1833A accepts serial audio data in MSB first, twos complement format. The AD1833A can be operated from a single 5 V power supply; it also features a separate supply pin for its digital interface that allows it to be interfaced to devices using 3.3 V power supplies.

The AD1833A is fabricated on a single monolithic integrated circuit and is housed in a 48-lead LQFP package for operation from –40°C to +85°C.

REV. 0

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AD1833A–SPECIFICATIONS

TEST CONDITIONS, UNLESS OTHERWISE NOTED*

Supply Voltages (AV_{DD}, DV_{DDX})	5 V
Ambient Temperature	25°C
Input Clock	12.288 MHz, (8× Mode)
Input Signal	Nominally 1 kHz, 0 dBFS (Full-Scale)
Input Sample Rate	48 kHz
Measurement Bandwidth	20 Hz to 20 kHz
Word Width	24 Bits
Load Capacitance	100 pF
Load Impedance	10 kΩ

*Performance is identical for all channels (except for the Interchannel Gain Mismatch and Interchannel Phase Deviation specifications).

Parameter	Min	Typ	Max	Unit	Test Conditions
ANALOG PERFORMANCE					
DIGITAL-TO-ANALOG CONVERTERS					
Dynamic Range (20 Hz to 20 kHz, –60 dBFS Input)					
with A-Weighted Filter					
AD1833AA	106.5	110.0		dB	
AD1833AA		110.5		dB	f_S = 96 kHz
AD1833AC		107.0		dB	
Total Harmonic Distortion + Noise		–95	–89	dB	Two channels active
		–94		dB	Six channels active
		–95		dB	96 kHz, two channels active
		–94		dB	96 kHz, six channels active
SNR		110		dB	
Interchannel Isolation		108		dB	
DC Accuracy					
Gain Error		±3		%	
Interchannel Gain Mismatch		0.2		%	
Gain Drift		80		ppm/°C	
Interchannel Crosstalk (EIAJ Method)		–120		dB	
Interchannel Phase Deviation		±0.1		Degrees	
Volume Control Step Size (1023 Linear Steps)		0.098		%	
Volume Control Range (Max Attenuation)		+63.5 (0.098)		dB (%)	
Mute Attenuation		–63.5 (0.098)		dB (%)	
De-emphasis Gain Error		±0.1		dB	
Full-Scale Output Voltage at Each Pin (Single-Ended)		1 (2.8)		V rms (V p-p)	
Output Resistance Measured Differentially		150		Ω	
Common-Mode Output Volts		2.2		V	
DAC INTERPOLATION FILTER—8× Mode (48 kHz)					
Pass Band			21.768	kHz	
Pass-Band Ripple		±0.01		dB	
Stop Band	24			kHz	
Stop-Band Attenuation	70			dB	
Group Delay		510		µs	
DAC INTERPOLATION FILTER—4× Mode (96 kHz)					
Pass Band			37.7	kHz	
Pass-Band Ripple		±0.03		dB	
Stop Band	55.034			kHz	
Stop-Band Attenuation	70			dB	
Group Delay		160		µs	
DAC INTERPOLATION FILTER—2× Mode (192 kHz)					
Pass Band			89.954	kHz	
Pass-Band Ripple		±1		dB	
Stop Band	104.85			kHz	
Stop-Band Attenuation	70			dB	
Group Delay		140		µs	

Parameter	Min	Typ	Max	Unit	Test Conditions
DIGITAL I/O					
Input Voltage HI	2.4			V	
Input Voltage LO			0.8	V	
Output Voltage HI	$DV_{DD2} - 0.4$			V	
Output Voltage LO			0.4	V	
POWER SUPPLIES					
Supply Voltage (AV_{DD} and DV_{DD1})	4.5	5	5.5	V	
Supply Voltage (DV_{DD2})	3.3		DV_{DD1}	V	
Supply Current I_{ANALOG}		38.5	42	mA	
Supply Current $I_{DIGITAL}$		42	48	mA	Active
		2		mA	Power-Down
Power Supply Rejection Ratio					
1 kHz 300 mV p-p Signal at Analog Supply Pins		–60		dB	
20 kHz 300 mV p-p Signal at Analog Supply Pins		–50		dB	

Specifications subject to change without notice.

DIGITAL TIMING (Guaranteed over –40°C to +85°C, $AV_{DD} = DV_{DD} = 5$ V ± 10%)

Parameter		Min	Max	Unit	Comments
MASTER CLOCK AND RESET					
t_{ML}	MCLK LO (All Modes)*	15		ns	24 MHz clock, clock doubler bypassed
t_{MH}	MCLK HI (All Modes)*	15		ns	24 MHz clock, clock doubler bypassed
t_{PDR}	$\overline{PD}/\overline{RST}$ LO	20		ns	
SPI PORT					
t_{CCH}	CCLK HI Pulsewidth	20		ns	
t_{CCL}	CCLK LO Pulsewidth	20		ns	
t_{CCP}	CCLK Period	80		ns	
t_{CDS}	CDATA Setup Time	10		ns	To CCLK rising
t_{CDH}	CDATA Hold Time	10		ns	From CCLK rising
t_{CLS}	CLATCH Setup	10		ns	To CCLK rising
t_{CLH}	CLATCH Hold	10		ns	From CCLK rising
DAC SERIAL PORT					
t_{DBH}	BCLK HI	15		ns	
t_{DBL}	BCLK LO	15		ns	
t_{DLS}	L/RCLK Setup	10		ns	To BCLK rising
t_{DLH}	L/RCLK Hold	10		ns	From BCLK rising
t_{DDS}	SDATA Setup	10		ns	To BCLK rising
t_{DDH}	SDATA Hold	15		ns	From BCLK rising
TDM MODE MASTER					
t_{TMBD}	BCLKTDM Delay		20	ns	From MCLK rising
t_{TMFSD}	FSTDM Delay		10	ns	From BCLKTDM rising
t_{TMDDS}	SDIN1 Setup	15		ns	To BCLKTDM falling
t_{TMDDH}	SDIN1 Hold	15		ns	From BCLKTDM falling
TDM MODE SLAVE					
f_{TSB}	BCLKTDM Frequency	$256 \times f_S$			
t_{TSBCH}	BCLKTDM High	20		ns	
t_{TSBCL}	BCLKTDM Low	20		ns	
t_{TSFS}	FSTDM Setup	10		ns	To BCLKTDM falling
t_{TSFH}	FSTDM Hold	10		ns	From BCLKTDM falling
t_{TSDDS}	SDIN1 Setup	15		ns	To BCLKTDM falling
t_{TSDDH}	SDIN1 Hold	15		ns	From BCLKTDM falling
AUXILIARY INTERFACE					
t_{AXLRD}	L/RCLK Delay		10	ns	From BCLK falling
t_{AXDD}	Data Delay		10	ns	From BCLK falling
t_{AXBD}	AUXBCLK Delay		20	ns	From MCLK rising

*MCLK symmetry must be better than 60:40 or 40:60.

Specifications subject to change without notice.

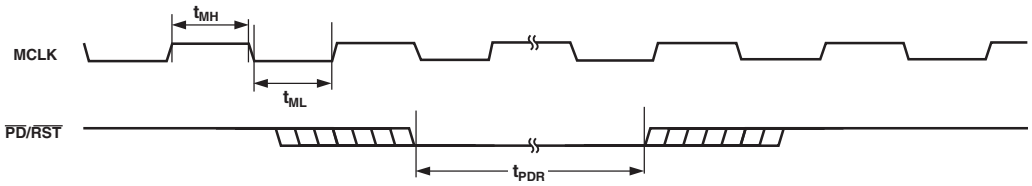


Figure 1. MCLK and $\overline{RESET}$ Timing

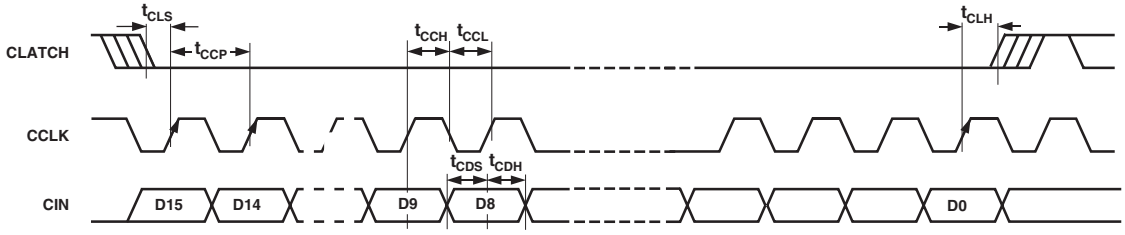


Figure 2. SPI Port Timing

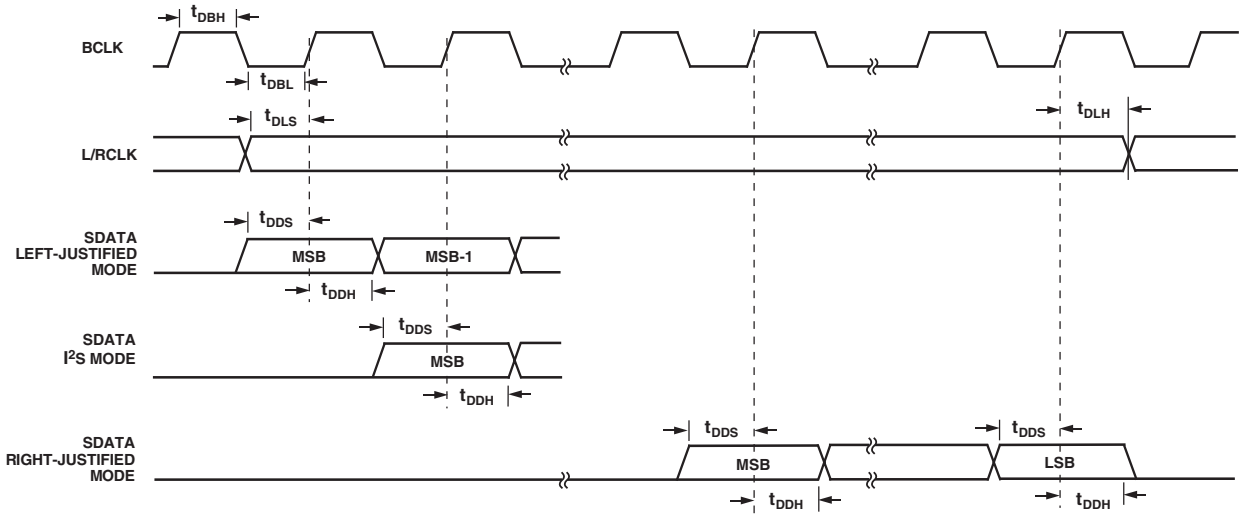


Figure 3. Serial Port Timing

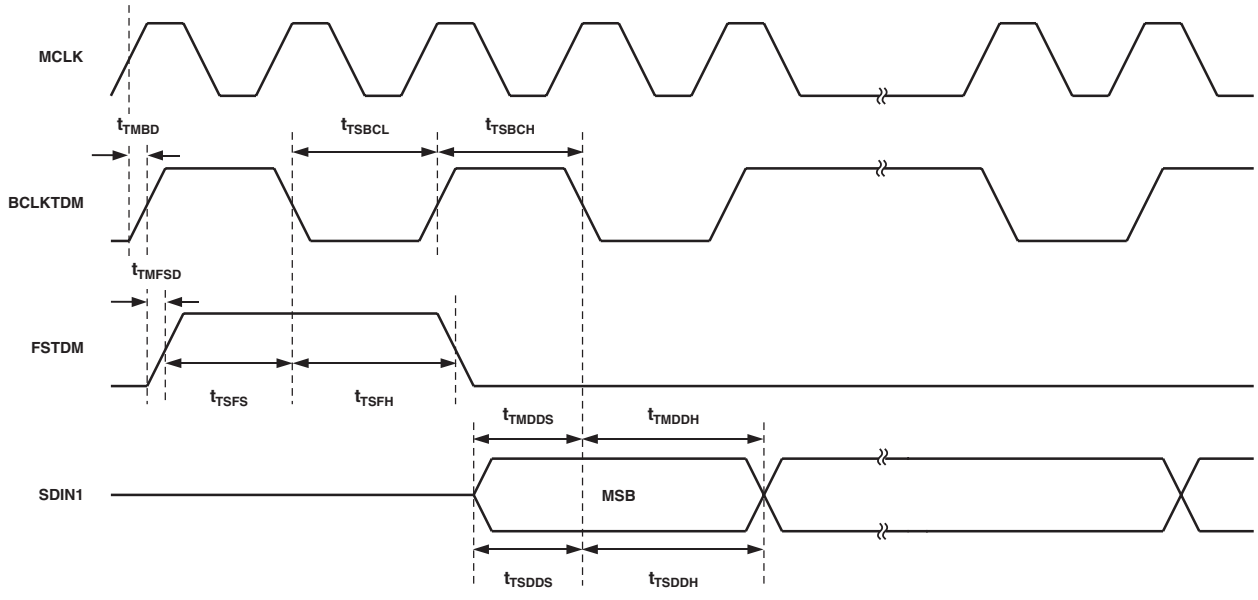


Figure 4. TDM Master and Slave Mode Timing

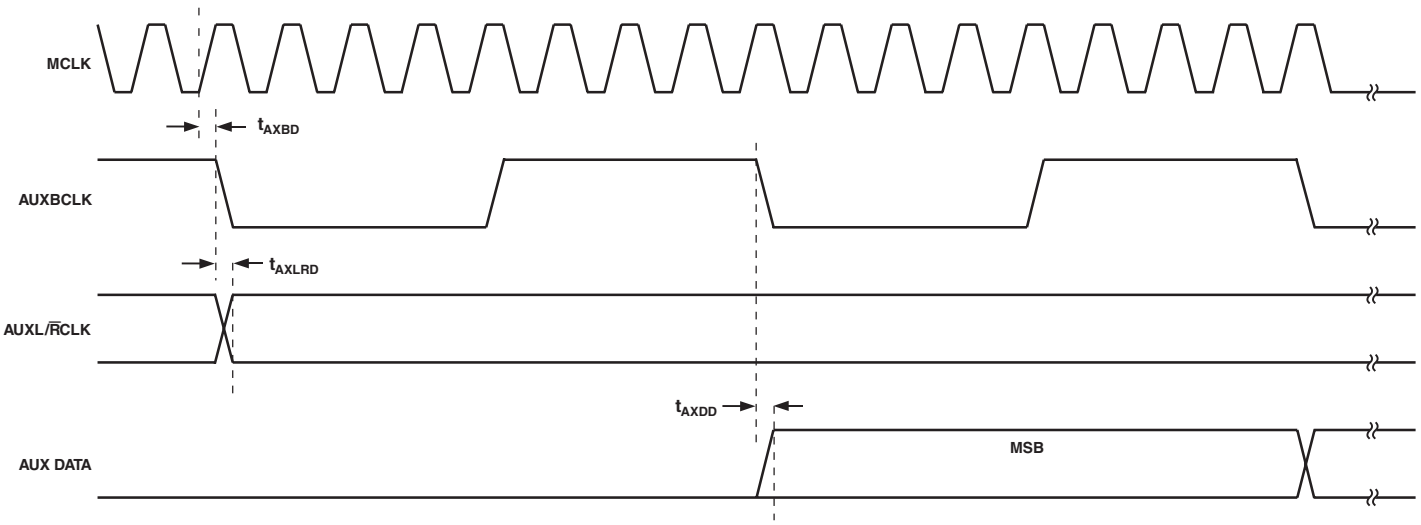


Figure 5. Auxiliary Interface Timing

ABSOLUTE MAXIMUM RATINGS*
(T_A = 25°C, unless otherwise noted.)

AV_{DD}, DV_{DDX} to AGND, DGND . . . . . –0.3 V to +6.5 V
AGND to DGND . . . . . –0.3 V to +0.3 V
Digital I/O Voltage to DGND . . . . . –0.3 V to DV_{DD2} + 0.3 V
Analog I/O Voltage to AGND . . . . . –0.3 V to AV_{DD} + 0.3 V
Operating Temperature Range
Industrial (A Version) . . . . . –40°C to +85°C
Storage Temperature Range . . . . . –65°C to +150°C
Maximum Junction Temperature . . . . . 150°C
LQFP, θ_{JA} Thermal Impedance . . . . . 91°C/W
Lead Temperature, Soldering
Vapor Phase (60 sec) . . . . . 215°C
Infrared (15 sec) . . . . . 220°C

*Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Only one absolute maximum rating may be applied at any one time.

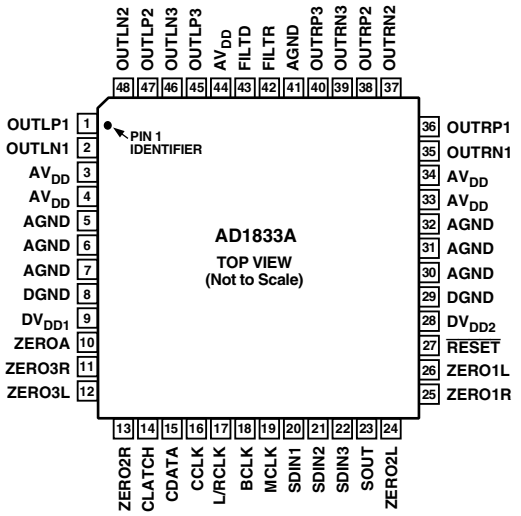
ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
AD1833AAST	–40°C to +85°C	Low Profile Quad Flat Package	ST-48
AD1833ACST	–40°C to +85°C	Low Profile Quad Flat Package	ST-48
EVAL-AD1833AEB		Evaluation Board	
AD1833AAST-REEL	–40°C to +85°C	Low Profile Quad Flat Package	ST-48
AD1833ACST-REEL	–40°C to +85°C	Low Profile Quad Flat Package	ST-48

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD1833A features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN CONFIGURATION



PIN FUNCTION DESCRIPTIONS

Pin No.	Mnemonic	IN/OUT	Description
1	OUTLP1	O	DAC 1 Left Channel Positive Output.
2	OUTLN1	O	DAC 1 Left Channel Negative Output.
3, 4, 33, 34, 44	AV_{DD}		Analog Supply.
5, 6, 7, 30, 31, 32, 41	AGND		Analog Ground.
8, 29	DGND		Digital Ground.
9	DV_{DD1}		Digital Supply to Core Logic.
10	ZEROA	O	Flag to Indicate Zero Input on All Channels.
11	ZERO3R	O	Flag to Indicate Zero Input on Channel 3 Right.
12	ZERO3L	O	Flag to Indicate Zero Input on Channel 3 Left.
13	ZERO2R	O	Flag to Indicate Zero Input on Channel 2 Right.
14	CLATCH	I	Latch Input for Control Data (SPI Port).
15	CDATA	I	Serial Control Data Input (SPI Port).
16	CCLK	I	Clock Input for Control Data (SPI Port).
17	L/RCLK	I/O	Left/Right Clock for DAC Data Input; FSTDM Input in TDM Slave Mode; FSTDM Output in TDM Master Mode.
18	BCLK	I/O	Bit Clock for DAC Data Input; BCLKTDM Input in TDM Slave Mode; BCLKTDM Output in TDM Master Mode.
19	MCLK	I	Master Clock Input.
20	SDIN1	I	Data Input for Channel 1 Left/Right (Data Stream Input in TDM and Packed Modes).
21	SDIN2	I/O	Data Input for Channel 2 Left/Right (L/RCLK Output to Auxiliary DAC in TDM Mode).
22	SDIN3	I/O	Data Input for Channel 3 Left/Right (BCLK Output to Auxiliary DAC in TDM Mode).
23	SOUT	O	Auxiliary I^2S Output (Available in TDM Mode).
24	ZERO2L	O	Flag to Indicate Zero Input on Channel 2 Left.
25	ZERO1R	O	Flag to Indicate Zero Input on Channel 1 Right.
26	ZERO1L	O	Flag to Indicate Zero Input on Channel 1 Left.
27	$\overline{\text{RESET}}$	I	Power-Down and Reset Control.
28	DV_{DD2}		Power Supply to Output Interface Logic.
35	OUTRN1	O	DAC 1 Right Channel Negative Output.
36	OUTRP1	O	DAC 1 Right Channel Positive Output.
37	OUTRN2	O	DAC 2 Right Channel Negative Output.
38	OUTRP2	O	DAC 2 Right Channel Positive Output.
39	OUTRN3	O	DAC 3 Right Channel Negative Output.

PIN FUNCTION DESCRIPTIONS (continued)

Pin No.	Mnemonic	IN/OUT	Description
40	OUTRP3	O	DAC 3 Right Channel Positive Output.
42	FILTR		Reference/Filter Capacitor Connection. Recommend 0.1 µF/10 µF decouple to analog ground.
43	FILTD		Filter Capacitor Connection. Recommend 0.1 µF/10 µF decouple to analog ground.
45	OUTLP3	O	DAC 3 Left Channel Positive Output.
46	OUTLN3	O	DAC 3 Left Channel Negative Output.
47	OUTLP2	O	DAC 2 Left Channel Positive Output.
48	OUTLN2	O	DAC 2 Left Channel Negative Output.

DEFINITION OF TERMS

Dynamic Range
The ratio of a full-scale input signal to the integrated input noise in the pass band (20 Hz to 20 kHz), expressed in decibels. Dynamic range is measured with a –60 dB input signal and is equal to (S/[THD + N]) +60 dB. Note that spurious harmonics are below the noise with a –60 dB input, so the noise level establishes the dynamic range. The dynamic range is specified with and without an A-Weight filter applied.

Signal to (Total Harmonic Distortion + Noise) [S/(THD + N)]
The ratio of the root-mean-square (rms) value of the fundamental input signal to the rms sum of all other spectral components in the pass band, expressed in decibels.

Pass Band
The region of the frequency spectrum unaffected by the attenuation of the digital decimator's filter.

Pass-Band Ripple
The peak-to-peak variation in amplitude response from equal-amplitude input signal frequencies within the pass band, expressed in decibels.

Stop Band
The region of the frequency spectrum attenuated by the digital decimator's filter to the degree specified by stop-band attenuation.

Gain Error
With a near full-scale input, the ratio of actual output to expected output, expressed as a percentage.

Interchannel Gain Mismatch
With identical near full-scale inputs, the ratio of outputs of the two stereo channels, expressed in decibels.

Gain Drift
Change in response to a nearly full-scale input with a change in temperature, expressed as parts-per-million (ppm/°C).

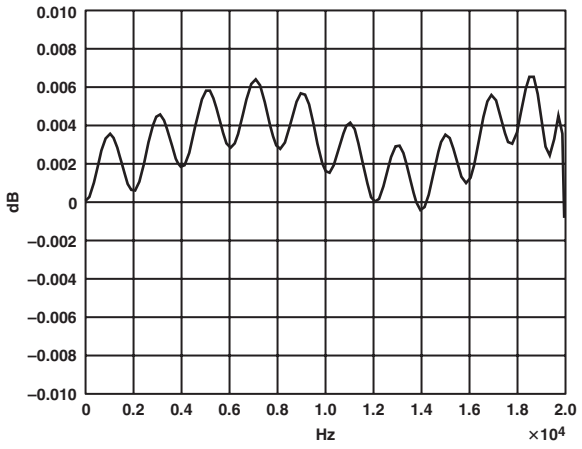
Crosstalk (EIAJ Method)
Ratio of response on one channel with a grounded input to a full-scale 1 kHz sine wave input on the other channel, expressed in decibels.

Power Supply Rejection
With no analog input, signal present at the output when a 300 mV p-p signal is applied to the power supply pins, expressed in decibels of full scale.

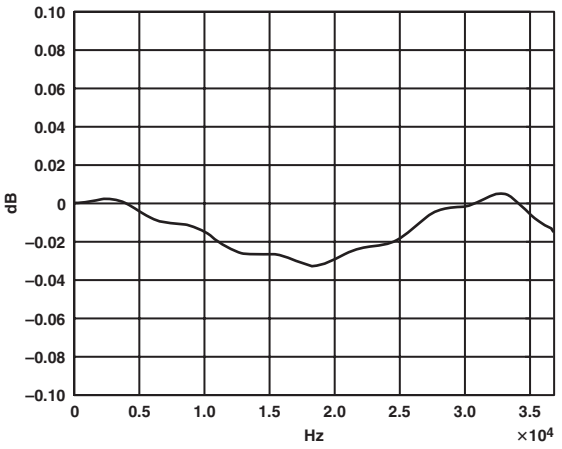
Group Delay
Intuitively, the time interval required for an input pulse to appear at the converter's output, expressed in ms. More precisely, the derivative of radian phase with respect to the radian frequency at a given frequency.

Group Delay Variation
The difference in group delays at different input frequencies. Specified as the difference between the largest and the smallest group delays in the pass band, expressed in µs.

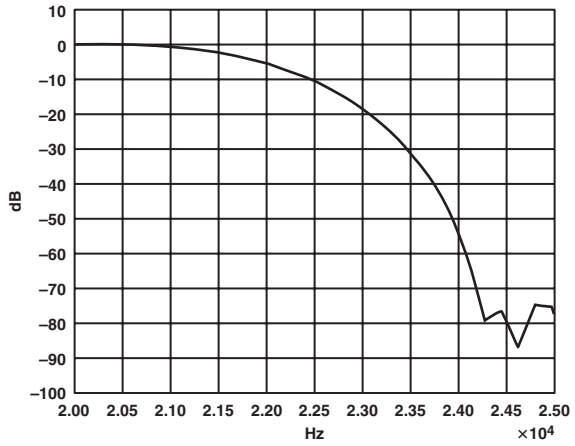
AD1833A–Typical Performance Characteristics



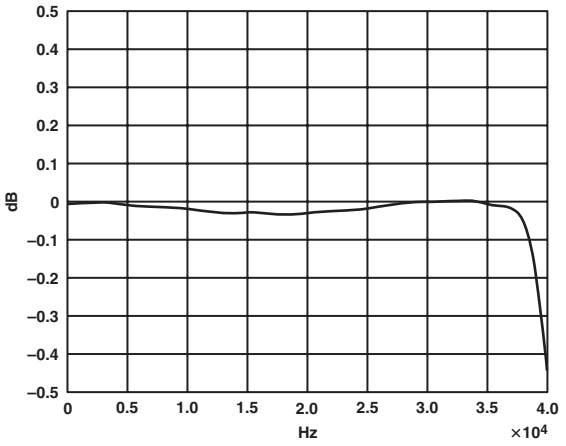
TPC 1. Pass-Band Response, 8× Mode



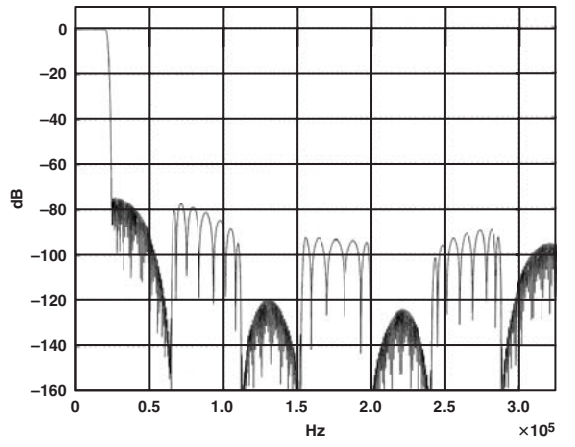
TPC 4. Pass-Band Response, 4× Mode



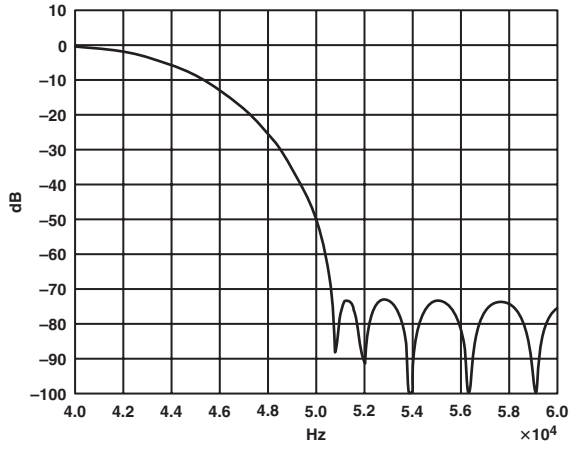
TPC 2. Transition Band Response, 8× Mode



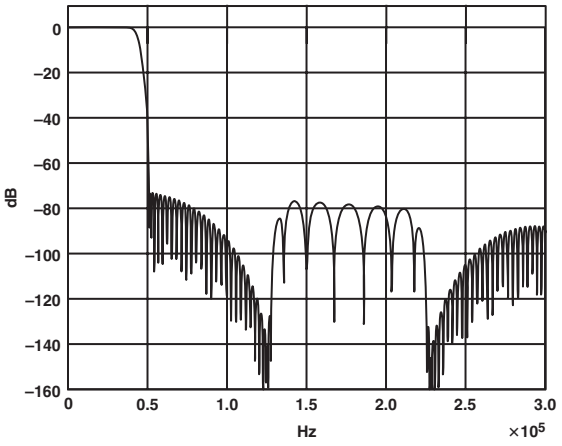
TPC 5. 40 kHz Pass-Band Response, 4× Mode



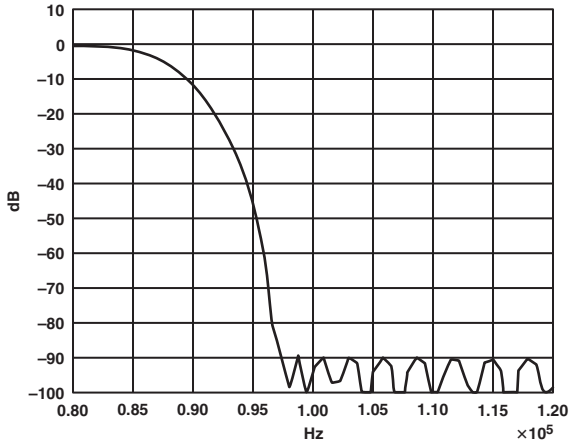
TPC 3. Complete Response, 8× Mode



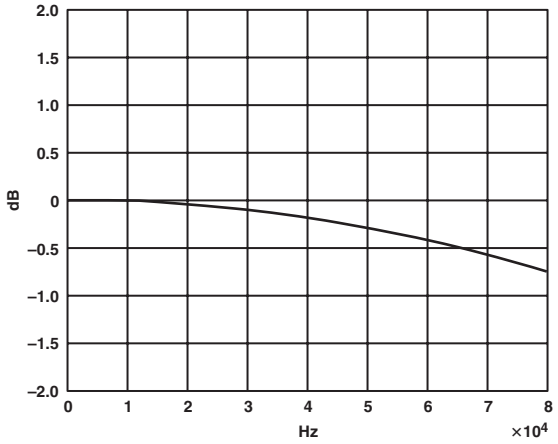
TPC 6. Transition Band Response, 4× Mode



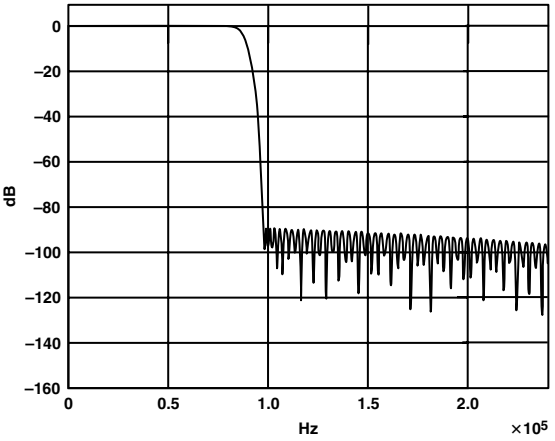
TPC 7. Complete Response, 4× Mode



TPC 9. Transition Band Response, 2× Mode



TPC 8. 80 kHz Pass-Band Response, 2× Mode



TPC 10. Complete Response, 2× Mode

FUNCTIONAL DESCRIPTION

Device Architecture

The AD1833A is a six-channel audio DAC featuring multibit sigma-delta (Σ-Δ) technology. The AD1833A features three stereo converters (providing six channels); each stereo channel is controlled by a common bit-clock (BCLK) and synchronization signal (L/RCLK).

General Overview

The AD1833A is designed to run with an internal MCLK (IMCLK) of 24.576 MHz and a modulator rate of 6.144 MHz (i.e., IMCLK/4). From this IMCLK frequency, sample rates of 48 kHz and 96 kHz can be achieved on six channels or 192 kHz can be achieved on two channels. The internal clock should never be run at a higher frequency but may be reduced to achieve lower sampling rates, i.e., for a sample rate of 44.1 kHz, the appropriate internal MCLK is 22.5792 MHz. The modulator rate scales in proportion with the MCLK scaling.

Interpolator

The interpolator consists of as many as three stages of sample rate doubling and half-band filtering followed by a 16-sample zero order hold (ZOH). The sample rate doubling is achieved by zero stuffing the input samples, and a digital half-band filter is used to remove any images above the band of interest and to bring the zero samples to their correct values.

The interpolator output must always be at a rate of IMCLK/64. Depending on the interpolation rates selected, one, two, or all three stages of doubling may be switched in. This allows for three different sample rate inputs for any given IMCLK. For an IMCLK of 24.576 MHz, all three doubling stages are used with a 48 kHz input sample rate; with a 96 kHz input sample rate, only two doubling stages are used; and with a 192 kHz input sample rate, only one doubling stage is used. In each case, the input sample frequency is increased to 384 kHz (IMCLK/64). The ZOH holds the interpolator samples for upsampling by the modulator. This is done at a rate 16 times the interpolator output sample rate.

Modulator

The modulator is a 6-bit, second order implementation and uses data scrambling techniques to achieve perfect linearity. The modulator samples the output of the interpolator stage(s) at a rate of (IMCLK/4).

OPERATING FEATURES

SPI Register Definitions

The SPI port allows flexible control of the device's programmable functions. It is organized around nine registers: six individual channel volume registers and three control registers. Each write operation to the AD1833A SPI control port requires 16 bits of serial data in MSB-first format. The four most significant bits are used to select one of nine registers (seven register addresses are reserved), and the bottom 10 bits are written to that register. This allows a write to one of the nine registers in a single 16-bit transaction. The SPI CCLK signal is used to clock in the data. The incoming data should change on the falling edge of this signal and remain valid during the rising edge. At the end of the 16 CCLK periods, the CLATCH signal should rise to latch the data internally into the AD1833A (see Figure 2).

The serial interface format used on the control port uses a 16-bit serial word, as shown in Table I. The 16-bit word is divided into several fields: Bits 15 through 12 define the register address, Bits 11 and 10 are reserved and must be programmed to 0, and Bits 9 through 0 are the data field (which has specific definitions, depending on the register selected).

Table I. Control Port Map

Register Address				Reserved[1]		Data Field									
15[2]	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

NOTES
[1]Must be programmed to zero.
[2]Bit 15 = MSB.

Bit 15	Bit 14	Bit 13	Bit 12	Register Function
0	0	0	0	DAC Control 1
0	0	0	1	DAC Control 2
0	0	1	0	DAC Volume 1
0	0	1	1	DAC Volume 2
0	1	0	0	DAC Volume 3
0	1	0	1	DAC Volume 4
0	1	1	0	DAC Volume 5
0	1	1	1	DAC Volume 6
1	0	0	0	DAC Control 3
1	0	0	1	Reserved
1	0	1	0	Reserved
1	0	1	1	Reserved
1	1	0	0	Reserved
1	1	0	1	Reserved
1	1	1	0	Reserved
1	1	1	1	Reserved

Table II. DAC Control Register 1

Address	Reserved[1]		De-emphasis	Function			
				Serial Mode	Data-Word Width	Power-Down RESET	Interpolator Mode
15–12	11	10	9–8	7–5	4–3	2	1–0
0000	0	0	00 = None 01 = 44.1 kHz 10 = 32.0 kHz 11 = 48.0 kHz	000 = I^2S 001 = RJ 010 = DSP 011 = LJ 100 = Pack Mode 1 (256) 101 = Pack Mode 2 (128) 110 = TDM Mode 111 = Reserved	00 = 24 Bits 01 = 20 Bits 10 = 16 Bits 11 = Reserved	0 = Normal 1 = PWRDWN	00 = 8× (48 kHz)[2] 01 = 2× (192 kHz)[2] 10 = 4× (96 kHz)[2] 11 = Reserved

NOTES
[1]Must be programmed to zero.
[2]For IMCLK = 24.576 MHz.

DAC CONTROL REGISTER 1

De-emphasis

The AD1833A has a built-in de-emphasis filter that can be used to decode CDs that have been encoded with the standard Redbook 50 µs/15 µs emphasis response curve. Three curves are available, one each for 32 kHz, 44.1 kHz, and 48 kHz sampling rates. The filters may be selected by writing to Control Bits 9 and 8 in DAC Control Register 1 (see Table III).

Table III. De-emphasis Settings

Bit 9	Bit 8	De-emphasis
0	0	Disabled
0	1	44.1 kHz
1	0	32 kHz
1	1	48 kHz

Data Serial Interface Mode

The AD1833A's serial data interface is designed to accept data in a wide range of popular formats including I^2S, right-justified (RJ), left-justified (LJ), and flexible DSP modes. The L/RCLK pin acts as the word clock (or frame sync) to indicate sample interval boundaries. The BCLK defines the serial data rate while the data is input on the SDIN1–SDIN3 pins. The serial mode settings may be selected by writing to Control Bits 7 through 5 in the DAC Control Register 1 (see Table IV).

Table IV. Data Serial Interface Mode Settings

Bit 7	Bit 6	Bit 5	Serial Mode
0	0	0	I^2S
0	0	1	Right Justify
0	1	0	DSP
0	1	1	Left Justify
1	0	0	Packed Mode 1 (256)
1	0	1	Packed Mode 2 (128)
1	1	0	TDM Mode
1	1	1	Reserved

DAC Word Width

The AD1833A will accept input data in three separate word-lengths—16 bits, 20 bits, and 24 bits. The word length may be selected by writing to Control Bits 4 and 3 in DAC Control Register 1 (see Table V).

Table V. Word Length Settings

Bit 4	Bit 3	Word Length
0	0	24 Bits
0	1	20 Bits
1	0	16 Bits
1	1	Reserved

Power-Down Control

The AD1833A can be powered down by writing to Control Bit 2 in DAC Control Register 1 (see Table VI).

Table VI. Power-Down Control

Bit 2	Power-Down Setting
0	Normal Operation
1	Power-Down Mode

Interpolator Mode

The AD1833A's DAC interpolators can be operated in one of three modes—8×, 4×, or 2×— then correspond to 48 kHz, 96 kHz, and 192 kHz modes, respectively (for IMCLK = 24.576 MHz). The interpolator mode may be selected by writing to Control Bits 1 and 0 in DAC Control Register 1 (see Table VII).

Table VII. Interpolator Mode Settings

Bit 1	Bit 0	Interpolator Mode
0	0	8x (48 kHz)*
0	1	2x (192 kHz)*
1	0	4x (96 kHz)*
1	1	Reserved

*For IMCLK = 24.576 MHz.

DAC CONTROL REGISTER 2

DAC Control Register 2 contains individual channel mute controls for each of the six DACs. Default operation (bit = 0) is muting off. Bits 9 through 6 of Control Register 2 are reserved and should be programmed to zero (see Table VIII).

DAC CONTROL REGISTER 3

Stereo Replicate

The AD1833A allows the stereo information on Channel 1 (SDIN1—Left 1 and Right 1) to be copied to Channels 2 and 3 (Left/Right 2 and Left/Right 3). These signals can be used in an external summing amplifier to increase potential signal SNR. Stereo replicate mode can be enabled by writing to control Bit 5 (see Table XI). Note that replication is not reflected in the zero flag status.

Table VIII. DAC Control Register 2

			Function						
Address	Reserved*		Reserved*	Mute Control					
15–12	11	10	9–6	5	4	3	2	1	0
0001	0	0	0	Channel 6 0 = Mute Off 1 = Mute On	Channel 5 0 = Mute Off 1 = Mute On	Channel 4 0 = Mute Off 1 = Mute On	Channel 3 0 = Mute Off 1 = Mute On	Channel 2 0 = Mute Off 1 = Mute On	Channel 1 0 = Mute Off 1 = Mute On

*Must be programmed to zero.

Table IX. Muting Control

Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Muting
X	X	X	X	X	1	Mute Channel 1
X	X	X	X	1	X	Mute Channel 2
X	X	X	1	X	X	Mute Channel 3
X	X	1	X	X	X	Mute Channel 4
X	1	X	X	X	X	Mute Channel 5
1	X	X	X	X	X	Mute Channel 6

Table X. DAC Control Register 3

				Function				
Address	Reserved*		Reserved*	Stereo Replicate (192 kHz)	MCLK Select	Zero Detect	Reserved*	TDM Mode
15–12	11	10	9–6	5	4–3	2	1	0
1000	0	0	0	0 = Normal 1 = Replicate	00 = IMCLK = MCLK × 2 01 = IMCLK = MCLK × 1 10 = IMCLK = MCLK × $^{2}/_{3}$	0 = Active High 1 = Active Low	0	0 = Master 1 = Slave

*Must be programmed to zero.

Table XI. Stereo Replicate

Bit 5	Stereo Mode
0	Normal
1	Channel 1 Data Replicated on Channels 2 and 3

MCLK Select

The AD1833A allows the matching of available external MCLK frequencies to the required internal MCLK rate. The MCLK modification factor can be selected from 2, 1, or $^2/_3$ by writing to Bit 4 and Bit 3 of Control Register 3. Internally, the AD1833A requires an MCLK of 24.576 MHz for sample rates of 48 kHz, 96 kHz, and 192 kHz. In the case of 48 kHz data with an MCLK of 256 × f_S, a clock doubler is used, whereas with an MCLK of 768 × f_S, a divide-by-3 block (÷3) is first implemented followed by a clock doubler. With an MCLK of 512 × f_S, the MCLK is passed through unmodified (see Table XII).

Table XII. MCLK Settings

Bit 4	Bit 3	Modification Factor
0	0	MCLK × 2 Internally
0	1	MCLK × 1 Internally
1	0	MCLK × $^2/_3$ Internally
1	1	Reserved

Channel Zero Status

The AD1833A provides individual logic output status indicators when zero data is sent to a channel for 1024 or more consecutive sample periods in all modes except right-justified. There is also a global zero flag that indicates all channels contain zero data. The polarity of the zero signal is programmable by writing to Control Bit 2 (see Table XIII). In right-justified mode, the six individual channel flags are best used as three stereo zero flags by combining pairs of them through suitable logic gates. Then, when both the left and right inputs are zero for 1024 clock cycles, i.e., a stereo zero input for 1024 sample periods, the combined result of the two individual flags will become active, indicating a stereo zero.

Table XIII. Zero Detect

Bit 2	Channel Zero Status
0	Active High
1	Active Low

DAC Volume Control Registers

The AD1833A has six volume control registers, one for each of the six DAC channels. Volume control is exercised by writing to the relevant register associated with each DAC. This setting is used to attenuate the DAC output. Full-scale setting (all 1s) is equivalent to zero attenuation (see Table XV).

Table XIV. MCLK vs. Sample Rate Selection

Sampling Rate f_S (kHz)	Interpolator Mode Required	Internal MCLK Required (MHz)	Suitable External MCLK Frequencies (MHz)		
			MCLK × 2	MCLK × 1	MCLK × $^2/_3$
32 64 128	8× 4× 2×	16.384	8192	16.384	24.576
44.1 88.2 176.4	8× 4× 2×	22.5792	11.2896	22.5792	33.8688
48 96 192	8× 4× 2×	24.576	12.288	24.576	36.864

Table XV. Volume Control Registers

Address	Reserved*		Volume Control
15–12	11	10	9–0
0 0 1 0	0	0	Channel 1 Volume Control (OUTL1)
0 0 1 1			Channel 2 Volume Control (OUTR1)
0 1 0 0			Channel 3 Volume Control (OUTL2)
0 1 0 1			Channel 4 Volume Control (OUTR2)
0 1 1 0			Channel 5 Volume Control (OUTL3)
0 1 1 1			Channel 6 Volume Control (OUTR3)

*Must be programmed to zero.

I²S Timing

I²S timing uses an $\overline{L}$/RCLK to define when the data being transmitted is for the left channel and when it is for the right channel. The $\overline{L}$/RCLK is low for the left channel and high for the right channel. A bit clock running at 64 × f_S is used to clock in the data. There is a delay of 1 bit clock from the time the $\overline{L}$/RCLK signal changes state to the first bit of data on the SDINx lines. The data is written MSB first and is valid on the rising edge of the bit clock.

Left-Justified Timing

Left-justified (LJ) timing uses an L/$\overline{R}$CLK to define when the data being transmitted is for the left channel and when it is for the right channel. The L/$\overline{R}$CLK is high for the left channel and low for the right channel. A bit clock running at 64 × f_S is used to clock in the data. The first bit of data appears on the SDINx lines when the L/$\overline{R}$CLK toggles. The data is written MSB first and is valid on the rising edge of the bit clock.

Right-Justified Timing

Right-justified (RJ) timing uses an L/$\overline{R}$CLK to define when the data being transmitted is for the left channel and when it is for the right channel. The L/$\overline{R}$CLK is high for the left channel and low for the right channel. A bit clock running at 64 × f_S is used to clock in the data. The first bit of data appears on the SDINx 8-bit clock periods (for 24-bit data) after L/$\overline{R}$CLK toggles. In RJ mode, the LSB of data is always clocked by the last bit clock before L/$\overline{R}$CLK transitions. The data is written MSB first and is valid on the rising edge of the bit clock.

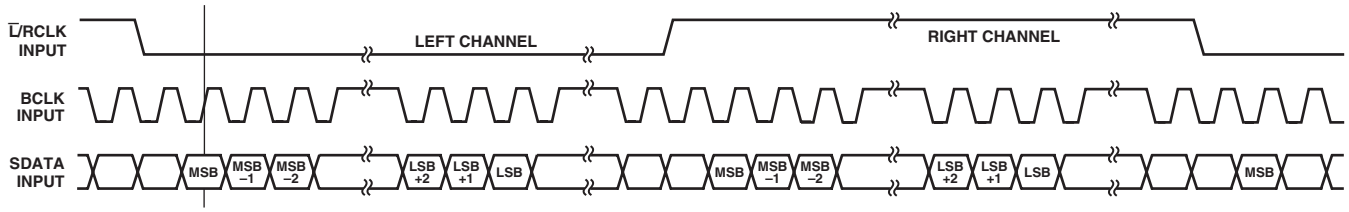


Figure 6. I²S Timing Diagram

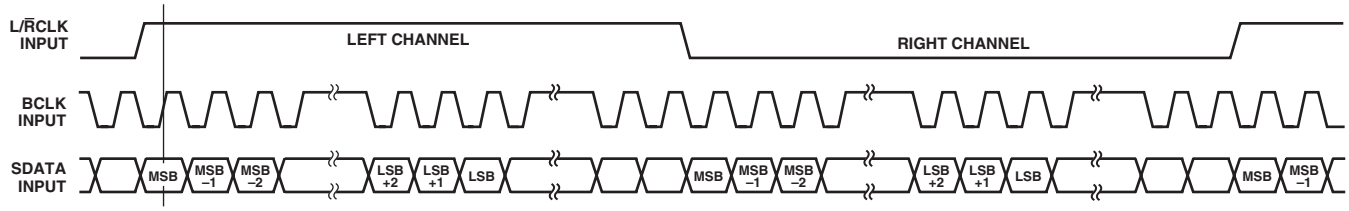


Figure 7. Left-Justified Timing Diagram

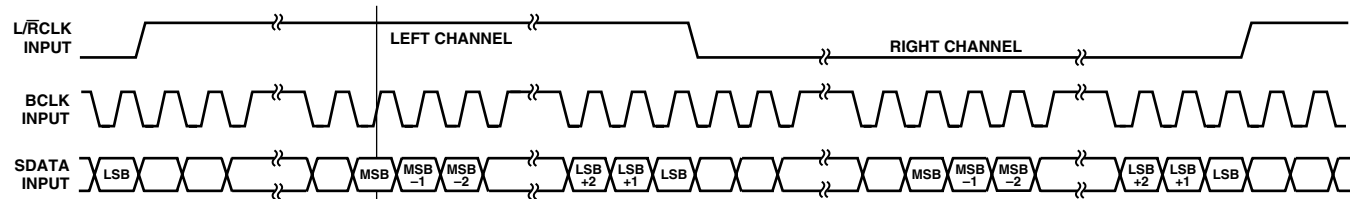


Figure 8. Right-Justified Timing Diagram

TDM Mode Timing—Interfacing to a SHARC®

In TDM mode, the AD1833A can be the master or slave, depending on Bit 0 in Control Register 3. In master mode, it generates a frame sync signal (FSTDM) on its L/RCLK pin and a bit clock (BCLKTDM) on its BCLK pin, whereas in slave mode it expects these signals to be provided. These signals are used to control the data transmission from the SHARC. The bit clock must run at a frequency of IMCLK/2 and the interpolation mode must be set to 8×, which limits TDM mode to frequencies of 48 kHz or less. In this mode, all data is written on the rising edge of the bit clock and read on the falling edge of the bit clock. The frame starts with a frame sync at the rising edge of the bit clock. The SHARC then starts outputting data on the next rising edge of the bit clock. Each channel is given a 32-bit clock slot, and the data is left-justified and uses 16, 20, or 24 of the 32 bits. An enlarged diagram detailing this is provided (see Figure 9). The data is sent from the SHARC to the AD1833A on the SDIN1 pin and provided in the following order: MSB first—Internal DACL0, Internal DACL1, Internal DACL2, AUX DACL0, Internal DACR0, Internal DACR1, Internal DACR2, and AUX DACR0. The data is written on the rising edge of the bit clock and read by the AD1833A on the falling edge of the bit clock. The left and right data destined for the auxiliary DAC is sent in standard I^2S format in the next frame using the SDIN2, SDIN3, and SOUT pins as the L/RCLK, BCLK, and SDATA pins, respectively, for communicating with the auxiliary DAC.

DSP Mode Timing

DSP mode timing uses the rising edge of the frame sync signal on the L/RCLK pin to denote the start of the transmission of a data-word. Note that for both left and right channels, a rising edge is used; therefore in this mode, there is no way to determine which data is intended for the left channel and which is intended for the right. The DSP writes data on the rising edge of BCLK and the AD1833A reads it on the falling edge. The DSP raises the frame sync signal on the rising edge of BCLK and then proceeds to transmit data, MSB first, on the next rising edge of BCLK. The data length can be 16, 20, or 24 bits. The frame sync signal can be brought low any time at or after the MSB is transmitted, but must be brought low at least one BCLK period before the start of the next channel transmission.

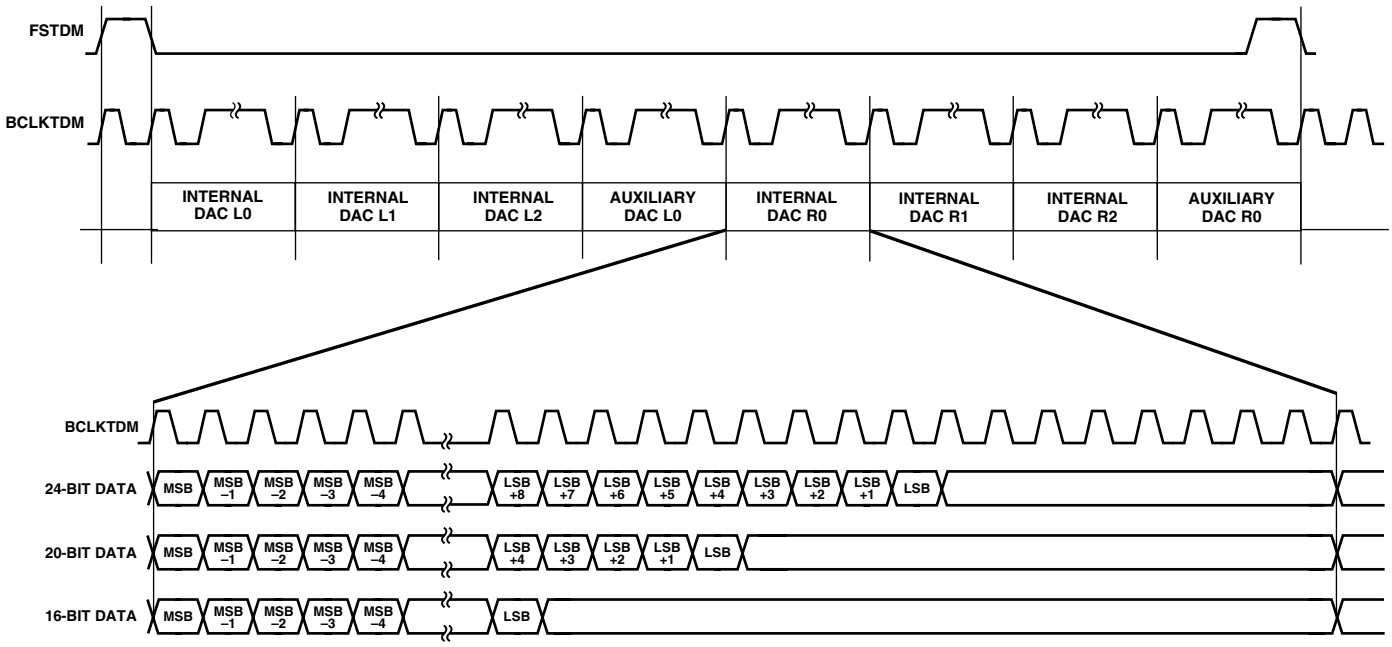


Figure 9. TDM Mode Timing

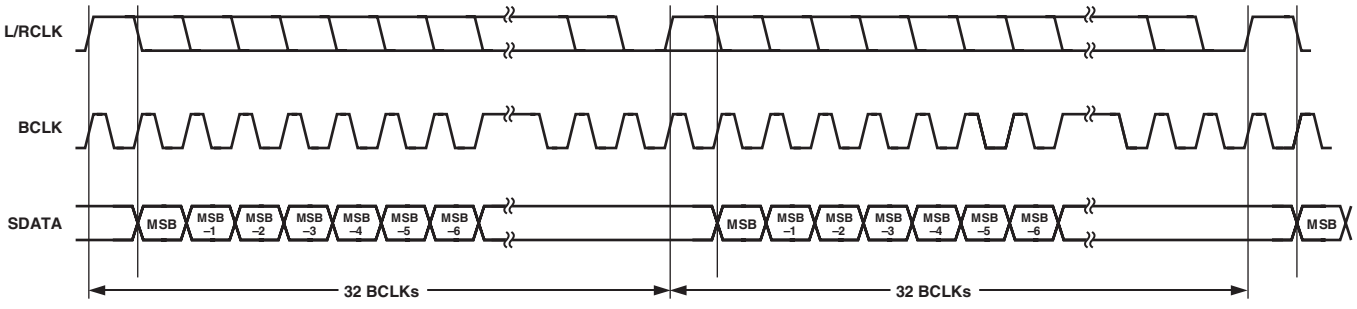


Figure 10. DSP Mode Timing

Packed Mode 128

In Packed Mode 128, all six data channels are packed into one sample interval on one data pin. The BCLK runs at 128 × f_S; therefore, there are 128 BCLK periods in each sample interval. Each sample interval is broken into eight time slots: six slots of 20 BCLK and two of 4 BCLK. In this mode, the data length is restricted to a maximum of 20 bits. The three left channels are written first, MSB first, and the data is written on the falling edge of BCLK. After the three left channels are written, there is a space of four BCLK, and then the three right channels are written. The L/$\overline{R}$CLK defines the left and right data transmission; it is high for the three left channels and low for the three right channels.

Packed Mode 256

In Packed Mode 256, all six data channels are packed into one sample interval on one data pin. The BCLK runs at 256 × f_S; therefore, there are 256 BCLK periods in each sample interval, and each sample interval is broken into eight time slots of 32 BCLK each. The data length can be 16, 20, or 24 bits. The three left channels are written first, MSB first, and the data is written on the falling edge of BCLK with a one BCLK period delay from the start of the slot. After the three left channels are written, there is a space of 32 BCLK, and then the three right channels are written. The $\overline{L}$/RCLK defines the left and right data transmission; it is low for the three left channels and high for the three right channels.

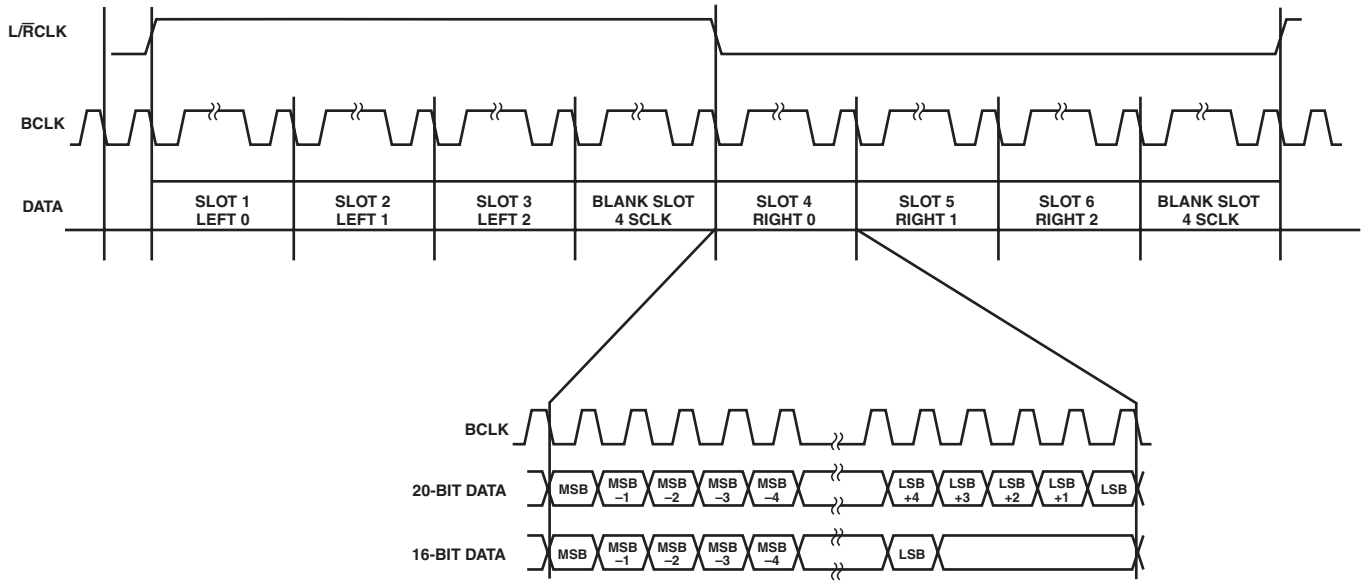


Figure 11. Packed Mode 128

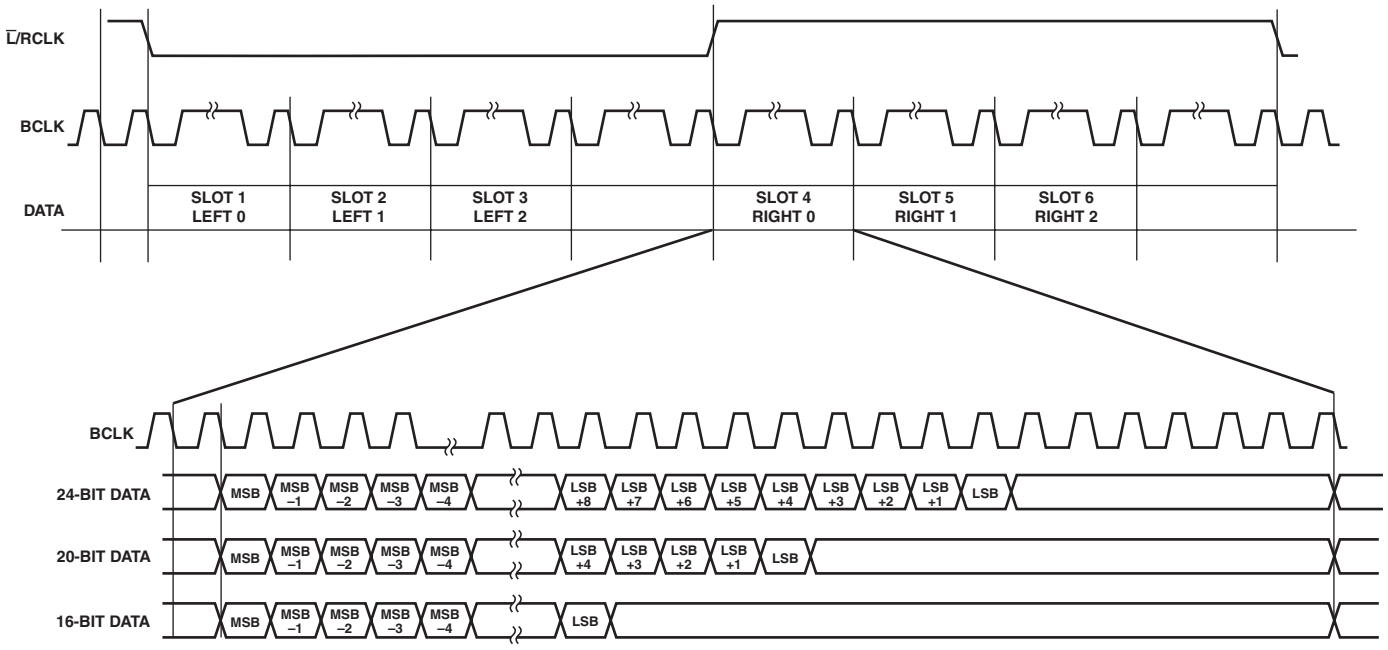


Figure 12. Packed Mode 256

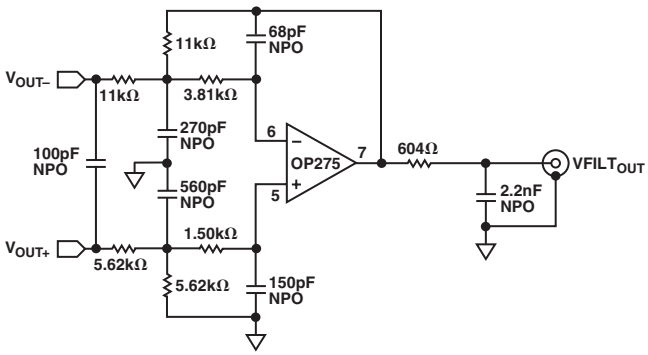


Figure 13. Suggested Output Filter Schematic

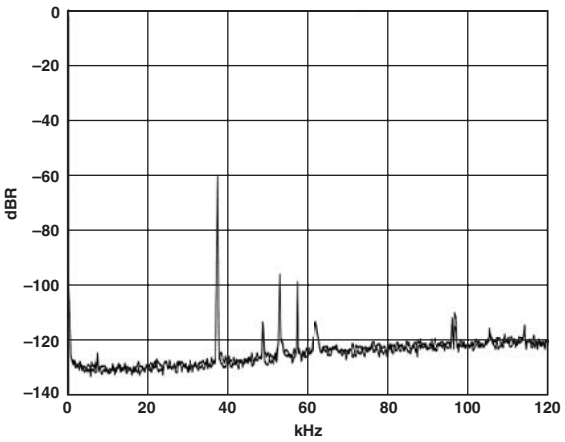


Figure 16. Dynamic Range for 37 kHz @ –60 dBFS, 110 dB, Triangular Dithered Input

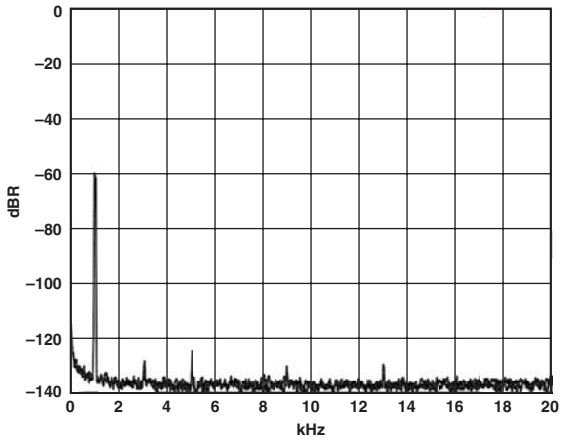


Figure 14. Dynamic Range for 1 kHz @ –60 dBFS, 110 dB, Triangular Dithered Input

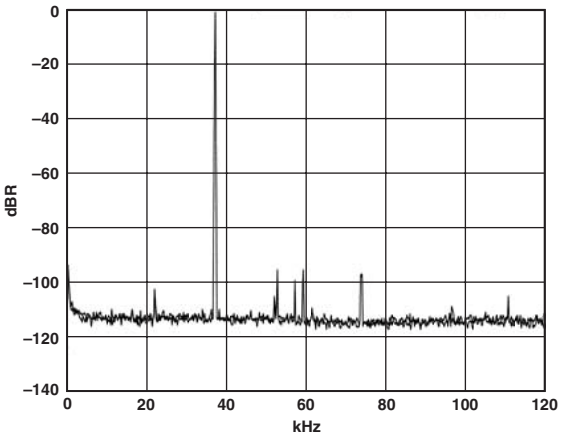


Figure 17. Input 0 dBFS @ 37 kHz, BW 20 Hz to 120 kHz, SR 96 kHz, THD + N –95 dBFS

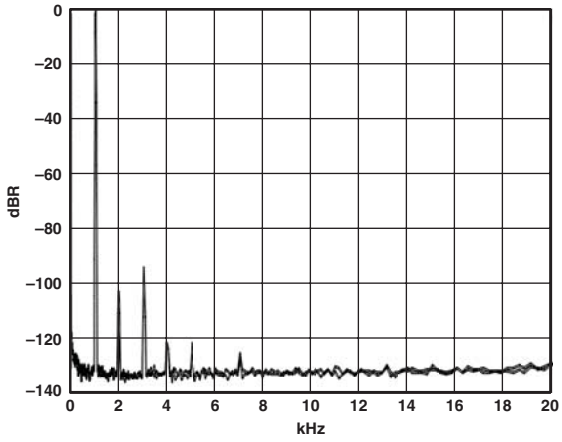


Figure 15. Input 0 dBFS @ 1 kHz, BW 20 Hz to 20 kHz, SR 48 kHz, THD + N –95 dBFS

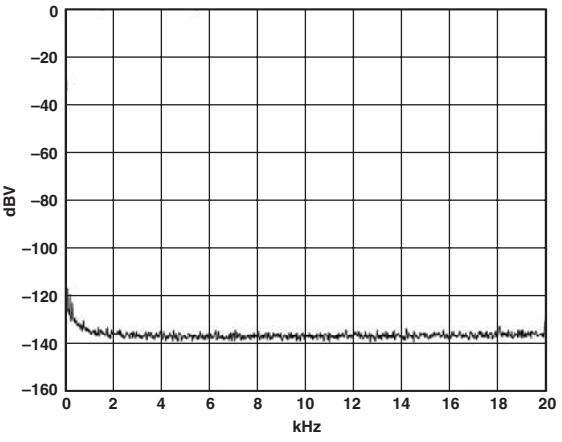


Figure 18. Noise Floor for Zero Input, SR 48 kHz, SNR 110 dBFS A-Weighted

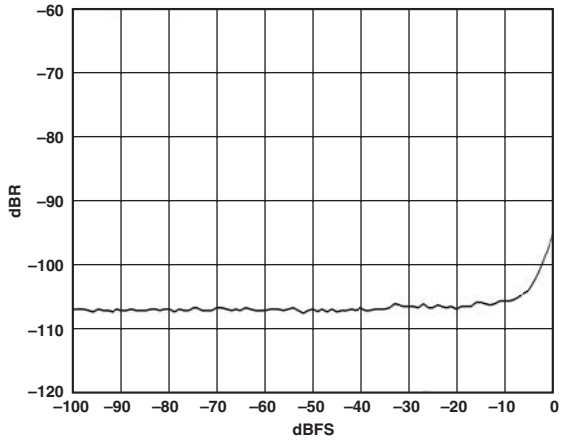


Figure 19. THD + N Amplitude vs. Input Amplitude, Input 1 kHz, SR 48 kHz, 24-Bit

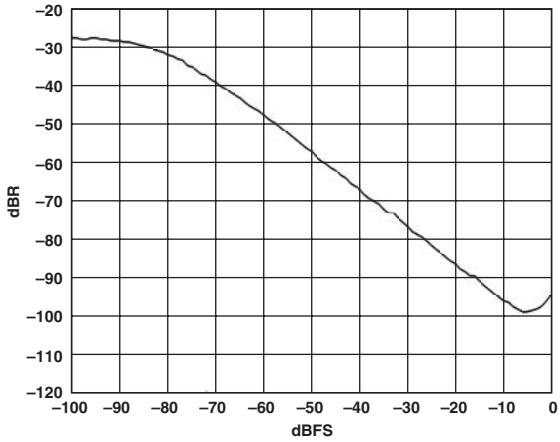


Figure 20. THD + N Ratio vs. Input Amplitude, Input 1 kHz, SR 48 kHz, 24-Bit

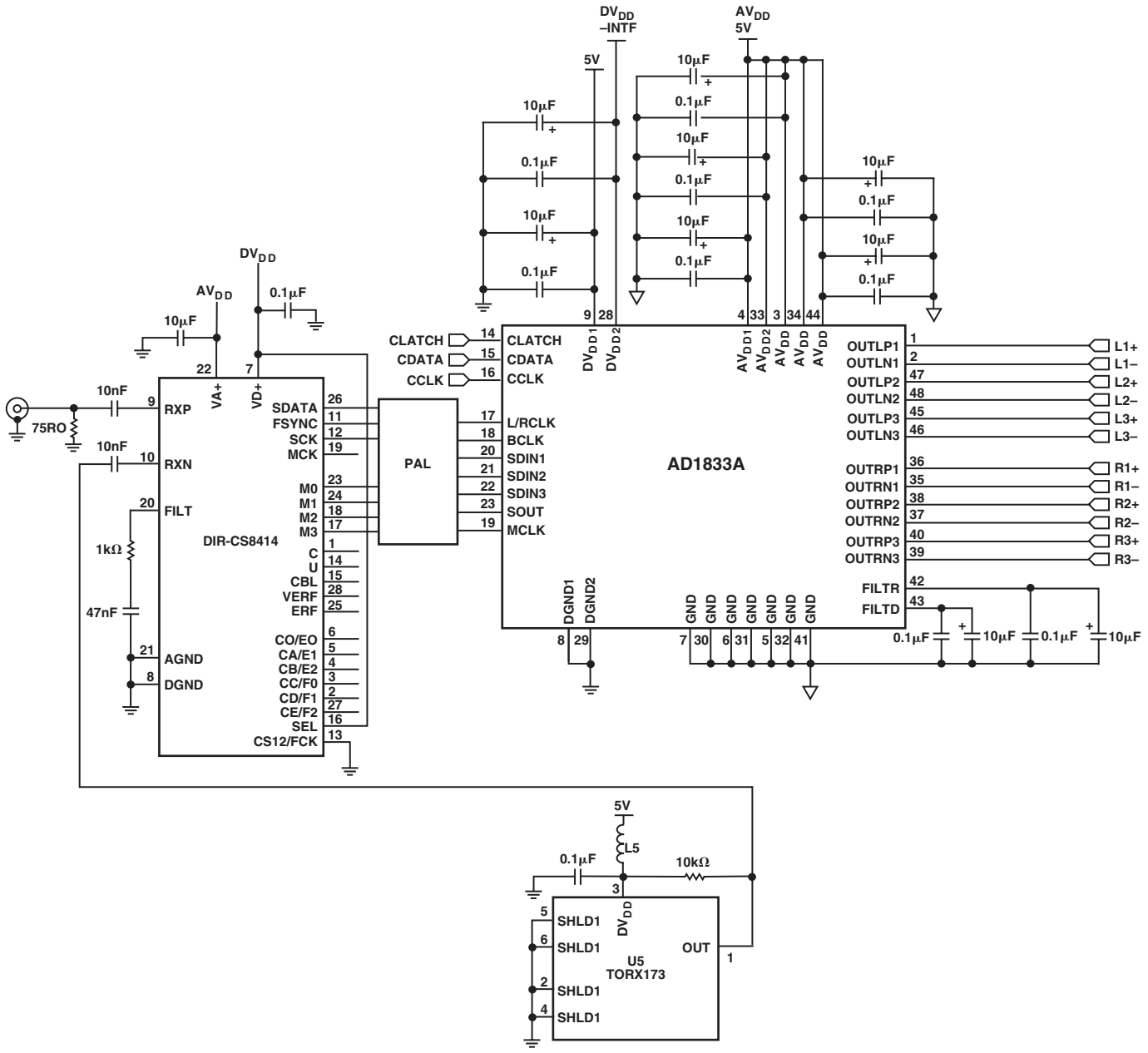
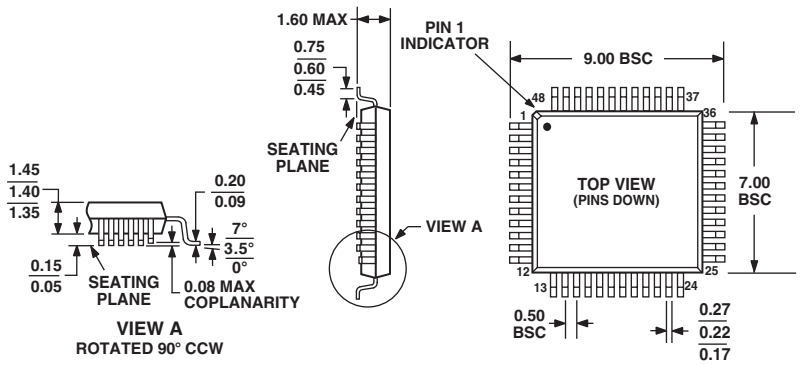


Figure 21. Example Digital Interface

OUTLINE DIMENSIONS

48-Lead Low Profile Quad Flat Package [LQFP]
1.4 mm Thick
(ST-48)

Dimensions shown in millimeters



COMPLIANT TO JEDEC STANDARDS MS-026BBC

C02336–0–5/03(0)

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С уважением,

Менеджер отдела продаж ООО

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