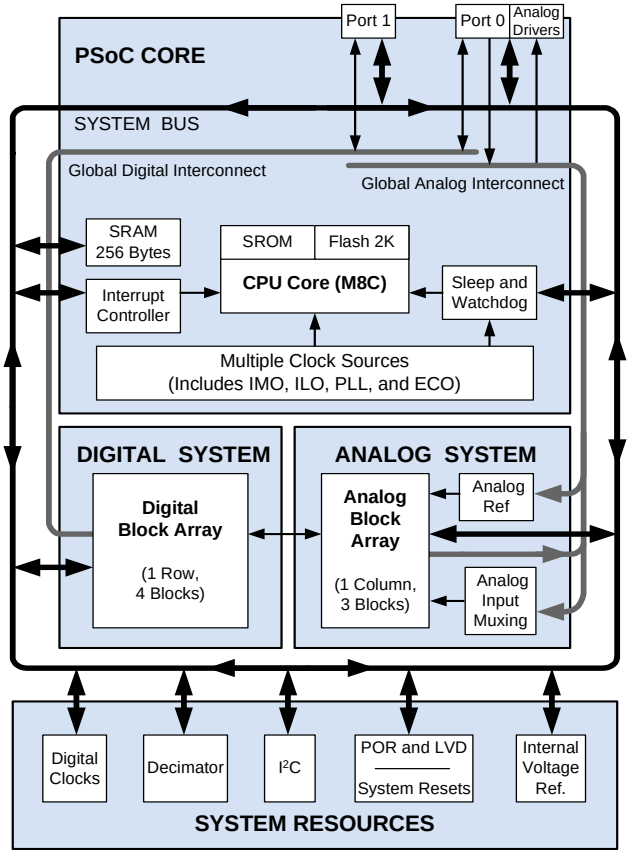
# PSoC™ Mixed Signal Array — Final Data Sheet

## CY8C22113 and CY8C22213

## Features

- **Powerful Harvard Architecture Processor**
  - M8C Processor Speeds to 24 MHz
  - Low Power at High Speed
  - 3.0 to 5.25 V Operating Voltage
  - Industrial Temperature Range: -40°C to +85°C
- **Advanced Peripherals (PSoC Blocks)**
  - 3 Rail-to-Rail Analog PSoC Blocks Provide:
    - Up to 14-Bit ADCs
    - Up to 9-Bit DACs
    - Programmable Gain Amplifiers
    - Programmable Filters and Comparators
  - 4 Digital PSoC Blocks Provide:
    - 8- to 32-Bit Timers, Counters, and PWMs
    - CRC and PRS Modules
    - Full-Duplex UART
    - SPI™ Masters or Slaves
    - Connectable to all GPIO Pins
  - Complex Peripherals by Combining Blocks
- **Precision, Programmable Clocking**
  - Internal ±2.5% 24/48 MHz Oscillator
  - High-Accuracy 24 MHz with Optional 32.768 kHz Crystal and PLL
  - Optional External Oscillator, up to 24 MHz
  - Internal Oscillator for Watchdog and Sleep
- **Flexible On-Chip Memory**
  - 2K Bytes Flash Program Storage 50,000 Erase/Write Cycles
  - 256 Bytes SRAM Data Storage
  - In-System Serial Programming (ISSP™)
  - Partial Flash Updates
  - Flexible Protection Modes
  - EEPROM Emulation in Flash
- **Programmable Pin Configurations**
  - 25 mA Sink on all GPIO
  - Pull up, Pull down, High Z, Strong, or Open Drain Drive Modes on all GPIO
  - Up to 8 Analog Inputs on GPIO
  - One 30 mA Analog Outputs on GPIO
  - Configurable Interrupt on all GPIO
- **Additional System Resources**
  - I²C™ Slave, Master, and Multi-Master to 400 kHz
  - Watchdog and Sleep Timers
  - User-Configurable Low Voltage Detection
  - Integrated Supervisory Circuit
  - On-Chip Precision Voltage Reference
- **Complete Development Tools**
  - Free Development Software (PSoC™ Designer)
  - Full-Featured, In-Circuit Emulator and Programmer
  - Full Speed Emulation
  - Complex Breakpoint Structure
  - 128K Bytes Trace Memory




## PSoC™ Functional Overview

The PSoC™ family consists of many *Mixed Signal Array with On-Chip Controller* devices. These devices are designed to replace multiple traditional MCU-based system components with one, low cost single-chip programmable device. PSoC devices include configurable blocks of analog and digital logic, as well as programmable interconnects. This architecture allows the user to create customized peripheral configurations that match the requirements of each individual application. Additionally, a fast CPU, Flash program memory, SRAM data memory, and configurable IO are included in a range of convenient pinouts and packages.

The PSoC architecture, as illustrated on the left, is comprised of four main areas: PSoC Core, Digital System, Analog System, and System Resources. Configurable global busing allows all the device resources to be combined into a complete custom system. The PSoC CY8C22x13 family can have up to two IO ports that connect to the global digital and analog interconnects, providing access to 4 digital blocks and 3 analog blocks.

### The PSoC Core

The PSoC Core is a powerful engine that supports a rich feature set. The core includes a CPU, memory, clocks, and configurable GPIO (General Purpose IO).

The M8C CPU core is a powerful processor with speeds up to 24 MHz, providing a four MIPS 8-bit Harvard architecture micro-

processor. The CPU utilizes an interrupt controller with 10 vectors, to simplify programming of real time embedded events. Program execution is timed and protected using the included Sleep and Watch Dog Timers (WDT).

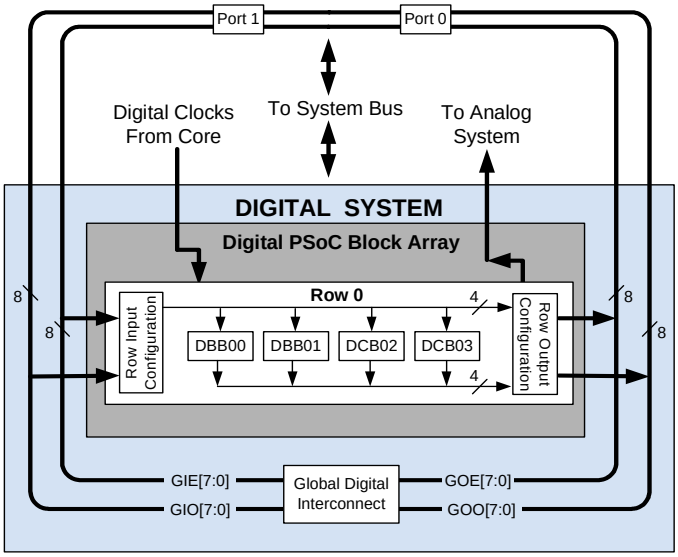
Memory encompasses 2 KB of Flash for program storage, 256 bytes of SRAM for data storage, and up to 2 KB of EEPROM emulated using the Flash. Program Flash utilizes four protection levels on blocks of 64 bytes, allowing customized software IP protection.

The PSoC device incorporates flexible internal clock generators, including a 24 MHz IMO (internal main oscillator) accurate to 2.5% over temperature and voltage. The 24 MHz IMO can also be doubled to 48 MHz for use by the digital system. A low power 32 kHz ILO (internal low speed oscillator) is provided for the Sleep timer and WDT. If crystal accuracy is desired, the ECO (32.768 kHz external crystal oscillator) is available for use as a Real Time Clock (RTC) and can optionally generate a crystal-accurate 24 MHz system clock using a PLL. The clocks, together with programmable clock dividers (as a System Resource), provide the flexibility to integrate almost any timing requirement into the PSoC device.

PSoC GPIOs provide connection to the CPU, digital and analog resources of the device. Each pin's drive mode may be selected from eight options, allowing great flexibility in external interfacing. Every pin also has the capability to generate a system interrupt on high level, low level, and change from last read.

## The Digital System

The Digital System is composed of 4 digital PSoC blocks. Each block is an 8-bit resource that can be used alone or combined with other blocks to form 8, 16, 24, and 32-bit peripherals, which are called user module references.




**Digital System Block Diagram**

Digital peripheral configurations include those listed below.

- PWMs (8 to 32 bit)
- PWMs with Dead band (8 to 32 bit)
- Counters (8 to 32 bit)
- Timers (8 to 32 bit)
- UART 8-bit with selectable parity (up to 1)
- SPI master and slave (up to 1)
- I2C slave and master (1 available as a System Resource)
- Cyclical Redundancy Checker/Generator (8 to 32 bit)
- IrDA (up to 1)
- Pseudo Random Sequence Generators (8 to 32 bit)

The digital blocks can be connected to any GPIO through a series of global buses that can route any signal to any pin. The buses also allow for signal multiplexing and for performing logic operations. This configurability frees your designs from the constraints of a fixed peripheral controller.

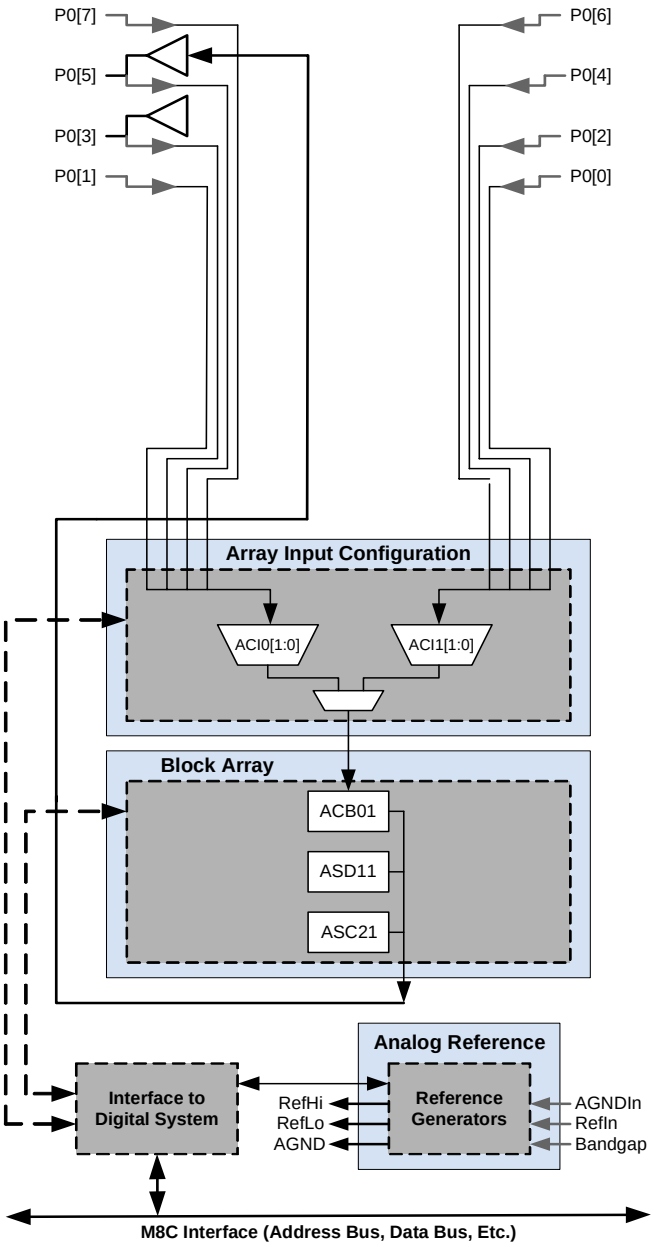
Digital blocks are provided in rows of four, where the number of blocks varies by PSoC device family. This allows you the optimum choice of system resources for your application. Family resources are shown in the table titled "PSoC Device Characteristics" on page 3.

## The Analog System

The Analog System is composed of 3 configurable blocks, each comprised of an opamp circuit allowing the creation of complex analog signal flows. Analog peripherals are very flexible and can be customized to support specific application requirements. Some of the more common PSoC analog functions (most available as user modules) are listed below.

- Analog-to-digital converters (one with 6- to 14-bit resolution, selectable as Incremental, Delta Sigma, and SAR)
- Filters (two pole band-pass, low-pass, and notch)
- Amplifiers (one with selectable gain to 48x)
- Comparators (one with 16 selectable thresholds)
- DACs (one with 6- to 9-bit resolution)
- Multiplying DACs (one with 6- to 9-bit resolution)
- High current output drivers (one with 30 mA drive as a Core Resource)
- 1.3V reference (as a System Resource)
- Many other topologies possible

Analog blocks are provided in columns of three, which includes one CT (Continuous Time) and two SC (Switched Capacitor) blocks. The number of blocks is dependant on the device family which is detailed in the table titled "PSoC Device Characteristics" on page 3.




**Analog System Block Diagram**

## Additional System Resources

System Resources, some of which have been previously listed, provide additional capability useful to complete systems. Additional resources include a decimator, low voltage detection, and power on reset. Brief statements describing the merits of each system resource are presented below.

- Digital clock dividers provide three customizable clock frequencies for use in applications. The clocks can be routed to both the digital and analog systems. Additional clocks can be generated using digital PSoC blocks as clock dividers.
- The decimator provides a custom hardware filter for digital signal processing applications including the creation of Delta Sigma ADCs.
- The I2C module provides 100 and 400 kHz communication over two wires. Slave, master, and multi-master modes are all supported.
- Low Voltage Detection (LVD) interrupts can signal the application of falling voltage levels, while the advanced POR (Power On Reset) circuit eliminates the need for a system supervisor.
- An internal 1.3 voltage reference provides an absolute reference for the analog system, including ADCs and DACs.

## PSoC Device Characteristics

Depending on your PSoC device characteristics, the digital and analog systems can have 16, 8, or 4 digital blocks and 12, 6, or 3 analog blocks. The following table lists the resources available for specific PSoC device groups.

**PSoC Device Characteristics**

| PSoC Part Number | Digital IO | Digital Rows | Digital Blocks | Analog Inputs | Analog Outputs | Analog Columns | Analog Blocks |
|---|---|---|---|---|---|---|---|
| CY8C29x66 | up to 64 | 4 | 16 | 12 | 4 | 4 | 12 |
| CY8C27x66 | up to 44 | 2 | 8 | 12 | 4 | 4 | 12 |
| CY8C27x43 | up to 44 | 2 | 8 | 12 | 4 | 4 | 12 |
| CY8C24x23 | up to 24 | 1 | 4 | 12 | 2 | 2 | 6 |
| **CY8C22x13** | **up to 16** | **1** | **4** | **8** | **1** | **1** | **3** |

# Getting Started

The quickest path to understanding the PSoC silicon is by reading this data sheet and using the PSoC Designer Integrated Development Environment (IDE). This data sheet is an overview of the PSoC integrated circuit and presents specific pin, register, and electrical specifications. For in-depth information, along with detailed programming information, reference the *PSoC™ Mixed Signal Array Technical Reference Manual*.

For up-to-date Ordering, Packaging, and Electrical Specification information, reference the latest PSoC device data sheets on the web at http://www.cypress.com/psoc.

## Development Kits

Development Kits are available from the following distributors: Digi-Key, Avnet, Arrow, and Future. The Cypress Online Store at http://www.onfulfillment.com/cypressstore/ contains development kits, C compilers, and all accessories for PSoC development. Click on *PSoC (Programmable System-on-Chip)* to view a current list of available items.

## Tele-Training

Free PSoC "Tele-training" is available for beginners and taught by a live marketing or application engineer over the phone. Five training classes are available to accelerate the learning curve including introduction, designing, debugging, advanced design, advanced analog, as well as application-specific classes covering topics like PSoC and the LIN bus. For days and times of the tele-training, see http://www.cypress.com/support/training.cfm.

## Consultants

Certified PSoC Consultants offer everything from technical assistance to completed PSoC designs. To contact or become a PSoC Consultant, go to the following Cypress support web site: http://www.cypress.com/support/cypros.cfm.

## Technical Support

PSoC application engineers take pride in fast and accurate response. They can be reached with a 4-hour guaranteed response at http://www.cypress.com/support/login.cfm.

## Application Notes

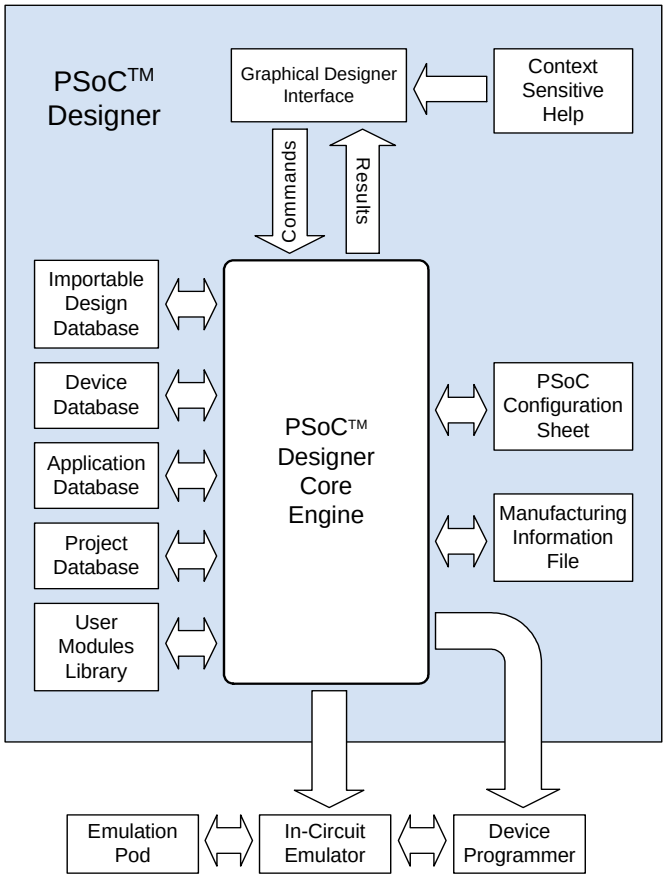
A long list of application notes will assist you in every aspect of your design effort. To locate the PSoC application notes, go to http://www.cypress.com/design/results.cfm.

# Development Tools

The Cypress MicroSystems PSoC Designer is a Microsoft® Windows-based, integrated development environment for the Programmable System-on-Chip (PSoC) devices. The PSoC Designer IDE and application runs on Windows 98, Windows NT 4.0, Windows 2000, Windows Millennium (Me), or Windows XP. (Reference the PSoC Designer Functional Flow diagram below.)

PSoC Designer helps the customer to select an operating configuration for the PSoC, write application code that uses the PSoC, and debug the application. This system provides design database management by project, an integrated debugger with In-Circuit Emulator, in-system programming support, and the CYASM macro assembler for the CPUs.

PSoC Designer also supports a high-level C language compiler developed specifically for the devices in the family.




**PSoC Designer Subsystems**

## PSoC Designer Software Subsystems

### *Device Editor*

The Device Editor subsystem allows the user to select different onboard analog and digital components called user modules using the PSoC blocks. Examples of user modules are ADCs, DACs, Amplifiers, and Filters.

The device editor also supports easy development of multiple configurations and dynamic reconfiguration. Dynamic configuration allows for changing configurations at run time.

PSoC Designer sets up power-on initialization tables for selected PSoC block configurations and creates source code for an application framework. The framework contains software to operate the selected components and, if the project uses more than one operating configuration, contains routines to switch between different sets of PSoC block configurations at run time. PSoC Designer can print out a configuration sheet for a given project configuration for use during application programming in conjunction with the Device Data Sheet. Once the framework is generated, the user can add application-specific code to flesh out the framework. It's also possible to change the selected components and regenerate the framework.

### *Design Browser*

The Design Browser allows users to select and import preconfigured designs into the user's project. Users can easily browse a catalog of preconfigured designs to facilitate time-to-design. Examples provided in the tools include a 300-baud modem, LIN Bus master and slave, fan controller, and magnetic card reader.

### *Application Editor*

In the Application Editor you can edit your C language and Assembly language source code. You can also assemble, compile, link, and build.

**Assembler.** The macro assembler allows the assembly code to be merged seamlessly with C code. The link libraries automatically use absolute addressing or can be compiled in relative mode, and linked with other software modules to get absolute addressing.

**C Language Compiler.** A C language compiler is available that supports Cypress MicroSystems' PSoC family devices. Even if you have never worked in the C language before, the product quickly allows you to create complete C programs for the PSoC family devices.

The embedded, optimizing C compiler provides all the features of C tailored to the PSoC architecture. It comes complete with embedded libraries providing port and bus operations, standard keypad and display support, and extended math functionality.

### *Debugger*

The PSoC Designer Debugger subsystem provides hardware in-circuit emulation, allowing the designer to test the program in a physical system while providing an internal view of the PSoC device. Debugger commands allow the designer to read and program and read and write data memory, read and write IO registers, read and write CPU registers, set and clear breakpoints, and provide program run, halt, and step control. The debugger also allows the designer to create a trace buffer of registers and memory locations of interest.

### *Online Help System*

The online help system displays online, context-sensitive help for the user. Designed for procedural and quick reference, each functional subsystem has its own context-sensitive help. This system also provides tutorials and links to FAQs and an Online Support Forum to aid the designer in getting started.

## Hardware Tools

### *In-Circuit Emulator*

A low cost, high functionality ICE (In-Circuit Emulator) is available for development support. This hardware has the capability to program single devices.

The emulator consists of a base unit that connects to the PC by way of the parallel or USB port. The base unit is universal and will operate with all PSoC devices. Emulation pods for each device family are available separately. The emulation pod takes the place of the PSoC device in the target board and performs full speed (24 MHz) operation.


**PSoC Development Tool Kit**

# User Modules and the PSoC Development Process

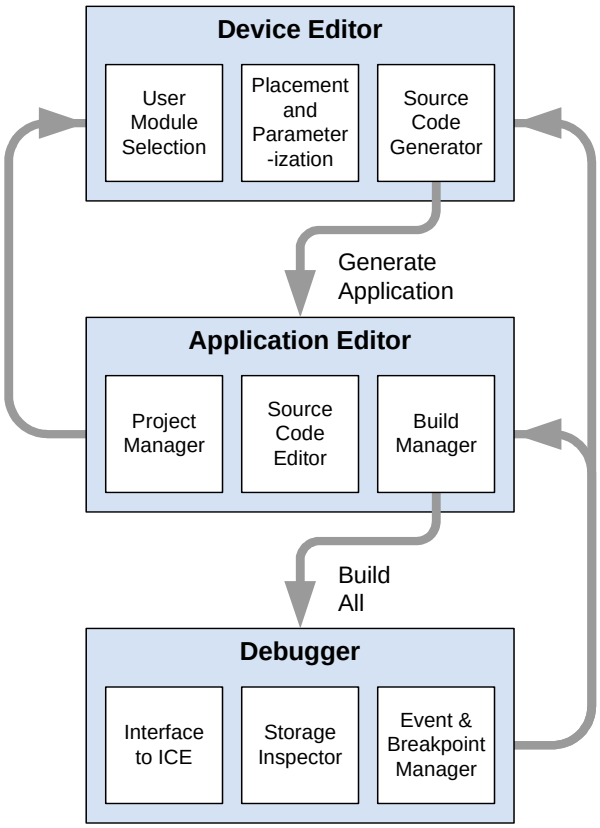
The development process for the PSoC device differs from that of a traditional fixed function microprocessor. The configurable analog and digital hardware blocks give the PSoC architecture a unique flexibility that pays dividends in managing specification change during development and by lowering inventory costs. These configurable resources, called PSoC Blocks, have the ability to implement a wide variety of user-selectable functions. Each block has several registers that determine its function and connectivity to other blocks, multiplexers, buses, and to the IO pins. Iterative development cycles permit you to adapt the hardware as well as the software. This substantially lowers the risk of having to select a different part to meet the final design requirements.

To speed the development process, the PSoC Designer Integrated Development Environment (IDE) provides a library of pre-built, pre-tested hardware peripheral functions, called “User Modules.” User modules make selecting and implementing peripheral devices simple, and come in analog, digital, and mixed signal varieties. The standard User Module library contains over 50 common peripherals such as ADCs, DACs Timers, Counters, UARTs, and other not-so common peripherals such as DTMF Generators and Bi-Quad analog filter sections.

Each user module establishes the basic register settings that implement the selected function. It also provides parameters that allow you to tailor its precise configuration to your particular application. For example, a Pulse Width Modulator User Module configures one or more digital PSoC blocks, one for each 8 bits of resolution. The user module parameters permit you to establish the pulse width and duty cycle. User modules also provide tested software to cut your development time. The user module application programming interface (API) provides high-level functions to control and respond to hardware events at run-time. The API also provides optional interrupt service routines that you can adapt as needed.

The API functions are documented in user module data sheets that are viewed directly in the PSoC Designer IDE. These data sheets explain the internal operation of the user module and provide performance specifications. Each data sheet describes the use of each user module parameter and documents the setting of each register controlled by the user module.

The development process starts when you open a new project and bring up the Device Editor, a pictorial environment (GUI) for configuring the hardware. You pick the user modules you need for your project and map them onto the PSoC blocks with point-and-click simplicity. Next, you build signal chains by interconnecting user modules to each other and the IO pins. At this stage, you also configure the clock source connections and enter parameter values directly or by selecting values from drop-down menus. When you are ready to test the hardware configuration or move on to developing code for the project, you perform the “Generate Application” step. This causes PSoC Designer to generate source code that automatically configures the device to your specification and provides the high-level user module API functions.




**User Modules and Development Process Flow Chart**

The next step is to write your main program, and any sub-routines using PSoC Designer’s Application Editor subsystem. The Application Editor includes a Project Manager that allows you to open the project source code files (including all generated code files) from a hierarchal view. The source code editor provides syntax coloring and advanced edit features for both C and assembly language. File search capabilities include simple string searches and recursive “grep-style” patterns. A single mouse click invokes the Build Manager. It employs a professional-strength “makefile” system to automatically analyze all file dependencies and run the compiler and assembler as necessary. Project-level options control optimization strategies used by the compiler and linker. Syntax errors are displayed in a console window. Double clicking the error message takes you directly to the offending line of source code. When all is correct, the linker builds a ROM file image suitable for programming.

The last step in the development process takes place inside the PSoC Designer’s Debugger subsystem. The Debugger downloads the ROM image to the In-Circuit Emulator (ICE) where it runs at full speed. Debugger capabilities rival those of systems costing many times more. In addition to traditional single-step, run-to-breakpoint and watch-variable features, the Debugger provides a large trace buffer and allows you define complex breakpoint events that include monitoring address and data bus values, memory locations and external signals.

# Document Conventions

## Acronyms Used

The following table lists the acronyms that are used in this document.

| Acronym | Description |
|---|---|
| AC | alternating current |
| ADC | analog-to-digital converter |
| API | application programming interface |
| CPU | central processing unit |
| CT | continuous time |
| DAC | digital-to-analog converter |
| DC | direct current |
| EEPROM | electrically erasable programmable read-only memory |
| FSR | full scale range |
| GPIO | general purpose IO |
| IO | input/output |
| IPOR | imprecise power on reset |
| LSb | least-significant bit |
| LVD | low voltage detect |
| MSb | most-significant bit |
| PC | program counter |
| POR | power on reset |
| PPOR | precision power on reset |
| PSoC™ | Programmable System-on-Chip |
| PWM | pulse width modulator |
| RAM | random access memory |
| ROM | read only memory |
| SC | switched capacitor |
| SMP | switch mode pump |

## Units of Measure

A units of measure table is located in the Electrical Specifications section. Table 3-1 on page 13 lists all the abbreviations used to measure the PSoC devices.

## Numeric Naming

Hexidecimal numbers are represented with all letters in uppercase with an appended lowercase ‘h’ (for example, ‘14h’ or ‘3Ah’). Hexidecimal numbers may also be represented by a ‘0x’ prefix, the C coding convention. Binary numbers have an appended lowercase ‘b’ (e.g., 01010100b’ or ‘01000011b’). Numbers not indicated by an ‘h’ or ‘b’ are decimal.

# Table of Contents

For an in depth discussion and more information on your PSoC device, obtain the *PSoC Mixed Signal Array Technical Reference Manual*. This document encompasses and is organized into the following chapters and sections.

# 1. Pin Information

This chapter describes, lists, and illustrates the CY8C22x13 PSoC device pins and pinout configurations.

## 1.1 Pinouts

The CY8C22x13 PSoC device is available in a variety of packages which are listed and illustrated in the following tables. Every port pin (labeled with a “P”) is capable of Digital IO. However, Vss, Vdd, SMP, and XRES are not capable of Digital IO.

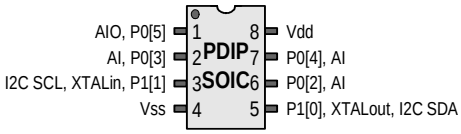
### 1.1.1 8-Pin Part Pinout

**Table 1-1. 8-Pin Part Pinout (PDIP, SOIC)**

| Pin No. | Type | | Pin Name | Description |
|---|---|---|---|---|
| | Digital | Analog | | |
| 1 | IO | IO | P0[5] | Analog column mux input and column output. |
| 2 | IO | I | P0[3] | Analog column mux input. |
| 3 | IO | | P1[1] | Crystal Input (XTALin), I2C Serial Clock (SCL) |
| 4 | Power | | Vss | Ground connection. |
| 5 | IO | | P1[0] | Crystal Output (XTALout), I2C Serial Data (SDA) |
| 6 | IO | I | P0[2] | Analog column mux input. |
| 7 | IO | I | P0[4] | Analog column mux input. |
| 8 | Power | | Vdd | Supply voltage. |

**LEGEND**: A = Analog, I = Input, and O = Output.

**CY8C22113 8-Pin PSoC Device**



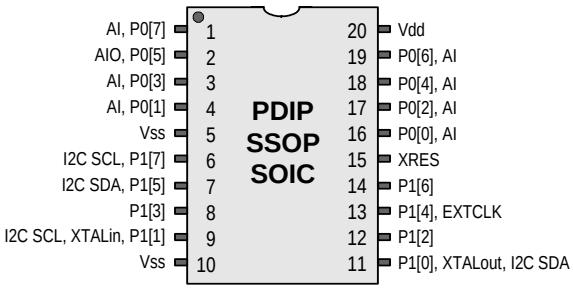

### 1.1.2 20-Pin Part Pinout

**Table 1-2. 20-Pin Part Pinout (PDIP, SSOP, SOIC)**

| Pin No. | Type | | Pin Name | Description |
|---|---|---|---|---|
| | Digital | Analog | | |
| 1 | IO | I | P0[7] | Analog column mux input. |
| 2 | IO | IO | P0[5] | Analog column mux input and column output. |
| 3 | IO | I | P0[3] | Analog column mux input. |
| 4 | IO | I | P0[1] | Analog column mux input. |
| 5 | Power | | Vss | Ground connection. |
| 6 | IO | | P1[7] | I2C Serial Clock (SCL) |
| 7 | IO | | P1[5] | I2C Serial Data (SDA) |
| 8 | IO | | P1[3] | |
| 9 | IO | | P1[1] | Crystal Input (XTALin), I2C Serial Clock (SCL) |
| 10 | Power | | Vss | Ground connection. |
| 11 | IO | | P1[0] | Crystal Output (XTALout), I2C Serial Data (SDA) |
| 12 | IO | | P1[2] | |
| 13 | IO | | P1[4] | Optional External Clock Input (EXTCLK) |
| 14 | IO | | P1[6] | |
| 15 | Input | | XRES | Active high external reset with internal pull down. |
| 16 | IO | I | P0[0] | Analog column mux input. |
| 17 | IO | I | P0[2] | Analog column mux input. |
| 18 | IO | I | P0[4] | Analog column mux input. |
| 19 | IO | I | P0[6] | Analog column mux input. |
| 20 | Power | | Vdd | Supply voltage. |

**LEGEND**: A = Analog, I = Input, and O = Output.

**CY8C22213 20-Pin PSoC Device**



## 1.1.3 32-Pin Part Pinout

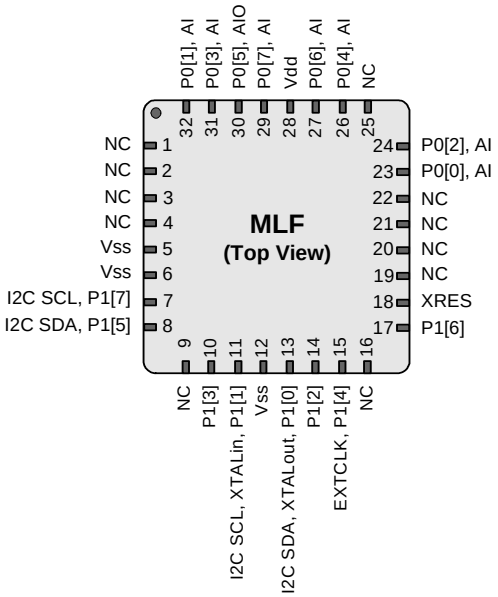
**Table 1-3. 32-Pin Part Pinout (MLF*)**

| Pin No. | Type | | Pin Name | Description |
|---|---|---|---|---|
| | Digital | Analog | | |
| 1 | | | NC | No connection. Do not use. |
| 2 | | | NC | No connection. Do not use. |
| 3 | | | NC | No connection. Do not use. |
| 4 | | | NC | No connection. Do not use. |
| 5 | Power | | Vss | Ground connection. |
| 6 | Power | | Vss | Ground connection. |
| 7 | IO | | P1[7] | I2C Serial Clock (SCL) |
| 8 | IO | | P1[5] | I2C Serial Data (SDA) |
| 9 | | | NC | No connection. Do not use. |
| 10 | IO | | P1[3] | |
| 11 | IO | | P1[1] | Crystal Input (XTALin), I2C Serial Clock (SCL) |
| 12 | Power | | Vss | Ground connection. |
| 13 | IO | | P1[0] | Crystal Output (XTALout), I2C Serial Data (SDA) |
| 14 | IO | | P1[2] | |
| 15 | IO | | P1[4] | Optional External Clock Input (EXTCLK) |
| 16 | | | NC | No connection. Do not use. |
| 17 | IO | | P1[6] | |
| 18 | Input | | XRES | Active high external reset with internal pull down. |
| 19 | | | NC | No connection. Do not use. |
| 20 | | | NC | No connection. Do not use. |
| 21 | | | NC | No connection. Do not use. |
| 22 | | | NC | No connection. Do not use. |
| 23 | IO | I | P0[0] | Analog column mux input. |
| 24 | IO | I | P0[2] | Analog column mux input. |
| 25 | | | NC | No connection. Do not use. |
| 26 | IO | I | P0[4] | Analog column mux input. |
| 27 | IO | I | P0[6] | Analog column mux input. |
| 28 | Power | | Vdd | Supply voltage. |
| 29 | IO | I | P0[7] | Analog column mux input. |
| 30 | IO | IO | P0[5] | Analog column mux input and column output. |
| 31 | IO | I | P0[3] | Analog column mux input. |
| 32 | IO | I | P0[1] | Analog column mux input. |

**LEGEND**: A = Analog, I = Input, and O = Output.

* The MLF package has a center pad that must be connected to the same ground as the Vss pin.

**CY8C22213 PSoC Device**



# 2. Register Reference

This chapter lists the registers of the CY8C22x13 PSoC device by way of mapping tables, in offset order. For detailed register information, reference the *PSoC™ Mixed Signal Array Technical Reference Manual*.

## 2.1 Register Conventions

### 2.1.1 Abbreviations Used

The register conventions specific to this section are listed in the following table.

| Convention | Description |
|---|---|
| RW | Read and write register or bit(s) |
| R | Read register or bit(s) |
| W | Write register or bit(s) |
| L | Logical register or bit(s) |
| C | Clearable register or bit(s) |
| # | Access is bit specific |

## 2.2 Register Mapping Tables

The PSoC device has a total register address space of 512 bytes. The register space is also referred to as IO space and is broken into two parts. The XOI bit in the Flag register determines which bank the user is currently in. When the XOI bit is set, the user is said to be in the “extended” address space or the “configuration” registers.

**Note** In the following register mapping tables, blank fields are Reserved and should not be accessed.

## Register Map Bank 0 Table: User Space

| Name | Addr (0,Hex) | Access | Name | Addr (0,Hex) | Access | Name | Addr (0,Hex) | Access | Name | Addr (0,Hex) | Access |
|---|---|---|---|---|---|---|---|---|---|---|---|
| PRT0DR | 00 | RW | | 40 | | | 80 | | | C0 | |
| PRT0IE | 01 | RW | | 41 | | | 81 | | | C1 | |
| PRT0GS | 02 | RW | | 42 | | | 82 | | | C2 | |
| PRT0DM2 | 03 | RW | | 43 | | | 83 | | | C3 | |
| PRT1DR | 04 | RW | | 44 | | ASD11CR0 | 84 | RW | | C4 | |
| PRT1IE | 05 | RW | | 45 | | ASD11CR1 | 85 | RW | | C5 | |
| PRT1GS | 06 | RW | | 46 | | ASD11CR2 | 86 | RW | | C6 | |
| PRT1DM2 | 07 | RW | | 47 | | ASD11CR3 | 87 | RW | | C7 | |
| | 08 | | | 48 | | | 88 | | | C8 | |
| | 09 | | | 49 | | | 89 | | | C9 | |
| | 0A | | | 4A | | | 8A | | | CA | |
| | 0B | | | 4B | | | 8B | | | CB | |
| | 0C | | | 4C | | | 8C | | | CC | |
| | 0D | | | 4D | | | 8D | | | CD | |
| | 0E | | | 4E | | | 8E | | | CE | |
| | 0F | | | 4F | | | 8F | | | CF | |
| | 10 | | | 50 | | | 90 | | | D0 | |
| | 11 | | | 51 | | | 91 | | | D1 | |
| | 12 | | | 52 | | | 92 | | | D2 | |
| | 13 | | | 53 | | | 93 | | | D3 | |
| | 14 | | | 54 | | ASC21CR0 | 94 | RW | | D4 | |
| | 15 | | | 55 | | ASC21CR1 | 95 | RW | | D5 | |
| | 16 | | | 56 | | ASC21CR2 | 96 | RW | I2C_CFG | D6 | RW |
| | 17 | | | 57 | | ASC21CR3 | 97 | RW | I2C_SCR | D7 | # |
| | 18 | | | 58 | | | 98 | | I2C_DR | D8 | RW |
| | 19 | | | 59 | | | 99 | | I2C_MSCR | D9 | # |
| | 1A | | | 5A | | | 9A | | INT_CLR0 | DA | RW |
| | 1B | | | 5B | | | 9B | | INT_CLR1 | DB | RW |
| | 1C | | | 5C | | | 9C | | | DC | |
| | 1D | | | 5D | | | 9D | | INT_CLR3 | DD | RW |
| | 1E | | | 5E | | | 9E | | INT_MSK3 | DE | RW |
| | 1F | | | 5F | | | 9F | | | DF | |
| DBB00DR0 | 20 | # | AMX_IN | 60 | RW | | A0 | | INT_MSK0 | E0 | RW |
| DBB00DR1 | 21 | W | | 61 | | | A1 | | INT_MSK1 | E1 | RW |
| DBB00DR2 | 22 | RW | | 62 | | | A2 | | INT_VC | E2 | RC |
| DBB00CR0 | 23 | # | ARF_CR | 63 | RW | | A3 | | RES_WDT | E3 | W |
| DBB01DR0 | 24 | # | CMP_CR0 | 64 | # | | A4 | | DEC_DH | E4 | RC |
| DBB01DR1 | 25 | W | ASY_CR | 65 | # | | A5 | | DEC_DL | E5 | RC |
| DBB01DR2 | 26 | RW | CMP_CR1 | 66 | RW | | A6 | | DEC_CR0 | E6 | RW |
| DBB01CR0 | 27 | # | | 67 | | | A7 | | DEC_CR1 | E7 | RW |
| DCB02DR0 | 28 | # | | 68 | | | A8 | | | E8 | |
| DCB02DR1 | 29 | W | | 69 | | | A9 | | | E9 | |
| DCB02DR2 | 2A | RW | | 6A | | | AA | | | EA | |
| DCB02CR0 | 2B | # | | 6B | | | AB | | | EB | |
| DCB03DR0 | 2C | # | | 6C | | | AC | | | EC | |
| DCB03DR1 | 2D | W | | 6D | | | AD | | | ED | |
| DCB03DR2 | 2E | RW | | 6E | | | AE | | | EE | |
| DCB03CR0 | 2F | # | | 6F | | | AF | | | EF | |
| | 30 | | | 70 | | RDI0RI | B0 | RW | | F0 | |
| | 31 | | | 71 | | RDI0SYN | B1 | RW | | F1 | |
| | 32 | | | 72 | | RDI0IS | B2 | RW | | F2 | |
| | 33 | | | 73 | | RDI0LT0 | B3 | RW | | F3 | |
| | 34 | | ACB01CR3 | 74 | RW | RDIOLT1 | B4 | RW | | F4 | |
| | 35 | | ACB01CR0 | 75 | RW | RDI0RO0 | B5 | RW | | F5 | |
| | 36 | | ACB01CR1 | 76 | RW | RDI0RO1 | B6 | RW | | F6 | |
| | 37 | | ACB01CR2 | 77 | RW | | B7 | | CPU_F | F7 | RL |
| | 38 | | | 78 | | | B8 | | | F8 | |
| | 39 | | | 79 | | | B9 | | | F9 | |
| | 3A | | | 7A | | | BA | | | FA | |
| | 3B | | | 7B | | | BB | | | FB | |
| | 3C | | | 7C | | | BC | | | FC | |
| | 3D | | | 7D | | | BD | | | FD | |
| | 3E | | | 7E | | | BE | | CPU_SCR1 | FE | # |
| | 3F | | | 7F | | | BF | | CPU_SCR0 | FF | # |

**Blank fields are Reserved and should not be accessed.** # Access is bit specific.

## Register Map Bank 1 Table: Configuration Space

| Name | Addr (1,Hex) | Access | Name | Addr (1,Hex) | Access | Name | Addr (1,Hex) | Access | Name | Addr (1,Hex) | Access |
|---|---|---|---|---|---|---|---|---|---|---|---|
| PRT0DM0 | 00 | RW | | 40 | | | 80 | | | C0 | |
| PRT0DM1 | 01 | RW | | 41 | | | 81 | | | C1 | |
| PRT0IC0 | 02 | RW | | 42 | | | 82 | | | C2 | |
| PRT0IC1 | 03 | RW | | 43 | | | 83 | | | C3 | |
| PRT1DM0 | 04 | RW | | 44 | | ASD11CR0 | 84 | RW | | C4 | |
| PRT1DM1 | 05 | RW | | 45 | | ASD11CR1 | 85 | RW | | C5 | |
| PRT1IC0 | 06 | RW | | 46 | | ASD11CR2 | 86 | RW | | C6 | |
| PRT1IC1 | 07 | RW | | 47 | | ASD11CR3 | 87 | RW | | C7 | |
| | 08 | | | 48 | | | 88 | | | C8 | |
| | 09 | | | 49 | | | 89 | | | C9 | |
| | 0A | | | 4A | | | 8A | | | CA | |
| | 0B | | | 4B | | | 8B | | | CB | |
| | 0C | | | 4C | | | 8C | | | CC | |
| | 0D | | | 4D | | | 8D | | | CD | |
| | 0E | | | 4E | | | 8E | | | CE | |
| | 0F | | | 4F | | | 8F | | | CF | |
| | 10 | | | 50 | | | 90 | | GDI_O_IN | D0 | RW |
| | 11 | | | 51 | | | 91 | | GDI_E_IN | D1 | RW |
| | 12 | | | 52 | | | 92 | | GDI_O_OU | D2 | RW |
| | 13 | | | 53 | | | 93 | | GDI_E_OU | D3 | RW |
| | 14 | | | 54 | | ASC21CR0 | 94 | RW | | D4 | |
| | 15 | | | 55 | | ASC21CR1 | 95 | RW | | D5 | |
| | 16 | | | 56 | | ASC21CR2 | 96 | RW | | D6 | |
| | 17 | | | 57 | | ASC21CR3 | 97 | RW | | D7 | |
| | 18 | | | 58 | | | 98 | | | D8 | |
| | 19 | | | 59 | | | 99 | | | D9 | |
| | 1A | | | 5A | | | 9A | | | DA | |
| | 1B | | | 5B | | | 9B | | | DB | |
| | 1C | | | 5C | | | 9C | | | DC | |
| | 1D | | | 5D | | | 9D | | OSC_GO_EN | DD | RW |
| | 1E | | | 5E | | | 9E | | OSC_CR4 | DE | RW |
| | 1F | | | 5F | | | 9F | | OSC_CR3 | DF | RW |
| DBB00FN | 20 | RW | CLK_CR0 | 60 | RW | | A0 | | OSC_CR0 | E0 | RW |
| DBB00IN | 21 | RW | CLK_CR1 | 61 | RW | | A1 | | OSC_CR1 | E1 | RW |
| DBB00OU | 22 | RW | ABF_CR0 | 62 | RW | | A2 | | OSC_CR2 | E2 | RW |
| | 23 | | | 63 | | | A3 | | VLT_CR | E3 | RW |
| DBB01FN | 24 | RW | | 64 | | | A4 | | VLT_CMP | E4 | R |
| DBB01IN | 25 | RW | | 65 | | | A5 | | | E5 | |
| DBB01OU | 26 | RW | AMD_CR1 | 66 | RW | | A6 | | | E6 | |
| | 27 | | ALT_CR0 | 67 | RW | | A7 | | | E7 | |
| DCB02FN | 28 | RW | | 68 | | | A8 | | IMO_TR | E8 | W |
| DCB02IN | 29 | RW | | 69 | | | A9 | | ILO_TR | E9 | W |
| DCB02OU | 2A | RW | | 6A | | | AA | | BDG_TR | EA | RW |
| | 2B | | | 6B | | | AB | | ECO_TR | EB | W |
| DCB03FN | 2C | RW | | 6C | | | AC | | | EC | |
| DCB03IN | 2D | RW | | 6D | | | AD | | | ED | |
| DCB03OU | 2E | RW | | 6E | | | AE | | | EE | |
| | 2F | | | 6F | | | AF | | | EF | |
| | 30 | | | 70 | | RDI0RI | B0 | RW | | F0 | |
| | 31 | | | 71 | | RDI0SYN | B1 | RW | | F1 | |
| | 32 | | | 72 | | RDI0IS | B2 | RW | | F2 | |
| | 33 | | | 73 | | RDI0LT0 | B3 | RW | | F3 | |
| | 34 | | ACB01CR3 | 74 | RW | RDIOLT1 | B4 | RW | | F4 | |
| | 35 | | ACB01CR0 | 75 | RW | RDI0RO0 | B5 | RW | | F5 | |
| | 36 | | ACB01CR1 | 76 | RW | RDI0RO1 | B6 | RW | | F6 | |
| | 37 | | ACB01CR2 | 77 | RW | | B7 | | CPU_F | F7 | RL |
| | 38 | | | 78 | | | B8 | | | F8 | |
| | 39 | | | 79 | | | B9 | | | F9 | |
| | 3A | | | 7A | | | BA | | | FA | |
| | 3B | | | 7B | | | BB | | | FB | |
| | 3C | | | 7C | | | BC | | | FC | |
| | 3D | | | 7D | | | BD | | | FD | |
| | 3E | | | 7E | | | BE | | CPU_SCR1 | FE | # |
| | 3F | | | 7F | | | BF | | CPU_SCR0 | FF | # |

**Blank fields are Reserved and should not be accessed.** # Access is bit specific.

# 3. Electrical Specifications

This chapter presents the DC and AC electrical specifications of the CY8C22x13 PSoC device. For the most up to date electrical specifications, confirm that you have the most recent data sheet by referencing the web at http://www.cypress.com/psoc.

Specifications are valid for -40°C ≤ $T_A$ ≤ 85°C and $T_J$ ≤ 100°C as specified, except where noted. Specifications for devices running at greater than 12 MHz are valid for -40°C ≤ $T_A$ ≤ 70°C and $T_J$ ≤ 82°C.

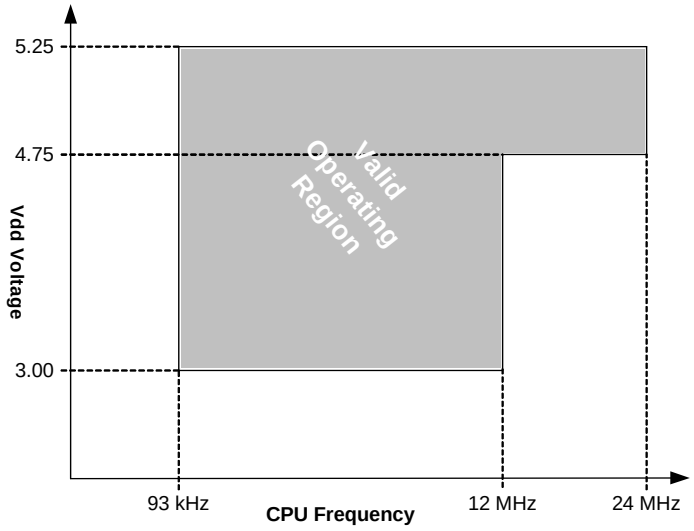



**Figure 3-1. Voltage versus Operating Frequency**

The following table lists the units of measure that are used in this chapter.

**Table 3-1: Units of Measure**

| Symbol | Unit of Measure | Symbol | Unit of Measure |
|---|---|---|---|
| °C | degree Celsius | µW | micro watts |
| dB | decibels | mA | milli-ampere |
| fF | femto farad | ms | milli-second |
| Hz | hertz | mV | milli-volts |
| KB | 1024 bytes | nA | nano ampere |
| Kbit | 1024 bits | ns | nanosecond |
| kHz | kilohertz | nV | nanovolts |
| kΩ | kilohm | Ω | ohm |
| MHz | megahertz | pA | pico ampere |
| MΩ | megaohm | pF | pico farad |
| µA | micro ampere | pp | peak-to-peak |
| µF | micro farad | ppm | parts per million |
| µH | micro henry | ps | picosecond |
| µs | microsecond | sps | samples per second |
| µV | micro volts | σ | sigma: one standard deviation |
| µVrms | micro volts root-mean-square | V | volts |

## 3.1 Absolute Maximum Ratings

**Table 3-2. Absolute Maximum Ratings**

| Symbol | Description | Min | Typ | Max | Units | Notes |
|---|---|---|---|---|---|---|
| $T_{STG}$ | Storage Temperature | -55 | – | +100 | °C | Higher storage temperatures will reduce data retention time. |
| $T_A$ | Ambient Temperature with Power Applied | -40 | – | +85 | °C | |
| Vdd | Supply Voltage on Vdd Relative to Vss | -0.5 | – | +6.0 | V | |
| $V_{IO}$ | DC Input Voltage | Vss - 0.5 | – | Vdd + 0.5 | V | |
| – | DC Voltage Applied to Tri-state | Vss - 0.5 | – | Vdd + 0.5 | V | |
| $I_{MIO}$ | Maximum Current into any Port Pin | -25 | – | +50 | mA | |
| $I_{MAIO}$ | Maximum Current into any Port Pin Configured as Analog Driver | -50 | – | +50 | mA | |
| – | Static Discharge Voltage | 2000 | – | – | V | |
| – | Latch-up Current | – | – | 200 | mA | |

## 3.2 Operating Temperature

**Table 3-3. Operating Temperature**

| Symbol | Description | Min | Typ | Max | Units | Notes |
|---|---|---|---|---|---|---|
| $T_A$ | Ambient Temperature | -40 | – | +85 | °C | |
| $T_J$ | Junction Temperature | -40 | – | +100 | °C | The temperature rise from ambient to junction is package specific. See “Thermal Impedances” on page 34. The user must limit the power consumption to comply with this requirement. |

# 3.3 DC Electrical Characteristics

## 3.3.1 DC Chip-Level Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C ≤ $T_A$ ≤ 85°C, or 3.0V to 3.6V and -40°C ≤ $T_A$ ≤ 85°C, respectively. Typical parameters apply to 5V and 3.3V at 25°C and are for design guidance only or unless otherwise specified.

**Table 3-4. DC Chip-Level Specifications**

| Symbol | Description | Min | Typ | Max | Units | Notes |
|---|---|---|---|---|---|---|
| Vdd | Supply Voltage | 3.00 | – | 5.25 | V | |
| $I_{DD}$ | Supply Current | – | 5 | 8 | mA | Conditions are Vdd = 5.0V, 25 °C, CPU = 3 MHz, 48 MHz disabled. VC1 = 1.5 MHz, VC2 = 93.75 kHz, VC3 = 93.75 kHz. |
| $I_{DD3}$ | Supply Current | – | 3.3 | 6.0 | mA | Conditions are Vdd = 3.3V, $T_A$ = 25 °C, CPU = 3 MHz, 48 MHz = Disabled, VC1 = 1.5 MHz, VC2 = 93.75 kHz, VC3 = 93.75 kHz. |
| $I_{SB}$ | Sleep (Mode) Current with POR, LVD, Sleep Timer, and WDT.[a] | – | 3 | 6.5 | µA | Conditions are with internal slow speed oscillator, Vdd = 3.3V, -40 °C <= $T_A$ <= 55 °C. |
| $I_{SBH}$ | Sleep (Mode) Current with POR, LVD, Sleep Timer, and WDT at high temperature.[a] | – | 4 | 25 | µA | Conditions are with internal slow speed oscillator, Vdd = 3.3V, 55 °C < $T_A$ <= 85 °C. |
| $I_{SBXTL}$ | Sleep (Mode) Current with POR, LVD, Sleep Timer, WDT, and external crystal.[a] | – | 4 | 7.5 | µA | Conditions are with properly loaded, 1 µW max, 32.768 kHz crystal. Vdd = 3.3V, -40 °C <= $T_A$ <= 55 °C. |
| $I_{SBXTLH}$ | Sleep (Mode) Current with POR, LVD, Sleep Timer, WDT, and external crystal at high temperature.[a] | – | 5 | 26 | µA | Conditions are with properly loaded, 1 µW max, 32.768 kHz crystal. Vdd = 3.3V, 55 °C < $T_A$ <= 85 °C. |
| $V_{REF}$ | Reference Voltage (Bandgap) | 1.275 | 1.3 | 1.325 | V | Trimmed for appropriate Vdd. |

a. Standby current includes all functions (POR, LVD, WDT, Sleep Time) needed for reliable system operation. This should be compared with devices that have similar functions enabled.

## 3.3.2 DC General Purpose IO Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C ≤ $T_A$ ≤ 85°C, or 3.0V to 3.6V and -40°C ≤ $T_A$ ≤ 85°C, respectively. Typical parameters apply to 5V and 3.3V at 25°C and are for design guidance only or unless otherwise specified.

**Table 3-5. DC GPIO Specifications**

| Symbol | Description | Min | Typ | Max | Units | Notes |
|---|---|---|---|---|---|---|
| $R_{PU}$ | Pull up Resistor | 4 | 5.6 | 8 | kΩ | |
| $R_{PD}$ | Pull down Resistor | 4 | 5.6 | 8 | kΩ | |
| $V_{OH}$ | High Output Level | Vdd - 1.0 | – | – | V | IOH = 10 mA, Vdd = 4.75 to 5.25V (80 mA maximum combined IOH budget) |
| $V_{OL}$ | Low Output Level | – | – | 0.75 | V | IOL = 25 mA, Vdd = 4.75 to 5.25V (150 mA maximum combined IOL budget) |
| $V_{IL}$ | Input Low Level | – | – | 0.8 | V | Vdd = 3.0 to 5.25 |
| $V_{IH}$ | Input High Level | 2.1 | – | | V | Vdd = 3.0 to 5.25 |
| $V_H$ | Input Hysterisis | – | 60 | – | mV | |
| $I_{IL}$ | Input Leakage (Absolute Value) | – | 1 | – | nA | Gross tested to 1 µA. |
| $C_{IN}$ | Capacitive Load on Pins as Input | – | 3.5 | 10 | pF | Package and pin dependent. Temp = 25°C. |
| $C_{OUT}$ | Capacitive Load on Pins as Output | – | 3.5 | 10 | pF | Package and pin dependent. Temp = 25°C. |

### 3.3.3 DC Operational Amplifier Specifications

The following tables list guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C ≤ $T_A$ ≤ 85°C, or 3.0V to 3.6V and -40°C ≤ $T_A$ ≤ 85°C, respectively. Typical parameters apply to 5V and 3.3V at 25°C and are for design guidance only or unless otherwise specified.

The Operational Amplifier is a component of both the Analog Continuous Time PSoC blocks and the Analog Switched Cap PSoC blocks. The guaranteed specifications are measured in the Analog Continuous Time PSoC block. Typical parameters apply to 5V at 25°C and are for design guidance only.

**Table 3-6. 5V DC Operational Amplifier Specifications**

| Symbol | Description | Min | Typ | Max | Units | Notes |
|---|---|---|---|---|---|---|
| $V_{OSOA}$ | Input Offset Voltage (absolute value) Low Power | – | 1.6 | 10 | mV | |
| | Input Offset Voltage (absolute value) Mid Power | – | 1.3 | 8 | mV | |
| | Input Offset Voltage (absolute value) High Power | – | 1.2 | 7.5 | mV | |
| $TCV_{OSOA}$ | Average Input Offset Voltage Drift | – | 7.0 | 35.0 | µV/°C | |
| $I_{EBOA}$ | Input Leakage Current (Port 0 Analog Pins) | – | 20 | – | pA | Gross tested to 1 µA. |
| $C_{INOA}$ | Input Capacitance (Port 0 Analog Pins) | – | 4.5 | 9.5 | pF | Package and pin dependent. Temp = 25°C. |
| $V_{CMOA}$ | Common Mode Voltage Range | 0.0 | – | Vdd | V | The common-mode input voltage range is measured through an analog output buffer. The specification includes the limitations imposed by the characteristics of the analog output buffer. |
| | Common Mode Voltage Range (high power or high opamp bias) | 0.5 | – | Vdd - 0.5 | | |
| $G_{OLOA}$ | Open Loop Gain | | – | – | dB | Specification is applicable at high power. For all other bias modes (except high power, high opamp bias), minimum is 60 dB. |
| | Power = Low | 60 | | | | |
| | Power = Medium | 60 | | | | |
| | Power = High | 80 | | | | |
| $V_{OHIGHOA}$ | High Output Voltage Swing (worst case internal load) | | | | | |
| | Power = Low | Vdd - 0.2 | – | – | V | |
| | Power = Medium | Vdd - 0.2 | – | – | V | |
| | Power = High | Vdd - 0.5 | – | – | V | |
| $V_{OLOWOA}$ | Low Output Voltage Swing (worst case internal load) | | | | | |
| | Power = Low | – | – | 0.2 | V | |
| | Power = Medium | – | – | 0.2 | V | |
| | Power = High | – | – | 0.5 | V | |
| $I_{SOA}$ | Supply Current (including associated AGND buffer) | | | | | |
| | Power = Low | – | 150 | 200 | µA | |
| | Power = Low, Opamp Bias = High | – | 300 | 400 | µA | |
| | Power = Medium | – | 600 | 800 | µA | |
| | Power = Medium, Opamp Bias = High | – | 1200 | 1600 | µA | |
| | Power = High | – | 2400 | 3200 | µA | |
| | Power = High, Opamp Bias = High | – | 4600 | 6400 | µA | |
| $PSRR_{OA}$ | Supply Voltage Rejection Ratio | 60 | – | – | dB | |

### Table 3-7. 3.3V DC Operational Amplifier Specifications

| Symbol | Description | Min | Typ | Max | Units | Notes |
|---|---|---|---|---|---|---|
| $V_{OSOA}$ | Input Offset Voltage (absolute value) Low Power | – | 1.65 | 10 | mV | |
| | Input Offset Voltage (absolute value) Mid Power | – | 1.32 | 8 | mV | |
| | High Power is 5 Volt Only | | | | | |
| $TCV_{OSOA}$ | Average Input Offset Voltage Drift | – | 7.0 | 35.0 | µV/°C | |
| $I_{EBOA}$ | Input Leakage Current (Port 0 Analog Pins) | – | 20 | – | pA | Gross tested to 1 µA. |
| $C_{INOA}$ | Input Capacitance (Port 0 Analog Pins) | – | 4.5 | 9.5 | pF | Package and pin dependent. Temp = 25°C. |
| $V_{CMOA}$ | Common Mode Voltage Range | 0.2 | – | Vdd - 0.2 | V | The common-mode input voltage range is measured through an analog output buffer. The specification includes the limitations imposed by the characteristics of the analog output buffer. |
| $G_{OLOA}$ | Open Loop Gain | | – | – | dB | Specification is applicable at high power. For all other bias modes (except high power, high opamp bias), minimum is 60 dB. |
| | Power = Low | 60 | | | | |
| | Power = Medium | 60 | | | | |
| | Power = High | 80 | | | | |
| $V_{OHIGHOA}$ | High Output Voltage Swing (worst case internal load) | | | | | |
| | Power = Low | Vdd - 0.2 | – | – | V | |
| | Power = Medium | Vdd - 0.2 | – | – | V | |
| | Power = High is 5V only | Vdd - 0.2 | – | – | V | |
| $V_{OLOWOA}$ | Low Output Voltage Swing (worst case internal load) | | | | | |
| | Power = Low | – | – | 0.2 | V | |
| | Power = Medium | – | – | 0.2 | V | |
| | Power = High | – | – | 0.2 | V | |
| $I_{SOA}$ | Supply Current (including associated AGND buffer) | | | | | |
| | Power = Low | – | 150 | 200 | µA | |
| | Power = Low, Opamp Bias = High | – | 300 | 400 | µA | |
| | Power = Medium | – | 600 | 800 | µA | |
| | Power = Medium, Opamp Bias = High | – | 1200 | 1600 | µA | |
| | Power = High | – | 2400 | 3200 | µA | |
| | Power = High, Opamp Bias = High | – | 4600 | 6400 | µA | |
| $PSRR_{OA}$ | Supply Voltage Rejection Ratio | 50 | – | – | dB | |

### 3.3.4 DC Analog Output Buffer Specifications

The following tables list guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C ≤ $T_A$ ≤ 85°C, or 3.0V to 3.6V and -40°C ≤ $T_A$ ≤ 85°C, respectively. Typical parameters apply to 5V and 3.3V at 25°C and are for design guidance only or unless otherwise specified.

**Table 3-8. 5V DC Analog Output Buffer Specifications**

| Symbol | Description | Min | Typ | Max | Units | Notes |
|---|---|---|---|---|---|---|
| $V_{OSOB}$ | Input Offset Voltage (Absolute Value) | – | 3 | 12 | mV | |
| $TCV_{OSOB}$ | Average Input Offset Voltage Drift | – | +6 | – | µV/°C | |
| $V_{CMOB}$ | Common-Mode Input Voltage Range | 0.5 | – | Vdd - 1.0 | V | |
| $R_{OUTOB}$ | Output Resistance | | | | | |
| | Power = Low | – | 1 | – | Ω | |
| | Power = High | – | 1 | – | Ω | |
| $V_{OHIGHOB}$ | High Output Voltage Swing (Load = 32 ohms to Vdd/2) | | | | | |
| | Power = Low | 0.5 x Vdd + 1.1 | – | – | V | |
| | Power = High | 0.5 x Vdd + 1.1 | – | – | V | |
| $V_{OLOWOB}$ | Low Output Voltage Swing (Load = 32 ohms to Vdd/2) | | | | | |
| | Power = Low | – | – | 0.5 x Vdd - 1.3 | V | |
| | Power = High | – | – | 0.5 x Vdd - 1.3 | V | |
| $I_{SOB}$ | Supply Current Including Bias Cell (No Load) | | | | | |
| | Power = Low | – | 1.1 | 5.1 | mA | |
| | Power = High | – | 2.6 | 8.8 | mA | |
| $PSRR_{OB}$ | Supply Voltage Rejection Ratio | 60 | – | – | dB | |

**Table 3-9. 3.3V DC Analog Output Buffer Specifications**

| Symbol | Description | Min | Typ | Max | Units | Notes |
|---|---|---|---|---|---|---|
| $V_{OSOB}$ | Input Offset Voltage (Absolute Value) | – | 3 | 12 | mV | |
| $TCV_{OSOB}$ | Average Input Offset Voltage Drift | – | +6 | – | µV/°C | |
| $V_{CMOB}$ | Common-Mode Input Voltage Range | 0.5 | - | Vdd - 1.0 | V | |
| $R_{OUTOB}$ | Output Resistance | | | | | |
| | Power = Low | – | 1 | – | Ω | |
| | Power = High | – | 1 | – | Ω | |
| $V_{OHIGHOB}$ | High Output Voltage Swing (Load = 1K ohms to Vdd/2) | | | | | |
| | Power = Low | 0.5 x Vdd + 1.0 | – | – | V | |
| | Power = High | 0.5 x Vdd + 1.0 | – | – | V | |
| $V_{OLOWOB}$ | Low Output Voltage Swing (Load = 1K ohms to Vdd/2) | | | | | |
| | Power = Low | – | – | 0.5 x Vdd - 1.0 | V | |
| | Power = High | – | – | 0.5 x Vdd - 1.0 | V | |
| $I_{SOB}$ | Supply Current Including Bias Cell (No Load) | | | | | |
| | Power = Low | | 0.8 | 2.0 | mA | |
| | Power = High | – | 2.0 | 4.3 | mA | |
| $PSRR_{OB}$ | Supply Voltage Rejection Ratio | 50 | – | – | dB | |

### 3.3.5 DC Analog Reference Specifications

The following tables list guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C ≤ $T_A$ ≤ 85°C, or 3.0V to 3.6V and -40°C ≤ $T_A$ ≤ 85°C, respectively. Typical parameters apply to 5V and 3.3V at 25°C and are for design guidance only or unless otherwise specified.

The guaranteed specifications are measured through the Analog Continuous Time PSoC blocks. The power levels for AGND refer to the power of the Analog Continuous Time PSoC block. The power levels for RefHi and RefLo refer to the Analog Reference Control register. The limits stated for AGND include the offset error of the AGND buffer local to the Analog Continuous Time PSoC block.

**Table 3-10. 5V DC Analog Reference Specifications**

| Symbol | Description | Min | Typ | Max | Units |
|---|---|---|---|---|---|
| – | AGND = Vdd/2[a]<br>CT Block Power = High | Vdd/2 - 0.043 | Vdd/2 - 0.025 | Vdd/2 + 0.003 | V |

a. AGND tolerance includes the offsets of the local buffer in the PSoC block. Bandgap voltage is 1.3V ± 2%.

**Table 3-11. 3.3V DC Analog Reference Specifications**

| Symbol | Description | Min | Typ | Max | Units |
|---|---|---|---|---|---|
| – | AGND = Vdd/2[a]<br>CT Block Power = High | Vdd/2 - 0.037 | Vdd/2 - 0.020 | Vdd/2 + 0.002 | V |

a. AGND tolerance includes the offsets of the local buffer in the PSoC block. Bandgap voltage is 1.3V ± 2%

### 3.3.6 DC Analog PSoC Block Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C ≤ $T_A$ ≤ 85°C, or 3.0V to 3.6V and -40°C ≤ $T_A$ ≤ 85°C, respectively. Typical parameters apply to 5V and 3.3V at 25°C and are for design guidance only or unless otherwise specified.

**Table 3-12. DC Analog PSoC Block Specifications**

| Symbol | Description | Min | Typ | Max | Units | Notes |
|---|---|---|---|---|---|---|
| $R_{CT}$ | Resistor Unit Value (Continuous Time) | – | 12.24 | – | kΩ | |
| $C_{SC}$ | Capacitor Unit Value (Switch Cap) | – | 80 | – | fF | |

## 3.3.7 DC POR and LVD Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C ≤ $T_A$ ≤ 85°C, or 3.0V to 3.6V and -40°C ≤ $T_A$ ≤ 85°C, respectively. Typical parameters apply to 5V and 3.3V at 25°C and are for design guidance only or unless otherwise specified.

**Note** The bits PORLEV and VM in the table below refer to bits in the VLT_CR register. See the *PSoC Mixed Signal Array Technical Reference Manual* for more information on the VLT_CR register.

**Table 3-13. DC POR and LVD Specifications**

| Symbol | Description | Min | Typ | Max | Units | Notes |
|---|---|---|---|---|---|---|
| | Vdd Value for PPOR Trip (positive ramp) | | | | | |
| $V_{PPOR0R}$ | PORLEV[1:0] = 00b | | 2.908 | | V | |
| $V_{PPOR1R}$ | PORLEV[1:0] = 01b | – | 4.394 | – | V | |
| $V_{PPOR2R}$ | PORLEV[1:0] = 10b | | 4.548 | | V | |
| | Vdd Value for PPOR Trip (negative ramp) | | | | | |
| $V_{PPOR0}$ | PORLEV[1:0] = 00b | | 2.816 | | V | |
| $V_{PPOR1}$ | PORLEV[1:0] = 01b | – | 4.394 | – | V | |
| $V_{PPOR2}$ | PORLEV[1:0] = 10b | | 4.548 | | V | |
| | PPOR Hysteresis | | | | | |
| $V_{PH0}$ | PORLEV[1:0] = 00b | – | 92 | – | mV | |
| $V_{PH1}$ | PORLEV[1:0] = 01b | – | 0 | – | mV | |
| $V_{PH2}$ | PORLEV[1:0] = 10b | – | 0 | – | mV | |
| | Vdd Value for LVD Trip | | | | | |
| $V_{LVD0}$ | VM[2:0] = 000b | 2.863 | 2.921 | 2.979[a] | V | |
| $V_{LVD1}$ | VM[2:0] = 001b | 2.963 | 3.023 | 3.083 | V | |
| $V_{LVD2}$ | VM[2:0] = 010b | 3.070 | 3.133 | 3.196 | V | |
| $V_{LVD3}$ | VM[2:0] = 011b | 3.920 | 4.00 | 4.080 | V | |
| $V_{LVD4}$ | VM[2:0] = 100b | 4.393 | 4.483 | 4.573 | V | |
| $V_{LVD5}$ | VM[2:0] = 101b | 4.550 | 4.643 | 4.736[b] | V | |
| $V_{LVD6}$ | VM[2:0] = 110b | 4.632 | 4.727 | 4.822 | V | |
| $V_{LVD7}$ | VM[2:0] = 111b | 4.718 | 4.814 | 4.910 | V | |

a. Always greater than 50 mV above PPOR (PORLEV = 00) for falling supply.
b. Always greater than 50 mV above PPOR (PORLEV = 10) for falling supply.

## 3.3.8 DC Programming Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C ≤ $T_A$ ≤ 85°C, or 3.0V to 3.6V and -40°C ≤ $T_A$ ≤ 85°C, respectively. Typical parameters apply to 5V and 3.3V at 25°C and are for design guidance only or unless otherwise specified.

**Table 3-14. DC Programming Specifications**

| Symbol | Description | Min | Typ | Max | Units | Notes |
|---|---|---|---|---|---|---|
| $I_{DDP}$ | Supply Current During Programming or Verify | – | 5 | 25 | mA | |
| $V_{ILP}$ | Input Low Voltage During Programming or Verify | – | – | 0.8 | V | |
| $V_{IHP}$ | Input High Voltage During Programming or Verify | 2.2 | – | – | V | |
| $I_{ILP}$ | Input Current when Applying Vilp to P1[0] or P1[1] During Programming or Verify | – | – | 0.2 | mA | Driving internal pull-down resistor. |
| $I_{IHP}$ | Input Current when Applying Vihp to P1[0] or P1[1] During Programming or Verify | – | – | 1.5 | mA | Driving internal pull-down resistor. |
| $V_{OLV}$ | Output Low Voltage During Programming or Verify | – | – | Vss + 0.75 | V | |
| $V_{OHV}$ | Output High Voltage During Programming or Verify | Vdd - 1.0 | – | Vdd | V | |
| $Flash_{ENPB}$ | Flash Endurance (per block) | 50,000 | – | – | – | Erase/write cycles per block. |
| $Flash_{ENT}$ | Flash Endurance (total)[a] | 1,800,000 | – | – | – | Erase/write cycles. |
| $Flash_{DR}$ | Flash Data Retention | 10 | – | – | Years | |

a. A maximum of 36 x 50,000 block endurance cycles is allowed. This may be balanced between operations on 36x1 blocks of 50,000 maximum cycles each, 36x2 blocks of 25,000 maximum cycles each, or 36x4 blocks of 12,500 maximum cycles each (and so forth to limit the total number of cycles to 36x50,000 and that no single block ever sees more than 50,000 cycles).

For the full industrial range, the user must employ a temperature sensor user module (FlashTemp) and feed the result to the temperature argument before writing. Refer to the Flash APIs Application Note AN2015 at http://www.cypress.com under Application Notes for more information.

# 3.4 AC Electrical Characteristics

## 3.4.1 AC Chip-Level Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C ≤ $T_A$ ≤ 85°C, or 3.0V to 3.6V and -40°C ≤ $T_A$ ≤ 85°C, respectively. Typical parameters apply to 5V and 3.3V at 25°C and are for design guidance only or unless otherwise specified.

**Table 3-15. AC Chip-Level Specifications**

| Symbol | Description | Min | Typ | Max | Units | Notes |
|---|---|---|---|---|---|---|
| $F_{IMO}$ | Internal Main Oscillator Frequency | 23.4 | 24 | 24.6[a] | MHz | Trimmed. Utilizing factory trim values. |
| $F_{CPU1}$ | CPU Frequency (5V Nominal) | 0.93 | 24 | 24.6[a,b] | MHz | |
| $F_{CPU2}$ | CPU Frequency (3.3V Nominal) | 0.93 | 12 | 12.3[b,c] | MHz | |
| $F_{48M}$ | Digital PSoC Block Frequency | 0 | 48 | 49.2[a,b,d] | MHz | Refer to the AC Digital Block Specifications below. |
| $F_{24M}$ | Digital PSoC Block Frequency | 0 | 24 | 24.6[b,e,d] | MHz | |
| $F_{32K1}$ | Internal Low Speed Oscillator Frequency | 15 | 32 | 64 | kHz | |
| $F_{32K2}$ | External Crystal Oscillator | – | 32.768 | – | kHz | Accuracy is capacitor and crystal dependent. 50% duty cycle. |
| $F_{PLL}$ | PLL Frequency | – | 23.986 | – | MHz | Is a multiple (x732) of crystal frequency. |
| Jitter24M2 | 24 MHz Period Jitter (PLL) | – | – | 600 | ps | |
| $T_{PLLSLEW}$ | PLL Lock Time | 0.5 | – | 10 | ms | |
| $T_{PLLSLEWS-LOW}$ | PLL Lock Time for Low Gain Setting | 0.5 | – | 50 | ms | |
| $T_{OS}$ | External Crystal Oscillator Startup to 1% | – | 1700 | 2620 | ms | |
| $T_{OSACC}$ | External Crystal Oscillator Startup to 100 ppm | – | 2800 | 3800[f] | ms | |
| Jitter32k | 32 kHz Period Jitter | – | 100 | | ns | |
| $T_{XRST}$ | External Reset Pulse Width | 10 | – | – | µs | |
| DC24M | 24 MHz Duty Cycle | 40 | 50 | 60 | % | |
| Step24M | 24 MHz Trim Step Size | – | 50 | – | kHz | |
| Fout48M | 48 MHz Output Frequency | 46.8 | 48.0 | 49.2[a,c] | MHz | Trimmed. Utilizing factory trim values. |
| Jitter24M1 | 24 MHz Period Jitter (IMO) | – | 600 | | ps | |
| $F_{MAX}$ | Maximum frequency of signal on row input or row output. | – | – | 12.3 | MHz | |
| $T_{RAMP}$ | Supply Ramp Time | 0 | – | – | µs | |

a. 4.75V < Vdd < 5.25V.
b. Accuracy derived from Internal Main Oscillator with appropriate trim for Vdd range.
c. 3.0V < Vdd < 3.6V. See Application Note AN2012 “Adjusting PSoC Microcontroller Trims for Dual Voltage-Range Operation” for information on trimming for operation at 3.3V.
d. See the individual user module data sheets for information on maximum frequencies for user modules.
e. 3.0V < 5.25V.
f. The crystal oscillator frequency is within 100 ppm of its final value by the end of the $T_{osacc}$ period. Correct operation assumes a properly loaded 1 uW maximum drive level 32.768 kHz crystal. 3.0V ≤ Vdd ≤ 5.5V, -40 °C ≤ $T_A$ ≤ 85 °C.

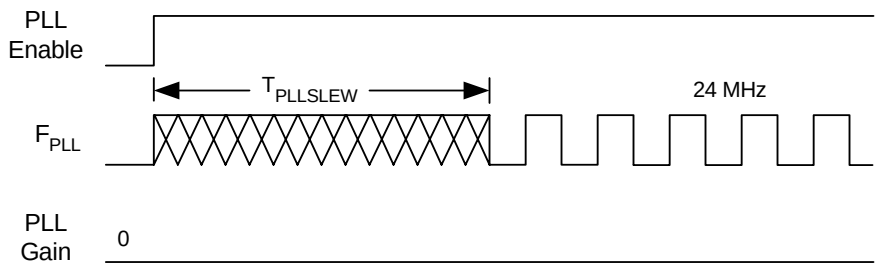



**Figure 3-2. PLL Lock Timing Diagram**

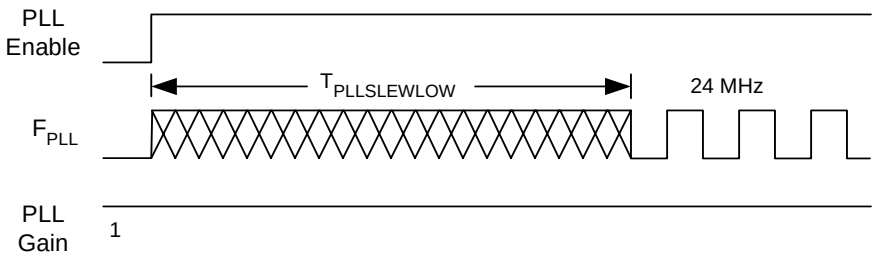



**Figure 3-3. PLL Lock for Low Gain Setting Timing Diagram**

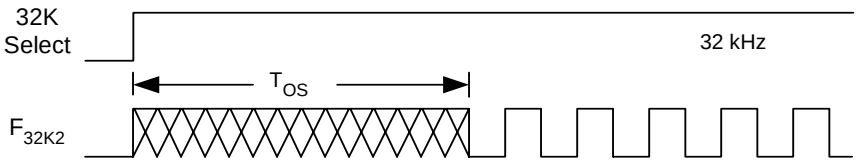



**Figure 3-4. External Crystal Oscillator Startup Timing Diagram**

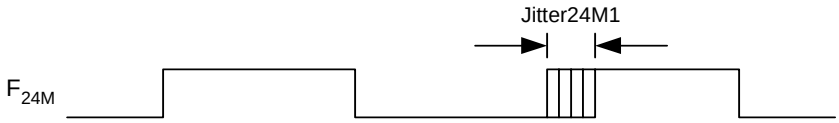



**Figure 3-5. 24 MHz Period Jitter (IMO) Timing Diagram**


**Figure 3-6. 32 kHz Period Jitter (ECO) Timing Diagram**

## 3.4.2 AC General Purpose IO Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C ≤ $T_A$ ≤ 85°C, or 3.0V to 3.6V and -40°C ≤ $T_A$ ≤ 85°C, respectively. Typical parameters apply to 5V and 3.3V at 25°C and are for design guidance only or unless otherwise specified.

**Table 3-16. AC GPIO Specifications**

| Symbol | Description | Min | Typ | Max | Units | Notes |
|---|---|---|---|---|---|---|
| $F_{GPIO}$ | GPIO Operating Frequency | 0 | – | 12 | MHz | |
| TRiseF | Rise Time, Normal Strong Mode, Cload = 50 pF | 3 | – | 18 | ns | Vdd = 4.5 to 5.25V, 10% - 90% |
| TFallF | Fall Time, Normal Strong Mode, Cload = 50 pF | 2 | – | 18 | ns | Vdd = 4.5 to 5.25V, 10% - 90% |
| TRiseS | Rise Time, Slow Strong Mode, Cload = 50 pF | 10 | 27 | – | ns | Vdd = 3 to 5.25V, 10% - 90% |
| TFallS | Fall Time, Slow Strong Mode, Cload = 50 pF | 10 | 22 | – | ns | Vdd = 3 to 5.25V, 10% - 90% |

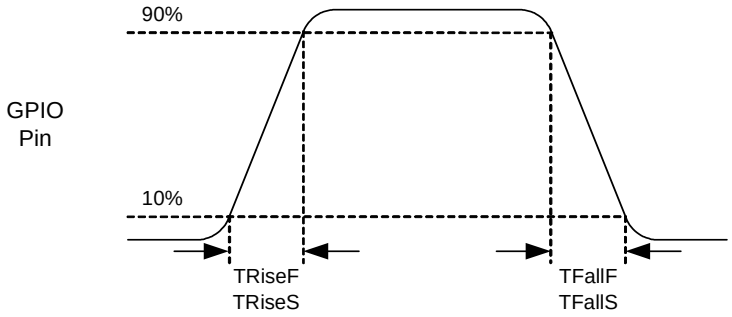



**Figure 3-7. GPIO Timing Diagram**

## 3.4.3 AC Operational Amplifier Specifications

The following tables list guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C ≤ $T_A$ ≤ 85°C, or 3.0V to 3.6V and -40°C ≤ $T_A$ ≤ 85°C, respectively. Typical parameters apply to 5V and 3.3V at 25°C and are for design guidance only or unless otherwise specified.

**Note** Settling times, slew rates, and gain bandwidth are based on the Analog Continuous Time PSoC block.

**Table 3-17. 5V AC Operational Amplifier Specifications**

| Symbol | Description | Min | Typ | Max | Units | Notes |
|---|---|---|---|---|---|---|
| $T_{ROA}$ | Rising Settling Time from 80% of ΔV to 0.1% of ΔV (10 pF load, Unity Gain) | | | | | Specification maximums for low power and high opamp bias, medium power, and medium power and high opamp bias levels are between low and high power levels. |
| | Power = Low | – | – | 3.9 | µs | |
| | Power = Low, Opamp Bias = High | – | | | µs | |
| | Power = Medium | – | | | µs | |
| | Power = Medium, Opamp Bias = High | – | – | 0.72 | µs | |
| | Power = High | – | | | µs | |
| | Power = High, Opamp Bias = High | – | – | 0.62 | µs | |
| $T_{SOA}$ | Falling Settling Time from 20% of ΔV to 0.1% of ΔV (10 pF load, Unity Gain) | | | | | Specification maximums for low power and high opamp bias, medium power, and medium power and high opamp bias levels are between low and high power levels. |
| | Power = Low | – | – | 5.9 | µs | |
| | Power = Low, Opamp Bias = High | – | | | µs | |
| | Power = Medium | – | | | µs | |
| | Power = Medium, Opamp Bias = High | – | – | 0.92 | µs | |
| | Power = High | – | | | µs | |
| | Power = High, Opamp Bias = High | – | – | 0.72 | µs | |
| $SR_{ROA}$ | Rising Slew Rate (20% to 80%)(10 pF load, Unity Gain) | | | | | Specification minimums for low power and high opamp bias, medium power, and medium power and high opamp bias levels are between low and high power levels. |
| | Power = Low | 0.15 | – | | V/µs | |
| | Power = Low, Opamp Bias = High | | | | V/µs | |
| | Power = Medium | | | | V/µs | |
| | Power = Medium, Opamp Bias = High | 1.7 | – | | V/µs | |
| | Power = High | | | | V/µs | |
| | Power = High, Opamp Bias = High | 6.5 | – | | V/µs | |
| $SR_{FOA}$ | Falling Slew Rate (20% to 80%)(10 pF load, Unity Gain) | | | | | Specification minimums for low power and high opamp bias, medium power, and medium power and high opamp bias levels are between low and high power levels. |
| | Power = Low | 0.01 | – | | V/µs | |
| | Power = Low, Opamp Bias = High | | | | V/µs | |
| | Power = Medium | | | | V/µs | |
| | Power = Medium, Opamp Bias = High | 0.5 | – | | V/µs | |
| | Power = High | | | | V/µs | |
| | Power = High, Opamp Bias = High | 4.0 | – | | V/µs | |
| $BW_{OA}$ | Gain Bandwidth Product | | | | | Specification minimums for low power and high opamp bias, medium power, and medium power and high opamp bias levels are between low and high power levels. |
| | Power = Low | 0.75 | – | | MHz | |
| | Power = Low, Opamp Bias = High | | | | MHz | |
| | Power = Medium | | | | MHz | |
| | Power = Medium, Opamp Bias = High | 3.1 | – | | MHz | |
| | Power = High | | | | MHz | |
| | Power = High, Opamp Bias = High | 5.4 | – | | MHz | |
| $E_{NOA}$ | Noise at 1 kHz (Power = Medium, Opamp Bias = High) | – | 200 | – | nV/rt-Hz | |

### Table 3-18. 3.3V AC Operational Amplifier Specifications

| Symbol | Description | Min | Typ | Max | Units | Notes |
|---|---|---|---|---|---|---|
| $T_{ROA}$ | Rising Settling Time from 80% of ΔV to 0.1% of ΔV (10 pF load, Unity Gain) | | | | | Specification maximums for low power and high opamp bias, medium power, and medium power and high opamp bias levels are between low and high power levels. |
| | Power = Low | – | – | 3.92 | µs | |
| | Power = Low, Opamp Bias = High | – | | | µs | |
| | Power = Medium | – | | | µs | |
| | Power = Medium, Opamp Bias = High | – | – | 0.72 | µs | |
| | Power = High (3.3 Volt High Bias Operation not supported) | – | – | – | µs | |
| | Power = High, Opamp Bias = High (3.3 Volt High Power, High Opamp Bias not supported) | – | – | – | µs | |
| $T_{SOA}$ | Falling Settling Time from 20% of ΔV to 0.1% of ΔV (10 pF load, Unity Gain) | | | | | Specification maximums for low power and high opamp bias, medium power, and medium power and high opamp bias levels are between low and high power levels. |
| | Power = Low | – | – | 5.41 | µs | |
| | Power = Low, Opamp Bias = High | – | | | µs | |
| | Power = Medium | – | | | µs | |
| | Power = Medium, Opamp Bias = High | – | – | 0.72 | µs | |
| | Power = High (3.3 Volt High Bias Operation not supported) | – | – | – | µs | |
| | Power = High, Opamp Bias = High (3.3 Volt High Power, High Opamp Bias not supported) | – | – | – | µs | |
| $SR_{ROA}$ | Rising Slew Rate (20% to 80%)(10 pF load, Unity Gain) | | | | | Specification minimums for low power and high opamp bias, medium power, and medium power and high opamp bias levels are between low and high power levels. |
| | Power = Low | 0.31 | – | | V/µs | |
| | Power = Low, Opamp Bias = High | | | | V/µs | |
| | Power = Medium | | | | V/µs | |
| | Power = Medium, Opamp Bias = High | 2.7 | – | | V/µs | |
| | Power = High (3.3 Volt High Bias Operation not supported) | – | – | – | V/µs | |
| | Power = High, Opamp Bias = High (3.3 Volt High Power, High Opamp Bias not supported) | – | – | – | V/µs | |
| $SR_{FOA}$ | Falling Slew Rate (20% to 80%)(10 pF load, Unity Gain) | | | | | Specification minimums for low power and high opamp bias, medium power, and medium power and high opamp bias levels are between low and high power levels. |
| | Power = Low | 0.24 | – | | V/µs | |
| | Power = Low, Opamp Bias = High | | | | V/µs | |
| | Power = Medium | | | | V/µs | |
| | Power = Medium, Opamp Bias = High | 1.8 | – | | V/µs | |
| | Power = High (3.3 Volt High Bias Operation not supported) | – | – | – | V/µs | |
| | Power = High, Opamp Bias = High (3.3 Volt High Power, High Opamp Bias not supported) | – | – | – | V/µs | |
| $BW_{OA}$ | Gain Bandwidth Product | | | | | Specification minimums for low power and high opamp bias, medium power, and medium power and high opamp bias levels are between low and high power levels. |
| | Power = Low | 0.67 | – | | MHz | |
| | Power = Low, Opamp Bias = High | | | | MHz | |
| | Power = Medium | | | | MHz | |
| | Power = Medium, Opamp Bias = High | 2.8 | – | | MHz | |
| | Power = High (3.3 Volt High Bias Operation not supported) | – | – | – | MHz | |
| | Power = High, Opamp Bias = High (3.3 Volt High Power, High Opamp Bias not supported) | – | – | – | MHz | |
| $E_{NOA}$ | Noise at 1 kHz (Power = Medium, Opamp Bias = High) | – | 200 | – | nV/rt-Hz | |

### 3.4.4 AC Digital Block Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C ≤ $T_A$ ≤ 85°C, or 3.0V to 3.6V and -40°C ≤ $T_A$ ≤ 85°C, respectively. Typical parameters apply to 5V and 3.3V at 25°C and are for design guidance only or unless otherwise specified.

**Table 3-19. AC Digital Block Specifications**

| Function | Description | Min | Typ | Max | Units | Notes |
|---|---|---|---|---|---|---|
| Timer | Capture Pulse Width | 50[a] | – | – | ns | |
| | Maximum Frequency, No Capture | – | – | 49.2 | MHz | 4.75V < Vdd < 5.25V. |
| | Maximum Frequency, With Capture | – | – | 24.6 | MHz | |
| Counter | Enable Pulse Width | 50[a] | – | – | ns | |
| | Maximum Frequency, No Enable Input | – | – | 49.2 | MHz | 4.75V < Vdd < 5.25V. |
| | Maximum Frequency, Enable Input | – | – | 24.6 | MHz | |
| Dead Band | Kill Pulse Width: | | | | | |
| | Asynchronous Restart Mode | 20 | – | – | ns | |
| | Synchronous Restart Mode | 50[a] | – | – | ns | |
| | Disable Mode | 50[a] | – | – | ns | |
| | Maximum Frequency | – | – | 49.2 | MHz | 4.75V < Vdd < 5.25V. |
| CRCPRS (PRS Mode) | Maximum Input Clock Frequency | – | – | 49.2 | MHz | 4.75V < Vdd < 5.25V. |
| CRCPRS (CRC Mode) | Maximum Input Clock Frequency | – | – | 24.6 | MHz | |
| SPIM | Maximum Input Clock Frequency | – | – | 8.2 | MHz | |
| SPIS | Maximum Input Clock Frequency | – | – | 4.1 | ns | |
| | Width of SS_ Negated Between Transmissions | 50[a] | – | – | ns | |
| Transmitter | Maximum Input Clock Frequency | – | – | 16.4 | MHz | |
| Receiver | Maximum Input Clock Frequency | – | 16 | 49.2 | MHz | 4.75V < Vdd < 5.25V. |

a. 50 ns minimum input pulse width is based on the input synchronizers running at 24 MHz (42 ns nominal period).

## 3.4.5 AC Analog Output Buffer Specifications

The following tables list guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C ≤ $T_A$ ≤ 85°C, or 3.0V to 3.6V and -40°C ≤ $T_A$ ≤ 85°C, respectively. Typical parameters apply to 5V and 3.3V at 25°C and are for design guidance only or unless otherwise specified.

**Table 3-20. 5V AC Analog Output Buffer Specifications**

| Symbol | Description | Min | Typ | Max | Units | Notes |
|---|---|---|---|---|---|---|
| $T_{ROB}$ | Rising Settling Time to 0.1%, 1V Step, 100pF Load | | | | | |
| | Power = Low | – | – | 2.5 | µs | |
| | Power = High | – | – | 2.5 | µs | |
| $T_{SOB}$ | Falling Settling Time to 0.1%, 1V Step, 100pF Load | | | | | |
| | Power = Low | – | – | 2.2 | µs | |
| | Power = High | – | – | 2.2 | µs | |
| $SR_{ROB}$ | Rising Slew Rate (20% to 80%), 1V Step, 100pF Load | | | | | |
| | Power = Low | 0.65 | – | – | V/µs | |
| | Power = High | 0.65 | – | – | V/µs | |
| $SR_{FOB}$ | Falling Slew Rate (80% to 20%), 1V Step, 100pF Load | | | | | |
| | Power = Low | 0.65 | – | – | V/µs | |
| | Power = High | 0.65 | – | – | V/µs | |
| $BW_{OB}$ | Small Signal Bandwidth, 20m$V_{pp}$, 3dB BW, 100pF Load | | | | | |
| | Power = Low | 0.8 | – | – | MHz | |
| | Power = High | 0.8 | – | – | MHz | |
| $BW_{OB}$ | Large Signal Bandwidth, 1$V_{pp}$, 3dB BW, 100pF Load | | | | | |
| | Power = Low | 300 | – | – | kHz | |
| | Power = High | 300 | – | – | kHz | |

**Table 3-21. 3.3V AC Analog Output Buffer Specifications**

| Symbol | Description | Min | Typ | Max | Units | Notes |
|---|---|---|---|---|---|---|
| $T_{ROB}$ | Rising Settling Time to 0.1%, 1V Step, 100pF Load | | | | | |
| | Power = Low | – | – | 3.8 | µs | |
| | Power = High | – | – | 3.8 | µs | |
| $T_{SOB}$ | Falling Settling Time to 0.1%, 1V Step, 100pF Load | | | | | |
| | Power = Low | – | – | 2.6 | µs | |
| | Power = High | – | – | 2.6 | µs | |
| $SR_{ROB}$ | Rising Slew Rate (20% to 80%), 1V Step, 100pF Load | | | | | |
| | Power = Low | 0.5 | – | – | V/µs | |
| | Power = High | 0.5 | – | – | V/µs | |
| $SR_{FOB}$ | Falling Slew Rate (80% to 20%), 1V Step, 100pF Load | | | | | |
| | Power = Low | 0.5 | – | – | V/µs | |
| | Power = High | 0.5 | – | – | V/µs | |
| $BW_{OB}$ | Small Signal Bandwidth, 20m$V_{pp}$, 3dB BW, 100pF Load | | | | | |
| | Power = Low | 0.7 | – | – | MHz | |
| | Power = High | 0.7 | – | – | MHz | |
| $BW_{OB}$ | Large Signal Bandwidth, 1$V_{pp}$, 3dB BW, 100pF Load | | | | | |
| | Power = Low | 200 | – | – | kHz | |
| | Power = High | 200 | – | – | kHz | |

## 3.4.6 AC External Clock Specifications

The following tables list guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C ≤ $T_A$ ≤ 85°C, or 3.0V to 3.6V and -40°C ≤ $T_A$ ≤ 85°C, respectively. Typical parameters apply to 5V and 3.3V at 25°C and are for design guidance only or unless otherwise specified.

**Table 3-22. 5V AC External Clock Specifications**

| Symbol | Description | Min | Typ | Max | Units | Notes |
|---|---|---|---|---|---|---|
| $F_{OSCEXT}$ | Frequency | 0 | – | 24.24 | MHz | |
| – | High Period | 20.6 | – | – | ns | |
| – | Low Period | 20.6 | – | – | ns | |
| – | Power Up IMO to Switch | 150 | – | – | µs | |

**Table 3-23. 3.3V AC External Clock Specifications**

| Symbol | Description | Min | Typ | Max | Units | Notes |
|---|---|---|---|---|---|---|
| $F_{OSCEXT}$ | Frequency with CPU Clock divide by 1[a] | 0 | – | 12.12 | MHz | |
| $F_{OSCEXT}$ | Frequency with CPU Clock divide by 2 or greater[b] | 0 | – | 24.24 | MHz | |
| – | High Period with CPU Clock divide by 1 | 41.7 | – | – | ns | |
| – | Low Period with CPU Clock divide by 1 | 41.7 | – | – | ns | |
| – | Power Up IMO to Switch | 150 | – | – | µs | |

a. Maximum CPU frequency is 12 MHz at 3.3V. With the CPU clock divider set to 1, the external clock must adhere to the maximum frequency and duty cycle requirements.
b. If the frequency of the external clock is greater than 12 MHz, the CPU clock divider must be set to 2 or greater. In this case, the CPU clock divider will ensure that the fifty percent duty cycle requirement is met.

## 3.4.7 AC Programming Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C ≤ $T_A$ ≤ 85°C, or 3.0V to 3.6V and -40°C ≤ $T_A$ ≤ 85°C, respectively. Typical parameters apply to 5V and 3.3V at 25°C and are for design guidance only or unless otherwise specified.

**Table 3-24. AC Programming Specifications**

| Symbol | Description | Min | Typ | Max | Units | Notes |
|---|---|---|---|---|---|---|
| $T_{RSCLK}$ | Rise Time of SCLK | 1 | – | 20 | ns | |
| $T_{FSCLK}$ | Fall Time of SCLK | 1 | – | 20 | ns | |
| $T_{SSCLK}$ | Data Set up Time to Falling Edge of SCLK | 40 | – | – | ns | |
| $T_{HSCLK}$ | Data Hold Time from Falling Edge of SCLK | 40 | – | – | ns | |
| $F_{SCLK}$ | Frequency of SCLK | 0 | – | 8 | MHz | |
| $T_{ERASEB}$ | Flash Erase Time (Block) | – | 15 | – | ms | |
| $T_{WRITE}$ | Flash Block Write Time | – | 30 | – | ms | |
| $T_{DSCLK}$ | Data Out Delay from Falling Edge of SCLK | – | – | 45 | ns | |

## 3.4.8 AC I²C Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C ≤ $T_A$ ≤ 85°C, or 3.0V to 3.6V and -40°C ≤ $T_A$ ≤ 85°C, respectively. Typical parameters apply to 5V and 3.3V at 25°C and are for design guidance only or unless otherwise specified.

**Table 3-25. AC Characteristics of the I²C SDA and SCL Pins**

| Symbol | Description | Standard Mode | | Fast Mode | | Units | Notes |
|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | | |
| $F_{SCLI2C}$ | SCL Clock Frequency | 0 | 100 | 0 | 400 | kHz | |
| $T_{HDSTAI2C}$ | Hold Time (repeated) START Condition. After this period, the first clock pulse is generated. | 4.0 | – | 0.6 | – | µs | |
| $T_{LOWI2C}$ | LOW Period of the SCL Clock | 4.7 | – | 1.3 | – | µs | |
| $T_{HIGHI2C}$ | HIGH Period of the SCL Clock | 4.0 | – | 0.6 | – | µs | |
| $T_{SUSTAI2C}$ | Set-up Time for a Repeated START Condition | 4.7 | – | 0.6 | – | µs | |
| $T_{HDDATI2C}$ | Data Hold Time | 0 | – | 0 | – | µs | |
| $T_{SUDATI2C}$ | Data Set-up Time | 250 | – | 100[a] | – | ns | |
| $T_{SUSTOI2C}$ | Set-up Time for STOP Condition | 4.0 | – | 0.6 | – | µs | |
| $T_{BUFI2C}$ | Bus Free Time Between a STOP and START Condition | 4.7 | – | 1.3 | – | µs | |
| $T_{SPI2C}$ | Pulse Width of spikes are suppressed by the input filter. | – | – | 0 | 50 | ns | |

a. A Fast-Mode I2C-bus device can be used in a Standard-Mode I2C-bus system, but the requirement $t_{SU;DAT} \geq 250$ ns must then be met. This will automatically be the case if the device does not stretch the LOW period of the SCL signal. If such device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line $t_{rmax} + t_{SU;DAT} = 1000 + 250 = 1250$ ns (according to the Standard-Mode I2C-bus specification) before the SCL line is released.

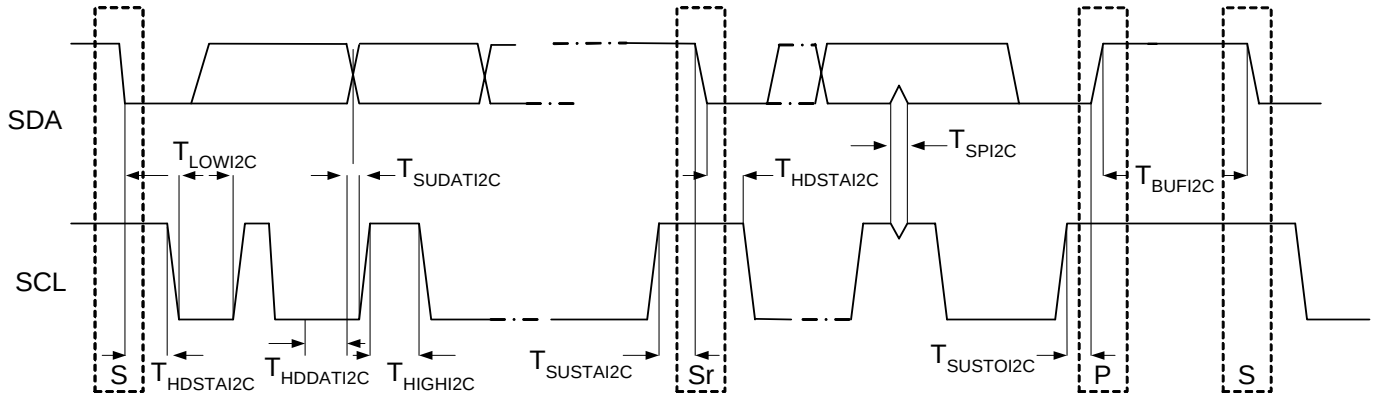



**Figure 3-8. Definition for Timing for Fast/Standard Mode on the I²C Bus**

# 4. Packaging Information

This chapter illustrates the packaging specifications for the CY8C22x13 PSoC device, along with the thermal impedances for each package and the typical package capacitance on crystal pins.

## 4.1 Packaging Dimensions

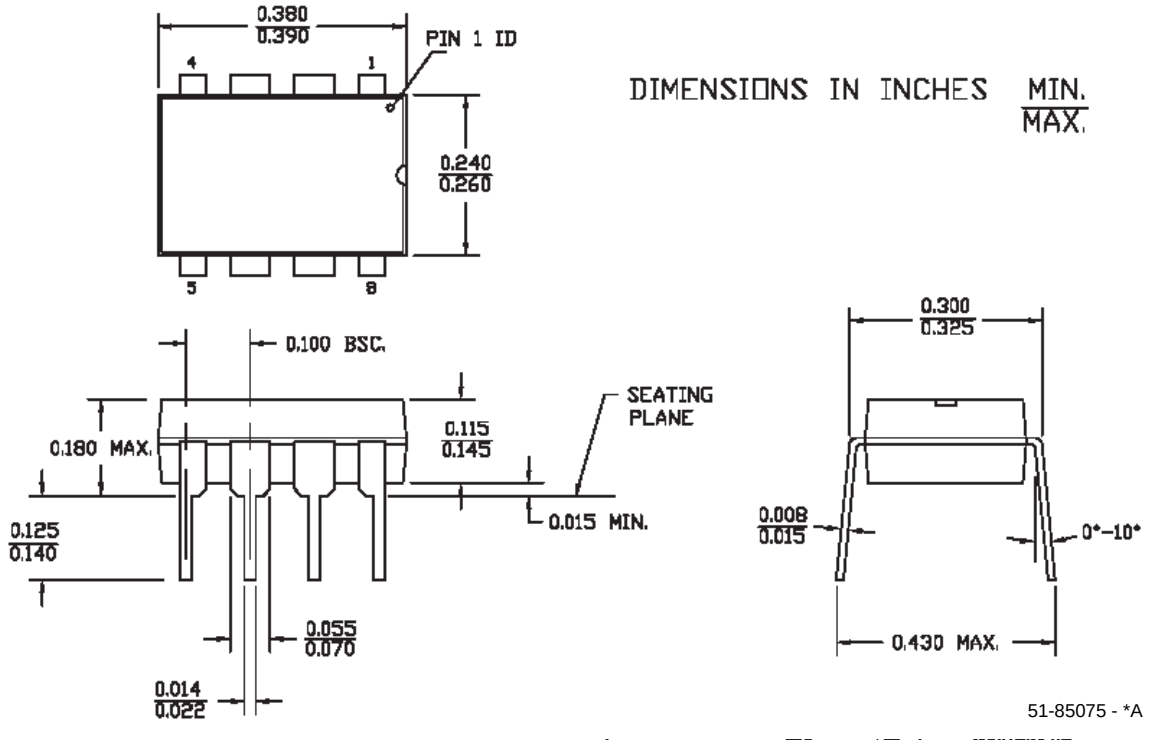



**Figure 4-1. 8-Lead (300-Mil) PDIP**

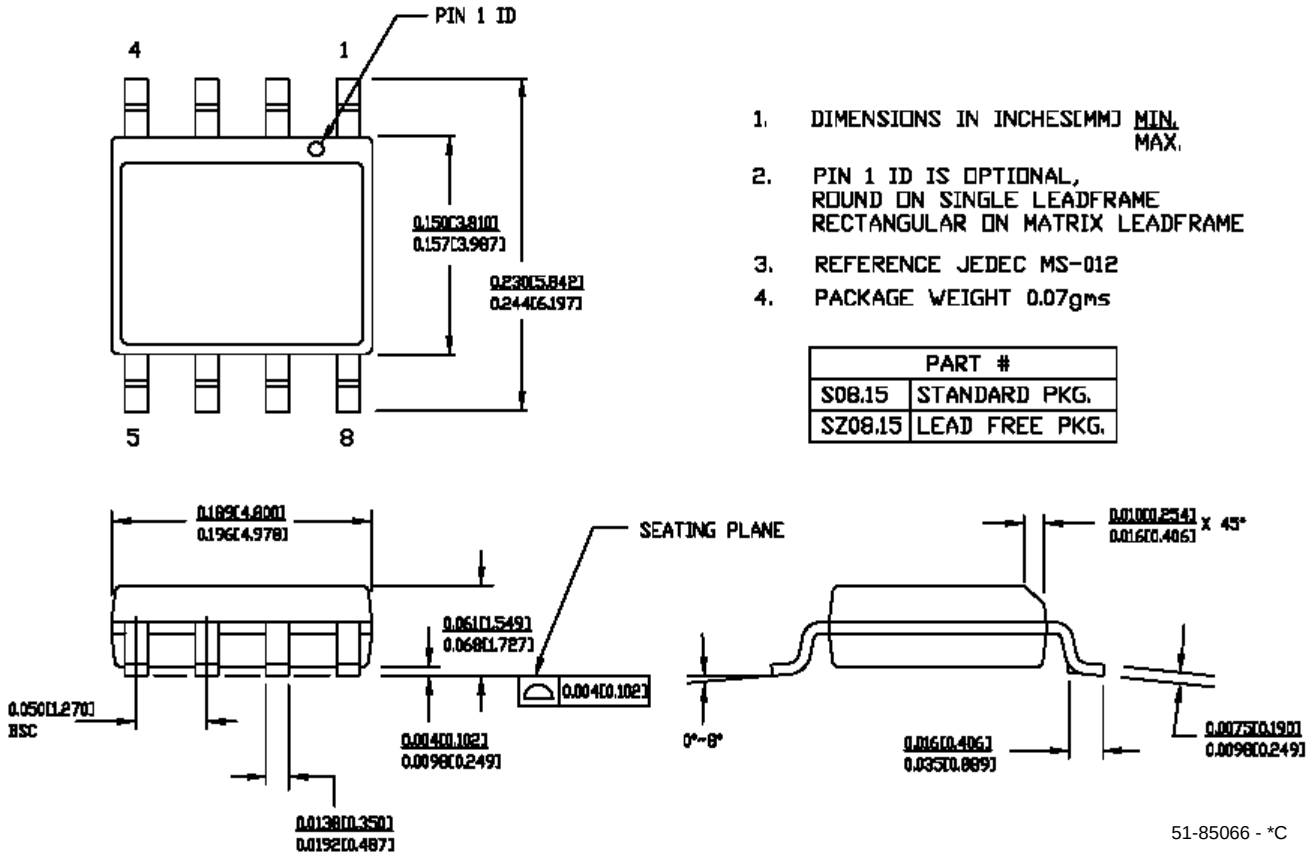



**Figure 4-2. 8-Lead (150-Mil) SOIC**

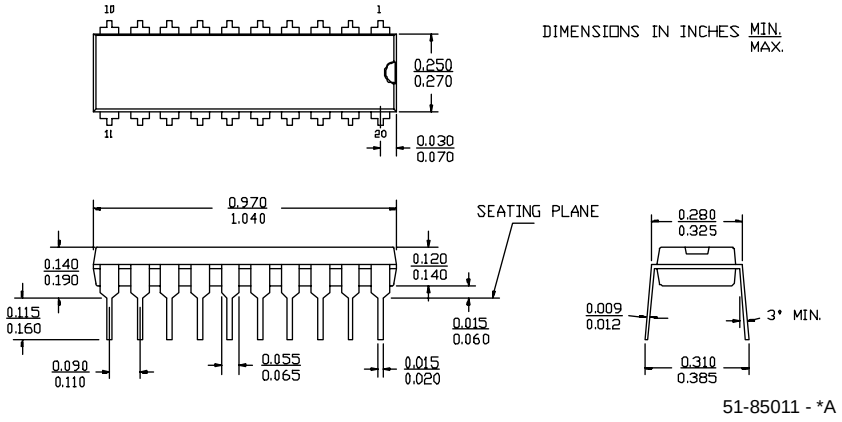



**Figure 4-3. 20-Lead (300-Mil) Molded DIP**

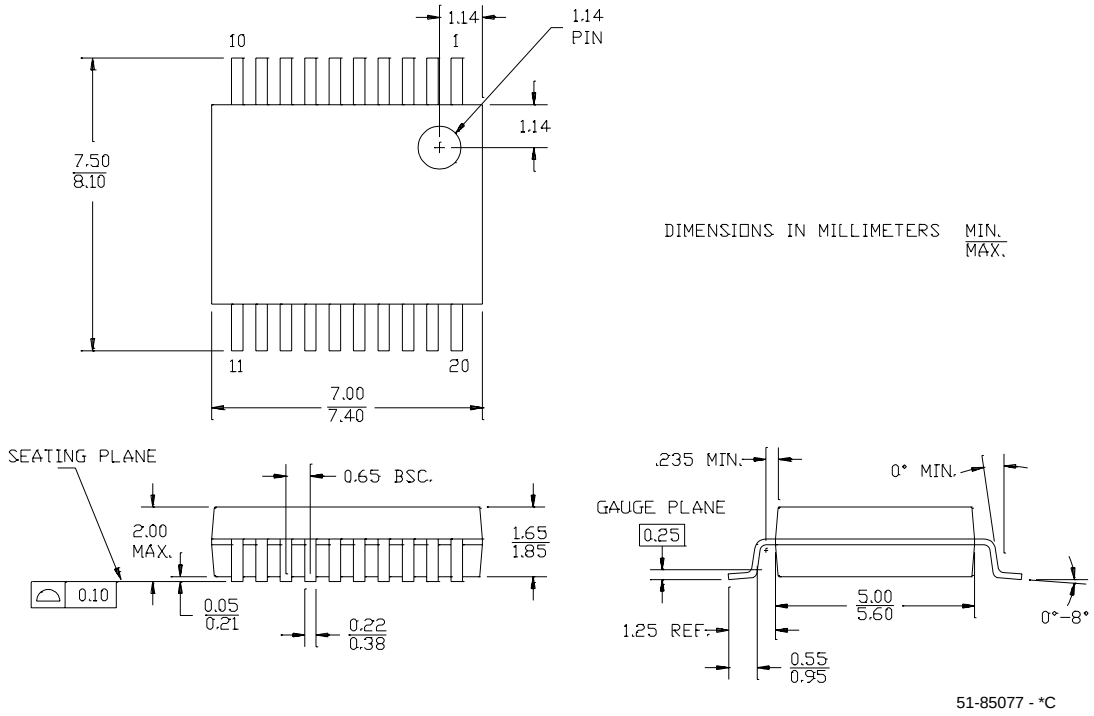



**Figure 4-4. 20-Lead (210-Mil) SSOP**

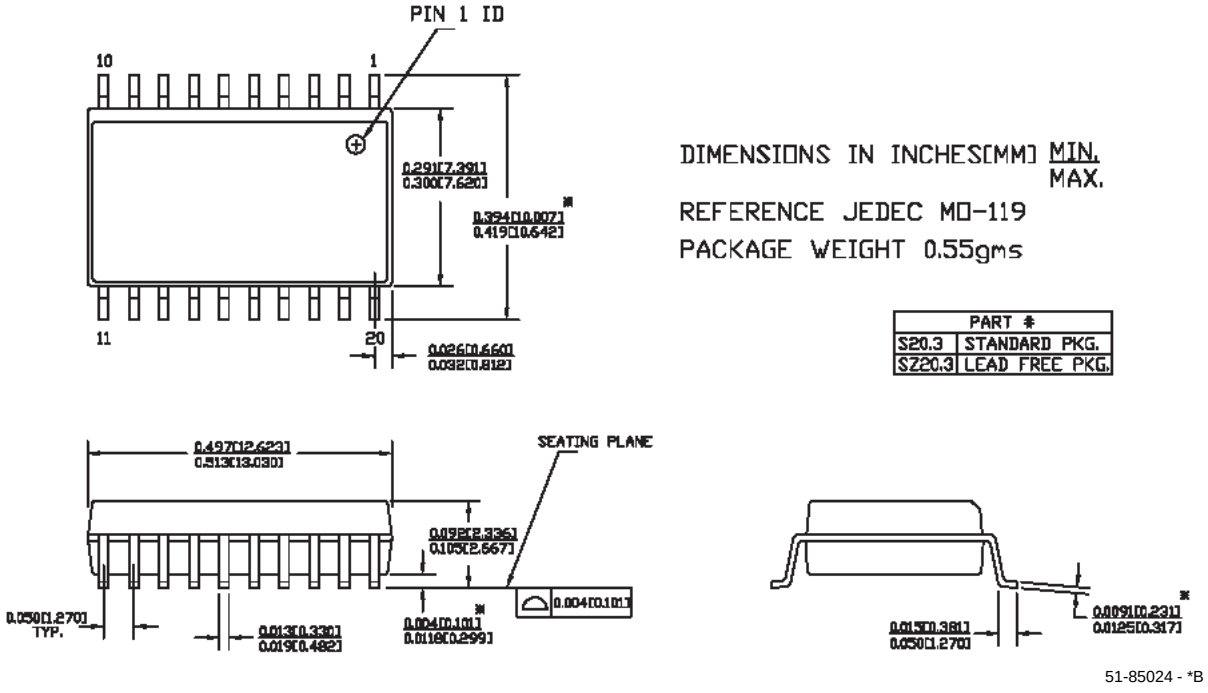



**Figure 4-5. 20-Lead (300-Mil) Molded SOIC**

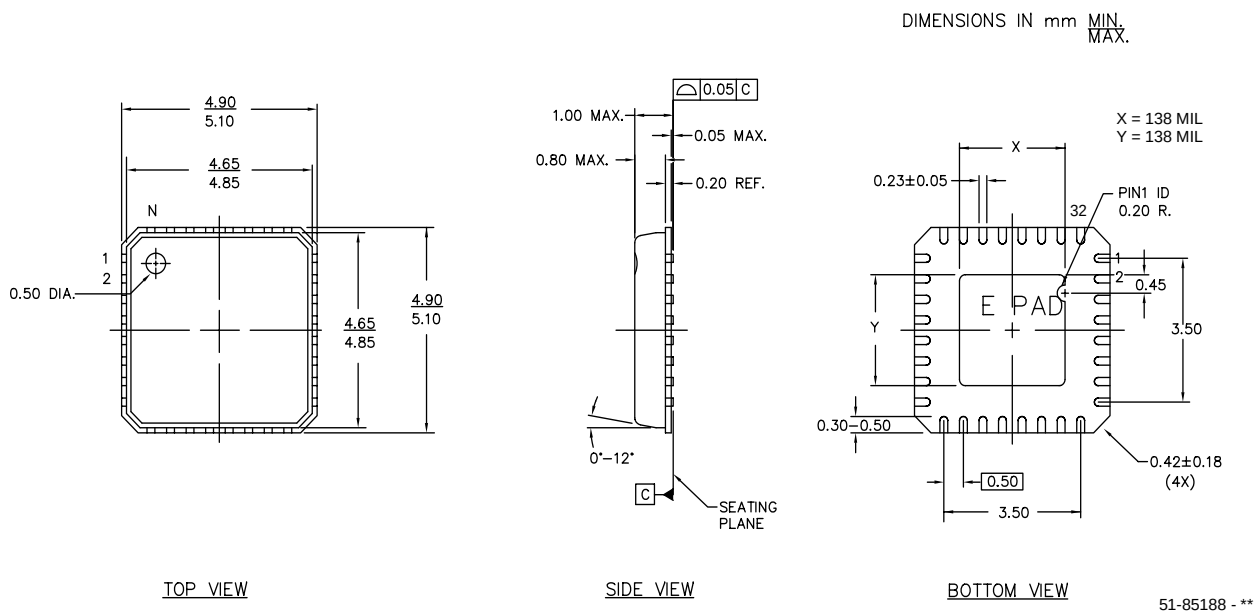



**Figure 4-6. 32-Lead (5x5 mm) MLF**

## 4.2 Thermal Impedances

**Table 4-1. Thermal Impedances per Package**

| Package | Typical $\theta_{JA}$ * |
|---|---|
| 8 PDIP | 123 °C/W |
| 8 SOIC | 185 °C/W |
| 20 PDIP | 109 °C/W |
| 20 SSOP | 117 °C/W |
| 20 SOIC | 81 °C/W |
| 32 MLF | 22 °C/W |

* $T_J = T_A + POWER \times \theta_{JA}$

## 4.3 Capacitance on Crystal Pins

**Table 4-2: Typical Package Capacitance on Crystal Pins**

| Package | Package Capacitance |
|---|---|
| 8 PDIP | 2.8 pF |
| 8 SOIC | 2.0 pF |
| 20 PDIP | 3.0 pF |
| 20 SSOP | 2.6 pF |
| 20 SOIC | 2.5 pF |
| 32 MLF | 2.0 pF |

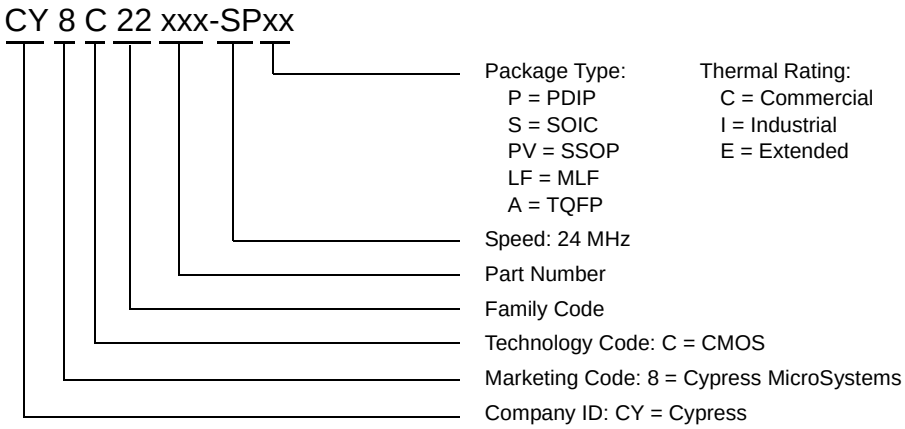
# 5. Ordering Information

The following table lists the CY8C22x13 PSoC Device family's key package features and ordering codes.

**Table 5-1. CY8C22x13 PSoC Device Family Key Features and Ordering Information**

| Package | Ordering Code | Flash (Kbytes) | RAM (Bytes) | Switch Mode Pump | Temperature Range | Digital Blocks (Rows of 4) | Analog Blocks (Columns of 3) | Digital IO Pins | Analog Inputs | Analog Outputs | XRES Pin |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 8 Pin (300 Mil) DIP | CY8C22113-24PI | 2 | 256 | No | -40C to +85C | 4 | 3 | 6 | 4 | 1 | No |
| 8 Pin (150 Mil) SOIC | CY8C22113-24SI | 2 | 256 | No | -40C to +85C | 4 | 3 | 6 | 4 | 1 | No |
| 8 Pin (150 Mil) SOIC (Tape and Reel) | CY8C22113-24SIT | 2 | 256 | No | -40C to +85C | 4 | 3 | 6 | 4 | 1 | No |
| 20 Pin (300 Mil) DIP | CY8C22213-24PI | 2 | 256 | No | -40C to +85C | 4 | 3 | 16 | 8 | 1 | Yes |
| 20 Pin (210 Mil) SSOP | CY8C22213-24PVI | 2 | 256 | No | -40C to +85C | 4 | 3 | 16 | 8 | 1 | Yes |
| 20 Pin (210 Mil) SSOP (Tape and Reel) | CY8C22213-24PVIT | 2 | 256 | No | -40C to +85C | 4 | 3 | 16 | 8 | 1 | Yes |
| 20 Pin (300 Mil) SOIC | CY8C22213-24SI | 2 | 256 | No | -40C to +85C | 4 | 3 | 16 | 8 | 1 | Yes |
| 20 Pin (300 Mil) SOIC (Tape and Reel) | CY8C22213-24SIT | 2 | 256 | No | -40C to +85C | 4 | 3 | 16 | 8 | 1 | Yes |
| 32 Pin (5x5 mm) MLF | CY8C22213-24LFI | 2 | 256 | No | -40C to +85C | 4 | 3 | 16 | 8 | 1 | Yes |

## 5.1 Ordering Code Definitions



# 6. Sales and Company Information

To obtain information about Cypress MicroSystems or PSoC sales and technical support, reference the following information or go to the section titled “Getting Started” on page 4 in this document.

**Cypress MicroSystems**
2700 162nd Street SW
Building D
Lynnwood, WA 98037

Phone: 800.669.0557
Facsimile: 425.787.4641

Web Sites: Company Information – http://www.cypress.com
Sales – http://www.cypress.com/aboutus/sales_locations.cfm
Technical Support – http://www.cypress.com/support/login.cfm

## 6.1 Revision History

**Table 6-1. CY8C22x13 Data Sheet Revision History**

| Document Title: CY8C22113 and CY8C22213 PSoC Mixed Signal Array Final Data Sheet<br>Document Number: 38-12009 | | | | |
|---|---|---|---|---|
| **Revision** | **ECN #** | **Issue Date** | **Origin of Change** | **Description of Change** |
| ** | 128180 | 06/30/2003 | New Silicon. | New document – Advanced Data Sheet (two page product brief). |
| *A | 129202 | 09/16/2003 | NWJ | New document – Preliminary Data Sheet (300 page product detail). |
| *B | 130127 | 10/15/2003 | NWJ | Revised document for Silicon Revision A. |
| *C | 131679 | 12/05/2003 | NWJ | Changes to Electrical Specifications section, Miscellaneous changes to I2C, GDI, RDI, Registers, and Digital Block chapters. |
| *D | 131803 | 12/22/2003 | NWJ | Changes to Electrical Specifications and miscellaneous small changes throughout the data sheet. |
| *E | 229421 | 06/03/2004 | SFV | New data sheet format and organization. Reference the *PSoC Mixed Signal Array Technical Reference Manual* for additional information. Title change. |
| **Distribution**: External/Public | | | **Posting**: None | |

## 6.2 Copyrights

TradeElectronics.ru

гарантия бесперебойности производства и качества выпускаемой продукции

## О компании

ООО "ТрейдЭлектроникс" - это оперативные поставки широкого спектра электронных компонентов отечественного и импортного производства напрямую от производителей и с крупнейших мировых складов. Реализуемая нашей компанией продукция насчитывает более полумиллиона наименований.

Благодаря этому наша компания предлагает к поставке практически не ограниченный ассортимент компонентов как оптовыми, мелкооптовыми партиями, так и в розницу.

Наличие собственной эффективной системы логистики обеспечивает надежную поставку продукции по конкурентным ценам в точно указанные сроки.

Срок поставки со стоков в **Европе и Америке – от 3 до 14 дней.**

Срок поставки из **Азии – от 10 дней.**

Благодаря развитой сети поставщиков, помогаем в поиске и приобретении экзотичных или снятых с производства компонентов.

Предоставляем спец цены на элементы для создания инженерных сэмплов.

**Упорный труд, качественный результат дают нам право быть уверенными в себе и надежными для наших клиентов.**

## Наша компания это:

- Гарантия качества поставляемой продукции
- Широкий ассортимент
- Минимальные сроки поставок
- Техническая поддержка
- Подбор комплектации
- Индивидуальный подход
- Гибкое ценообразование

Наша организация особенно сильна в поставках модулей, микросхем, пассивных компонентов, ксайленсах (XC), EPF, EPM и силовой электроники.

Большой выбор предлагаемой продукции, различные виды оплаты и доставки, позволят Вам сэкономить время и получить максимум выгоды от сотрудничества с нами!

Trade Electronics.ru

гарантия бесперебойности производства и качества выпускаемой продукции

## Перечень производителей, продукцию которых мы поставляем на российский рынок

Trade Electronics.ru

гарантия бесперебойности производства и качества выпускаемой продукции

С удовольствием будем прорабатывать для Вас поставки всех необходимых компонентов по текущим запросам для скорейшего выявления групп элементов, по которым сотрудничество именно с нашей компанией будет для Вас максимально выгодным!

С уважением,

Менеджер отдела продаж ООО

«Трейд Электроникс»

Шишлаков Евгений

8 (495)668-30-28 доб 169

manager28@tradeelectronics.ru

http://www.tradeelectronics.ru/