

# AMMC-5033

## 17.7 - 32 GHz Power Amplifier



### Data Sheet



Chip Size: 2730 x 1300  $\mu\text{m}$  (108 x 51.6 mils)  
Chip Size Tolerance:  $\pm 10 \mu\text{m}$  ( $\pm 0.4$  mils)  
Chip Thickness: 100  $\pm 10 \mu\text{m}$  ( $4 \pm 0.4$  mils)  
Pad Dimensions: 80 x 80  $\mu\text{m}$  ( $2.95 \pm 0.4$  mils)

### Description

Avago's AMMC-5033 is a MMIC power amplifier designed for use in wireless transmitters that operate within 17.7 GHz to 32 GHz range. At 25 GHz, it provides 27 dBm of output power (P-1dB) and 20 dB of small-signal gain from a small easy-to-use device. The device has input and output matching circuitry for use in 50  $\Omega$  environments. The AMMC-5033 also integrates a temperature compensated RF power detection circuit that enables power detection of 0.1V/W at 22 GHz. For improved reliability and moisture protection, the die is passivated at the active areas.

### AMMC-5033 Absolute Maximum Ratings<sup>[1]</sup>

Symbol	Parameters/Conditions	Units	Min.	Max.
$V_{d1,2}$	Positive Drain Voltage	V		7
$V_{g1}, V_{gg}$	Gate Supply Voltage	V	-3	0.5
Det Bias	Applied Detector Bias (Optional)	V		7
$I_{d1}$	First Stage Drain Current	mA		320
$I_{d2}$	Second Stage Drain Current	mA		640
$P_{in}$	CW Input Power	dBm		23
$T_{ch}$	Operating Channel Temp.	$^{\circ}\text{C}$		+150
$T_{stg}$	Storage Case Temp.	$^{\circ}\text{C}$	-65	+150
$T_{max}$	Maximum Assembly Temp. (60 sec max)	$^{\circ}\text{C}$		+300

#### Note:

1. Operation in excess of any one of these conditions may result in permanent damage to this device.

### Features

- Wide frequency range: 17.7 – 32 GHz
- High power: P-1dB @ 25 GHz = 27 dBm
- High gain: 20 dB
- Return loss: Input: -13 dB, Output: -20 dB
- Integrated RF power detector

### Applications

- Designed for use in transmitters that operate in various frequency bands between 17.7 GHz and 32 GHz.
- Can be driven by the AMMC-5040 (20-40 GHz) or the AMMC-5618 (6-20 GHz) MMIC amplifiers, increasing the power handling capability of transmitters requiring linear operation.

*Note: These devices are ESD sensitive. The following precautions are strongly recommended: Ensure that an ESD approved carrier is used when dice are transported from one destination to another. Personal grounding is to be worn at all times when handling these devices.*

## AMMC-5033 DC Specifications/Physical Properties<sup>[1]</sup>

Symbol	Parameters and Test Conditions	Units	Min.	Typ.	Max.
$I_{d1}$	First Stage Drain Supply Current ( $V_{d1} = 3.5\text{ V}$ , $V_{g1} = \text{Open}$ , $V_{gg}$ set for $I_{d2}$ Typical)	mA		280	320
$I_{d2}$	Second Stage Drain Supply Current ( $V_{d2} = 5\text{ V}$ , $V_{g1} = \text{Open}$ , $V_{gg}$ set for $I_{d2}$ Typical)	V		500	
V <sub>gg</sub>	Gate Supply Operating Voltage ( $I_{d1(Q)} + I_{d2(Q)} = 780\text{ (mA)}$ )	V	-0.95	-0.6	-0.4
DETBias	Detector Bias Voltage (Optional)	V		V <sub>d2</sub>	
$\theta_{c1(\text{ch-bs})}$	First Stage Thermal Resistance <sup>[2]</sup> (Backside Temperature, $T_b = 25^\circ\text{C}$ )	$^\circ\text{C/W}$		31	
$\theta_{c2(\text{ch-bs})}$	Second Stage Thermal Resistance <sup>[2, 3]</sup> (Backside Temperature, $T_b = 25^\circ\text{C}$ )	$^\circ\text{C/W}$		19	

### Notes:

1. Backside temperature  $T_b = 25^\circ\text{C}$  unless otherwise noted.
2. Channel-to-backside Thermal Resistance ( $\theta_{\text{ch-b}}$ ) =  $42^\circ\text{C/W}$  at Tchannel ( $T_c$ ) =  $150^\circ\text{C}$  as measured using infrared microscopy. Thermal Resistance at backside temperature ( $T_b$ ) =  $25^\circ\text{C}$  calculated from measured data.

## AMMC-5033 RF Specifications<sup>[4, 5]</sup>

$T_b = 25^\circ\text{C}$ ,  $V_{d1} = 3.5\text{ V}$ ,  $V_{d2} = 5\text{ V}$ ,  $I_{d1(Q)} = 280\text{ mA}$ ,  $I_{d2(Q)} = 500\text{ mA}$ ,  $Z_o = 50\ \Omega$

Symbol	Parameters and Test Condition	Unit	Lower Band Specifications (17.7 - 21 GHz)			Mid Band Specifications (21 - 26.5 GHz)		Upper Band Specifications (26.5 - 32 GHz)		
			Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.
Gain	Small-Signal Gain <sup>[5]</sup>	dB	20	22		17.5	20		16.5	18.5
$P_{-1\text{dB}}$	Output Power at 1dB Gain Compression <sup>[6]</sup>	dB	23.5	25		25.5	27		25	26.5
$P_{-3\text{dB}}$	Output Power at 3dB Gain Compression <sup>[6]</sup>	dB		27			28			27
$\text{OIP}_3$	Output Third Order Intercept Point <sup>[6]</sup> ; $\Delta f = 2\text{ MHz}$ ; Pin = +2 dBm	dBm	27	29		29	32		29	32
$\text{RL}_{\text{in}}$	Input Return Loss <sup>[5]</sup>	dB	11.5	13.5		11	13		11	13
$\text{RL}_{\text{out}}$	Output Return Loss <sup>[5]</sup>	dB	14	20		14	19		15	22
Isolation	Min. Reverse Isolation	dB		47			48			46

### Notes:

4. Data measured in wafer form  $T_b = 25^\circ\text{C}$ .
5. 100% on-wafer RF test is done at frequency = 17.7, 21, 26.5 and 32 GHz.
6. 100% on-wafer test frequency = 17.7, 26.5 and 32 GHz.

## AMMC-5033 Typical Performances

( $T_b = 25^\circ\text{C}$ ,  $V_{d1} = 3.5\text{ V}$ ,  $I_{D1} = 280\text{ mA}$ ,  $V_{d2} = 5\text{ V}$ ,  $I_{D2} = 500\text{ mA}$ ,  $Z_{in} = Z_{out} = 50\ \Omega$ )

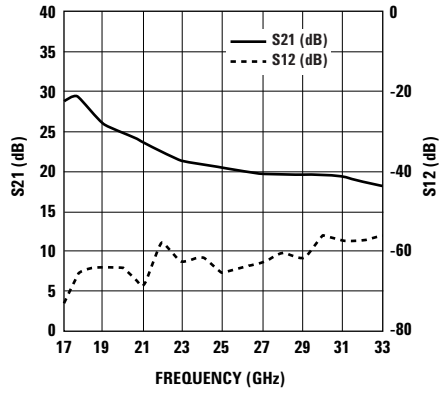


Figure 1. Gain and reverse isolation

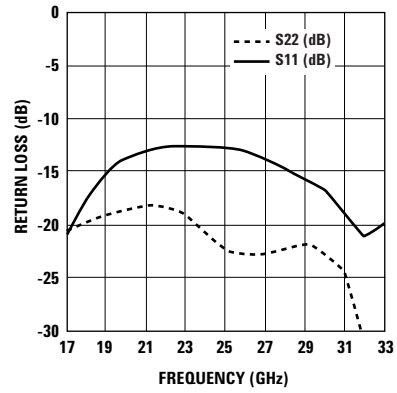


Figure 2. Return loss (input and output)

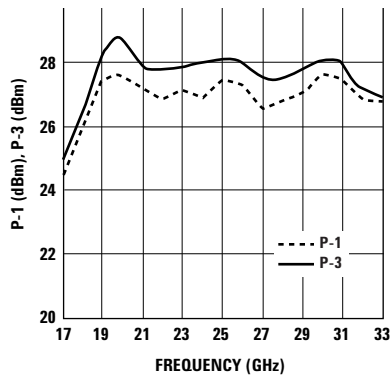


Figure 3. Output power at 1 dB and 3 dB gain compression

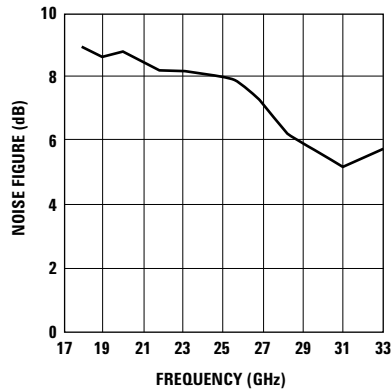


Figure 4. Noise figure

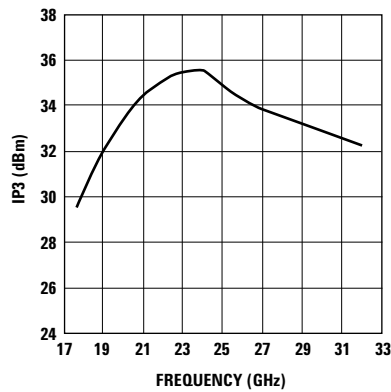


Figure 5. Output 3rd order intercept point

# AMMC-5033 Typical Performance Curves (Over Temperature and Voltage)

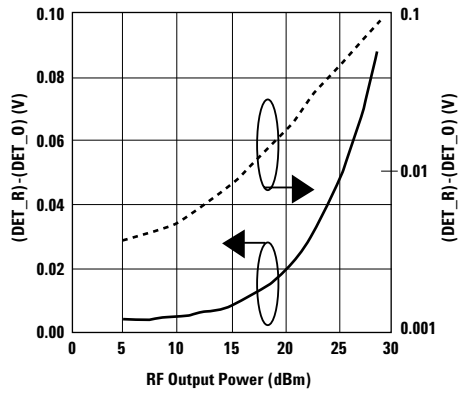


Figure 6. Linear and log detector voltage and output power, freq. = 22 GHz, Det\_B = 5 V

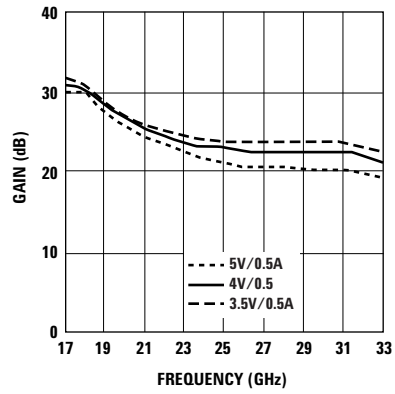


Figure 7. Gain and  $V_{d2}$  voltage,  $V_{d1} = 3.5 V$  (constant)

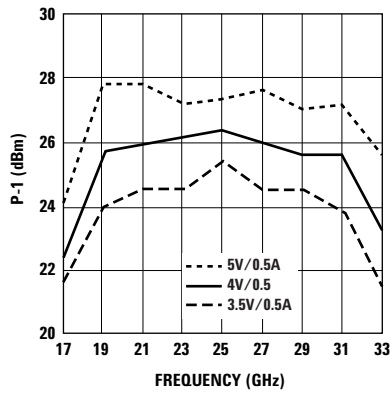


Figure 8. Output power at 1 dB gain compression and  $V_{d2}$  voltage,  $V_{d1} = 3.5 V$  (constant)

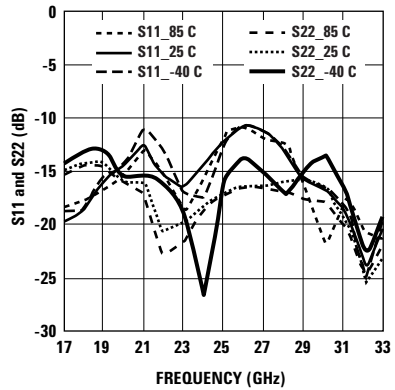


Figure 9. Return-loss with temperature

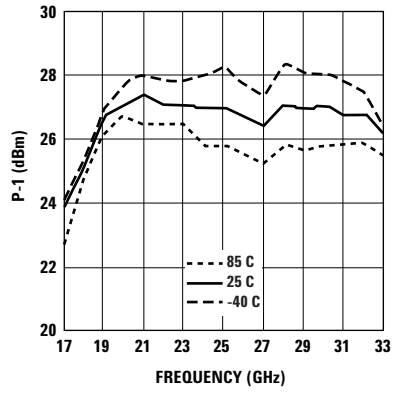


Figure 10. Output power at 1 dB gain compression and temperature

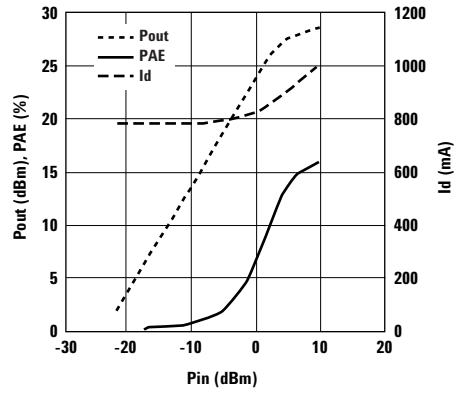


Figure 11. Output power, PAE, and total drain current vs. input power at 25 GHz

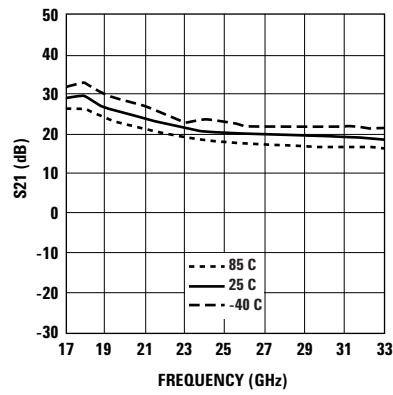


Figure 12. Gain with temperature

## Typical Scattering Parameters<sup>[1]</sup>

( $T_b = 25^\circ\text{C}$ ,  $V_{d1} = 3.5\text{ V}$ ,  $I_{D1} = 280\text{ mA}$ ,  $V_{d2} = 5\text{ V}$ ,  $I_{D2} = 500\text{ mA}$ ,  $Z_{in} = Z_{out} = 50\ \Omega$ )

Freq [GHz]	S11			S21			S12			S22		
	dB	Mag	Phase	dB	Mag	Phase	dB	Mag	Phase	dB	Mag	Phase
1	-10.7	0.29	173	-51.1	0.003	-163	-95.1	1.77E-05	128	-0.5	0.95	-26
2	-11.0	0.28	167	-70.1	0	79	-83.1	6.97E-05	76	-0.7	0.92	-51
3	-11.4	0.27	161	-46.6	0.005	-103	-74.5	1.89E-04	81	-1.2	0.87	-76
4	-12.1	0.25	153	-37.3	0.014	72	-74.5	1.88E-04	69	-2.2	0.78	-95
5	-15.3	0.17	140	-22.6	0.074	-31	-80.3	9.66E-05	-47	-2.4	0.76	-112
6	-12.2	0.25	149	-20.4	0.096	144	-80.1	9.90E-05	-126	-2.8	0.73	-130
7	-14.0	0.2	143	-20.5	0.095	79	-80.3	9.68E-05	94	-4.0	0.63	-146
8	-15.3	0.17	139	-25.4	0.053	-3	-74.1	1.97E-04	35	-4.2	0.62	-150
9	-17.6	0.13	138	-33.1	0.022	108	-81.4	8.52E-05	-62	-3.5	0.67	-166
10	-19.4	0.11	145	-18.9	0.113	54	-81.4	8.56E-05	-162	-3.8	0.64	177
11	-18.6	0.12	152	-18.2	0.123	-37	-81.3	8.59E-05	151	-4.4	0.6	161
12	-19.7	0.1	141	-29.0	0.035	-77	-74.6	1.86E-04	178	-5.2	0.55	146
13	-24.5	0.06	134	-15.4	0.169	103	-81.3	8.65E-05	-180	-6.3	0.48	131
14	-27.4	0.04	159	0.9	1.107	61	-81.2	8.70E-05	-20	-7.9	0.41	115
15	-30.6	0.03	-148	12.7	4.316	-8	-74.6	1.86E-04	152	-10.1	0.31	100
16	-24.1	0.06	-121	22.6	13.52	-87	-76.2	1.55E-04	144	-13.3	0.22	86
17	-21.2	0.09	-116	28.8	27.62	174	-74.7	1.84E-04	-164	-20.5	0.09	76
18	-18.0	0.13	-116	28.7	27.25	73	-64.8	5.75E-04	165	-20.0	0.1	133
19	-15.5	0.17	-123	26.4	20.92	3	-64.3	6.08E-04	123	-19.4	0.11	130
20	-14.0	0.2	-133	24.7	17.18	-53	-64.4	6.03E-04	90	-19.1	0.11	135
21	-13.3	0.22	-142	23.4	14.82	-103	-69.7	3.27E-04	76	-18.7	0.12	133
22	-13.0	0.22	-151	22.4	13.2	-151	-58.2	1.23E-03	80	-18.5	0.12	129
23	-12.9	0.23	-157	21.5	11.9	164	-63.3	6.80E-04	92	-19.0	0.11	124
24	-12.9	0.23	-163	20.8	10.97	121	-61.0	8.96E-04	44	-20.7	0.09	119
25	-13.0	0.23	-172	20.3	10.36	79	-66.1	4.97E-04	55	-21.8	0.08	122
26	-13.3	0.22	-178	19.9	9.895	37	-64.3	6.09E-04	53	-22.9	0.07	131
27	-13.9	0.2	174	19.7	9.691	-6	-63.1	7.00E-04	58	-22.9	0.07	135
28	-14.9	0.18	165	19.5	9.457	-49	-60.2	9.75E-04	68	-22.6	0.07	142
29	-15.8	0.16	155	19.4	9.384	-94	-61.9	8.00E-04	38	-22.1	0.08	136
30	-17.0	0.14	140	19.3	9.247	-141	-56.3	1.53E-03	25	-22.4	0.08	125
31	-19.1	0.11	113	19.1	8.972	171	-57.7	1.31E-03	15	-24.9	0.06	117
32	-21.0	0.09	75	18.6	8.519	121	-58.2	1.23E-03	1	-31.9	0.03	126
33	-20.5	0.1	30	18.1	7.989	69	-56.0	1.59E-03	-15	-31.4	0.03	-148
34	-17.0	0.14	-9	17.2	7.281	14	-57.7	1.31E-03	-12	-24.4	0.06	-141
35	-14.9	0.18	-31	16.2	6.44	-43	-59.0	1.12E-03	-36	-20.0	0.1	-145
36	-12.8	0.23	-45	14.6	5.378	-104	-60.8	9.14E-04	-40	-16.2	0.16	-152
37	-10.7	0.29	-58	12.1	4.014	-171	-62.9	7.13E-04	-31	-13.1	0.22	-167
38	-9.8	0.33	-71	7.7	2.42	122	-57.1	1.40E-03	-55	-11.1	0.28	174
39	-9.1	0.35	-77	1.9	1.238	65	-61.0	8.94E-04	-61	-10.1	0.31	154
40	-8.5	0.38	-85	-3.5	0.671	14	-60.9	9.04E-04	-59	-9.8	0.33	134
41	-8.6	0.37	-92	-9.2	0.347	-41	-67.6	4.15E-04	-65	-9.7	0.33	116
42	-8.6	0.37	-92	-16.1	0.157	-90	-59.2	1.09E-03	-82	-10.1	0.31	98
43	-8.0	0.4	-92	-23.2	0.069	-134	-61.0	8.95E-04	-75	-10.6	0.29	80
44	-7.6	0.42	-90	-32.0	0.025	-172	-62.0	7.96E-04	-59	-11.4	0.27	62
45	-6.0	0.5	-87	-31.7	0.026	-148	-64.6	5.91E-04	-123	-12.3	0.24	41
46	-4.4	0.6	-93	-40.7	0.009	-164	-61.1	8.84E-04	-82	-13.2	0.22	21
47	-3.5	0.67	-98	-46.2	0.005	62	-102.4	7.57E-06	-171	-14.2	0.2	0
48	-2.7	0.74	-102	-58.4	0.001	80	-60.1	9.93E-04	176	-14.8	0.18	-27
49	-1.8	0.81	-111	-46.4	0.005	50	-59.2	1.10E-03	-69	-14.7	0.18	-49
50	-1.7	0.83	-118	-44.2	0.006	113	-61.9	8.00E-04	26	-14.9	0.18	-77

**Note:**

1. Data obtained from on-wafer measurements.

## Biasing and Operation

The recommended quiescent DC bias condition for optimum efficiency, performance, and reliability is  $V_{d1} = 3.5$  volts and  $V_{d2} = 5$  volts with  $V_{gg}$  set for  $I_{d1} + I_{d2} = 780$  mA (no connection to  $V_{g1}$ ). This bias arrangement results in default quiescent drain currents  $I_{d1} = 280$  mA,  $I_{d2} = 500$  mA. A single DC gate supply connected to  $V_{gg}$  will bias all gain stages.

If operation with both  $V_{d1}$  and  $V_{d2}$  at 5 volts is desired, an additional wire bond connection from the  $V_{g1}$  pad to  $V_{gg}$  external bypass chip capacitor (shorting  $V_{g1}$  to  $V_{gg}$ ) will balance the current in each gain stage.  $V_{gg}$  (=  $V_{g1}$ ) can be adjusted for  $I_{d1} + I_{d2} = 780$  mA. Muting can be accomplished by setting  $V_{g1}$  and/or  $V_{gg}$  to the pinch-off voltage  $V_p$ .

An optional output power detector network is also provided. Detector sensitivity can be adjusted by biasing the diodes with typically 1 to 5 volts applied to the Det-bias terminal. Simply connecting Det-Bias to the  $V_{d2}$  supply is a convenient method of biasing this detector network. The differential voltage between the Det-Ref and Det-Out pads can be correlated with the RF power emerging from the RF output port. The detected voltage is given by:

$$V = (V_{ref} - V_{det}) - V_{ofs}$$

Where  $V_{ref}$  is the voltage at the DET\_REF port,  $V_{det}$  is a voltage at the DET\_OUT port, and  $V_{ofs}$  is the zero-input-power offset voltage. There are three methods to calculate  $V_{ofs}$ :

1.  $V_{ofs}$  can be measured before each detector measurement (by removing or switching off the power source and measuring  $V_{ref} - V_{det}$ ). This method gives an error due to temperature drift of less than 0.0002 dB/°C.
2.  $V_{ofs}$  can be measured at a single reference temperature. The drift error will be less than 0.25 dB.
3.  $V_{ofs}$  can either be characterized over temperature and stored in a lookup table, or it can be measured at two temperatures and a linear fit used to calculate  $V_{ofs}$  at any temperature. This method gives an error close to method #1.

With reference to Figure 13, the RF input is DC coupled to a shunt 50  $\Omega$  resistor but it is DC blocked to the input of the first stage. The RF output is DC blocked to the output of the second stage, however, it is DC coupled to the detector bias circuit. If the output detector is biased using the on-chip optional Det-Bias network, an external DC blocking capacitor may be required at the RF Output port.

No ground wires are needed since ground connections are made with plated through-holes to the backside of the device.

## Assembly Techniques

The backside of the AMMC- 5033 chip is RF ground. For microstripline applications, the chip should be attached directly to the ground plane (e.g., circuit carrier or heat-sink) using electrically conductive epoxy.<sup>[1,2]</sup>

For best performance, the topside of the MMIC should be brought up to the same height as the circuit surrounding it. This can be accomplished by mounting a gold plated metal shim (same length and width as the MMIC) under the chip, which is of the correct thickness to make the chip and adjacent circuit coplanar.

The amount of epoxy used for chip and or shim attachment should be just enough to provide a thin fillet around the bottom perimeter of the chip or shim. The ground plane should be free of any residue that may jeopardize electrical or mechanical attachment.

The location of the RF bond pads is shown in Figure 14. Note that all the RF input and output ports are in a Ground-Signal-Ground configuration.

RF connections should be kept as short as reasonable to minimize performance degradation due to undesirable series inductance. A single bond wire is sufficient for signal connections, however double-bonding with 0.7 mil gold wire or the use of gold mesh is recommended for best performance, especially near the high end of the frequency range.

Thermosonic wedge bonding is the preferred method for wire attachment to the bond pads. Gold mesh can be attached using a 2 mil round tracking tool and a tool force of approximately 22 grams with an ultrasonic power of roughly 55 dB for a duration of  $76 \pm 8$  mS. A guided wedge at an ultrasonic power level of 64 dB can be used for the 0.7 mil wire. The recommended wire bond stage temperature is  $150 \pm 2^\circ\text{C}$ .

Caution should be taken to not exceed the Absolute Maximum Rating for assembly temperature and time.

The chip is 100  $\mu\text{m}$  thick and should be handled with care. This MMIC has exposed air bridges on the top surface and should be handled by the edges or with a custom collet (do not pick up die with vacuum on die center.)

This MMIC is also static sensitive and ESD handling precautions should be taken.

### Notes:

1. Ablebond 84-1 LM1 silver epoxy is recommended.
2. Eutectic attach is not recommended and may jeopardize reliability of the device.

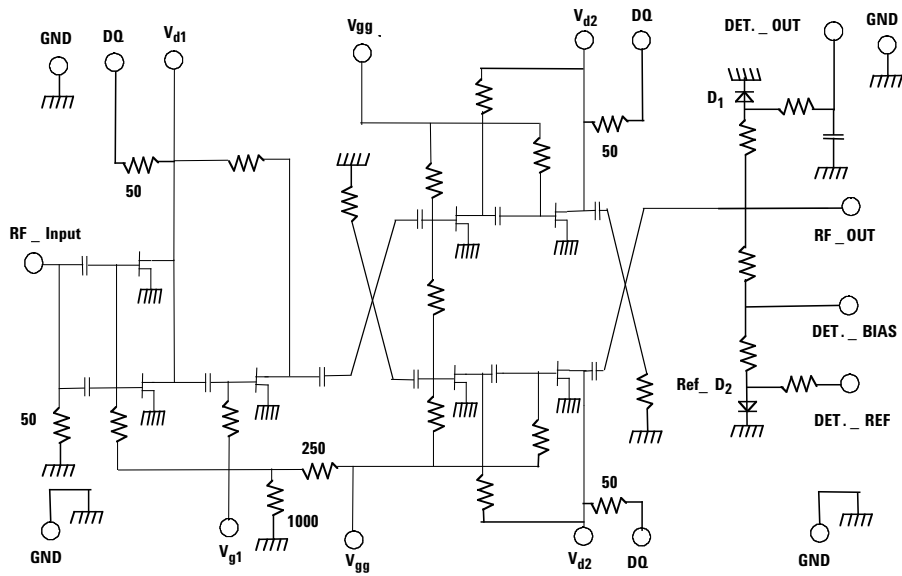


Figure 13. AMMC-5033 schematic

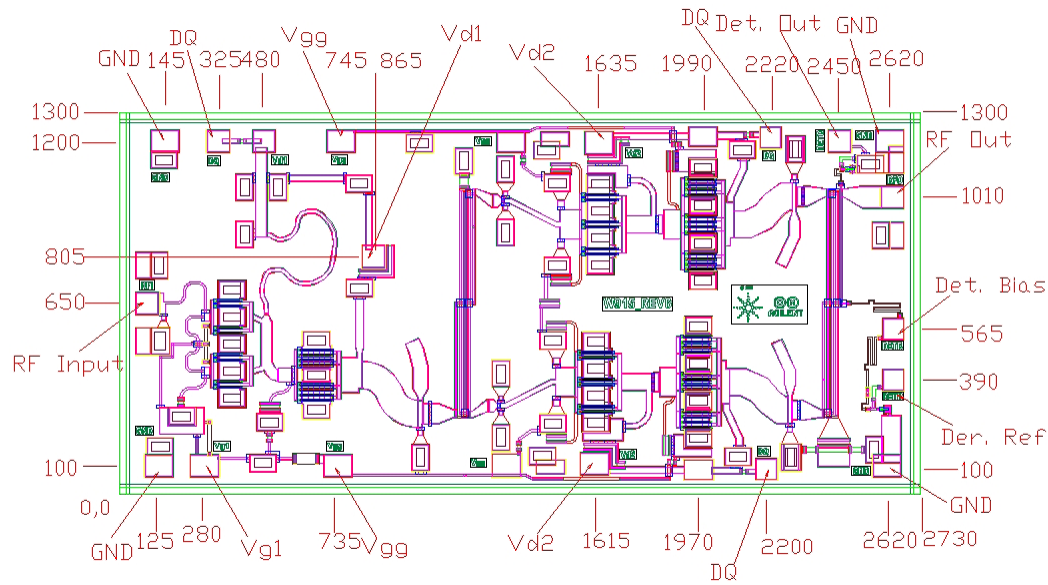


Figure 14. AMMC-5033 bonding pad locations, dimensions are in microns



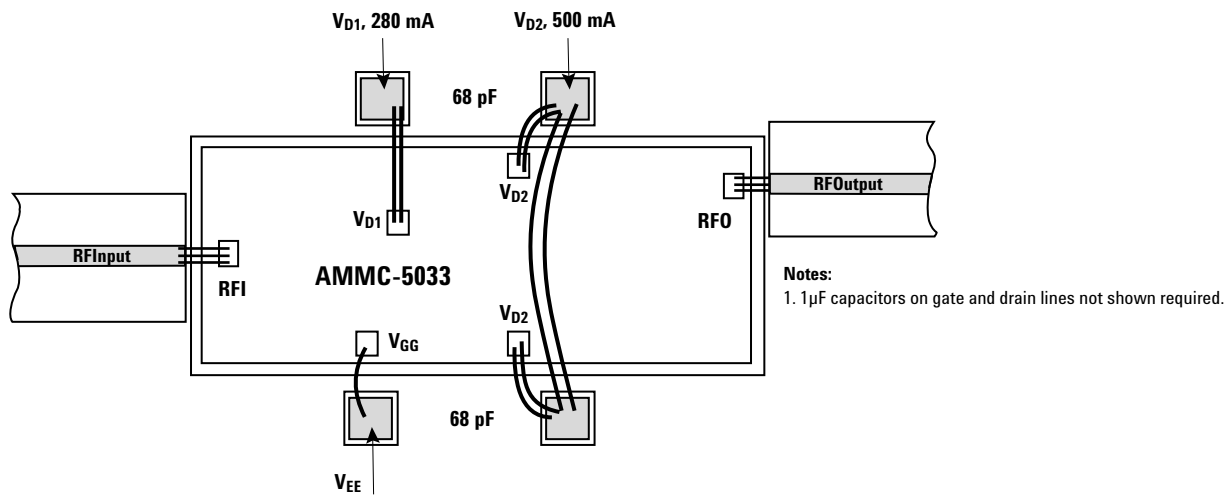


Figure 15. AMMC-5033 assembly diagram

### Ordering Information:

AMMC-5033-W10 = 10 devices per tray

AMMC-5033-W50 = 50 devices per tray

For product information and a complete list of distributors, please go to our website: [www.avagotech.com](http://www.avagotech.com)

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Благодаря развитой сети поставщиков, помогаем в поиске и приобретении экзотичных или снятых с производства компонентов.

Предоставляем спец цены на элементы для создания инженерных сэмплов.

**Упорный труд, качественный результат дают нам право быть уверенными в себе и надежными для наших клиентов.**

### **Наша компания это:**

- Гарантия качества поставляемой продукции
- Широкий ассортимент
- Минимальные сроки поставок
- Техническая поддержка
- Подбор комплектации
- Индивидуальный подход
- Гибкое ценообразование

Наша организация особенно сильна в поставках модулей, микросхем, пассивных компонентов, ксайленсах (XC), EPF, EPM и силовой электроники.

Большой выбор предлагаемой продукции, различные виды оплаты и доставки, позволят Вам сэкономить время и получить максимум выгоды от сотрудничества с нами!

## Перечень производителей, продукцию которых мы поставляем на российский рынок



С удовольствием будем прорабатывать для Вас поставки всех необходимых компонентов по текущим запросам для скорейшего выявления групп элементов, по которым сотрудничество именно с нашей компанией будет для Вас максимально выгодным!

С уважением,

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