ADP3611

Dual Bootstrapped, High Voltage MOSFET Driver with Output Disable

The ADP3611 is a dual MOSFET driver optimized for driving two N−channel switching MOSFETs in nonisolated synchronous buck power converters used to power CPUs in portable computers. The driver impedances have been chosen to provide optimum performance in multiphase regulators at up to 25 A per phase. The high−side driver can be bootstrapped relative to the switch node of the buck converter and is designed to accommodate the high voltage slew rate associated with floating high−side gate drivers. An internal synchronous MOSFET is used to replace an external bootstrap Schottky diode. This allows a larger high side gate voltage for increased efficiency.

The ADP3611 includes an anticross−conduction protection circuit, undervoltage lockout to hold the switches off until the driver has sufficient voltage for proper operation, a crowbar input that turns on the low−side MOSFET independently of the input signal state, and a low−side MOSFET disable pin to provide higher efficiency at light loads. The $\overline{SD}$ pin shuts off both the high−side and the low−side MOSFETs to prevent rapid output capacitor discharge during system shutdown.

The ADP3611 is specified over the extended commercial temperature range of −10°C to 100°C and is available in a 10−lead MSOP package and 8−lead DFN 2x2 mm package.

Features

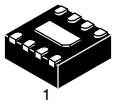
- All−in−one Synchronous Buck Driver
- One PWM Signal Generates Both Drives
- Anticross−conduction Protection Circuitry
- Output Disable Function
- Crowbar Control
- Synchronous Override Control
- This is a Pb−Free Device

Applications

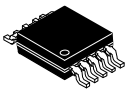
- Mobile Computing CPU Core Power Converters
- Multiphase Desk−note CPU Supplies
- Single−supply Synchronous Buck Converters
- Nonsynchronous−to−Synchronous Drive Conversion

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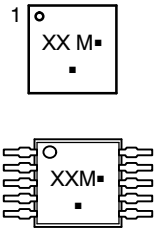


DFN8
CP SUFFIX
CASE 506AA



MSOP10
JRM SUFFIX
CASE 846AC

MARKING DIAGRAMS



X = Specific Device Code
M = Date Code
▪ = Pb−Free Package
(Note: Microdot may be in either location)

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 2 of this data sheet.

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SIMPLIFIED FUNCTIONAL BLOCK DIAGRAM

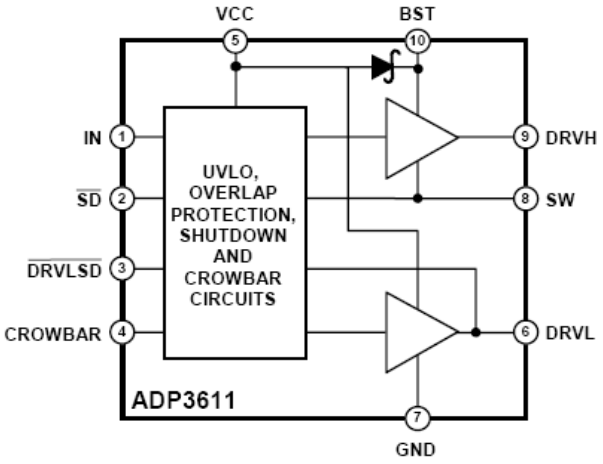


Figure 1. MSOP−10 Package Block Diagram

GENERAL APPLICATION CIRCUIT

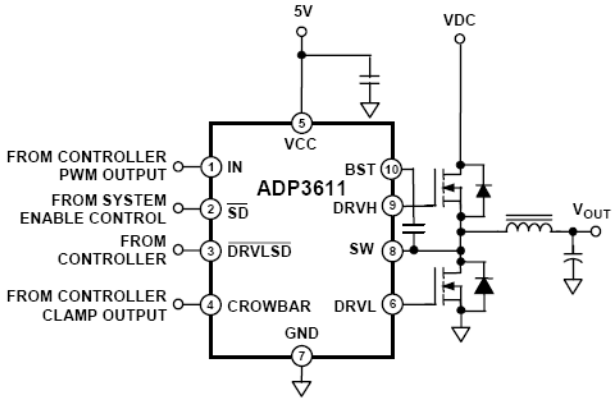


Figure 2. MSOP−10 Package Application Circuit

Table 1. ORDERING INFORMATION

Model	Temperature Range	Package Description	Package Option	Quantity per Reel†	Branding
ADP3611JRMZ−REEL*	−10°C to 100°C	10−Lead Mini Small Outline Package (MSOP)	RM−10	3000	3611
ADP3611MNR2G*	−10°C to 100°C	8−Lead 2x2 mm Package	DFN	3000	D6 M

* Z or G = Pb−Free Part

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

Table 2. ELECTRICAL CHARACTERISTICS (V_{CC} = $\overline{SD}$ = 5 V, BST − SW = 5 V, T_A = −10°C to 100°C, unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
LOGIC INPUTS (IN, $\overline{SD}$, $\overline{DRVLSD}$, CROWBAR)						
Input Voltage High	V_{IH}		2.0			V
Input Voltage Low	V_{IL}				0.8	V
Input Current	I_{IN}	Inputs = 0 V or 5 V, IN, $\overline{SD}$, $\overline{DRVLSD}$	−1		+1	μA
CROWBAR Resistance	R_{IN}	Resistance from CROWBAR to GND		250		kΩ
$\overline{DRVLSD}$ Propagation Delay Time	$t_{pdl\overline{DRVLSD}}$ $t_{pdhDRVLSD}$	C_{LOAD} = 3 nF, Figure 3		20		ns
HIGH−SIDE DRIVER						
Output Resistance, Sourcing Current				1.9	3.3	Ω
Output Resistance, Sinking Current				1.0	2.3	Ω
Transition Times	t_{rDRVH}	C_{LOAD} = 3 nF, Figure 4		20	35	ns
	t_{fDRVH}	C_{LOAD} = 3 nF, Figure 4		15	25	ns
Propagation Delay Times (Note 1)	$t_{pdhDRVH}$	C_{LOAD} = 3 nF, Figure 4	15	30	60	ns
	$t_{pdlDRVH}$	C_{LOAD} = 3 nF, Figure 4		20	40	ns
LOW−SIDE DRIVER						
Output Resistance, Sourcing Current				1.7	3.3	Ω
Output Resistance, Sinking Current				0.8	2.3	Ω
Transition Times	t_{rDRVL}	C_{LOAD} = 3 nF, Figure 4		20	30	ns
	t_{fDRVL}	C_{LOAD} = 3 nF, Figure 4		15	25	ns
Propagation Delay Times (Notes 1 and 2)	$t_{pdhDRVL}$	C_{LOAD} = 3 nF, Figure 4		15	40	ns
	$t_{pdlDRVL}$	C_{LOAD} = 3 nF, Figure 4		15	30	ns
SW Transition Timeout (Note 2)	t_{SWTO}	SW = 2 V	150	270	450	ns
Zero−crossing Threshold	V_{ZC}			1.8		V
BOOTSTRAP RECTIFIER						
Output Resistance	R_{BOOT}			10	18	Ω
SWITCH NODE RESISTOR						
Switch Node Resistor	R_{SW}	EN = 0 V		3		kΩ
SUPPLY						
Supply Voltage Range	V_{CC}		4.6		5.5	V
Supply Current − Normal Mode	$I_{SYS(NM)}$	I_{CC} + I_{BST}, IN = 0 V or 5 V		0.5	1	mA
− Shutdown Mode	$I_{SYS(SD)}$	I_{CC} + I_{BST}, $\overline{SD}$ = 0 V		30	200	μA
Undervoltage Lockout Threshold		V_{CC} Rising	4	4.35	4.5	V
Undervoltage Lockout Hysteresis (Note 3)		V_{CC} Falling	50	210		mV

NOTE: All limits at temperature extremes are guaranteed via correlation using standard statistical quality control (SQC) methods.

1. For propagation delays, t_{pdh} refers to the specified signal going high, and t_{pdl} refers to the signal going low with transitions measured at 50%.
2. The turn−on of DRVL is initiated after IN goes low by either SW crossing a ~1 V threshold or by expiration of t_{SWTO}.
3. Guaranteed by characterization, not production tested.

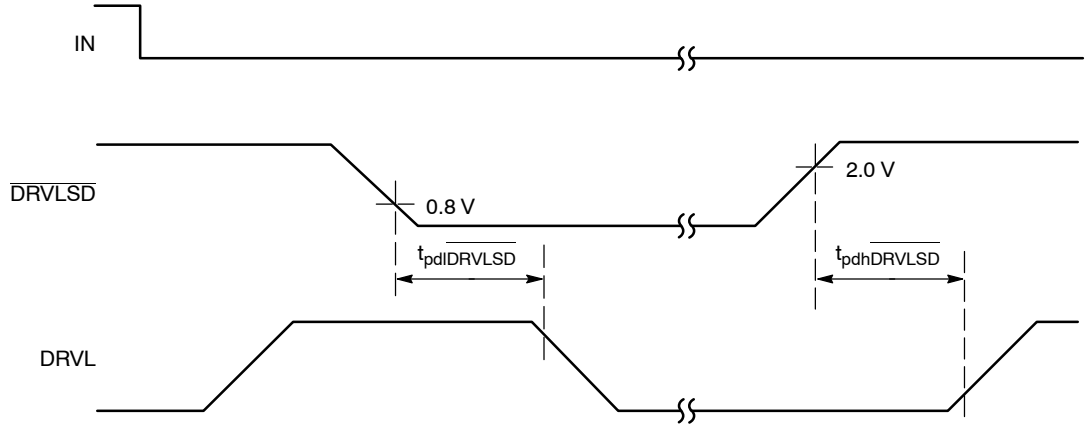


Figure 3. Output Disable Timing Diagram (Timing is Referenced to the 90% and 10% Points Unless Otherwise Noted)

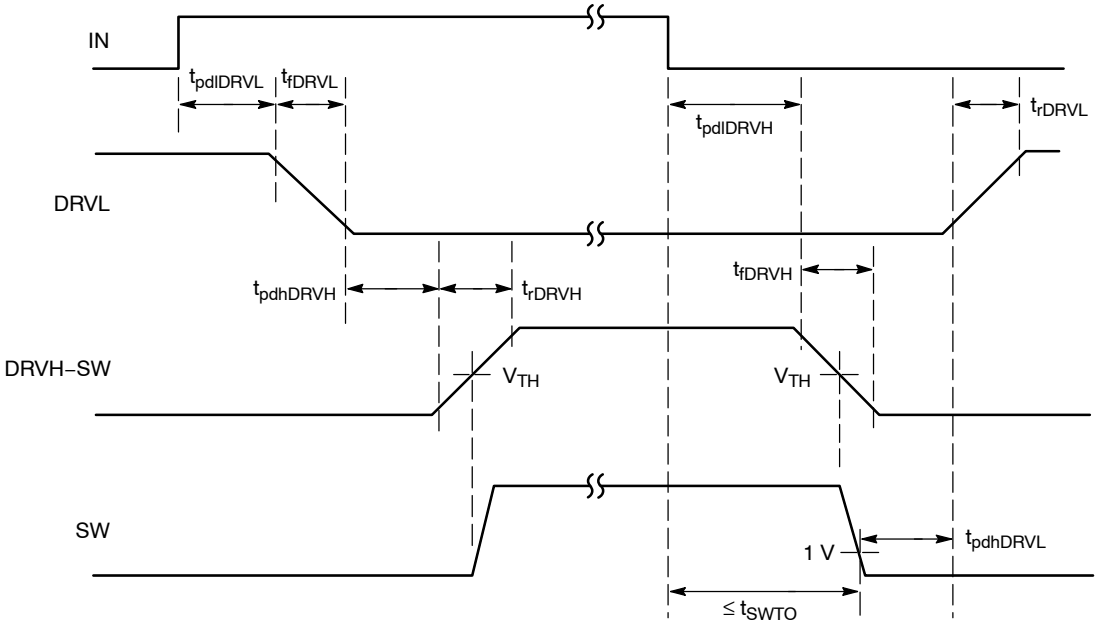


Figure 4. Nonoverlap Timing Diagram (Timing is Referenced to the 90% and 10% Points Unless Otherwise Noted)

Table 3. ABSOLUTE MAXIMUM RATINGS (Unless otherwise specified, all voltages are referenced to GND.)

Parameter		Rating	Unit
VCC		−0.3 to +6	V
BST, DRVH	DC t < 200 ns	−0.3 to +26 −0.3 to +31	V
BST to SW		−0.3 to +6	V
BST to VCC	DC t < 200 ns	−0.3 to +21 −0.3 to +26	V
SW	DC t < 200 ns	−1 to +21 −6 to +26	V
DRVH to SW		−0.3 to +6	V
DRVH		SW − 0.3 to BST + 0.3	V
DRVL	DC t < 200 ns	−0.3 to +6 −5 to +6	V
All Other Inputs and Outputs		−0.3 to +6	V
θ_{JA} MSOP−10 Package	2−Layer Board 4−Layer Board	340 220	°C/W
θ_{JA} QFN−8 2 mm x 2 mm Package		143	°C/W
Operating Ambient Temperature Range		−10 to +100	°C
Junction Temperature Range		−10 to +150	°C
Storage Temperature Range		−65 to +150	°C
Lead Temperature Range	Soldering (10 s) Vapor Phase (60 s) Infrared (15 s)	300 215 220	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

NOTE: This device is ESD sensitive. Use standard ESD precautions when handling.

Pin Configuration

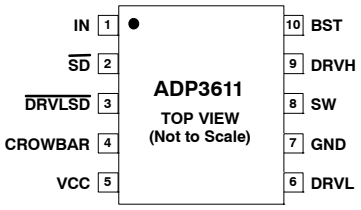


Figure 5. 10−Lead MSOP Package

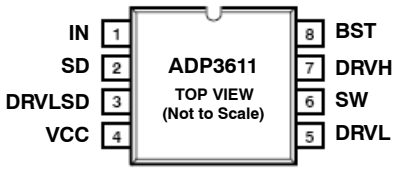


Figure 6. 8−Lead DFN 2 x 2 mm Package

Table 4. PIN FUNCTION DESCRIPTIONS

Pin No. QFN	Pin No. MSOP	Symbol	Description
1	1	IN	Logic Level PWM Input. This pin has primary control of the drive outputs. In normal operation, pulling this pin low turns on the low−side driver; pulling it high turns on the high−side driver.
2	2	$\overline{SD}$	Shutdown Input. When low, this pin disables normal operation, forcing DRVH and DRVL low.
3	3	$\overline{DRVLSD}$	Synchronous Rectifier Shutdown Input. When low, DRVL is forced low; when high, DRVL is enabled and controlled by IN and by the adaptive overlap protection control circuitry.
	4	CROWBAR	Crowbar Input. When high, DRVL is forced high regardless of the high−side MOSFET switch condition.
4	5	VCC	Input Supply. This pin should be bypassed to GND with a 4.7 μF or larger ceramic capacitor.
5	6	DRVL	Synchronous Rectifier Drive. Output drive for the lower (synchronous rectifier) MOSFET.
Tab	7	GND	Ground. This pin should be closely connected to the source of the lower MOSFET.
6	8	SW	Switch Node Input. This pin is connected to the buck−switching node, close to the upper MOSFET's source. It is the floating return for the upper MOSFET drive signal. It is also used to monitor the switched voltage to prevent turn−on of the lower MOSFET until the voltage is below ~1 V.
7	9	DRVH	Buck Drive. Output drive for the upper (buck) MOSFET.
8	10	BST	Upper MOSFET Floating Bootstrap Supply. A capacitor connected between the BST and SW pins holds this bootstrapped voltage for the high−side MOSFET as it is switched.

TYPICAL PERFORMANCE CHARACTERISTICS

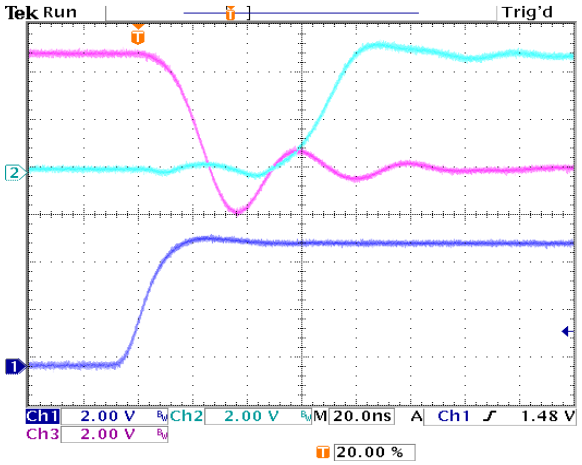


Figure 7. DRVH Rise and DRVL Fall Times CH1 = IN, CH2 = DRVH, CH3 = DRVL

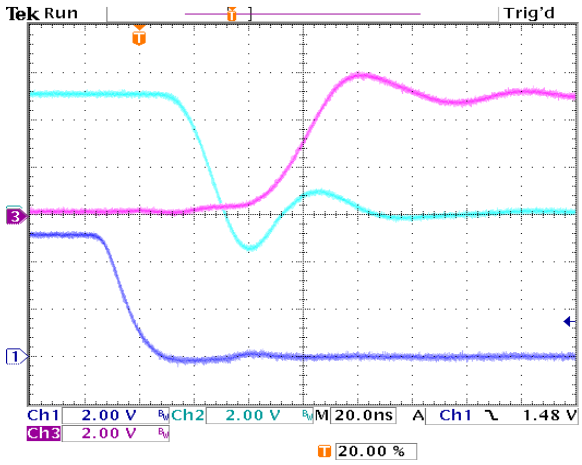


Figure 8. DRVH Fall and DRVL Rise Times CH1 = IN, CH2 = DRVH, CH3 = DRVL

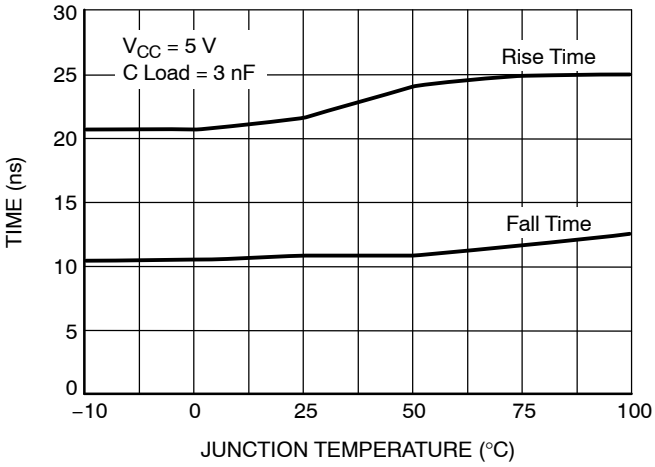


Figure 9. DRVH Rise and Fall Times vs. Temperature

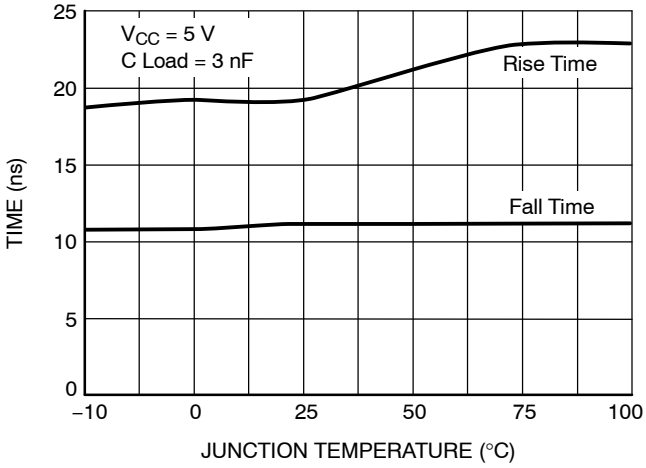


Figure 10. DRVL Rise and Fall Times vs. Temperature

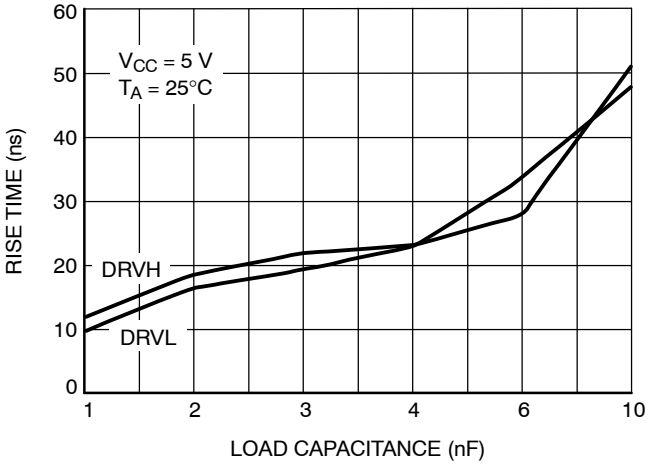


Figure 11. DRVH and DRVL Rise Times vs. Load Capacitance

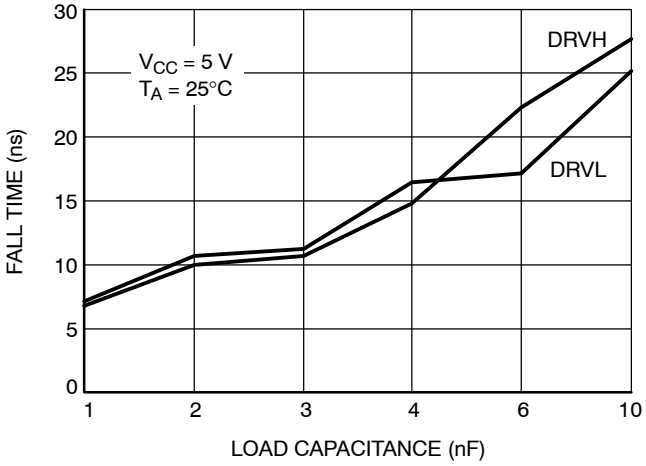


Figure 12. DRVH and DRVL Fall Times vs. Load Capacitance

TYPICAL PERFORMANCE CHARACTERISTICS

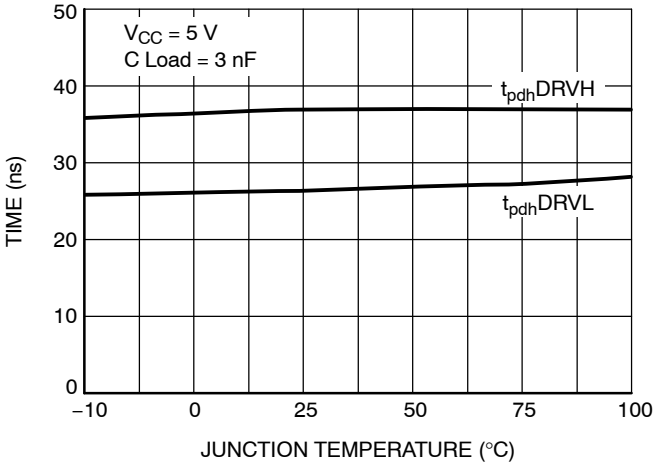


Figure 13. DRVH and DRVL t_{pdh} vs. Temperature

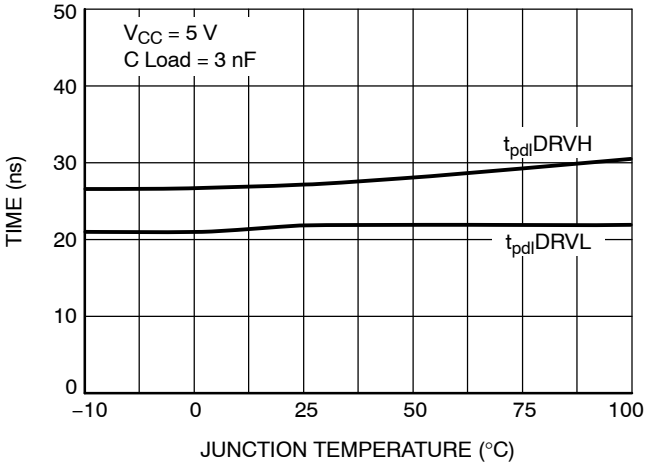


Figure 14. DRVH and DRVL t_{pdl} vs. Temperature

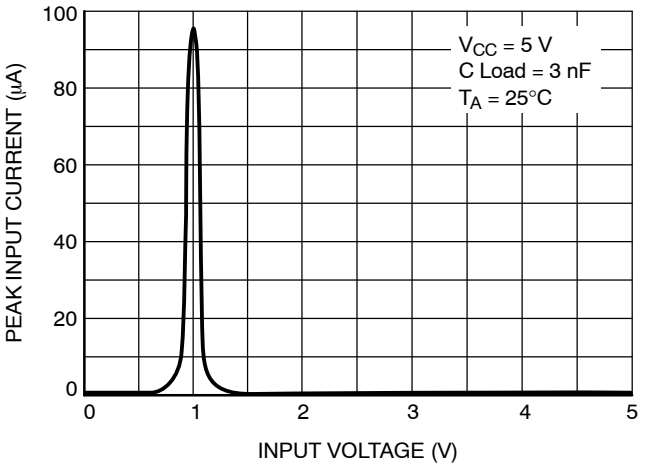


Figure 15. IN Pin Input Current vs. Input Voltage

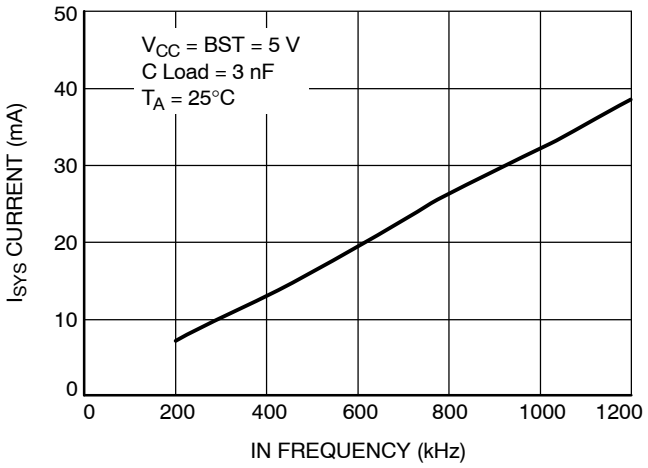


Figure 16. Supply Current vs. Frequency

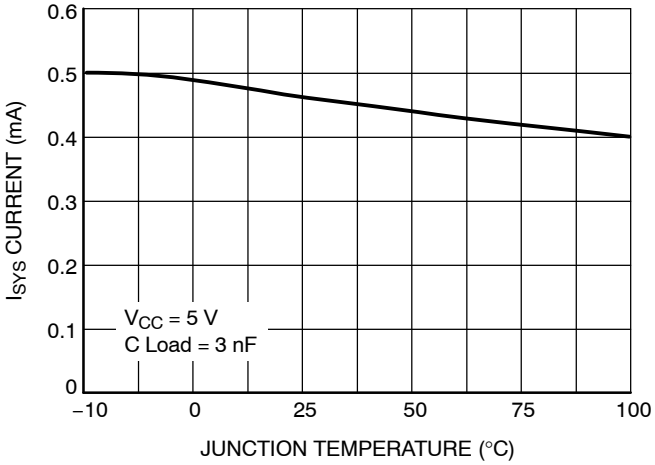


Figure 17. Supply Current vs. Temperature

THEORY OF OPERATION

The ADP3611 is a dual MOSFET driver optimized for driving two N-channel MOSFETs in a synchronous buck converter topology. A single PWM input signal is all that is required to properly drive the high-side and the low-side MOSFETs. Each driver is capable of driving a 3 nF load at speeds up to 1 MHz. A more detailed description of the ADP3611 and its features follows. Refer to the detailed block diagram in Figure 18.

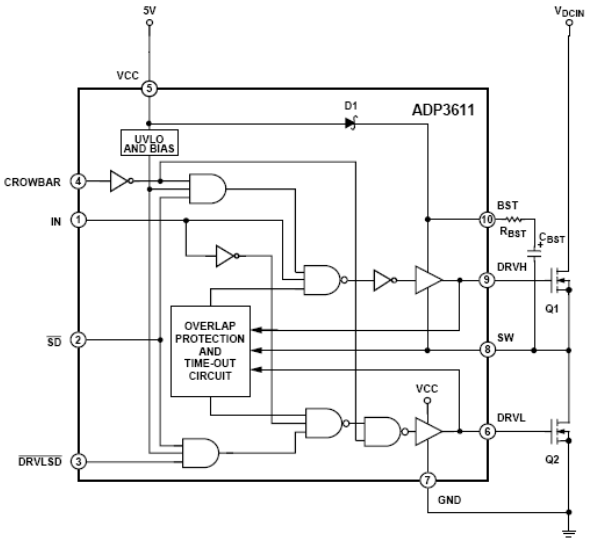


Figure 18. Detailed Block Diagram of the ADP3611

Undervoltage Lockout

The undervoltage lockout (UVLO) circuit holds both MOSFET driver outputs low during VCC supply ramp-up. The UVLO logic becomes active and in control of the driver outputs at a supply voltage of no greater than 1.5 V. The UVLO circuit waits until the VCC supply has reached a voltage high enough to bias logic level MOSFETs fully on before releasing control of the drivers to the control pins.

Driver Control Input

The driver control input (IN) is connected to the duty ratio modulation signal of a switch-mode controller. IN can be driven by 2.5 V to 5.0 V logic. The output MOSFETs are driven so that the SW node follows the polarity of IN.

Low−Side Driver

The low-side driver is designed to drive a ground-referenced low $R_{DS(ON)}$ N-channel synchronous rectifier MOSFET. The bias to the low-side driver is internally connected to the VCC supply and GND. Once the supply voltage ramps up and exceeds the UVLO threshold, the driver is enabled. When the driver is enabled, the driver's output is 180° out of phase with the IN pin. Table 5 shows the relationship between DRVL and the different control inputs of the ADP3611.

High−Side Driver

The high-side driver is designed to drive a floating low $R_{DS(ON)}$ N-channel MOSFET. The bias voltage for the high-side driver is developed by an external bootstrap supply circuit, which is connected between the BST and SW pins.

The bootstrap circuit comprises a diode, D1, and bootstrap capacitor, C_{BST}. When the ADP3611 is starting up, the SW pin is at ground, so the bootstrap capacitor charges up to VCC through D1. Once the supply voltage ramps up and exceeds the UVLO threshold, the driver is enabled. When IN goes high, the high-side driver begins to turn on the high-side MOSFET (Q1) by transferring charge from C_{BST}. As Q1 turns on, the SW pin rises up to V_{DCIN}, forcing the BST pin to $V_{DCIN} + V_{C(BST)}$, which is enough gate-to-source voltage to hold Q1 on. To complete the cycle, Q1 is switched off by pulling the gate down to the voltage at the SW pin. When the low-side MOSFET (Q2) turns on, the SW pin is pulled to ground. This allows the bootstrap capacitor to charge up to VCC again.

When the driver is enabled, the driver's output is in phase with the IN pin. Table 5 shows the relationship between DRVH and the different control inputs of the ADP3611.

Overlap Protection Circuit

The overlap protection circuit prevents both main power switches, Q1 and Q2, from being on at the same time. This is done to prevent shoot-through currents from flowing through both power switches and the associated losses that can occur during their on-off transitions. The overlap protection circuit accomplishes this by adaptively controlling the delay from Q1's turn-off to Q2's turn-on, and the delay from Q2's turn-off to Q1's turn-on.

To prevent the overlap of the gate drives during Q1's turn-off and Q2's turn-on, the overlap circuit monitors the voltage at the SW pin and DRVH pin. When IN goes low, Q1 begins to turn off. The overlap protection circuit waits for the voltage at the SW and DRVH pins to both fall below 1.6 V. Once both of these conditions are met, Q2 begins to turn on. Using this method, the overlap protection circuit ensures that Q1 is off before Q2 turns on, regardless of variations in temperature, supply voltage, gate charge, and drive current. There is, however, a timeout circuit that overrides the waiting period for the SW and DRVH pins to reach 1.6 V. After the timeout period has expired, DRVL is asserted high regardless of the SW and DRVH voltages. In the opposite case, when IN goes high, Q2 begins to turn off after a propagation delay. The overlap protection circuit waits for the voltage at DRVL to fall below 1.6 V, after which DRVH is asserted high and Q1 turns on.

Low−Side Driver Shutdown

The low-side driver shutdown $\overline{\text{DRVLSD}}$ allows a control signal to shut down the synchronous rectifier. Under light load conditions, $\overline{\text{DRVLSD}}$ should be pulled low before the

polarity reversal of the inductor current to maximize light load conversion efficiency. $\overline{\text{DRVLSD}}$ can also be pulled low for reverse voltage protection purposes.

When $\overline{\text{DRVLSD}}$ is low, the low-side driver stays low. When $\overline{\text{DRVLSD}}$ is high, the low-side driver is enabled and controlled by the driver signals, as previously described.

Low−Side Driver Timeout

In normal operation, the DRVH signal tracks the IN signal and turns off the Q1 high-side switch with a few 10 ns delay ($t_{pdlDRVH}$) following the falling edge of the input signal. When Q1 is turned off, DRVL is allowed to go high, Q2 turns on, and the SW node voltage collapses to zero. But in a fault condition such as a high-side Q1 switch drain-source short circuit, the SW node cannot fall to zero, even when DRVH goes low. The ADP3611 has a timer circuit to address this scenario. Every time the IN goes low, a DRVL on-time delay timer is triggered. If the SW node voltage does not trigger a low-side turn-on, the DRVL on-time delay circuit does it instead, when it times out with $t_{SW(TO)}$ delay. If Q1 is still turned on, that is, its drain is shorted to the source, Q2 turns on and creates a direct short circuit across the V_{DCIN} voltage rail. The crowbar action causes the fuse in the V_{DCIN} current path to open. The opening of the fuse saves the load (CPU) from potential damage that the high-side switch short circuit could have caused.

Crowbar Function

In addition to the internal low-side drive time-out circuit, the ADP3611 includes a CROWBAR input pin to provide a means for additional overvoltage protection. When CROWBAR goes high, the ADP3611 turns off DRVH and turns on DRVL. The crowbar logic overrides the overlap protection circuit, the shutdown logic, the $\overline{\text{DRVLSD}}$ logic, and the UVLO protection on DRVL. Thus, the crowbar function maximizes the overvoltage protection coverage in the application. The CROWBAR can be either driven by the CLAMP pin of buck controllers, such as the ADP3207A, or ADP3210, or controlled by an independent overvoltage monitoring circuit.

Table 5. ADP3611 Truth Table

CROWBAR	UVLO	$\overline{\text{SD}}$	$\overline{\text{DRVLSD}}$	IN	DRVH	DRVL
L	L	H	H	H	H	L
L	L	H	H	L	L	H
L	L	H	L	H	H	L
L	L	H	L	L	L	L
L	L	L	*	*	L	L
L	H	*	*	*	L	L
H	L	*	*	*	L	H
H	H	*	*	*	L	H

* = Don't Care

APPLICATION INFORMATION

Supply Capacitor Selection

For the supply input (VCC) of the ADP3611, a local bypass capacitor is recommended to reduce the noise and to supply some of the peak currents drawn. Use a 10 μF or 4.7 μF multilayer ceramic (MLC) capacitor. MLC capacitors provide the best combination of low ESR and small size, and can be obtained from the following vendors.

Table 6.

Vendor	Part Number	Web Address
Murata	GRM235Y5V106Z16	www.murata.com
Taiyo−Yuden	EMK325F106ZF	www.t−yuden.com
Tokin	C23Y5V1C106ZP	www.tokin.com

Keep the ceramic capacitor as close as possible to the ADP3611.

Bootstrap Circuit

The bootstrap circuit uses a charge storage capacitor (CBST) and a synchronous MOSFET rectifier (D1), as shown in Figure 18. Selection of these components can be done after the high-side MOSFET has been chosen. The bootstrap capacitor must have a voltage rating that is able to handle at least 5 V more than the maximum supply voltage. The capacitance is determined by

$$C_{BST} = \frac{Q_{HSGATE}}{\Delta V_{BST}} \qquad \text{(eq. 1)}$$

where:

Q_{HSGATE} is the total gate charge of the high-side MOSFET.

ΔV_{BST} is the voltage droop allowed on the high-side MOSFET drive.

For example, two NTMFS4821N MOSFETs in parallel have a total gate charge of about 20 nC. For an allowed droop of 100 mV, the required bootstrap capacitance is 200 nF. A good quality ceramic capacitor should be used, and derating for the significant capacitance drop of MLCs at high temperature must be applied. In this example, selection of 470 nF or even 1 μF would be recommended.

Normally a Schottky diode is recommended for the bootstrap diode due to its low forward drop, which maximizes the drive available for the high-side MOSFET. Using a synchronous MOSFET rectifier instead of a Schottky diode has the advantage of an even lower forward voltage drop. A lower forward voltage drop gives a larger drive voltage for the high-side MOSFET and a lower conduction loss for the high-side MOSFET. The bootstrap diode must also be able to handle at least 5 V more than the maximum battery voltage. The average forward current can be estimated by

$$I_{F(AVG)} = Q_{HSGATE} \times f_{MAX} \qquad \text{(eq. 2)}$$

where f_{MAX} is the maximum switching frequency of the controller.

Power and Thermal Considerations

The major power consumption of the ADP3611-based driver circuit is from the dissipation of MOSFET gate charge. It can be estimated as

$$P_{MAX} \approx VCC \times (Q_{HSGATE} + Q_{LSGATE}) \times f_{MAX} \quad \text{(eq. 3)}$$

where:

V_{CC} is the supply voltage 5 V.

f_{MAX} is the highest switching frequency.

Q_{HSGATE} and Q_{LSGATE} are the total gate charge of high-side and low-side MOSFETs, respectively.

For example, the ADP3611 drives two NTMFS4821N high-side MOSFETs and two NTMFS4846N low-side MOSFETs. According to the MOSFET data sheets, Q_{HSGATE} = 20 nC and Q_{LSGATE} = 40 nC. Given that f_{MAX} is 300 kHz, P_{MAX} would be about 90 mW.

Part of this power consumption generates heat inside the ADP3611. The temperature rise of the ADP3611 against its environment is estimated as

$$\Delta T \approx \theta_{JA} \times P_{MAX} \times \eta \quad \text{(eq. 4)}$$

where θ_{JA} is ADP3611's thermal resistance from junction to air, given in the absolute maximum ratings as 220°C/W for a 4 layer board.

The total MOSFET drive power dissipates in the output resistance of ADP3611 and in the MOSFET gate resistance as well. η represents the ratio of power dissipation inside the ADP3611 over the total MOSFET gate driving power. For normal applications, a rough estimation for η is 0.7. A more accurate estimation can be calculated using

$$\eta \approx \frac{Q_{HSGATE}}{Q_{HSGATE} + Q_{LSGATE}} \times \left(\frac{0.5 \times R1}{R1 + R_{HSGATE} + R} + \frac{0.5 \times R2}{R2 + R_{HSGATE}} \right) \frac{Q_{LSGATE}}{Q_{HSGATE} + Q_{LSGATE}} \times \left(\frac{0.5 \times R3}{R3 + R_{LSGATE}} + \frac{0.5 \times R4}{R4 + R_{LSGATE}} \right) \quad \text{(eq. 5)}$$

where:

R1 and R2 are the output resistances of the high-side driver: R1 = 1.7 (DRVH − BST), R2 = 0.8 (DRVH − SW).

R3 and R4 are the output resistances of the low-side driver: R3 = 1.7 (DRVL − VCC), R4 = 0.8 (DRVL − GND).

R is the external resistor between the BST pin and the BST capacitor.

R_{HSGATE} and R_{LSGATE} are gate resistances of high-side and low-side MOSFETs, respectively.

Assuming that R = 0 and that $R_{HSGATE} = R_{LSGATE} = 0.5$, Equation 5 gives a value of η = 0.71. Based on Equation 4, the estimated temperature rise in this example is about 22°C.

PC Board Layout Considerations

Use the following general guidelines when designing printed circuit boards. Figure 19 gives an example of the typical land patterns based on the guidelines given here.

- The VCC bypass capacitor should be located as close as possible to the VCC and GND pins. Place the ADP3611 and bypass capacitor on the same layer of the board, so that the PCB trace between the ADP3611 VCC pin and the MLC capacitor does not contain any via. An ideal location for the bypass MLC capacitor is near Pin 5 and Pin 6 of the ADP3611.
- High frequency switching noise can be coupled into the VCC pin of the ADP3611 via the BST diode. Therefore, do not connect the anode of the BST diode to the VCC pin with a short trace. Use a separate via or trace to connect the anode of the BST diode directly to the VCC 5 V power rail.
- It is best to have the low-side MOSFET gate close to the DRVL pin; otherwise, use a short and very thick PCB trace between the DRVL pin and the low-side MOSFET gate.
- Fast switching of the high-side MOSFET can reduce switching loss. However, EMI problems can arise due to the severe ringing of the switch node voltage. Depending on the character of the low-side MOSFET, a very fast turn-on of the high-side MOSFET may falsely turn on the low-side MOSFET through the dv/dt coupling of its Miller capacitance. Therefore, when fast turn-on of the high-side MOSFET is not required by the application, a resistor of about 1 Ω to 2 Ω can be placed between the BST pin and the BST capacitor to limit the turn-on speed of the high-side MOSFET.

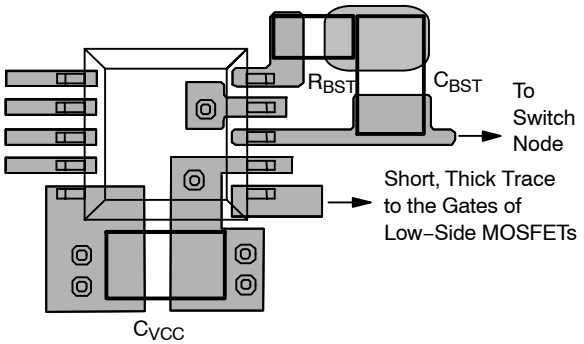
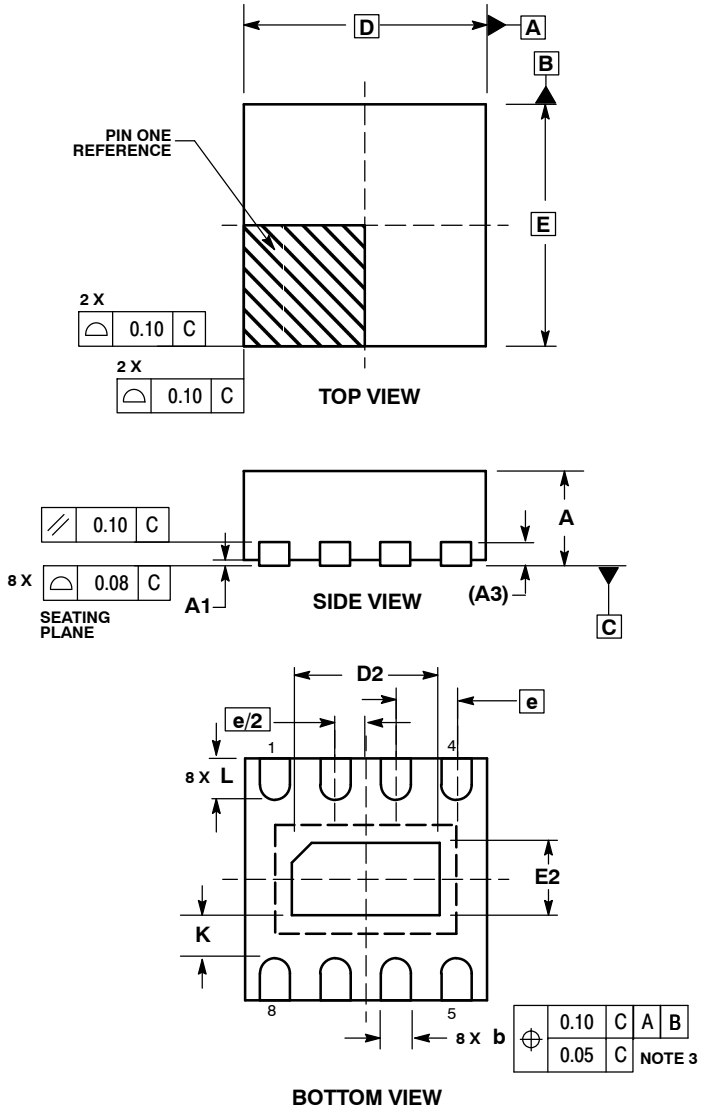


Figure 19. External Component Placement Example

PACKAGE DIMENSIONS

DFN8
CASE 506AA−01
ISSUE D

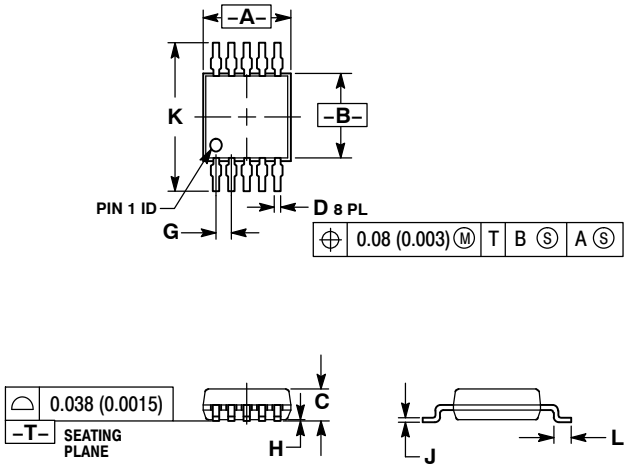


NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994 .
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.25 AND 0.30 MM FROM TERMINAL.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

	MILLIMETERS	
DIM	MIN	MAX
A	0.80	1.00
A1	0.00	0.05
A3	0.20 REF	
b	0.20	0.30
D	2.00 BSC	
D2	1.10	1.30
E	2.00 BSC	
E2	0.70	0.90
e	0.50 BSC	
K	0.20	−−−
L	0.25	0.35

PACKAGE DIMENSIONS

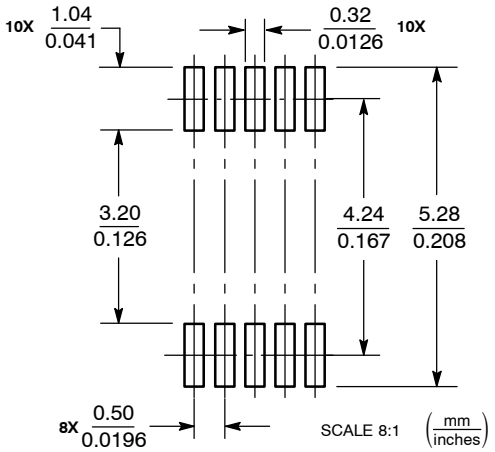
MSOP10
CASE 846AC−01
ISSUE O



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION “A” DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION “B” DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. 846B−01 OBSOLETE. NEW STANDARD 846B−02

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	2.90	3.10	0.114	0.122
B	2.90	3.10	0.114	0.122
C	0.95	1.10	0.037	0.043
D	0.20	0.30	0.008	0.012
G	0.50 BSC		0.020 BSC	
H	0.05	0.15	0.002	0.006
J	0.10	0.21	0.004	0.008
K	4.75	5.05	0.187	0.199
L	0.40	0.70	0.016	0.028

SOLDERING FOOTPRINT*



*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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