CS8481

3.3 V/250 mA, 5.0 V/100 mA Micropower Low Dropout Regulator with ENABLE

The CS8481 is a precision, dual Micropower linear voltage regulator. The switched 3.3 V primary output (V_{OUT1}) supplies up to 250 mA while the secondary 5.0 V (V_{OUT2}) is capable of supplying 100 mA. Both outputs have a maximum dropout voltage of 600 mV and low reverse current. Quiescent current drain is typically 150 μA when supplying 100 μA from each output.

The ENABLE input provides logic level control of the primary output. With the primary output disabled, quiescent current drain is typically 100 μA when supplying 100 μA from the secondary output.

The CS8481 is extremely robust with protection provided for reverse battery, short circuit, overvoltage, and overtemperature on both outputs.

The CS8481 is available in a D^2PAK−5.

Features

- 3.3 V/250 mA Primary Output
- 5.0 V/100 mA Secondary Output
- 3.0% Tolerance, Both Outputs
- ON/OFF Control for Primary Output
- Low Quiescent Current Drain (100 μA V_{OUT2})
- Low Reverse Current
- Protection Features
  - Reverse Battery (−15 V)
  - 74 V Peak Transient Voltage
  - Short Circuit
  - Overtemperature
  - Overvoltage (34 V)

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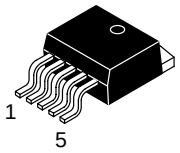
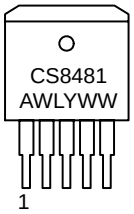


D^2PAK−5
DP SUFFIX
CASE 936AC

PIN CONNECTIONS AND MARKING DIAGRAM



Tab = GND
Pin 1. V_{IN}
2. V_{OUT1}
3. GND
4. V_{OUT2}
5. ENABLE

A = Assembly Location
WL, L = Wafer Lot
YY, Y = Year
WW, W = Work Week

ORDERING INFORMATION*

Device	Package	Shipping†
CS8481YDP5	D^2PAK−5	50 Units/Rail
CS8481YDPR5	D2PAK−5	750 Tape & Reel

*Consult your local sales representative for SO−8, SO−16, DIP−8, DIP−16, TO−220−5, and D^2PAK−7 packaging options.

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

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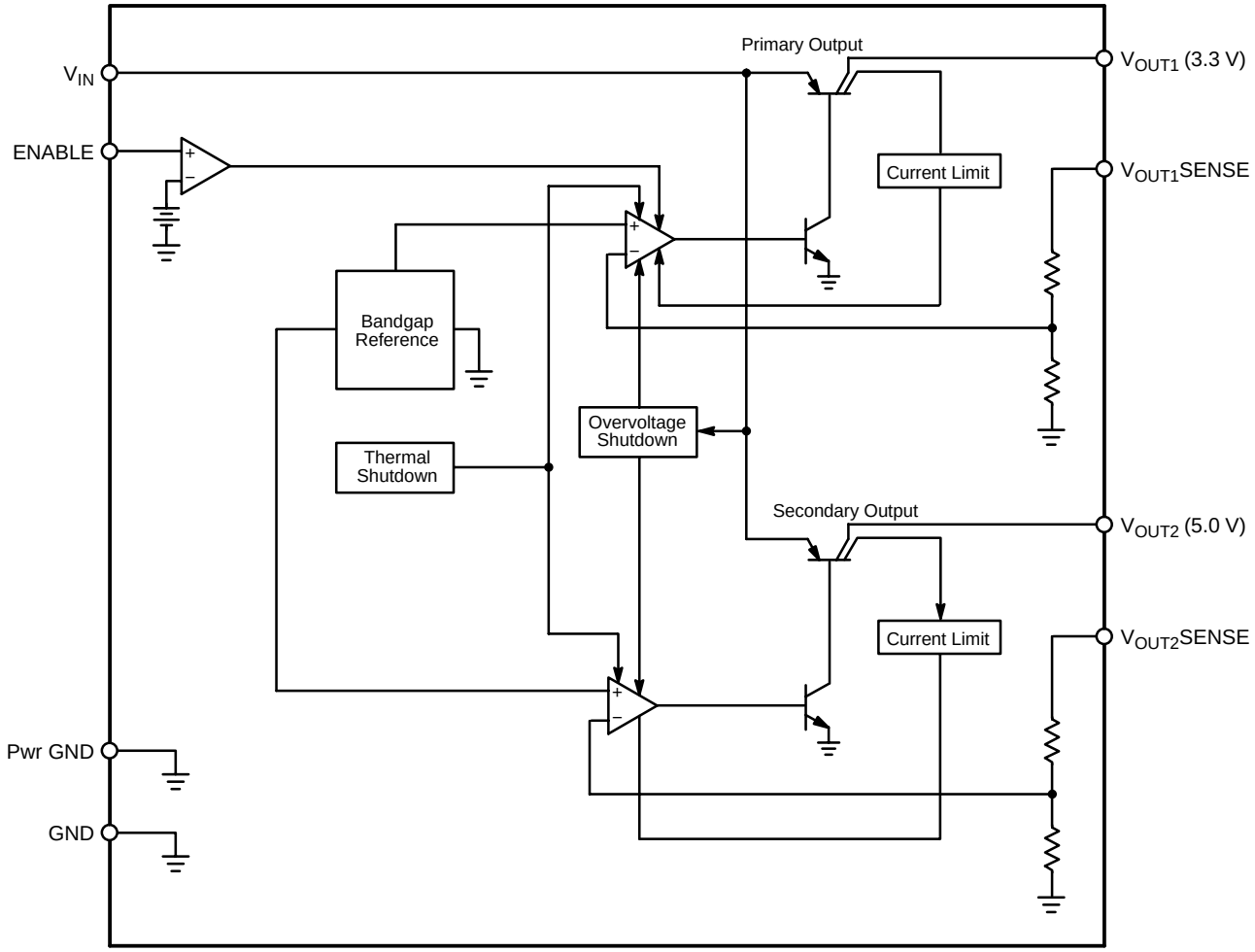


Figure 1. Block Diagram

MAXIMUM RATINGS*

Rating	Value	Unit
Input Voltage (V_{IN}) Operating Range Reverse Battery Peak Transient Voltage (60 V Load Dump @ 14 V V_{IN})	30 −15 74	V V V
ENABLE	10	V
Power Dissipation	Internally Limited	−
Maximum Junction Temperature	−40 to +150	°C
Storage Temperature Range	−55 to +150	°C
Electrostatic Discharge (Human Body Model)	4.0	kV
Lead Temperature Soldering Reflow (SMD styles only) (Note 1)	230 peak	°C

1. 60 second maximum above 183°C

*The maximum package power dissipation must be observed.

ELECTRICAL CHARACTERISTICS: (6.0 V ≤ V_{IN} ≤ 26 V, I_{OUT1} = I_{OUT2} = 100 μA, −40°C ≤ T_A ≤ 125°C, −40°C ≤ T_C ≤ 125°C; unless otherwise specified.)

Characteristic	Test Conditions	Min	Typ	Max	Unit
Primary Output Stage (V_{OUT1})					
Output Voltage, V_{OUT1}	100 μA ≤ I_{OUT1} ≤ 250 mA	3.2	3.3	3.4	V
Line Regulation	6.0 V ≤ V_{IN} ≤ 26 V	–	5.0	50	mV
Load Regulation	1.0 mA ≤ I_{OUT1} ≤ 250 mA, V_{IN} = 14 V	–	5.0	50	mV
Quiescent Current	ENABLE = HIGH, V_{IN} = 16V, I_{OUT1} = 250 mA	–	22	50	mA
Ripple Rejection	f = 120 Hz, I_{OUT1} = 125 mA, 7.0 V ≤ V_{IN} ≤ 17 V	60	70	–	dB
Current Limit	9.0 V ≤ V_{IN} ≤ 26 V	260	400	–	mA
Short Circuit Current Limit	V_{OUT1} = 0 V, V_{IN} = 16 V	25	–	–	mA
Reverse Current	V_{OUT1} = 3.3 V, V_{IN} = 0 V	–	100	1500	μA
Secondary Output (V_{OUT2})					
Output Voltage, (V_{OUT2})	100 μA ≤ I_{OUT2} ≤ 100 mA	4.85	5.00	5.15	V
Dropout Voltage	I_{OUT2} = 100 mA I_{OUT2} = 100 μA	 –	400 100	600 150	mV mV
Line Regulation	6.0 V ≤ V_{IN} ≤ 26 V	–	5.0	50	mV
Load Regulation	100 μA ≤ I_{OUT2} ≤ 100 mA, V_{IN} = 14 V	–	5.0	50	mV
Quiescent Current	ENABLE = LOW, V_{IN} = 12.8 V ENABLE = HIGH, V_{IN} = 16 V, I_{OUT2} = 100 mA	– –	100 8.0	150 30	μA mA
Ripple Rejection	f = 120 Hz; I_{OUT2} = 10 mA, 7.0 V ≤ V_{IN} ≤ 17 V	60	70	–	dB
Current Limit	9.0 V ≤ V_{IN} ≤ 26 V	105	200	–	mA
Short Circuit Current Limit	V_{OUT2} = 0 V, V_{IN} = 16 V, I_{OUT1} = 0 A	25	–	–	mA
Reverse Current	V_{OUT2} = 5.0 V, V_{IN} = 0 V	–	100	250	μA
ENABLE Function (ENABLE)					
Input Threshold	ENABLE = LOW, 6.0 V ≤ V_{IN} ≤ 26 V ENABLE = HIGH, 6.0 V ≤ V_{IN} ≤ 26 V	– 2.0	1.2 1.2	0.8 –	V V
Input Bias Current	0 V ≤ V_{ENABLE} ≤ 5.0 V	−2.0	0	2.0	μA
Protection Circuits					
Overtemperature Threshold	Note 2	150	180	–	°C
Overvoltage Shutdown	–	30	34	38	V

2. Guaranteed by Design.

PACKAGE PIN DESCRIPTION

PACKAGE LEAD # D²PAK−5	LEAD SYMBOL	FUNCTION
1	V_{IN}	Supply voltage to IC, usually direct from battery.
2	V_{OUT1}	3.3 V regulated output which is activated by ENABLE input.
3	GND	Ground connection.
4	V_{OUT2}	Standby output 5.0 V, 100 mA capability; always on.
5	ENABLE	CMOS compatible input lead; switches V_{OUT1}. When ENABLE is high, V_{OUT1} is active.

DEFINITION OF TERMS

Current Limit − Peak current that can be delivered to the output.

Dropout Voltage − The input−output voltage differential at which the circuit ceases to regulate against further reduction in input voltage. Measured when the output voltage has dropped 100 mV from the nominal value obtained at 14 V input, dropout voltage is dependent upon load current and junction temperature.

Input Output Differential − The voltage difference between the unregulated input voltage and the regulated output voltage for which the regulator will operate.

Input Voltage − The DC voltage applied to the input terminals with respect to ground.

Line Regulation − The change in output voltage for a change in the input voltage. The measurement is made under conditions of low dissipation or by using pulse techniques such that the average chip temperature is not significantly affected.

Load Regulation − The change in output voltage for a change in load current at constant chip temperature.

Long Term Stability − Output voltage stability under accelerated life−test conditions after 1000 hours with maximum rated voltage and junction temperature.

Quiescent Current − The part of the positive input current that does not contribute to the positive load current, i.e., the regulator ground lead current.

Ripple Rejection − The ratio of the peak−to−peak input ripple voltage to the peak−to−peak output ripple voltage.

Short Circuit Current Limit − Peak current that can be delivered by the outPut when forced to 0 V.

Temperature Stability of V_{OUT} − The percentage change in output voltage for a thermal variation from room temperature to either temperature extreme.

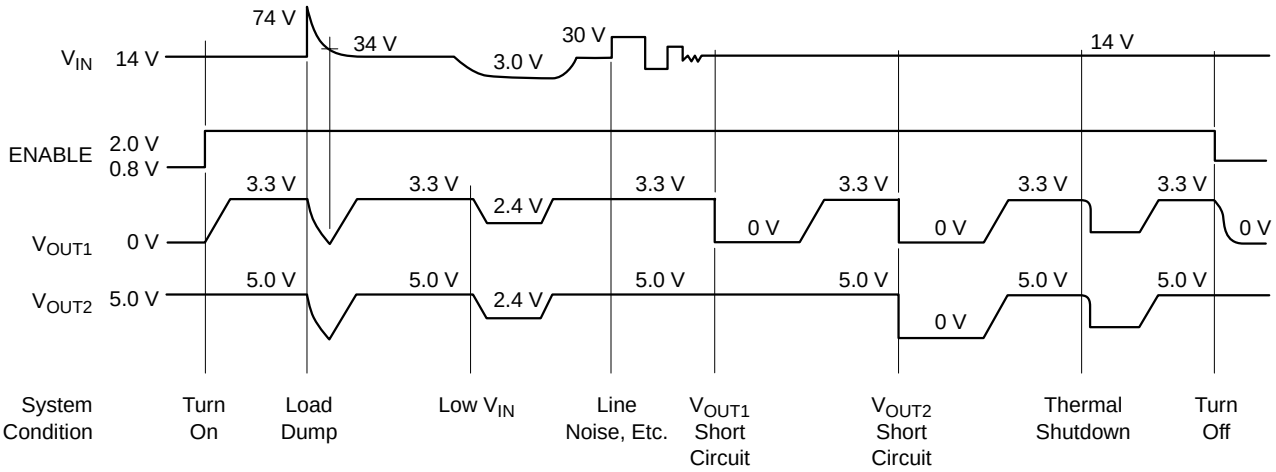


Figure 2. Typical Circuit Waveform

APPLICATION NOTES

General

The CS8481 is a Micropower dual regulator. All bias required to operate the internal circuitry is derived from the standby output, V_{OUT2}. If this output experiences an over current situation and collapses, then V_{OUT1} will also collapse (see Figure 2).

If there is critical circuitry that must remain active under most conditions it should be connected to V_{OUT2}. Any circuitry that is likely to be subjected to a short circuit, e.g., circuitry outside the module, should be connected to V_{OUT1}.

External Capacitors

Output capacitors are required for stability with the CS8481. Without them, the regulator outputs will oscillate. Actual size and type may vary depending upon the application load and temperature range. Capacitor effective series resistance (ESR) is also a factor in the IC stability. Worst−case is determined at the minimum ambient temperature and maximum load expected.

Output capacitors can be increased in size to any desired value above the minimum. One possible purpose of this would be to maintain the output voltages during brief conditions of negative input transients that might be characteristic of a particular system.

Capacitors must also be rated at all ambient temperatures expected in the system. To maintain regulator stability down to −40°C, capacitors rated at that temperature must be used.

More information on capacitor selection for SMART REGULATOR®s is available in the SMART REGULATOR application note, “Compensation for Linear Regulators,” document number SR003AN/D, available through the Literature Distribution Center or via our website at http://www.onsemi.com.

ENABLE

The ENABLE function controls V_{OUT1}. When ENABLE is high, V_{OUT1} is on. When ENABLE is low, V_{OUT1} is off.

Calculating Power Dissipation in a Dual Output Linear Regulator

The maximum power dissipation for a dual output regulator (Figure 3) is

$$P_{D(max)} = (V_{IN(max)} - V_{OUT1(min)})I_{OUT1(max)} + (V_{IN(max)} - V_{OUT2(min)})I_{OUT2(max)} + V_{IN(max)}I_Q \quad (1)$$

where:

$V_{IN(max)}$ is the maximum input voltage,

$V_{OUT1(min)}$ is the minimum output voltage from V_{OUT1},

$V_{OUT2(min)}$ is the minimum output voltage from V_{OUT2},

$I_{OUT1(max)}$ is the maximum output current, for the application,

$I_{OUT2(max)}$ is the maximum output current, for the application, and

I_Q is the quiescent current the regulator consumes at both $I_{OUT1(max)}$ and $I_{OUT2(max)}$.

Once the value of $P_{D(max)}$ is known, the maximum permissible value of $R_{\theta JA}$ can be calculated:

$$R_{\Theta JA} = \frac{150^\circ C - T_A}{P_D} \quad (2)$$

The value of $R_{\theta JA}$ can be compared with those in the package section of the data sheet. Those packages with $R_{\theta JA}$'s less than the calculated value in equation 2 will keep the die temperature below 150°C.

In some cases, none of the packages will be sufficient to dissipate the heat generated by the IC, and an external heatsink will be required.

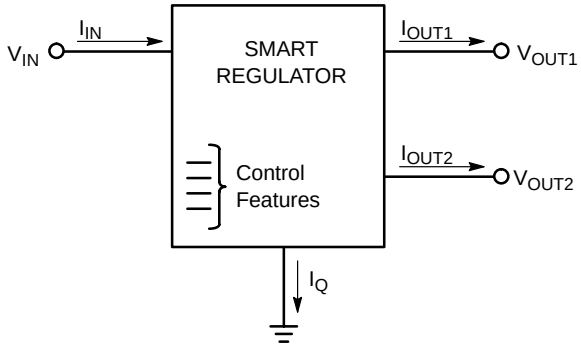


Figure 3. Dual Output Regulator With Key Performance Parameters Labeled.

Heat Sinks

A heat sink effectively increases the surface area of the package to improve the flow of heat away from the IC and into the surrounding air.

Each material in the heat flow path between the IC and the outside environment will have a thermal resistance. Like series electrical resistances, these resistances are summed to determine the value of $R_{\theta JA}$:

$$R_{\Theta JA} = R_{\Theta JC} + R_{\Theta CS} + R_{\Theta SA} \quad (3)$$

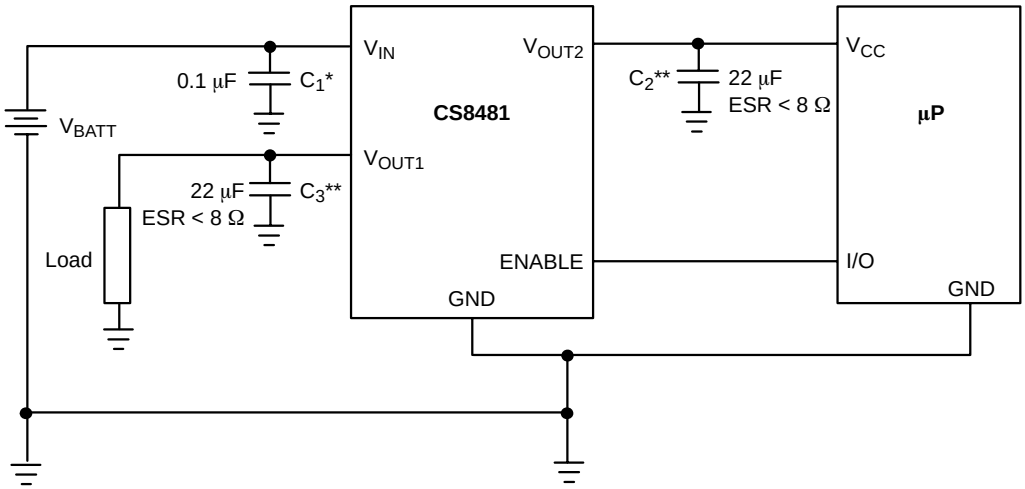
where:

$R_{\theta JC}$ = the junction−to−case thermal resistance,

$R_{\theta CS}$ = the case−to−heatsink thermal resistance, and

$R_{\theta SA}$ = the heatsink−to−ambient thermal resistance.

$R_{\theta JC}$ appears in the package section of the data sheet. Like $R_{\theta JA}$, it too is a function of package type. $R_{\theta CS}$ and $R_{\theta SA}$ are functions of the package type, heatsink and the interface between them. These values appear in heat sink data sheets of heat sink manufacturers.



* C_1 required if regulator is located far from power supply filter.

** C_2 and C_3 required for stability. Capacitor must operate at minimum temperature expected during system operations.

Figure 4. Test and Application Circuit

PACKAGE DIMENSIONS

D^2PAK−5
DP SUFFIX
CASE 936AC−01
ISSUE O

For D^2PAK Outline and Dimensions − Contact Factory

PACKAGE THERMAL DATA

Parameter		D^2PAK−5	Unit
$R_{\theta JC}$	Typical	2.4	°C/W
$R_{\theta JA}$	Typical	10−50*	°C/W

* Depending on thermal properties of substrate. $R_{\theta JA} = R_{\theta JC} + R_{\theta CA}$

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