Datasheet, V1.2, 06 Feb 2007

CCM-PFC

ICE1PCS02

ICE1PCS02G

Standalone Power Factor Correction (PFC) Controller in Continuous Conduction Mode (CCM) with Input Brown-Out Protection

Power Management & Supply

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Page	Subjects(major changes since last revision)
	Update package information

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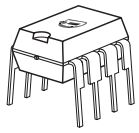
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CCM-PFC

ICE1PCS02
ICE1PCS02G

Standalone Power Factor Correction (PFC) Controller in Continuous Conduction Mode (CCM) with Input Brown-Out Protection

ICE1PCS02
PG-DIP-8



ICE1PCS02G
PG-DSO-8



Product Highlights

- **Leadfree DIP and DSO Package**
- **Wide Input Range**
- **Direct sensing, Input Brown-Out Detection**
- **Optimized for applications which require fast Startup**
- **Output Power Controllable by External Sense Resistor**
- **Fast Output Dynamic Response during Load Jumps**
- **Trimmed, internal fixed Switching Frequency (65kHz)**

Features

- Ease of Use with Few External Components
- Supports Wide Input Range
- Average Current Control
- External Current and Voltage Loop Compensation for Greater User Flexibility
- Trimmed internal fixed Switching Frequency (65kHz±7.7% at 25°C)
- Direct sensing, Input Brown-Out Detection with Hysteresis
- Short Startup(SoftStart) duration
- Max Duty Cycle of 97% (typ)
- Trimmed Internal Reference Voltage (5V±2%)
- VCC Under-Voltage Lockout
- Cycle by Cycle Peak Current Limiting
- Over-Voltage Protection
- Open Loop Detection
- Soft Overcurrent Protection
- Enhanced Dynamic Response
- Fulfills Class D Requirements of IEC 1000-3-2

Description

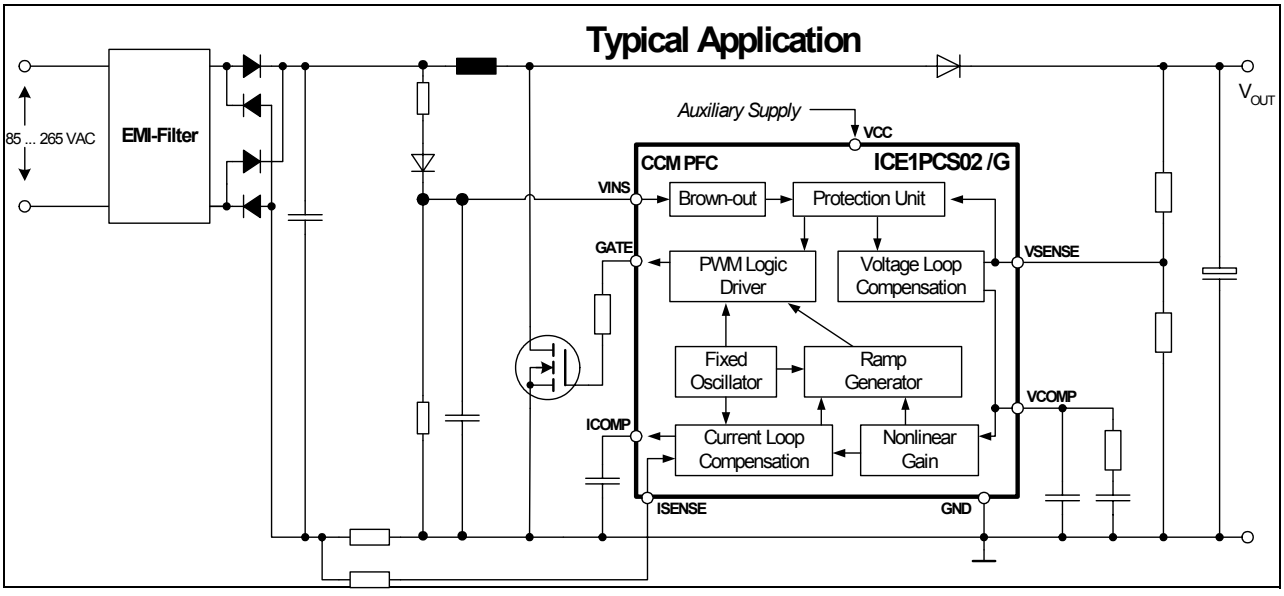
The ICE1PCS02/G is a 8-pin wide input range controller IC for active power factor correction converters. It is designed for converters in boost topology, and requires few external components. Its power supply is recommended to be provided by an external auxiliary supply which will switch on and off the IC.

The IC operates in the CCM with average current control, and in DCM only under light load condition. The switching frequency is trimmed and fixed internally at 65kHz. Both current and voltage loop compensations are done externally to allow full user control.

There are various protection features incorporated to ensure safe system operation conditions. The internal reference is trimmed (5V±2%) to ensure precise protection and output control level.

The ICE1PCS02/G is a design variant of ICE1PCS01 to incorporate the new input brown-out protection function and optimised to have a faster startup time with controlled peak startup current.

Typical Application



Type	Package
ICE1PCS02	PG-DIP-8
ICE1PCS02G	PG-DSO-8

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1 Pin Configuration and Functionality

1.1 Pin Configuration

Pin	Symbol	Function
1	GND	IC Ground
2	ICOMP	Current Loop Compensation
3	ISENSE	Current Sense Input
4	VINS	Brown-out Sense Input
5	VCOMP	Voltage Loop Compensation
6	VSENSE	V_{OUT} Sense (Feedback) Input
7	VCC	IC Supply Voltage
8	GATE	Gate Drive Output

Package PG-DIP-8 / PG-DSO-8

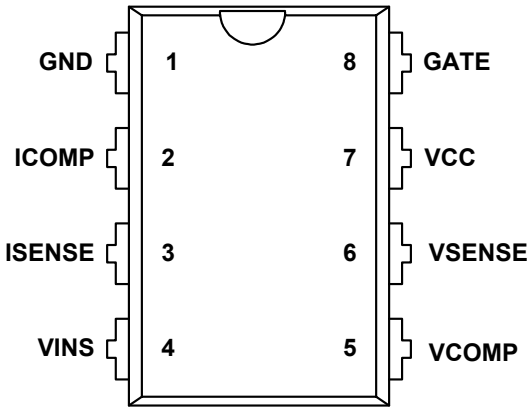


Figure 1 Pin Configuration (top view)

1.2 Pin Functionality

GND (Ground)

The ground potential of the IC.

ICOMP (Current Loop Compensation)

Low pass filter and compensation of the current control loop. The capacitor which is connected at this pin integrates the output current of OTA2 and averages the current sense signal.

ISENSE (Current Sense Input)

The ISENSE Pin senses the voltage drop at the external sense resistor (R1). This is the input signal for the average current regulation in the current loop. It is also fed to the peak current limitation block.

During power up time, high inrush currents cause high voltage drop at R1, driving currents into pin 3 which could be beyond the absolute maximum ratings. Therefore a series resistor (R2) of around 220Ω is recommended in order to limit this current into the IC.

VINS (Brown-out Sense Input)

This VINS pin senses a filtered input voltage divider and detects for the input voltage Brown-out condition. A Brown-out condition of VINS<0.8V, shuts down the IC. The IC turns on at VINS>1.5V.

VSENSE (Voltage Sense/Feedback)

The output bus voltage is sensed at this pin via a resistive divider. The reference voltage for this pin is 5V.

VCOMP (Voltage Loop Compensation)

This pin provides the compensation of the output voltage loop with a compensation network to ground (see Figure 2).

VCC (Power Supply)

The VCC pin is the positive supply of the IC and should be connected to an external auxiliary supply. The operating range is between 10V and 21V. The turn-on threshold is at 11.2V and under voltage occurs at 10.2V. There is no internal clamp for a limitation of the power supply.

GATE

The GATE pin is the output of the internal driver stage, which has a capability of 1.5A source and sink current.

Its gate drive voltage is internally clamped at 11.5V (typically).

2 Representative Block diagram

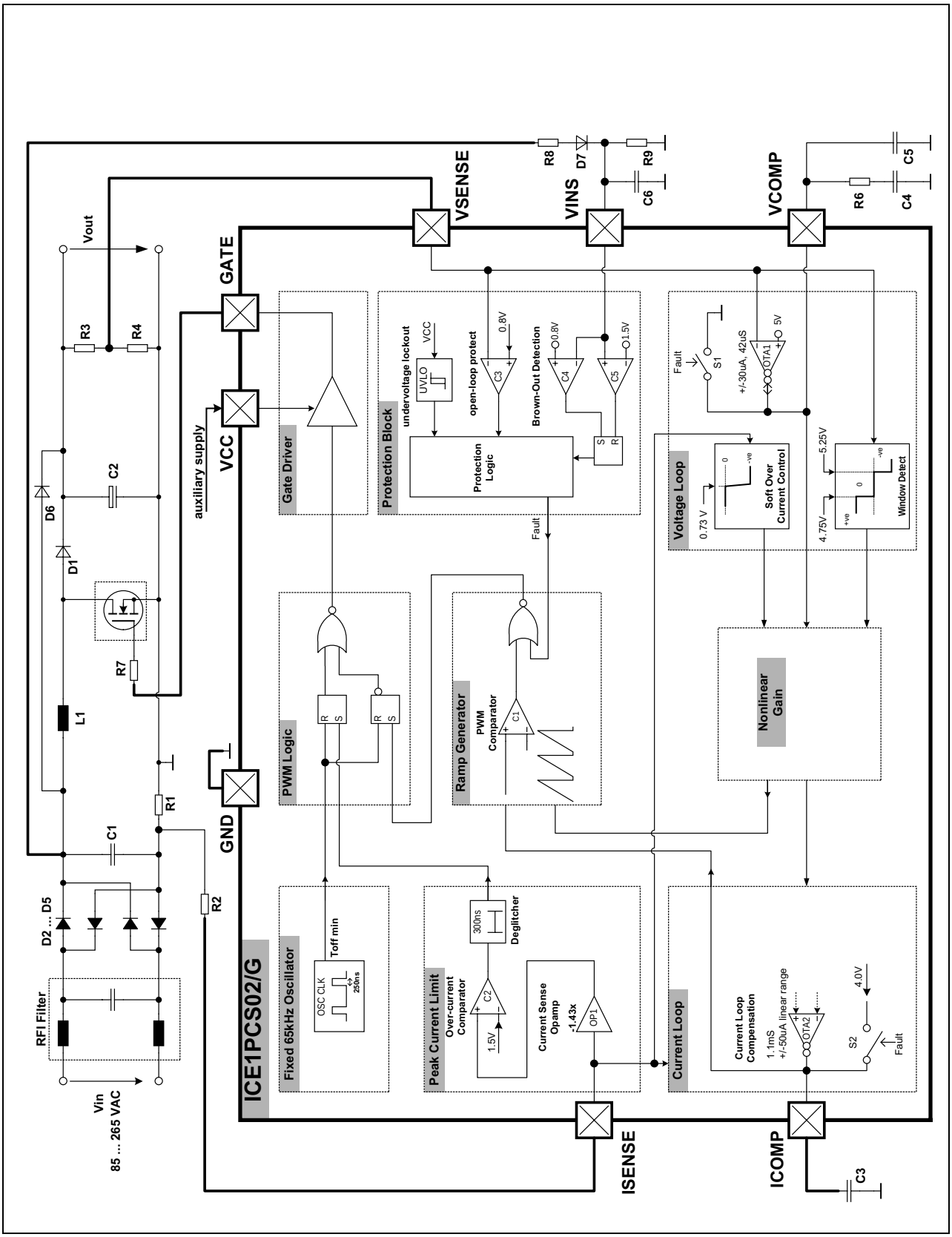


Figure 2 Representative Block diagram

3 Functional Description

3.1 General

The ICE1PCS02/G is a 8 pin control IC for power factor correction converters. It comes in both DIP and DSO packages and is suitable for wide range line input applications from 85 to 265 VAC. The IC supports converters in boost topology and it operates in continuous conduction mode (CCM) with average current control.

It is a design derivative from the ICE1PCS01/G with the differences in the supporting functions, namely the input brown-out detection, internal fixed switching frequency 65kHz and shortened startup time.

The IC operates with a cascaded control; the inner current loop and the outer voltage loop. The inner current loop of the IC controls the sinusoidal profile for the average input current. It uses the dependency of the PWM duty cycle on the line input voltage to determine the corresponding input current. This means the average input current follows the input voltage as long as the device operates in CCM. Under light load condition, depending on the choke inductance, the system may enter into discontinuous conduction mode (DCM) resulting in a higher harmonics but still meeting the Class D requirement of IEC 1000-3-2.

The outer voltage loop controls the output bus voltage. Depending on the load condition, OTA1 establishes an appropriate voltage at VCOMP pin which controls the amplitude of the average input current.

The IC is equipped with various protection features to ensure safe operating condition for both the system and device.

3.2 Power Supply

An internal under voltage lockout (UVLO) block monitors the VCC power supply. As soon as it exceeds 11.2V and both voltages at pin 6 (VSENSE) >0.8V and pin 4 (VINS) >1.5V, the IC begins operating its gate drive and performs its Startup as shown in Figure 3.

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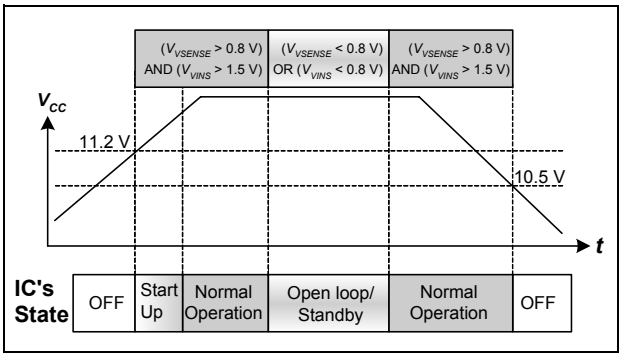


Figure 3 State of Operation respect to VCC

If VCC drops below 10.2V, the IC is off. The IC will then be consuming typically 200µA, whereas consuming 18mA during normal operation.

The IC can be turned off and forced into standby mode by pulling down the voltage at pin 6 (VSENSE) to lower than 0.8V. In this standby mode, the current consumption is reduced to 3mA. Other condition that can result in the standby mode is when a Brown-out condition occurs, ie pin 4 (VINS) <0.8V.

3.3 Start-up

Figure 4 shows the operation of voltage loop's OTA1 during startup. The VCOMP pin is pull internally to ground via switch S1 during UVLO and other fault conditions (see later section on "System Protection").

During power up when V_{OUT} is less than 85% of the rated level, it sources a constant 30µA into the compensation network at pin 5 (VCOMP) causing the voltage at this pin to rise linearly. This results in a controlled linear increase of the input current from 0A thus reducing the stress on the external component.

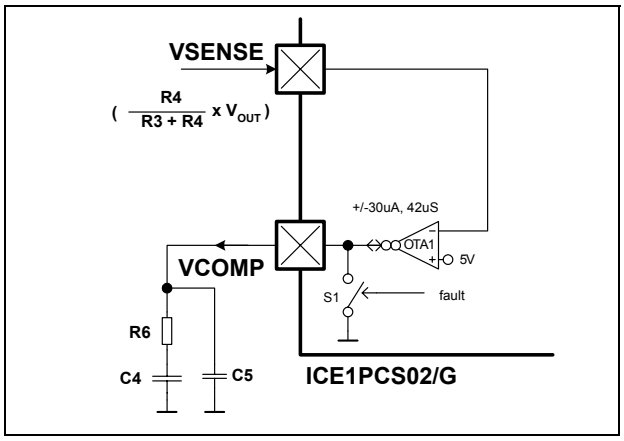


Figure 4 Startup Circuit

As V_{OUT} has not reached within 5% from the rated value, VCOMP voltage is level-shifted by the window detect block as shown in Figure 5, to ensure there is no long period of low or no current.

When V_{OUT} approaches its rated value, OTA1's sourcing current drops and so does the level shift of the window detect block. The normal voltage loop then takes control.

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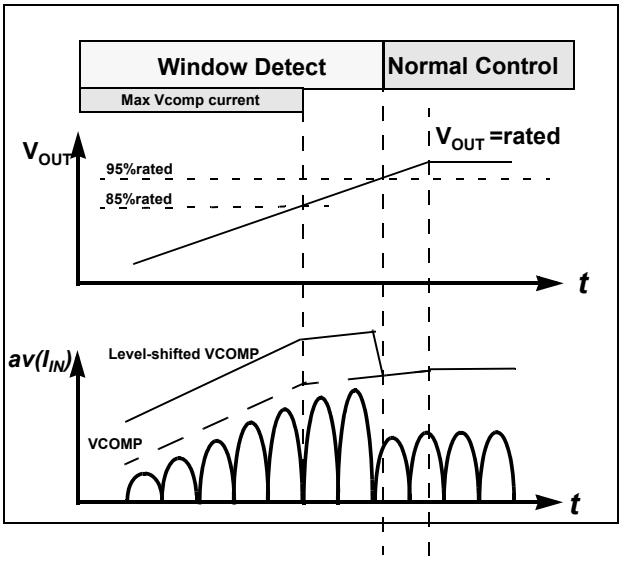


Figure 5 Startup with controlled maximum current

ICE1PCS02/G is different from ICE1PCS01/G in this block as it does not has a reduced current (~10uA in ICE1PCS01/G) during startup. The OTA1 in ICE1PCS02/G has the same maximum source current of 30uA (typ) in startup as in the normal operation. This higher sourcing current in the startup time, will charge VCOMP faster to its normal operating point, which in turn results in a faster startup for V_{OUT}.

3.4 System Protection

The IC provides several protection features in order to ensure the PFC system in safe operating range:

- VCC Undervoltage Lockout (UVLO)
- Input Brown-out Detection (IBOP)
- Soft Over Current Control (SOC)
- Peak Current Limit (PCL)
- Open-Loop Detection (OLP)
- Output Over-Voltage Protection (OVP)

After the system is supplied with the correct level of VCC and V_{IN}, the system will enter into its normal mode of operation. Figure 6 shows situation when these protections features are active, as a function of the output voltage V_{OUT}.

An activation of the UVLO, IBOP and OLP results in the internal fault signal going high and brings the IC into the standby mode.

As the function of UVLO has already described in the earlier “Power Supply” section, the following sections continue to describe the functionality of these protection features.

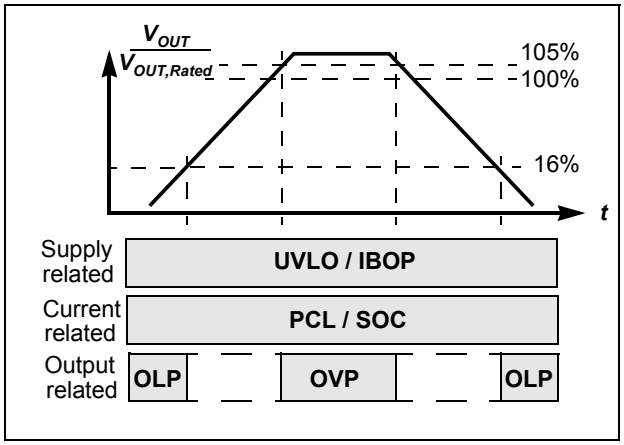


Figure 6 Protection Features

3.4.1 Input Brown-Out Protection (IBOP)

Brown-out occurs when the input voltage V_{IN} falls below the minimum input voltage of the design (i.e. 85V for universal input voltage range) and the VCC has not entered into the V_{CCUVLO} level yet. For a system without IBOP, the boost converter will increasingly draw a higher current from the mains at a given output power which may exceed the maximum design values of the input current.

ICE1PCS02/G provides a new IBOP feature whereby it senses directly the input voltage for Input Brown-Out condition via an external resistor/capacitor/diode network as shown in Figure 7. This network provides a filtered value of V_{IN} which turns the IC on when the voltage at pin 4 (VINS) is more than 1.5V. The IC enters into the standby mode when VINS goes below 0.8V. The hysteresis prevents the system to oscillate between normal and standby mode. Note also that V_{IN} needs to at least 16% of the rated V_{OUT} in order to overcome OLP and powerup the system.

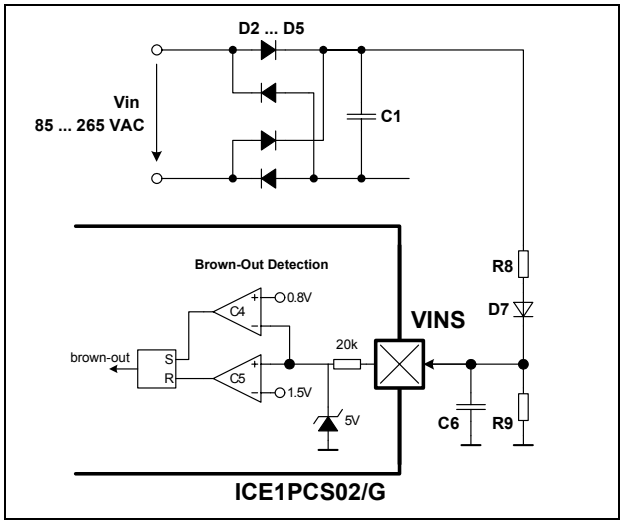


Figure 7 Input Brown-Out Protection (IBOP)

3.4.2 Soft Over Current Control (SOC)

The IC is designed **not** to support any output power that corresponds to a voltage lower than -0.73V at the ISENSE pin. A further increase in the inductor current, which results in a lower ISENSE voltage, will activate the Soft Over Current Control (SOC). This is a soft control as it does not directly switch off the gate drive like the PCL. It acts on the nonlinear gain block to result in a reduced PWM duty cycle.

3.4.3 Peak Current Limit (PCL)

The IC provides a cycle by cycle peak current limitation (PCL). It is active when the voltage at pin 3 (ISENSE) reaches -1.08V. This voltage is amplified by OP1 by a factor of -1.43 and connected to comparator C2 with a reference voltage of 1.5V as shown in Figure 8. A deglitcher with 300ns after the comparator improves noise immunity to the activation of this protection.

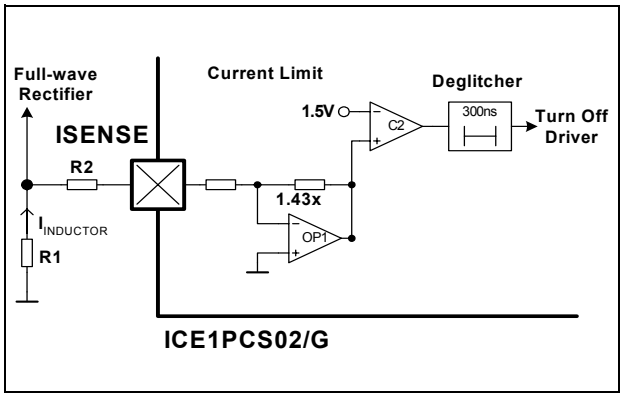


Figure 8 Peak Current Limit (PCL)

3.4.4 Open Loop Protection (OLP)

Whenever VSENSE voltage falls below 0.8V, or equivalently V_{OUT} falls below 16% of its rated value, it indicates an open loop condition (i.e. VSENSE pin not connected) or an insufficient input voltage V_{IN} for normal operation. In this case, most of the blocks within the IC will be shutdown. It is implemented using comparator C3 with a threshold of 0.8V as shown in the IC block diagram in Figure 2.

3.4.5 Over-Voltage Protection (OVP)

Whenever V_{OUT} exceeds the rated value by 5%, the over-voltage protection OVP is active as shown in Figure 6. This is implemented by sensing the voltage at pin VSENSE with respect to a reference voltage of 5.25V. A VSENSE voltage higher than 5.25V will immediately reduce the output duty cycle, bypassing the normal voltage loop control. This results in a lower input power to reduce the output voltage V_{OUT}.

3.5 Fixed Switching Frequency

ICE1PCS02/G has an internally fixed switching frequency as opposed to the ICE1PCS01/G which can be externally set. This frequency is trimmed to 65kHz with an accuracy +/-7.7% at 25°C.

3.6 Average Current Control

3.6.1 Complete Current Loop

The complete system current loop is shown in Figure 9.

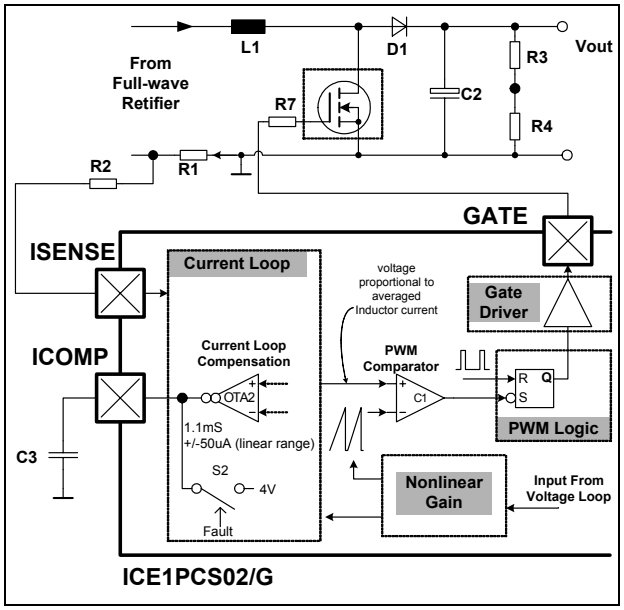


Figure 9 Complete System Current Loop

It consists of the current loop block which averages the voltage at pin ISENSE, resulted from the inductor current flowing across R1. The averaged waveform is compared with an internal ramp in the ramp generator and PWM block. Once the ramp crosses the average waveform, the comparator C1 turns on the driver stage through the PWM logic block. The Nonlinear Gain block defines the amplitude of the inductor current. The following sections describe the functionality of each individual blocks.

3.6.2 Current Loop Compensation

The compensation of the current loop is done at the ICOMP pin. This is the OTA2 output and a capacitor C3 has to be installed at this node to ground (see Figure 9). Under normal mode of operation, this pin gives a voltage which is proportional to the averaged inductor current. This pin is internally shorted to 4V in the event of standby mode.

3.6.3 Pulse Width Modulation (PWM)

The IC employs an average current control scheme in continuous conduction mode (CCM) to achieve the power factor correction.

Assuming the voltage loop is working and output voltage is kept constant, the off duty cycle D_{OFF} for a CCM PFC system is given as

$$D_{OFF} = \frac{V_{IN}}{V_{OUT}}$$

From the above equation, D_{OFF} is proportional to V_{IN}.

The objective of the current loop is to regulate the average inductor current such that it is proportional to the off duty cycle D_{OFF}, and thus to the input voltage V_{IN}. Figure 10 shows the scheme to achieve the objective.

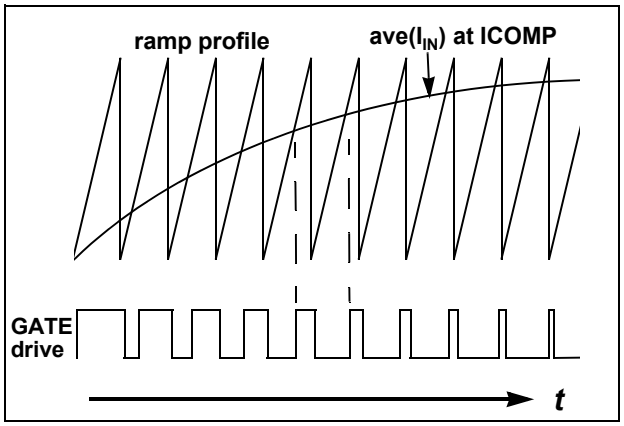


Figure 10 Average Current Control in CCM

The PWM is performed by the intersection of a ramp signal with the averaged inductor current at pin 5 (ICOMP). The PWM cycle starts with the Gate turn off for a duration of T_{OFFMIN} (250ns typ.) and the ramp is kept discharged. The ramp is then allowed to rise after T_{OFFMIN} expires. The off time of the boost transistor ends at the intersection of the ramp signal and the averaged current waveform. This results in the proportional relationship between the average current and the off duty cycle D_{OFF}.

Figure 11 shows the timing diagrams of T_{OFFMIN} and the PWM waveforms.

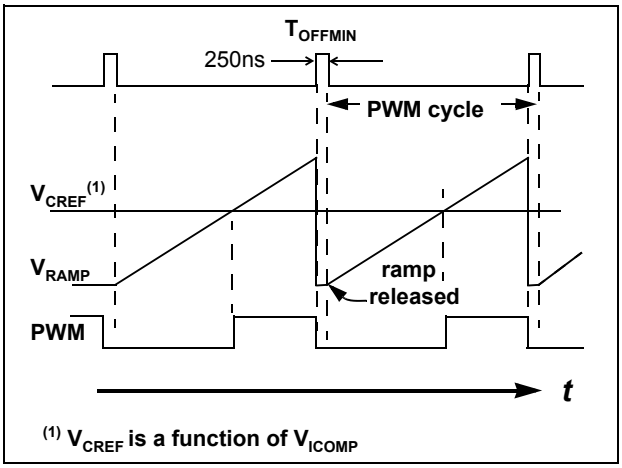


Figure 11 Ramp and PWM waveforms

3.6.4 Nonlinear Gain Block

The nonlinear gain block controls the amplitude of the regulated inductor current. The input of this block is the voltage at pin VCOMP. This block has been designed to support the wide input voltage range (85-265VAC).

3.7 PWM Logic

The PWM logic block prioritizes the control input signals and generates the final logic signal to turn on the driver stage. The speed of the logic gates in this block, together with the width of the reset pulse T_{OFFMIN}, are designed to meet a maximum duty cycle D_{MAX} of 95% at the GATE output.

In case of high input currents which result in Peak Current Limitation, the GATE will be turned off immediately and maintained in off state for the current PWM cycle. The signal Toffmin resets (highest priority, overriding other input signals) both the current limit latch and the PWM on latch as illustrated in Figure 12.

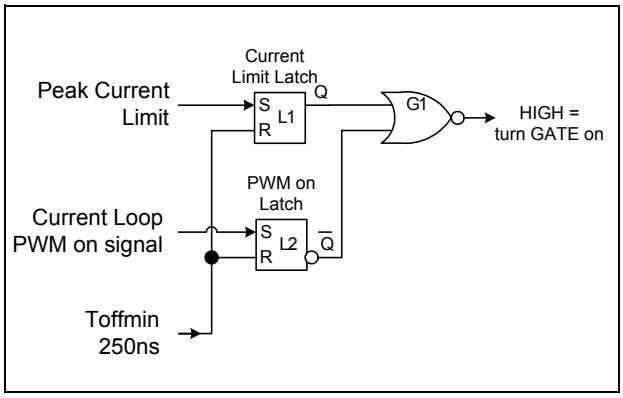


Figure 12 PWM Logic

3.8 Voltage Loop

The voltage loop is the outer loop of the cascaded control scheme which controls the PFC output bus voltage V_{OUT}. This loop is closed by the feedback sensing voltage at VSENSE which is a resistive divider tapping from V_{OUT}. The pin VSENSE is the input of OTA1 which has an accurate internal reference of 5V (+/-2%). Figure 13 shows the important blocks of this voltage loop.

3.8.1 Voltage Loop Compensation

The compensation of the voltage loop is installed at the VCOMP pin (see Figure 13). This is the output of OTA1 and the compensation must be connected at this pin to ground. The compensation is also responsible for the soft start function which controls an increasing AC input current during start-up.

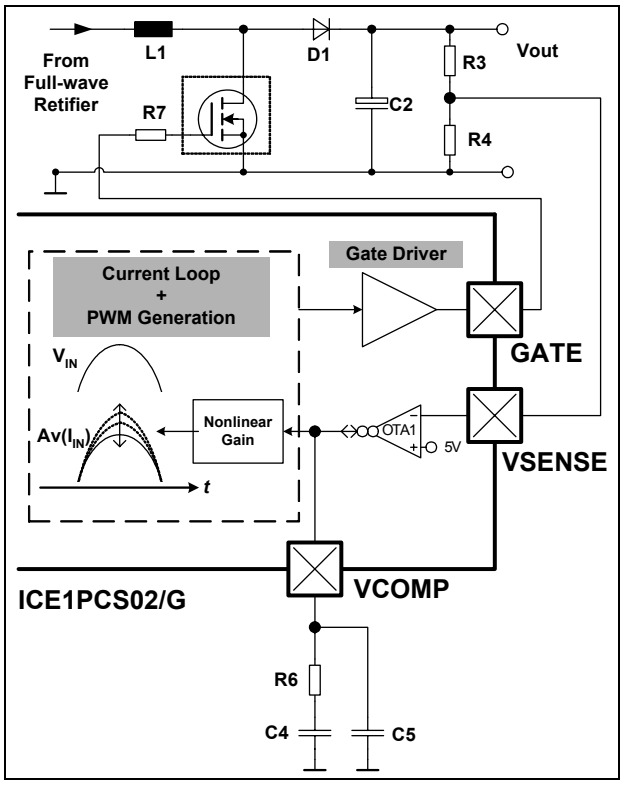


Figure 13 Voltage Loop

3.8.2 Enhanced Dynamic Response

Due to the low frequency bandwidth of the voltage loop, the dynamic response is slow and in the range of about several 10ms. This may cause additional stress to the bus capacitor and the switching transistor of the PFC in the event of heavy load changes.

The IC provides therefore a “window detector” for the feedback voltage V_{VSENSE} at pin 6 (VSENSE). Whenever V_{VSENSE} exceeds the reference value (5V) by ±5%, it will act on the nonlinear gain block which in turn affect the gate drive duty cycle directly. This change in duty cycle is bypassing the slow changing VCOMP voltage, thus results in a fast dynamic response of V_{OUT}.

3.9 Output Gate Driver

The output gate driver is a fast totem pole gate drive. It has an in-built cross conduction currents protection and a Zener diode Z1 (see Figure 14) to protect the external transistor switch against undesirable over voltages. The maximum voltage at pin 8 (GATE) is typically clamped at 11.5V.

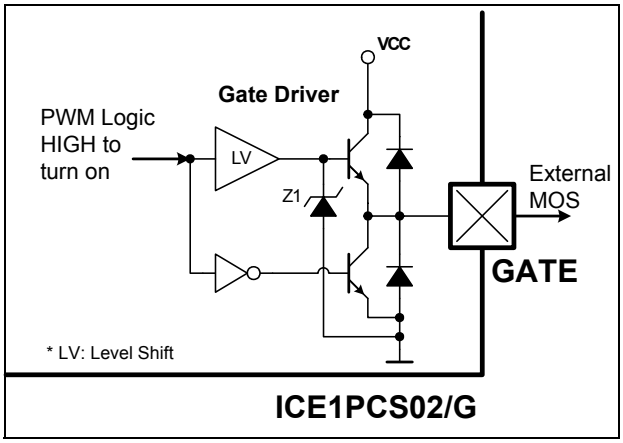


Figure 14 Gate Driver

The output is active HIGH and at VCC voltages below the under voltage lockout threshold V_{CCUVLO}, the gate drive is internally pull low to maintain the off state.

4 Electrical Characteristics

4.1 Absolute Maximum Ratings

Note: Absolute maximum ratings are defined as ratings, which when being exceeded may lead to destruction of the integrated circuit.

Parameter	Symbol	Limit Values		Unit	Remarks
		min.	max.		
V_{CC} Supply Voltage	V_{CC}	-0.3	22	V	
VINS Voltage	V_{VINS}	-0.3	20	V	
ICOMP Voltage	V_{ICOMP}	-0.3	7	V	
ISENSE Voltage	V_{ISENSE}	-24	7	V	
ISENSE Current	I_{ISENSE}	-1	1	mA	Recommended *R2*=220Ω
VSENSE Voltage	V_{VSENSE}	-0.3	7	V	
VSENSE Current	I_{VSENSE}	-1	1	mA	*R3*>400kΩ
VCOMP Voltage	V_{VCOMP}	-0.3	7	V	
GATE Voltage	V_{GATE}	-0.3	22	V	Clamped at 11.5V(typ) if driven internally.
Junction Temperature	T_j	-40	150	°C	
Storage Temperature	T_S	-55	150	°C	
Thermal Resistance Junction-Ambient for PG-DSO-8	R_{thJA} *(DSO)*	-	185	K/W	PG-DSO-8
Thermal Resistance Junction-Ambient for PG-DIP-8	R_{thJA}*(DIP)*	-	90	K/W	PG-DIP-8
ESD Protection	V_{ESD}	-	2	kV	Human Body Model[1)]

1) According to EIA/JESD22-A114-B (discharging a 100pF capacitor through a 1.5kΩ series resistor)

4.2 Operating Range

Note: Within the operating range the IC operates as described in the functional description.

Parameter	Symbol	Limit Values		Unit	Remarks
		min.	max.		
V_{CC} Supply Voltage	V_{CC}	V_{CCUVLO}	21	*V*	
Junction Temperature	T_{JCon}	-40	125	°C	

4.3 Characteristics

Note: The electrical characteristics involve the spread of values within the specified supply voltage and junction temperature range T_J from – 40 °C to 125°C.Typical values represent the median values, which are related to 25°C. ***If not otherwise stated, a supply voltage of V_{CC} =15V is assumed for test condition****.*

4.3.1 Supply Section

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
VCC Turn-On Threshold	V_{CCon}	10.5	11.2	11.9	V	
VCC Turn-Off Threshold/ Under Voltage Lock Out	V_{CCUVLO}	9.4	10.2	10.8	V	
VCC Turn-On/Off Hysteresis	V_{CChy}	0.8	1	1.3	V	
Start Up Current Before V_{CCon}	$I_{CCstart}$	50	100	200	µA	V_{VCC}=V_{VCCon} -0.1V
Operating Current with active GATE	I_{CCHG}	9.6	13	16.3	mA	C_L= 4.7nF
Operating Current during Standby	$I_{CCStdby}$	1.7	2.3	2.9	mA	V_{VSENSE}= 0.5V

4.3.2 PWM Section

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Fixed Oscillator Frequency	f_{SW}	56	65	72	kHz	
	f_{SW}	60	65	70	kHz	T_j = 25°C
Max. Duty Cycle	D_{MAX}	94	97	99.3	%	
Min. Duty Cycle	D_{MIN}			0	%	V_{VCOMP}= 0V, V_{VSENSE}= 5V V_{ICOMP}= 6.4V
Min. Off Time	T_{OFFMIN}	100	250	600	ns	V_{VCOMP}= 5V, V_{VSENSE}= 5V V_{ISENSE}= 0.1V

4.3.3 System Protection Section

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Open Loop Protection (OLP) VSENSE Threshold	V_{OLP}	0.77	0.81	0.86	V	
Peak Current Limitation (PCL) ISENSE Threshold	V_{PCL}	-1.15	-1.08	-1.00	V	
Soft Over Current Control (SOC) ISENSE Threshold	V_{SOC}	-0.79	-0.73	-0.66	V	
Output Over-Voltage Protection (OVP)	V_{OVP}	5.12	5.25	5.38	V	
Input Brown-out Protection (IBOP) High to Low Threshold	V_{VINSL}	0.76	0.82	0.88	V	
Input Brown-out Protection (IBOP) Low to High Threshold	V_{VINSH}	1.40	1.50	1.60	V	
Input Brown-out Protection (IBOP) VINS Bias Current	I_{VIN0V}	-1.0	-0.2	0	µA	V_{VINS}= 0V

4.3.4 Current Loop Section

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
OTA2 Transconductance Gain	Gm_{OTA2}	0.75	0.95	1.15	mS	At Temp = 25°C
OTA2 Output Linear Range[1)]	I_{OTA2}		+/- 50		µA	
ICOMP Voltage during OLP	V_{ICOMPF}	3.6	4.0		V	V_{VSENSE}= 0.5V

1) The parameter is not subject to production test - verified by design/characterization

4.3.5 Voltage Loop Section

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
OTA1 Reference Voltage	V_{OTA1}	4.90	5.00	5.10	V	
OTA1 Transconductance Gain	Gm_{OTA1}	31.5	42	52.5	µS	
OTA1 Max. Source Current At Startup	$I_{OTA1SO1}$	21	30	38	µA	V_{VSENSE}= 4V V_{VCOMP}= 0V
OTA1 Max. Source Current Under Normal Operation	I_{OTA1SO}	21	30	38	µA	V_{VSENSE}= 4.25V V_{VCOMP}= 4V
OTA1 Max. Sink Current Under Normal Operation	I_{OTA1SK}	21	30	38	µA	V_{VSENSE}= 6V V_{VCOMP}= 4V
Enhanced Dynamic Response VSENSE High Threshold VSENSE Low Threshold	 V_{Hi} V_{Lo}	 5.12 4.63	 5.25 4.75	 5.38 4.87	 V V	
VSENSE Input Bias Current at 5V	I_{VSEN5V}	0		1.5	µA	V_{VSENSE}= 5V
VSENSE Input Bias Current at 1V	I_{VSEN1V}	0		1	µA	V_{VSENSE}= 1V
VCOMP Voltage during OLP	V_{VCOMPF}	0	0.2	0.4	V	V_{VSENSE}= 0.5V I_{VCOMP}= 0.5mA

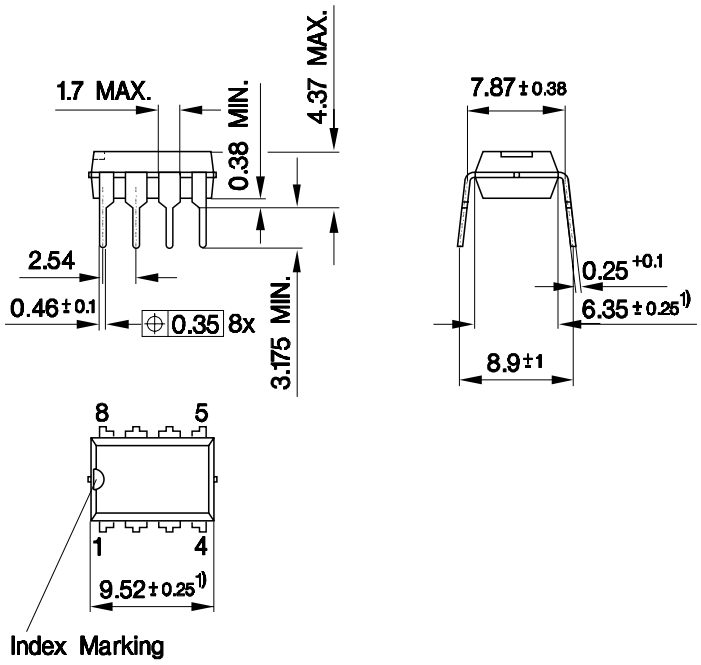
4.3.6 Driver Section

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
GATE Low Voltage	V_{GATEL}	-	-	1.2	V	V_{CC} = 5 V I_{GATE} = 5 mA
		-	-	1.5	V	V_{CC} = 5 V I_{GATE} = 20 mA
		-	0.8	-	V	I_{GATE} = 0 A
		-	1.6	2.0	V	I_{GATE} = 20 mA
		-0.2	0.2	-	V	I_{GATE} = -20 mA
GATE High Voltage	V_{GATEH}	-	11.5	-	V	V_{CC} = 20V C_L = 4.7nF
		-	10.5	-	V	V_{CC} = 11V C_L = 4.7nF
		-	7.5	-	V	V_{CC} = V_{VCCoff} + 0.2V C_L = 4.7nF
GATE Rise Time	t_r	-	60	-	ns	V_{Gate} = 2V ...8V C_L = 4.7nF
GATE Fall Time	t_f	-	40	-	ns	V_{Gate} = 8V ...2V C_L = 4.7nF
GATE Current, Peak, Rising Edge	I_{GATE}	-1.5	-	-	A	C_L = 4.7nF[1)]
GATE Current, Peak, Falling Edge	I_{GATE}	-	-	1.5	A	C_L = 4.7nF[1)]

[1)] Design characteristics (not meant for production testing)

5 Outline Dimension

PG-DIP-8-4
(Plastic Dual In-Line Package)

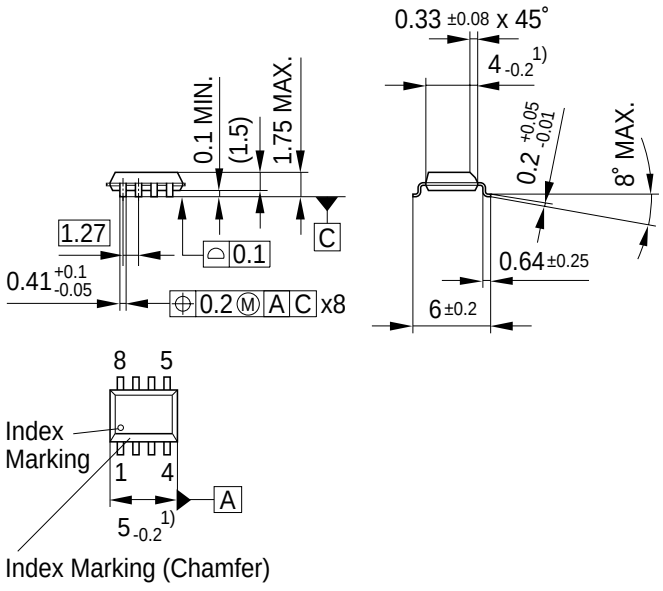


Dimensions in mm

1) Does not include plastic or metal protrusion of 0.25 max. per side

Figure 15 PG-DIP-8 Outline Dimension

PG-DSO-8-13
(Plastic Dual Small Outline)



Dimensions in mm

1) Does not include plastic or metal protrusion of 0.15 max. per side

Figure 16 PG-DSO-8 Outline Dimension

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