Data Sheet
October 1997

microelectronics group

Lucent Technologies
Bell Labs Innovations

# L7591 Subscriber Line Interface Circuit Protector

## Features

- Shunts lightning pulses to ground
  — Positive or negative 30 A, 10 x 1000 µs
  — Positive or negative 40 A, 5 x 320 µs
  — Positive or negative 80 A, 2 x 10 µs
- Power-cross protection
  — 3.5 APEAK, 50 Hz to 60 Hz, 1 s
  — 5.0 APEAK, 50 Hz to 60 Hz, 10 ms
- Gate trigger current, 15 mA max
- Up to –80 V capability
- Holding current, 150 mA min

## Pin Information

**Table 1. Pin Description**
(Applies to DIP and SONB packages)

| Pin | Symbol | Name/Function |
|---|---|---|
| 1 | TIP | Tip signal from customer. |
| 2 | VS | Supply voltage to gate (–20 V to –80 V). |
| 3 | — | Test Point, do not use. |
| 4 | RING | Ring signal from customer. |
| 5 | PR | Protected ring signal to line-feed-circuitry. |
| 6 | GND | Device ground/fault current return. |
| 7 | GND | Device ground/fault current return. |
| 8 | PT | Protected tip signal to line-feed circuitry. |

Note: Pins 1 and 4 must always be connected to the protection resistors shown in Figures 4 and 5 (Line Feed Circuitry). The SLIC can be connected either to the protected outputs (pins 5 and 8) or to the inputs (pins 1 and 4).

## Description

The L7591 Subscriber Line Interface Circuit (SLIC) Protector is designed to protect line-feed circuitry from fault-induced lightning and power-cross surge pulses. If a fault current forces TIP and/or RING to a more negative voltage than Vs, current is conducted through the trip circuit. When the specified trip current level is reached, transistors PNPN1 and/or PNPN2 will turn on and "crowbar" the majority of the current to ground. If similar pulses force TIP and/or RING to a more positive state than ground, diodes D1 and/or D2 will conduct the pulse to ground. The L7591 SLIC Protector is available in an 8-pin, plastic DIP (L7591AB) and in an 8-pin, plastic SONB package (L7591AS).

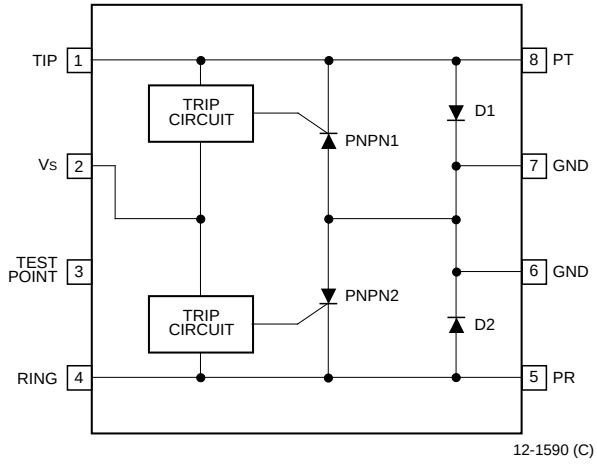



**Figure 1. Functional and Pin Diagram**

## Absolute Maximum Ratings (At 25 °C)

Stresses in excess of the Absolute Maximum Ratings can cause permanent damage to the device. These are absolute stress ratings only. Functional operation of the device is not implied at these or any other conditions in excess of those given in the operational sections of the data sheet. Exposure to Absolute Maximum Ratings for extended periods can adversely affect the device reliability.

| Parameter | Symbol | Value | Unit |
|---|---|---|---|
| Ambient Operating Temperature | $T_A$ | –40 to +85 | °C |
| Storage Temperature Range | $T_{stg}$ | –40 to +125 | °C |
| Pin Soldering Temperature (t = 15 s max) | — | 300 | °C |
| Supply Voltage | $V_S$ | –83 | V |
| Peak Pulse Current: * (See Figure 2.) | | | |
| 10 x 1000 µs | — | 30 | A |
| 5 x 320 µs | — | 40 | A |
| 2 x 10 µs | — | 80 | A |
| Nonrepetitive Peak ON-state Current: | | | |
| t = 1 s, f = 50 Hz to 60 Hz | — | 3.5 | A |
| t = 10 ms, f = 50 Hz to 60 Hz | — | 5 | A |
| Maximum Gate Current (Half Sine Wave 10 ms) | — | 2 | A |
| Maximum Voltage: | | | |
| TIP or RING to Gnd | — | –100 | V |
| $V_S$ to Gnd | — | –80 | V |

*Pulse Waveform Data:

| | | |
|---|---|---|
| 10 x 1000 µs | tr = 10 µs | tp = 1000 µs |
| 5 x 320 µs | tr = 5 µs | tp = 320 µs |
| 2 x 10 µs | tr = 2 µs | tp = 10 µs |

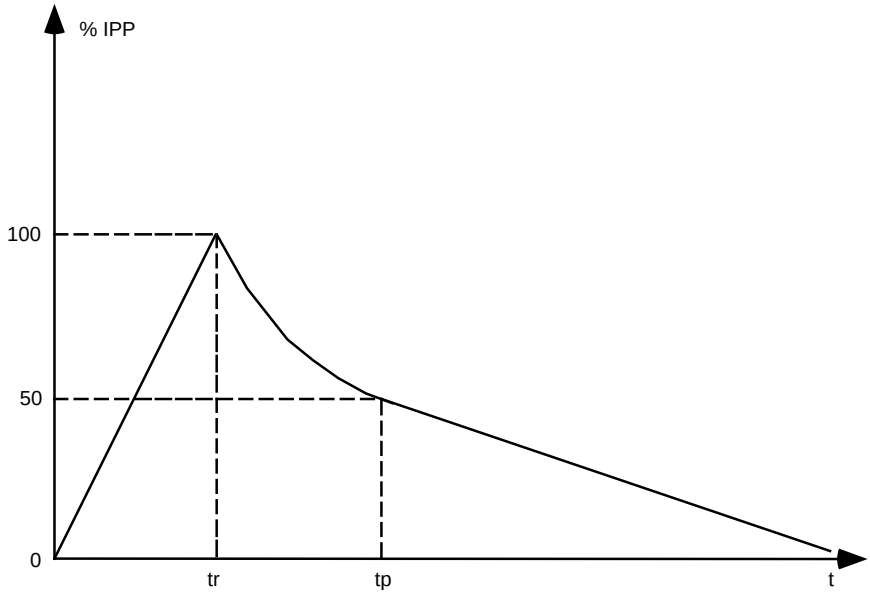



**Figure 2. Pulse Waveform**

## Electrical Specifications ($T_A$ = 25 °C)

The minimum and/or maximum limits specified for the parameters are based on the absolute system. The algebraic sign only applies to the direction of the parameter. These requirements apply to either the TIP or RING terminal; however, the device is capable of simultaneous Tip and Ring surges and continuous current, as noted below in Tip and Ring leads. See Figure 3 and Table 5 for symbol and test condition definition.

**Table 2. Electrical Characteristics D1 and D2**

| Characteristic | Symbol | Test Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Forward Voltage | $V_F$ | $I_P$ = 5 A, $t_P$ = 1 ms | — | 1.6 | 3 | V |
| Peak Forward Voltage | $V_{FP}$ | $I_{PP}$ = 30 A, 10 x 1000 µs | — | 5.2 | 15 | V |

**Table 3. Electrical Characteristics, PNPN Circuitry**

| Characteristic | Symbol | Test Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Gate Trigger Current | $I_{GT}$ | $V_S$ = 48 V | 0.2 | — | 15 | mA |
| Holding Current | $I_H$ | $t_P$ = 10 ms, $V_S$ = 48 V | –150 | –250 | — | mA |
| Trip Voltage | $V_T$ | dc | — | $V_S$ –2.0 | $V_S$ –2.8 | V |
| Dynamic Trip Voltage | $V_{SGL}$ | $I_{PP}$ = 30 A, $V_S$ = –48 V, 10 x 1000 µs | — | –51 | –63 | V |
| Reverse Leakage Current: $V_S$ to Tip or Ring | $I_{RG}$ | $V_S$ = –75 V | | | | |
| $T_A$ = 25 °C | — | — | — | 0.12 | 5 | µA |
| $T_A$ = 70 °C | — | — | — | — | 50 | µA |
| dv/dt Sensitivity | — | Tip or Ring Lead | ±1000 | — | — | V/µs |
| On-state Voltage: | $V_{ON}$ | $t_P$ = 1 ms | | | | |
| $I_T$ = 0.5 A | — | — | — | –1.3 | — | V |
| $I_T$ = 3.0 A | — | — | — | –2.3 | — | V |

**Table 4. Electrical Characteristics, Diode and PNPN Circuitry**

| Characteristic | Symbol | Test Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Reverse Leakage Current: (Gate Open) | $I_R$ | $V_R$ = –85 V | | | | |
| $T_A$ = 25 °C | — | — | — | 0.14 | 5 | µA |
| $T_A$ = 70 °C | — | — | — | — | 50 | µA |
| Off-state Capacitance: | $C_{off}$ | f = 1 MHz | | | | |
| $V_R$ = –3 V | — | — | — | 50 | — | pF |
| $V_R$ = –48 V | — | — | — | 40 | — | pF |

## Characteristic Curves

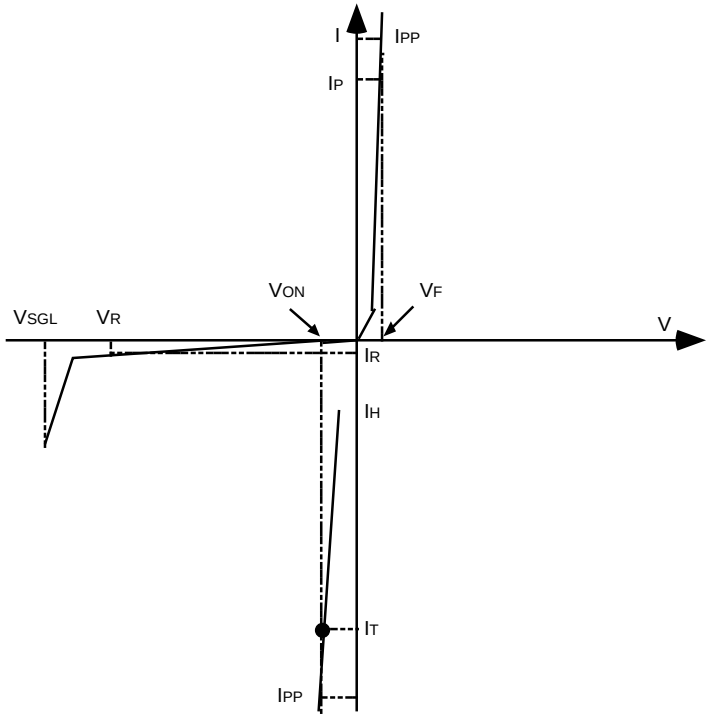
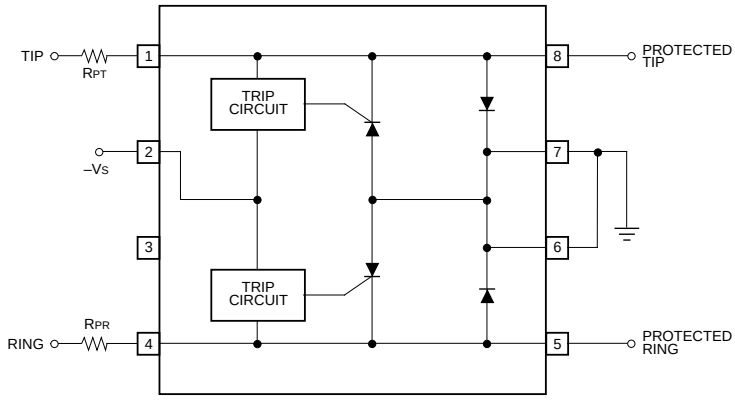



**Figure 3. Typical Trip Characteristics of the SLIC Protector**

**Table 5. Symbols Definition**

| Symbol | Parameter |
|---|---|
| $I_H$ | PNPN holding current |
| $I_{GT}$ | Gate trigger current out of pin $V_S$ |
| $I_P$ | Pulse current |
| $I_{PP}$ | Peak pulse current |
| $I_{RG}$ | Reverse leakage current $V_S$ to Tip or Ring |
| $I_T$ | Tip or Ring current when PNPN is on |
| $I_R$ | Reverse leakage current, Tip or Ring to Ground |
| $V_F$ | Forward voltage, Tip or Ring to Ground |
| $V_{FP}$ | Peak forward voltage, Tip or Ring to Ground |
| $V_T$ | Trip voltage, Tip or Ring to $V_S$ |
| $V_{SGL}$ | Dynamic trip voltage, Tip or Ring to $V_S$ |
| $V_{ON}$ | PNPN on voltage at $I_T$ |
| $V_R$ | Tip or Ring voltage when PNPN is off |
| Coff | Off-state capacitance, Tip or Ring to Ground |

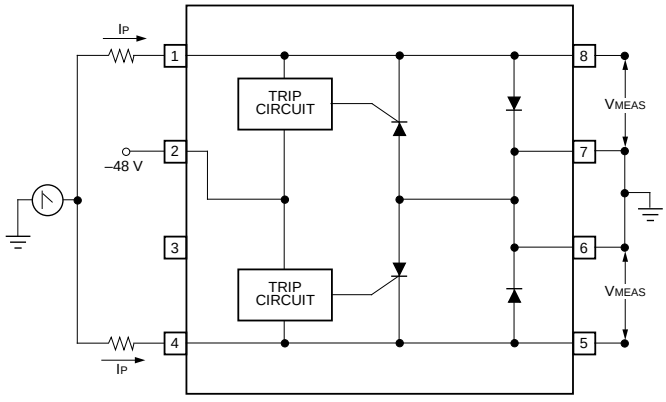
## Applications




12-1632 (C)

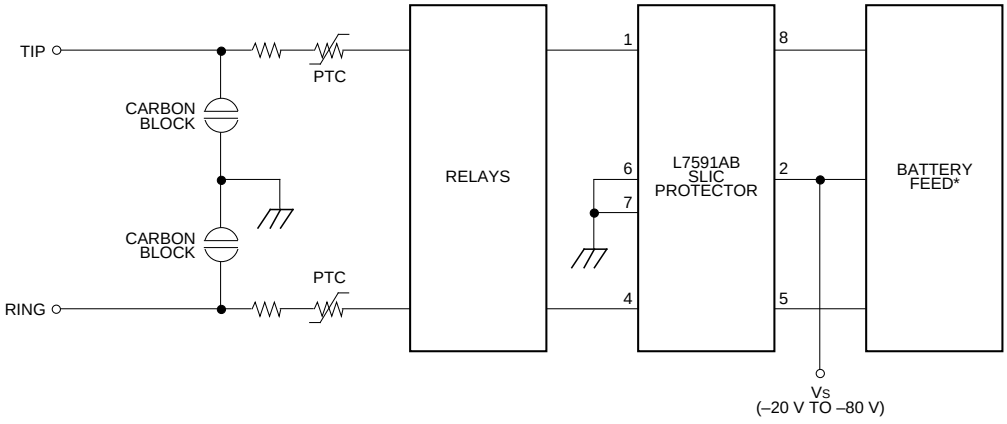
RPT and RPR must be properly selected for proper operation and/or response.

**Figure 4. Standard Configuration**




12-1596 (C)

**Figure 5. Test Circuit**




12-1598 (C)

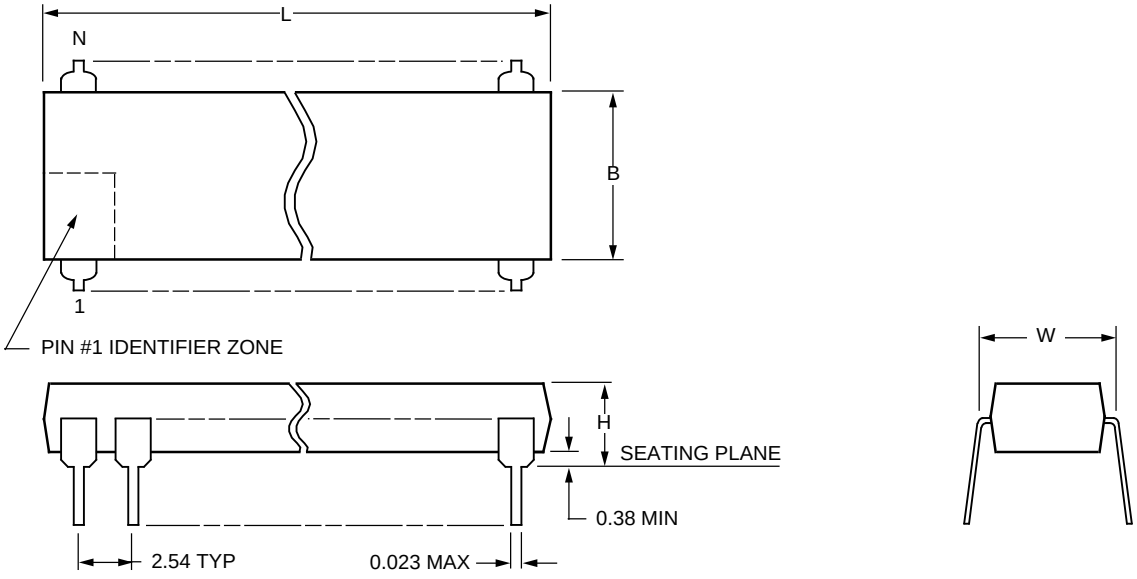
*An example device is Lucent Technologies Microelectronics Group's LB1276 High Balance SLIC.

**Figure 6. Fully Protected Electronic TIP-RING Interface** (Not all devices needed in all applications)

# Outline Drawings

## 8-Pin DIP (L7591AB)

Dimensions are in millimeters.



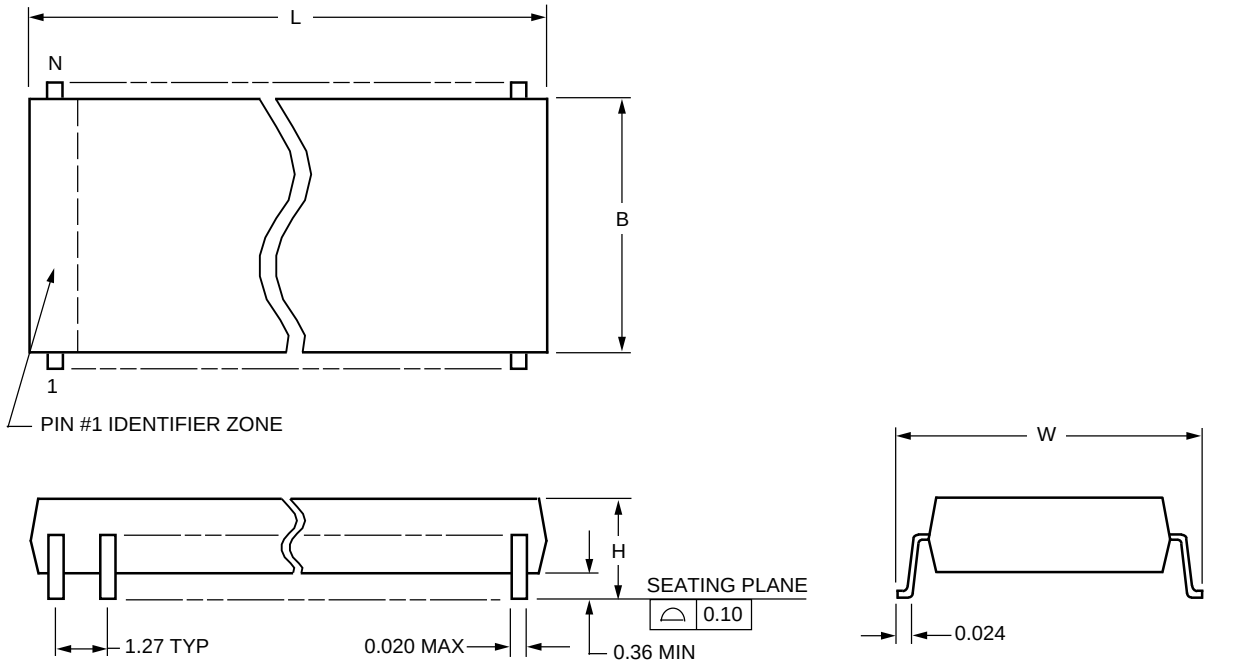

5-4410r.1

| Package Description | Number of Pins (N) | Package Dimensions | | | |
|---|---|---|---|---|---|
| | | Maximum Length (L) | Maximum Width Without Leads (B) | Maximum Width Including Leads (W) | Maximum Height Above Board (H) |
| PDIP3 (Plastic Dual-In-Line Package) | 8 | 10.16 | 6.48 | 7.87 | 5.46 |

## Outline Drawings (continued)

### 8-Pin, SONB (L7591AS)

Dimensions are in millimeters.




5-4414r.2

| Package Description | Number of Pins (N) | Package Dimensions | | | |
|---|---|---|---|---|---|
| | | Maximum Length (L) | Maximum Width Without Leads (B) | Maximum Width Including Leads (W) | Maximum Height Above Board (H) |
| SONB (Small Outline, Narrow Body) | 8 | 5.08 | 4.01 | 6.17 | 1.73 |

## Ordering Information

| Device Part No. | Description | Package | Comcode |
|---|---|---|---|
| ATTL7591AB | SLIC Protector | 8-Pin DIP | 107056582 |
| ATTL7591AS | SLIC Protector | 8-Pin SONB | 107056590 |
| ATTL7591AS-TR | SLIC Protector | 8-Pin SONB (Tape and Reel) | 107232787 |

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