

# DATA SHEET

**74ABT00**

Quad 2-input NAND gate

Product specification

1995 Sep 18

IC23 Data Handbook

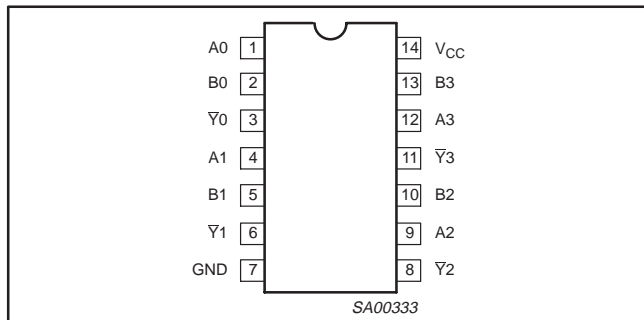
# Quad 2-input NAND gate

# 74ABT00

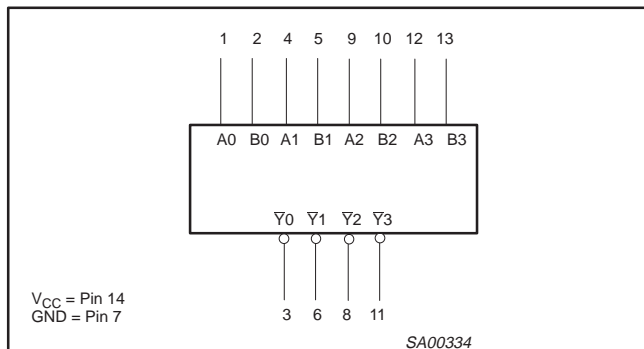
### QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS $T_{amb} = 25^{\circ}\text{C};$ $GND = 0V$	TYPICAL	UNIT
$t_{PLH}$ $t_{PHL}$	Propagation delay An or Bn to $\bar{Y}_n$	$C_L = 50\text{pF};$ $V_{CC} = 5V$	2.5 2.0	ns
$t_{OSLH}$ $t_{OSHL}$	Output to Output skew		0.4	ns
$C_{IN}$	Input capacitance	$V_I = 0V$ or $V_{CC}$	3	pF
$I_{CC}$	Total supply current	Outputs disabled; $V_{CC} = 5.5V$	50	$\mu\text{A}$

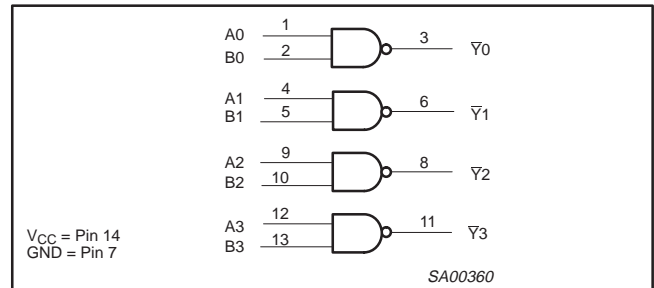
### PIN CONFIGURATION



### LOGIC SYMBOL



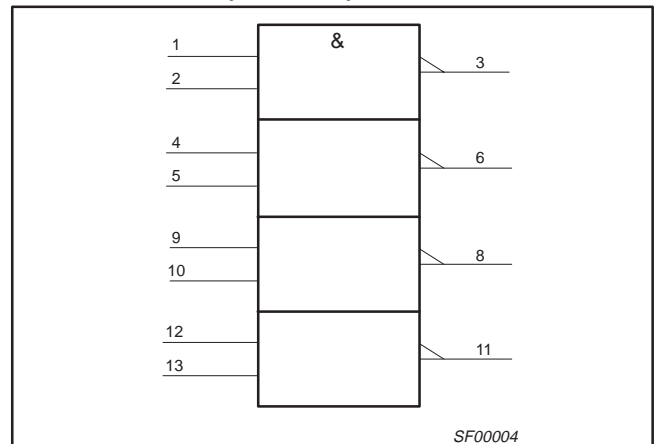
### LOGIC DIAGRAM



### PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
1, 2, 4, 5, 9, 10, 12, 13	An-Bn	Data inputs
3, 6, 8, 11	$\bar{Y}_n$	Data outputs
7	GND	Ground (0V)
14	$V_{CC}$	Positive supply voltage

### LOGIC SYMBOL (IEEE/IEC)



### FUNCTION TABLE

INPUTS		OUTPUT
A	B	$\bar{Y}$
L	L	H
L	H	H
H	L	H
H	H	L

#### NOTES:

- H = High voltage level
- L = Low voltage level

### ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	DWG NUMBER
14-Pin Plastic DIP	-40°C to +85°C	74ABT00 N	74ABT00 N	SOT27-1
14-Pin plastic SO	-40°C to +85°C	74ABT00 D	74ABT00 D	SOT108-1
14-Pin Plastic SSOP Type II	-40°C to +85°C	74ABT00 DB	74ABT00 DB	SOT337-1
14-Pin Plastic TSSOP Type I	-40°C to +85°C	74ABT00 PW	74ABT00PW DH	SOT402-1

## Quad 2-input NAND gate

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ABSOLUTE MAXIMUM RATINGS<sup>1, 2</sup>

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
$V_{CC}$	DC supply voltage		-0.5 to +7.0	V
$I_{IK}$	DC input diode current	$V_I < 0$	-18	mA
$V_I$	DC input voltage <sup>3</sup>		-1.2 to +7.0	V
$I_{OK}$	DC output diode current	$V_O < 0$	-50	mA
$V_{OUT}$	DC output voltage <sup>3</sup>	output in Off or High state	-0.5 to +5.5	V
$I_{OUT}$	DC output current	output in Low state	40	mA
$T_{stg}$	Storage temperature range		-65 to 150	°C

## NOTES:

- Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
- The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

## RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS		UNIT
		MIN	MAX	
$V_{CC}$	DC supply voltage	4.5	5.5	V
$V_I$	Input voltage	0	$V_{CC}$	V
$V_{IH}$	High-level input voltage	2.0		V
$V_{IL}$	Low-level input voltage		0.8	V
$I_{OH}$	High-level output current		-15	mA
$I_{OL}$	Low-level output current		20	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0	5	ns/V
$T_{amb}$	Operating free-air temperature range	-40	+85	°C

## DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			$T_{amb} = +25^\circ\text{C}$			$T_{amb} = -40^\circ\text{C}$ to $+85^\circ\text{C}$		
			MIN	TYP	MAX	MIN	MAX	
$V_{IK}$	Input clamp voltage	$V_{CC} = 4.5\text{V}; I_{IK} = -18\text{mA}$		-0.9	-1.2		-1.2	V
$V_{OH}$	High-level output voltage	$V_{CC} = 4.5\text{V}; I_{OH} = -15\text{mA}; V_I = V_{IL}$ or $V_{IH}$	2.5	2.9		2.5		V
$V_{OL}$	Low-level output voltage	$V_{CC} = 4.5\text{V}; I_{OL} = 20\text{mA}; V_I = V_{IL}$ or $V_{IH}$		0.35	0.5		0.5	V
$I_I$	Input leakage current	$V_{CC} = 5.5\text{V}; V_I = \text{GND}$ or $5.5\text{V}$		$\pm 0.01$	$\pm 1.0$		$\pm 1.0$	$\mu\text{A}$
$I_{OFF}$	Power-off leakage current	$V_{CC} = 0.0\text{V}; V_O$ or $V_I \leq 4.5\text{V}$		$\pm 5.0$	$\pm 100$		$\pm 100$	$\mu\text{A}$
$I_{CEX}$	Output High leakage current	$V_{CC} = 5.5\text{V}; V_O = 5.5\text{V}; V_I = \text{GND}$ or $V_{CC}$		5.0	50		50	$\mu\text{A}$
$I_O$	Output current <sup>1</sup>	$V_{CC} = 5.5\text{V}; V_O = 2.5\text{V}$	-50	-75	-180	-50	-180	mA
$I_{CC}$	Quiescent supply current	$V_{CC} = 5.5\text{V}; V_I = \text{GND}$ or $V_{CC}$		2	50		50	$\mu\text{A}$
$\Delta I_{CC}$	Additional supply current per input pin <sup>2</sup>	$V_{CC} = 5.5\text{V}$ ; One data input at 3.4V, other inputs at $V_{CC}$ or GND		0.25	500		500	$\mu\text{A}$

## NOTES:

- Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
- This is the increase in supply current for each input at 3.4V.

# Quad 2-input NAND gate

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## AC CHARACTERISTICS

GND = 0V;  $t_R = t_F = 2.5\text{ns}$ ;  $C_L = 50\text{pF}$ ,  $R_L = 500\Omega$

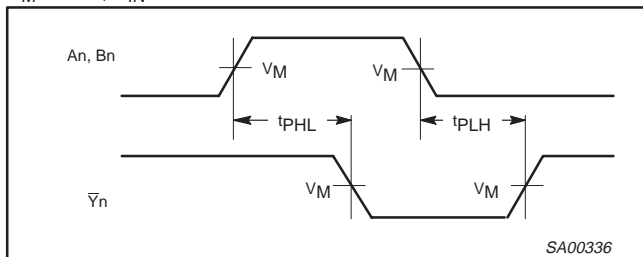
SYMBOL	PARAMETER	WAVEFORM	LIMITS					UNIT
			$T_{\text{amb}} = +25^\circ\text{C}$ $V_{\text{CC}} = +5.0\text{V}$			$T_{\text{amb}} = -40^\circ\text{C to } +85^\circ\text{C}$ $V_{\text{CC}} = +5.0\text{V} \pm 0.5\text{V}$		
			MIN	TYP	MAX	MIN	MAX	
$t_{\text{PLH}}$ $t_{\text{PHL}}$	Propagation delay An or Bn to $\bar{Y}_n$	1	1.0	2.5	3.6	1.0	4.1	ns
$t_{\text{OSHL}}$ $t_{\text{OSLH}}$	Output to Output skew An or Bn to $\bar{Y}_n$	2		0.4	0.5		0.5	ns

**NOTE:**

- Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the the same direction, either HIGH-to-LOW ( $t_{\text{OSHL}}$ ) or LOW-to-HIGH ( $t_{\text{OSLH}}$ ); parameter guaranteed by design.

## AC WAVEFORMS

$V_M = 1.5\text{V}$ ,  $V_{\text{IN}} = \text{GND to } 3.0\text{V}$



Waveform 1. Propagation delay for inverting outputs



Waveform 2. Common edge skew

## TEST CIRCUIT AND WAVEFORMS

**Test Circuit for Outputs**

**Input Pulse Definition**

**DEFINITIONS**

$R_L$  = Load resistor; see AC CHARACTERISTICS for value.

$C_L$  = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

$R_T$  = Termination resistance should be equal to  $Z_{\text{OUT}}$  of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	$t_W$	$t_R$	$t_F$
74ABT	3.0V	1MHz	500ns	2.5ns	2.5ns

SH00067

# Quad 2-input NAND gate

## 74ABT00

DIP14: plastic dual in-line package; 14 leads (300 mil)

SOT27-1



**DIMENSIONS (inch dimensions are derived from the original mm dimensions)**

UNIT	A max.	A <sub>1</sub> min.	A <sub>2</sub> max.	b	b <sub>1</sub>	c	D <sup>(1)</sup>	E <sup>(1)</sup>	e	e <sub>1</sub>	L	M <sub>E</sub>	M <sub>H</sub>	w	Z <sup>(1)</sup> max.
mm	4.2	0.51	3.2	1.73 1.13	0.53 0.38	0.36 0.23	19.50 18.55	6.48 6.20	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	2.2
inches	0.17	0.020	0.13	0.068 0.044	0.021 0.015	0.014 0.009	0.77 0.73	0.26 0.24	0.10	0.30	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.087

**Note**

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ		
SOT27-1	050G04	MO-001AA			92-11-17 95-03-11

# Quad 2-input NAND gate

## 74ABT00

**SO14: plastic small outline package; 14 leads; body width 3.9 mm**

**SOT108-1**



**DIMENSIONS (inch dimensions are derived from the original mm dimensions)**

UNIT	A max.	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	b <sub>p</sub>	c	D <sup>(1)</sup>	E <sup>(1)</sup>	e	H <sub>E</sub>	L	L <sub>p</sub>	Q	v	w	y	z <sup>(1)</sup>	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	8.75 8.55	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8° 0°
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.35 0.34	0.16 0.15	0.050	0.244 0.228	0.041	0.039 0.016	0.028 0.024	0.01	0.01	0.004	0.028 0.012	

**Note**

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ		
SOT108-1	076E06S	MS-012AB			95-01-29 97-05-22

Quad 2-input NAND gate

74ABT00

SSOP14: plastic shrink small outline package; 14 leads; body width 5.3 mm

SOT337-1



**DIMENSIONS (mm are the original dimensions)**

UNIT	A max.	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	b <sub>p</sub>	c	D <sup>(1)</sup>	E <sup>(1)</sup>	e	H <sub>E</sub>	L	L <sub>p</sub>	Q	v	w	y	Z <sup>(1)</sup>	θ
mm	2.0	0.21 0.05	1.80 1.65	0.25	0.38 0.25	0.20 0.09	6.4 6.0	5.4 5.2	0.65	7.9 7.6	1.25	1.03 0.63	0.9 0.7	0.2	0.13	0.1	1.4 0.9	8° 0°

**Note**

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT337-1		MO-150AB				<del>95-02-04</del> 96-01-18

# Quad 2-input NAND gate

# 74ABT00

**TSSOP14:** plastic thin shrink small outline package; 14 leads; body width 4.4 mm

**SOT402-1**



**DIMENSIONS (mm are the original dimensions)**

UNIT	A max.	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	b <sub>p</sub>	c	D <sup>(1)</sup>	E <sup>(2)</sup>	e	H <sub>E</sub>	L	L <sub>p</sub>	Q	v	w	y	Z <sup>(1)</sup>	θ
mm	1.10	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	5.1 4.9	4.5 4.3	0.65	6.6 6.2	1.0	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.72 0.38	8° 0°

**Notes**

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT402-1		MO-153				-94-07-12- 95-04-04



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Quad 2-input NAND gate

74ABT00

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**NOTES**

## Quad 2-input NAND gate

74ABT00

## DEFINITIONS

Data Sheet Identification	Product Status	Definition
<i>Objective Specification</i>	<b>Formative or in Design</b>	This data sheet contains the design target or goal specifications for product development. Specifications may change in any manner without notice.
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