FAIRCHILD SEMICONDUCTOR TM

November 2000

FDW2520C

Complementary PowerTrench® MOSFET

General Description

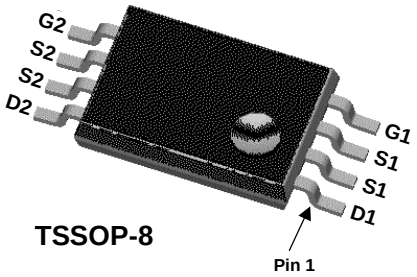
This complementary MOSFET device is produced using Fairchild's advanced PowerTrench process that has been especially tailored to minimize the on-state resistance and yet maintain low gate charge for superior switching performance.

Applications

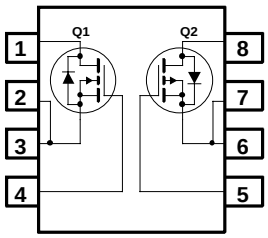
- DC/DC conversion
- Power management
- Load switch

Features

- **Q1: N-Channel**
  6 A, 20 V. $R_{DS(ON)}$ = 18 mΩ @ V_{GS} = 4.5 V
  $R_{DS(ON)}$ = 28 mΩ @ V_{GS} = 2.5 V
- **Q2: P-Channel**
  –4.4A, 20 V. $R_{DS(ON)}$ = 35 mΩ @ V_{GS} = –4.5 V
  $R_{DS(ON)}$ = 57 mΩ @ V_{GS} = –2.5 V
- High performance trench technology for extremely low $R_{DS(ON)}$
- Low profile TSSOP-8 package



TSSOP-8



Absolute Maximum Ratings T_A = 25°C unless otherwise noted

Symbol	Parameter		Q1	Q2	Units
V_{DSS}	Drain-Source Voltage		20	–20	V
V_{GSS}	Gate-Source Voltage		±12	±12	V
I_D	Drain Current - Continuous	(Note 1a)	6	–4.4	A
	- Pulsed		30	–30	
P_D	Power Dissipation	(Note 1a)	1.0		W
		(Note 1b)	0.6		
T_J, T_{STG}	Operating and Storage Junction Temperature Range		–55 to +150		°C

Thermal Characteristics

$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	(Note 1a)	125	°C/W
		(Note 1b)	208	

Package Marking and Ordering Information

Device Marking	Device	Reel Size	Tape width	Quantity
2520C	FDW2520C	13''	12mm	3000 units

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Electrical Characteristics

T_A = 25°C unless otherwise noted

Symbol	Parameter	Test Conditions	Type	Min	Typ	Max	Units
Off Characteristics							
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS} = 0 V, I_D = 250 µA V_{GS} = 0 V, I_D = –250 µA	Q1 Q2	20 –20			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	I_D = 250 µA, Referenced to 25°C I_D = –250 µA, Referenced to 25°C	Q1 Q2		14 –17		mV/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 16 V, V_{GS} = 0 V V_{DS} = –16 V, V_{GS} = 0 V	Q1 Q2			1 –1	µA
I_{GSS}	Gate-Body Leakage	V_{GS} = ±12 V, V_{DS} = 0 V V_{GS} = ±12 V, V_{DS} = 0 V	Q1 Q2			±100 ±100	nA
On Characteristics (Note 2)							
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 250 µA V_{DS} = V_{GS}, I_D = –250 µA	Q1 Q2	0.4 –0.4	1.0 –1.0	1.5 –1.5	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate Threshold Voltage Temperature Coefficient	I_D = 250 µA, Referenced to 25°C I_D = –250 µA, Referenced to 25°C	Q1 Q2		–3.3 3.1		mV/°C
$R_{DS(on)}$	Static Drain-Source On-Resistance	V_{GS} = 4.5 V, I_D = 6 A V_{GS} = 2.5 V, I_D = 5 A V_{GS} = 4.5 V, I_D = 6 A, T_J = 125°C	Q1		14 19 19	18 28 29	mΩ
		V_{GS} = –4.5 V, I_D = –4.4 A V_{GS} = –2.5 V, I_D = –3.3 A V_{GS} = –4.5 V, I_D = –4.4 A, T_J = 125°C	Q2		28 43 39	35 57 56	mΩ
$I_{D(on)}$	On-State Drain Current	V_{GS} = 4.5 V, V_{DS} = 5 V V_{GS} = –4.5 V, V_{DS} = –5 V	Q1 Q2	30 –30			A
g_{FS}	Forward Transconductance	V_{DS} = 5 V, I_D = 6 A V_{DS} = –5 V, I_D = –4.4 A	Q1 Q2		30 17		S
Dynamic Characteristics							
C_{iss}	Input Capacitance	Q1: V_{DS} = 10 V, V_{GS} = 0 V, f = 1.0 MHz Q2: V_{DS} = –10 V, V_{GS} = 0 V, f = 1.0 MHz	Q1 Q2		1325 1330		pF
C_{oss}	Output Capacitance		Q1 Q2		358 552		pF
C_{rss}	Reverse Transfer Capacitance		Q1 Q2		168 153		pF
Switching Characteristics							
$t_{d(on)}$	Turn-On Delay Time	Q1: V_{DD} = 10 V, I_D = 1 A, V_{GS} = 4.5V, R_{GEN} = 6 Ω Q2: V_{DD} = –10 V, I_D = –1 A, V_{GS} = –4.5V, R_{GEN} = 6 Ω	Q1 Q2		6 12	20 25	ns
t_r	Turn-On Rise Time		Q1 Q2		11 19	40 40	ns
$t_{d(off)}$	Turn-Off Delay Time		Q1 Q2		32 60	60 100	ns
t_f	Turn-Off Fall Time		Q1 Q2		19 37	34 70	ns
Q_g	Total Gate Charge	Q1: V_{DS} = 10 V, I_D = 6 A, V_{GS} = 4.5 V Q2: V_{DS} = –5 V, I_D = –4.4 A, V_{GS} = –4.5 V	Q1 Q2		14 14	20 20	nC
Q_{gs}	Gate-Source Charge		Q1 Q2		2.6 3.0		nC
Q_{gd}	Gate-Drain Charge		Q1 Q2		3.7 3.9		nC

Electrical Characteristics (continued)

T_A = 25°C unless otherwise noted

Symbol	Parameter	Test Conditions	Type	Min	Typ	Max	Units
Drain-Source Diode Characteristics and Maximum Ratings							
I_S	Maximum Continuous Drain-Source Diode Forward Current		Q1 Q2			0.83 –0.83	A
V_{SD}	Drain-Source Diode Forward Voltage	V_{GS} = 0 V, I_S = 0.83 A (Note 2) V_{GS} = 0 V, I_S = –0.83 A (Note 2)	Q1 Q2		0.5 –0.7	1.2 –1.2	V

Notes:

1. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.

a) $R_{\theta JA}$ is 125°C/W (steady state) when mounted on a 1 inch² copper pad on FR-4.

b) $R_{\theta JA}$ is 208°C/W (steady state) when mounted on a minimum copper pad on FR-4.

2. Pulse Test: Pulse Width < 300µs, Duty Cycle < 2.0%

Typical Characteristics: Q1

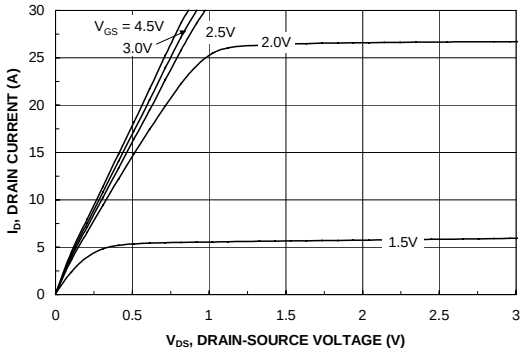


Figure 1. On-Region Characteristics.

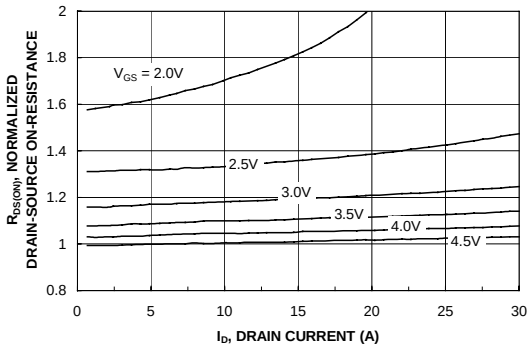


Figure 2. On-Resistance Variation with Drain Current and Gate Voltage.

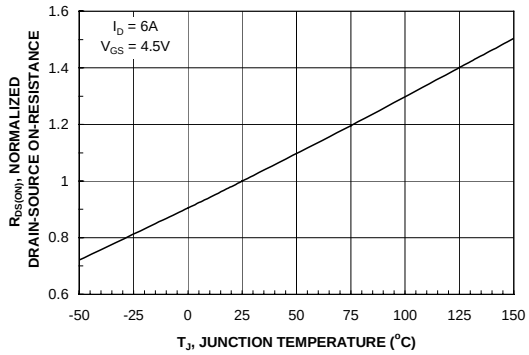


Figure 3. On-Resistance Variation with Temperature.

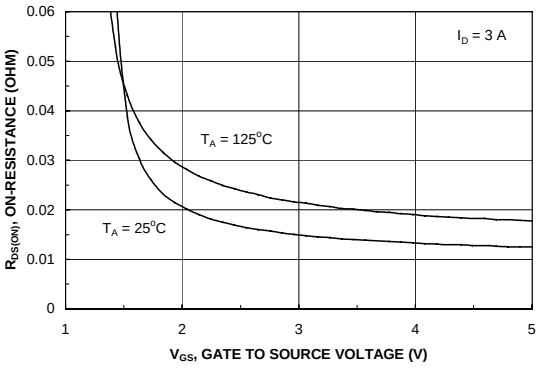


Figure 4. On-Resistance Variation with Gate-to-Source Voltage.

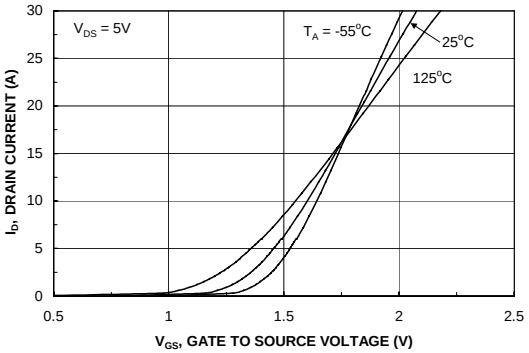


Figure 5. Transfer Characteristics.

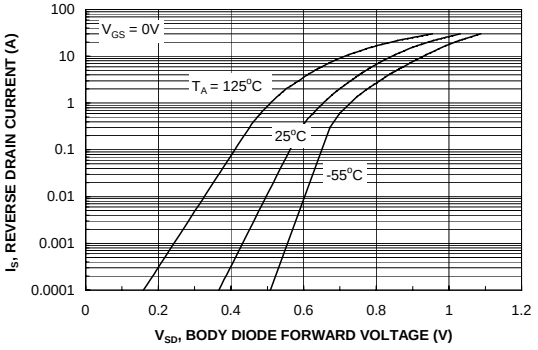


Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature.

Typical Characteristics: Q1

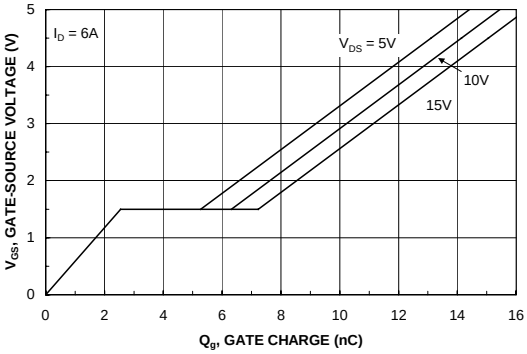


Figure 7. Gate Charge Characteristics.

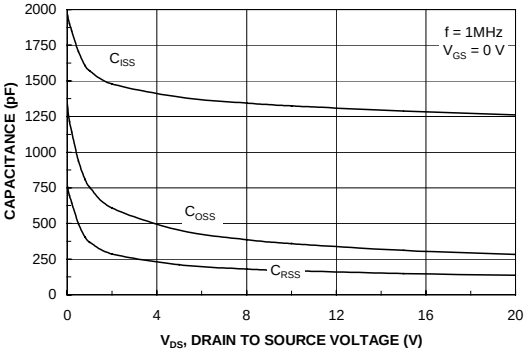


Figure 8. Capacitance Characteristics.

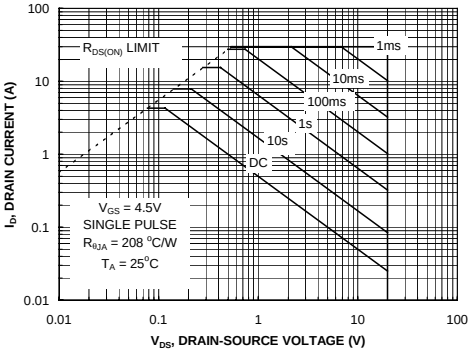


Figure 9. Maximum Safe Operating Area.

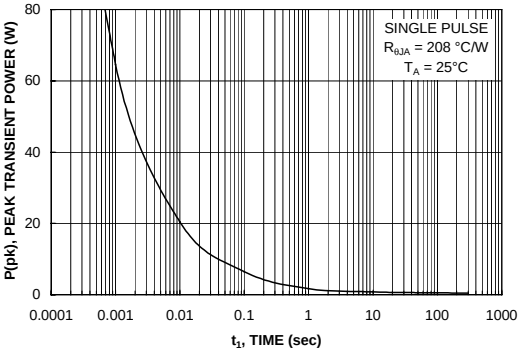


Figure 10. Single Pulse Maximum Power Dissipation.

Typical Characteristics: Q2

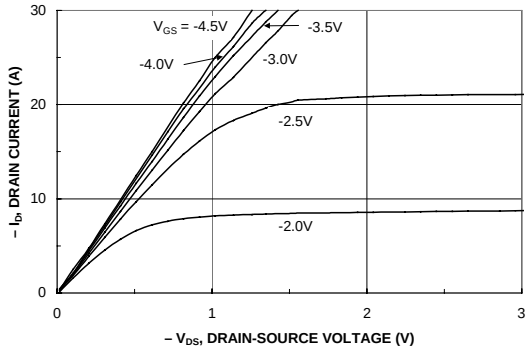


Figure 11. On-Region Characteristics.

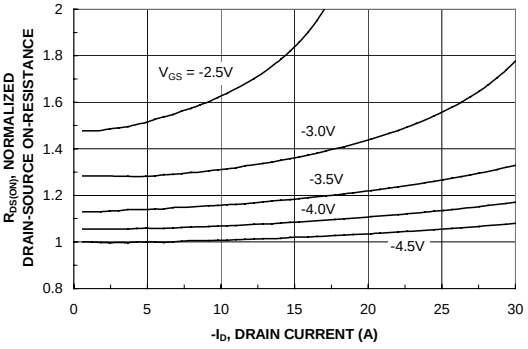


Figure 12. On-Resistance Variation with Drain Current and Gate Voltage.

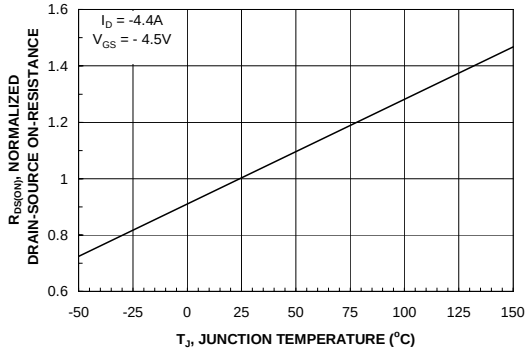


Figure 13. On-Resistance Variation with Temperature.

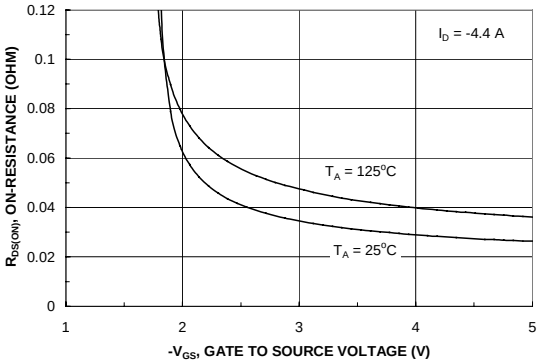


Figure 14. On-Resistance Variation with Gate-to-Source Voltage.

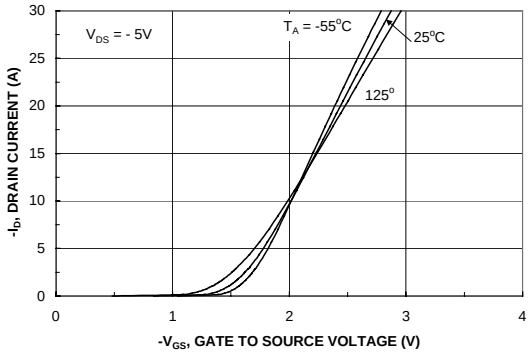


Figure 15. Transfer Characteristics.

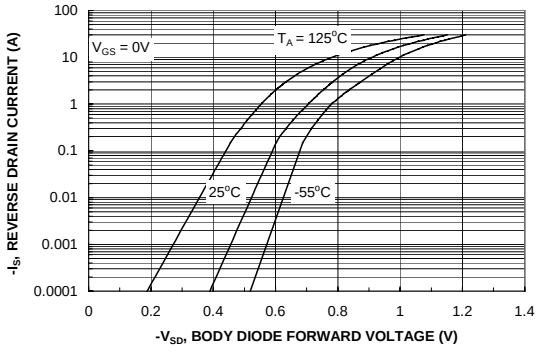


Figure 16. Body Diode Forward Voltage Variation with Source Current and Temperature.

Typical Characteristics: Q2

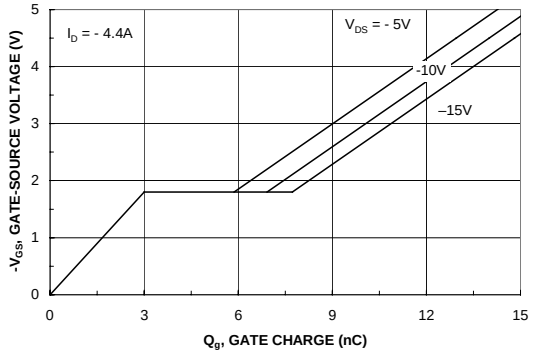


Figure 17. Gate Charge Characteristics.

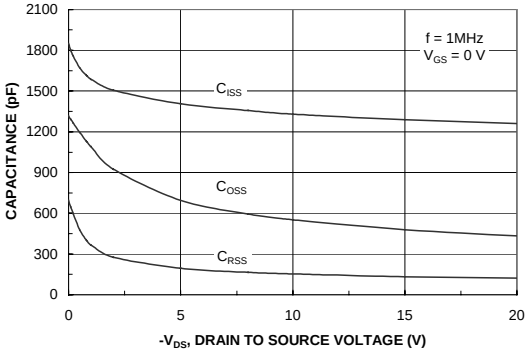


Figure 18. Capacitance Characteristics.

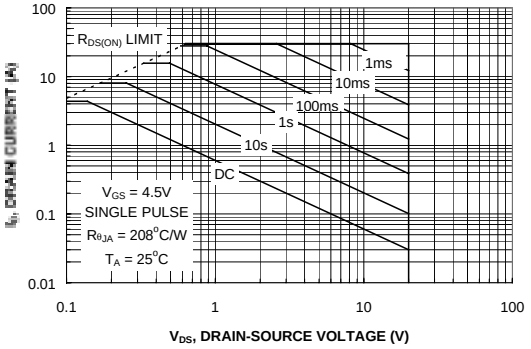


Figure 19. Maximum Safe Operating Area.

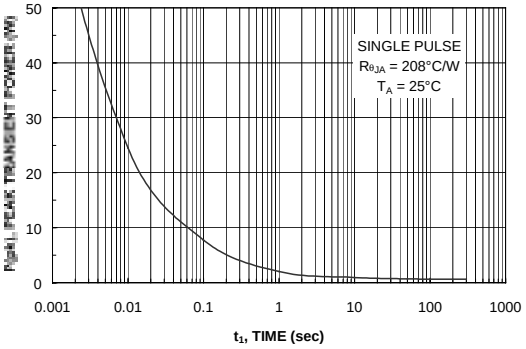


Figure 20. Single Pulse Maximum Power Dissipation.

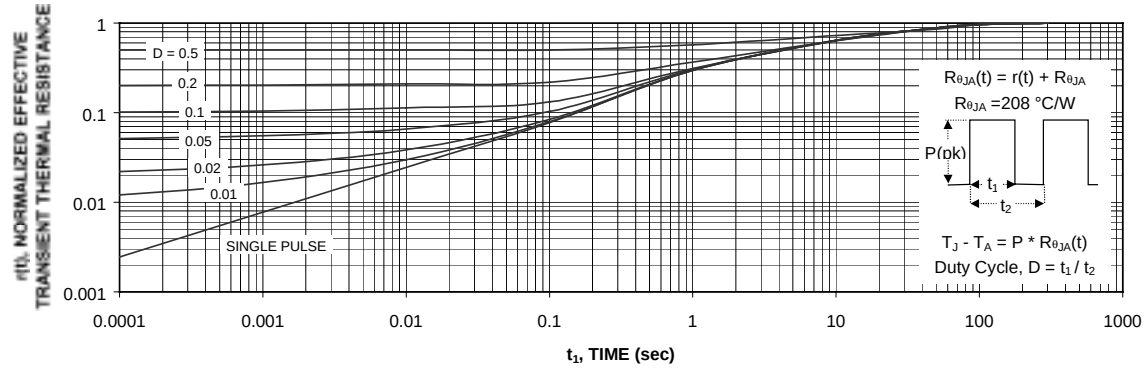


Figure 21. Transient Thermal Response Curve.

Thermal characterization performed using the conditions described in Note 1b.
Transient thermal response will change depending on the circuit board design.

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