FUJITSU SEMICONDUCTOR
DATA SHEET

DS04-28221-1E

ASSP For Video Applications

CMOS

3 ch 8-bit 162 MSPS A/D Converter

MB40C338V

■ DESCRIPTION

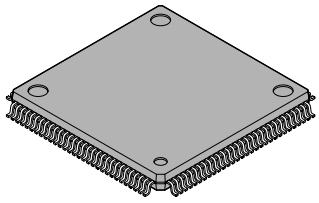
MB40C338V is a high-speed 3 ch A/D converter using a fast CMOS technology.

■ FEATURES

- Resolution : 8 bit
- No. of A/D channels : 3 ch
- Linearity error : ±0.40 %(typical)
- Maximum conversion rate : 162 MSPS (minimum)
- Power supply voltage : 3.3 V (typical : internal circuit)
- Digital input voltage range : TTL level
- Digital output voltage range : 3.3 V CMOS level
- Video amp. input voltage range : 0.7 V_{P-P} (typical)
- Video amp. gain : 1.9 double fixed
- A/D input capacity : 15 pF (typical)
- Power dissipation : 1100 mW (typical)
- Additional features : PLL circuit
  Video amp. circuit (1.9 double fixed gain, OFF operation is possible)
  CLAMP circuit
  V_{RT} AMP circuit (RGB 3 ch separate)
  V_{RB} AMP circuit (RGB 3 ch common)
  Overflow output
  High impedance output, power down function
- Package : LQFP120 (16 mm × 16 mm, lead pitch : 0.5 mm)

■ PACKAGE

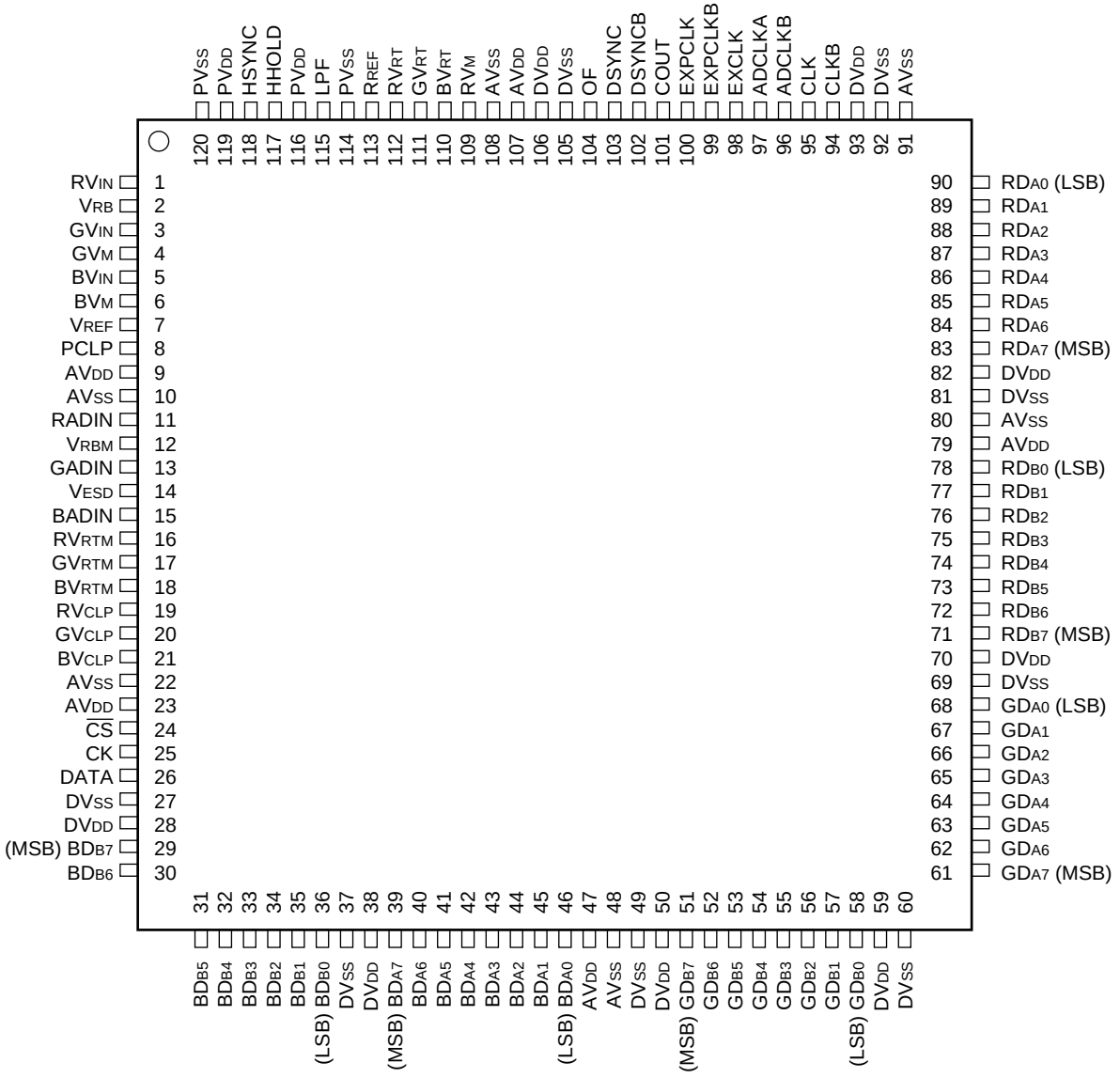
120-pin plastic LQFP



(FPT-120P-M21)

■ PIN ASSIGNMENT

(TOP VIEW)



(FPT-120P-M21)

■ PIN DESCRIPTION

Pin No.	Symbol	Description
9, 23, 47, 79, 107	AV_{DD}	Analog power supply (+3.3 V)
28, 38, 50, 59, 70, 82, 93, 106	DV_{DD}	Digital power supply (+3.3 V)
116, 119	PV_{DD}	PLL Power supply pin (+3.3 V)
14	V_{ESD}	Digital input power supply for protect device (+3.3 V or +5 V)
10, 22, 48, 80, 91, 108	AV_{SS}	Analog power supply ground pin (0 V)
27, 37, 49, 60, 69, 81, 92, 105	DV_{SS}	Digital power supply ground pin (0 V)
114, 120	PV_{SS}	PLL Power supply ground pin (0 V)
1 3 5	RV_{IN} GV_{IN} BV_{IN}	1.9 double amp. input pin
11 13 15	RADIN GADIN BADIN	A/D converter input pin This pin inputs directly is possible when 1.9 double amp.OFF
19 20 21	RV_{CLP} GV_{CLP} BV_{CLP}	Clamp voltage setting input pin
16 17 18	RV_{RTM} GV_{RTM} BV_{RTM}	Reference voltage output pin on top side
112 111 110	RV_{RT} GV_{RT} BV_{RT}	Reference voltage input pin on top side
12	V_{RBM}	Reference voltage output pin on bottom side
2	V_{RB}	Reference voltage input pin on bottom side
109 4 6	RV_M GV_M BV_M	Reference 1/2 voltage output pin (Add 0.1 µF for AV_{SS})
25	CK	Serial data transfer clock input pin
26	DATA	Serial data input pin
24	$\overline{CS}$	Chip select signal input pin It is possible to input to the shift register at $\overline{CS}$ falling The content of the shift register is executed at $\overline{CS}$ rising.
98	EXCLK	Clock input pin for A/D converter (CMOS level) Fix to “L” level when unused.

Note: The values in parentheses are standard.

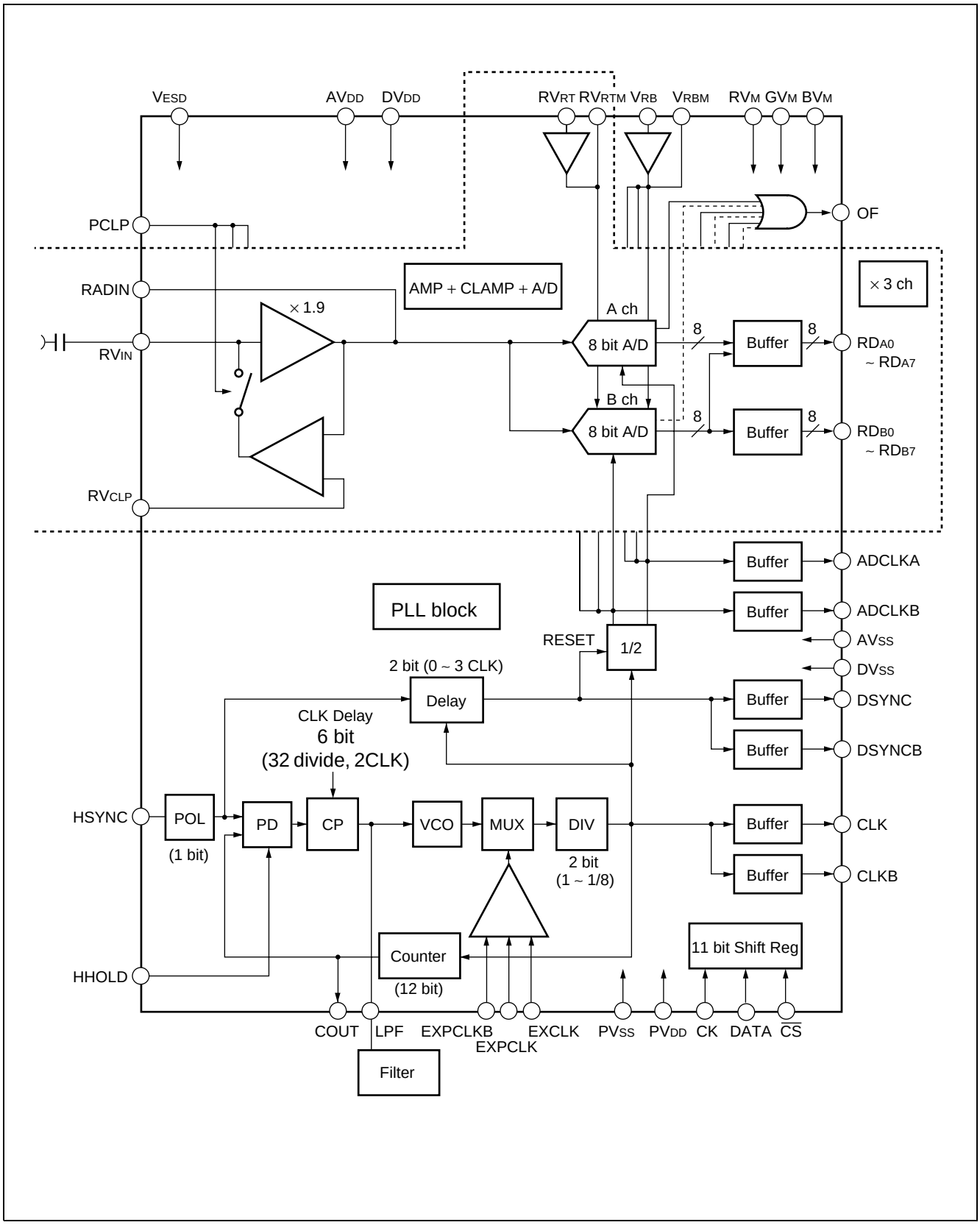
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Parameter	Symbol	Description	
99	EXPCLKB	Differential clock (negative-phase) input pin for A/D converter Fix to “H” level when unused.	PECL level
100	EXPCLK	Differential clock (positive-phase) input pin for A/D converter Fix to “L” level when unused.	
8	PCLP	Clamp pulse input pin	
113	R_{REF}	Internal current setting pin (Add 12 kΩ for AV_{SS})	
103	DSYNC	Delay sync signal output pin	
102	DSYNCB	Inverted delay sync signal output pin	
95	CLK	Clock output pin (See “ ■ TIMING DIAGRAM ”.)	
94	CLKB		
97	ADCLKA		
96	ADCLKB		
83 to 90 61 to 68 39 to 46	RD_{A7} to RD_{A0} GD_{A7} to GD_{A0} BD_{A7} to BD_{A0}	Digital output pin (Port A) RD_{A7}, GD_{A7}, BD_{A7} : MSB RD_{A0}, GD_{A0}, BD_{A0} : LSB	
71 to 78 51 to 58 29 to 36	RD_{B7} to RD_{B0} GD_{B7} to GD_{B0} BD_{B7} to BD_{B0}	Digital output pin (Port B) RD_{B7}, GD_{B7}, BD_{B7} : MSB RD_{B0}, GD_{B0}, BD_{B0} : LSB	
101	COUT	PLL counter output pin	
115	LPF	External capacitor/resistor connection pin	
117	HHOLD	Phase detector operation is hold by input “H” level	
118	HSYNC	Horizontal sync signal input pin	
7	V_{REF}	Internal voltage output pin (Add 3.3µF for AV_{SS})	
104	OF	Overflow output pin (“H” level output at overflow)	

Note: The values in parentheses are standard.

■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating		Unit
		Min.	Max.	
Power supply voltage	AV_{DD}, DV_{DD}, PV_{DD}	–0.3	+4.0	V
	V_{ESD}	–0.3	+7.0	V
Input/output voltage	RV_{IN}, GV_{IN}, BV_{IN}, RADIN, GADIN, BADIN, RV_{CLP}, GV_{CLP}, BV_{CLP}, RV_{RT}, GV_{RT}, BV_{RT}, RV_{RTM}, GV_{RTM}, BV_{RTM}, V_{RB}, V_{RBM}, RV_M, GV_M, BV_M, V_{REF}, R_{REF}	–0.3	AV_{DD}+0.3*1	V
	RD_{A0} to RD_{A7}, RD_{B0} to RD_{B7}, GD_{A0} to GD_{A7}, GD_{B0} to GD_{B7}, BD_{A0} to BD_{A7}, BD_{B0} to BD_{B7}, DSYNC, DSYNCB, OF, COUT, CLK, CLKB, ADCLKA, ADCLKB	–0.3	DV_{DD}+0.3*1	V
	LPF	–0.3	PV_{DD}+0.3*1	V
	CK, DATA, $\overline{CS}$, EXPCLKB, EXPCLK, PCLP, EXCLK, HHOLD, HSYNC	–0.3	V_{ESD}+0.3*2	V
Storage temperature	T_{STG}	–55	+125	°C

*1 : Do not exceed +4.0 V.

*2 : Do not exceed +7.0 V.

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

■ RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value			Unit
		Min.	Typ.	Max.	
Power supply voltage	AV_{DD}, DV_{DD}	3.00	3.30	3.60	V
	PV_{DD}	3.00	3.30	3.60	V
	V_{ESD}	3.00	—	5.25	V
A/D converter input voltage	V_{ADIN}	V_{RB}	—	V_{RT}	V
Analog reference voltage: T	V_{RT}	—	2.2	AV_{DD} – 0.6	V
Analog reference voltage : B	V_{RB}	0.6	0.7	—	V
Analog reference voltage range	$V_{RT} – V_{RB}$	1.0	1.5	1.8	V
Video AMP input voltage	V_{IN} (P-P)	0.5	—	0.9	V_{P-P}
Clamp input voltage	V_{CLP}	0.6	V_{RB}	1.7	V
Digital “H” level input voltage	V_{IHD}	2.5	—	V_{ESD}	V
Digital “L” level input voltage	V_{ILD}	0	—	0.5	V
Digital “H” level output current	I_{OHD}	–400	—	—	µA
Digital “L” level output current	I_{OLD}	—	—	1.6	mA
PLL counter	P_C	100	—	4095	—
HSYNC input frequency range	f_{HSYNC}	10	—	100	kHz
HHOLD set up time	t_{sHHOLD}	20	—	—	ns
HHOLD hold time	t_{hHHOLD}	20	—	—	ns
Clamp pulse width	t_{WCLP}	0.5	—	—	µs
CK clock pulse width	t_{WCKL}, t_{WCKH}	100	—	—	ns
DATA set up time	t_{sDATA}	30	—	—	ns
DATA hold time	t_{hDATA}	30	—	—	ns
$\overline{CS}$ set up time	t_{sCS}	50	—	—	ns
$\overline{CS}$ hold time	t_{hCS}	50	—	—	ns
$\overline{CS}$ “H” level hold time	t_{WCSH}	100	—	—	ns
Operating temperature range	Ta	–20	—	70	°C

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device’s electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their FUJITSU representatives beforehand.

■ ELECTRICAL CHARACTERISTICS

1. DC Characteristics in Analog Section

• Power supply current (AV_{DD} = DV_{DD} = PV_{DD} = 3.0 V to 3.6 V, V_{ESD} = 3.0 V to 5.25 V, Ta = –20 °C to +70 °C)

Parameter	Symbol	Value			Unit
		Min.	Typ.	Max.	
Analog power supply current	AI_{DD}	—	220	310	mA
Digital power supply current	DI_{DD}	—	100	110	mA
Power supply current PLL section (@ f_{VCOH} = 162 MHz, Icp = 0.5 mA, DIV = 1/1)	PI_{DD}	—	16	20	mA
Standby current	I_{SB}	—	10	—	mA

• A/D Block (AV_{DD} = DV_{DD} = PV_{DD} = 3.0 V to 3.6 V, V_{ESD} = 3.0 V to 5.25 V, Ta = –20 °C to +70 °C)

Parameter	Symbol	Value			Unit
		Min.	Typ.	Max.	
Resolution	—	—	8	—	bit
Linearity error (DC Accuracy)	LE	–0.8	±0.4	+0.8	%
Differential linearity error (DC Accuracy)	DLE	–0.36	±0.2	+0.65	%
Analog reference voltage input current	I_{RT}, I_{RB}	—	5	20	µA
ADIN input capacity	C_{ADIN}	—	15	—	pF

• Video AMP Block (AV_{DD} = DV_{DD} = PV_{DD} = 3.0 V to 3.6 V, V_{ESD} = 3.0 V to 5.25 V, Ta = –20 °C to +70 °C)

Parameter	Symbol	Value			Unit
		Min.	Typ.	Max.	
Video AMP gain	G_{AMP}	1.8	1.9	2.0	—
Video AMP output voltage range	V_{AMPOUT}	0.5	—	AV_{DD} – 0.6	V
Video AMP frequency width	BW	—	250	—	MHz
Video AMP input capacity	C_{VIN}	—	5	—	pF

• CLAMP Block (AV_{DD} = DV_{DD} = PV_{DD} = 3.0 V to 3.6 V, V_{ESD} = 3.0 V to 5.25 V, Ta = –20 °C to +70 °C)

Parameter	Symbol	Value			Unit
		Min.	Typ.	Max.	
V_{CLP} input current	I_{CLP}	—	5	20	µA
Clamp voltage	V_{CLAMP}	V_{CLP} – 0.1	V_{CLP}	V_{CLP} + 0.1	V

• PLL Block (AV_{DD} = DV_{DD} = PV_{DD} = 3.0 V to 3.6 V, V_{ESD} = 3.0 V to 5.25 V, Ta = –20 °C to +70 °C)

Parameter	Symbol	Value			Unit
		Min.	Typ.	Max.	
CLK jitter (@ f_{HSYNC} = 79.98 kHz, f_{CLK} = 135.0 MHz)	P_{tj}	—	1.0	1.5	ns

2. DC characteristics in Digital Section

(AV_{DD} = DV_{DD} = PV_{DD} = 3.0 V to 3.6 V, V_{ESD} = 3.0 V to 5.25 V, Ta = –20 °C to +70 °C)

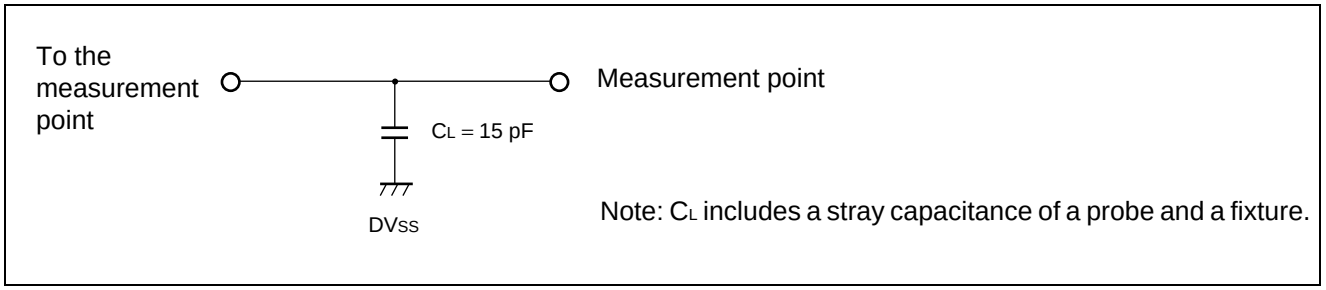
Parameter	Symbol	Value			Unit
		Min.	Typ.	Max.	
Digital input current	I_{ID}	–20	—	5	µA
Digital “H” level output voltage	V_{OHD}	DV_{DD} – 0.4	—	—	V
Digital “L” level output voltage	V_{OLD}	—	—	0.4	V

3. Switching Characteristics

(AV_{DD} = DV_{DD} = PV_{DD} = 3.0 V to 3.6 V, V_{ESD} = 3.0 V to 5.25 V, Ta = –20 °C to +70 °C)

Parameter		Symbol	Value			Unit
			Min.	Typ.	Max.	
A/D Maximum conversion rate	Timing diagram 1	f_{S1}	100	—	—	MSPS
	Timing diagram 2	f_{S2}	162	—	—	MSPS
Aperture time		t_{AD}	—	1.5	—	ns
VCO oscillation frequency	VCOL	f_{VCOL}	75	—	140	MHz
	VCOH	f_{VCOH}	85	—	162	MHz
CLK output delay time		t_{pd} (HSYNC-CLK)	1.0	2.0	4.0	ns
Digital output delay time	Timing diagram 1	t_{pd} (CLK-ADCLK1)	0.0	1.0	2.0	ns
		t_{pd} (CLK-DATA1)	2.5	4.0	6.0	ns
	Timing diagram 2	t_{pd} (CLK-ADCLK2)	0.0	1.0	2.0	ns
		t_{pd} (CLK-DATA2)	2.5	4.0	6.0	ns
DSYNC output delay time		t_{pd} (CLK-DSYNC)	0.5	1.5	2.0	ns

■ DIGITAL OUTPUT BUFFER LOAD CIRCUIT



■ SERIAL DATA SETTING (MSB FAST)

(Address) (Data)

LSB ← → MSB

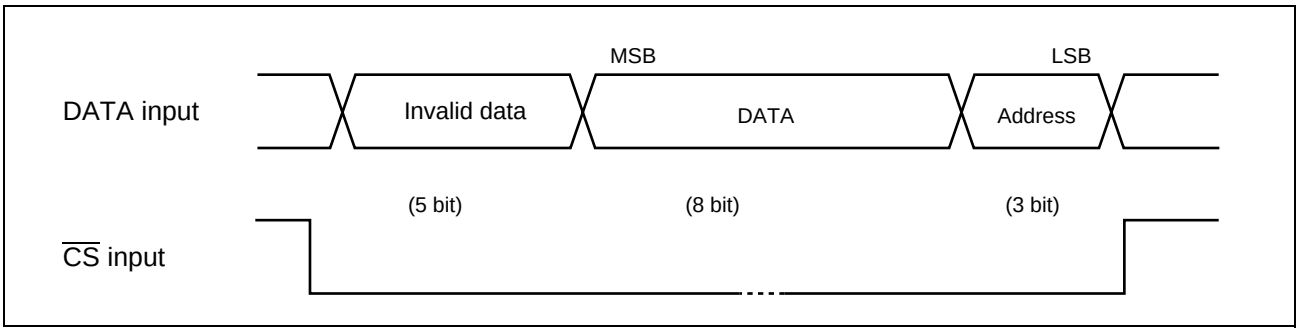
RES	D0	D1	D2	D3	D4	D5	D6	D7	D8	D9	D10	Function
0	0	0	0	0	0	0	X	X	X	X	X	$\overline{CE}$: 0 = operation mode, 1 = all function power off
	0	0	0	0	0	0	X	X	X	X	X	DSEL : 0 = demultiplex output, 1 = straight output
	0	0	0	0	0	0	X	X	X	X	X	Video AMP : 0 = operation , 1 = off
1	1	0	0	0	0	0	0	0	0	1	0	Counter low ranking 8 bit
2	0	1	0	0	0	0	0	X	X	X	X	Counter high ranking 4 bit
3	1	1	0	0	0	0	0	0	0	1	0	CLK delay adjust*1 : $t_d = N / (32 \times f_{CLK})$
	1	1	0	0	0	0	0	0	0	1	0	HSYNC polarity : 0 = through, 1 = inversion
	1	1	0	0	0	0	0	0	0	1	0	A/D converter output : 0 = operation, 1 = high impedance
4	0	0	1	0	0	0	0	0	0	1	0	CLK output : 0 = on, 1 = “L”
	0	0	1	0	0	0	0	0	0	1	0	CLKB output : 0 = on, 1 = “L”
	0	0	1	0	0	0	0	0	0	1	0	DSYNC output : 0 = on, 1 = “L”
	0	0	1	0	0	0	0	0	0	1	0	DSYNCB output : 0 = on, 1 = “L”
	0	0	1	0	0	0	0	0	0	1	0	ADCLKA output : 0 = on, 1 = “L”
	0	0	1	0	0	0	0	0	0	1	0	ADCLKB output : 0 = on, 1 = “L”
	0	0	1	0	0	0	0	0	0	1	0	DSYNC delay*2 : 0, 1, 2, 3
5	1	0	1	0	0	0	0	0	0	1	0	CLK change : 0 = VCO, 1 = External clock
	1	0	1	0	0	0	0	0	0	1	0	External clock input : 0 = CMOS, 1 = PECL
	1	0	1	0	0	0	0	0	0	1	0	Counter operation : 0 = on, 1 = off
	1	0	1	0	0	0	0	0	0	1	0	Charge pump current*3 : 0.1 mA, 0.5 mA, 1 mA
	1	0	1	0	0	0	0	0	0	1	0	VCO select : 0 = VCOL, 1 = VCOH
	1	0	1	0	0	0	0	0	0	1	0	Divider setting*4 : 1, 1/2, 1/4, 1/8

*1 : Setting at 6bit Resolution : 1/32 × CLK, Setting range : 0 to 63/32 × CLK

*2, *3, *4 : See under table

Setting	0 (0, 0)	1 (1, 0)	2 (0, 1)	3 (1, 1)
DSYNC delay*2	0 CLK	1 CLK	2 CLK	3 CLK
Charge pump current*3	0.1 mA	0.5 mA	1.0 mA	—
Divider setting*4	1/1	1/2	1/4	1/8

Example: input at 16 bit



■ RECOMMENDED VALUE OF SERIAL DATA SETTING

	f_{CLK} (MHz)	f_{HSYNC} (kHz)	Counter	Icp (mA)	VCO select	Divider	f_{VCO} (MHz)
UXGA	162.000	75.000	2160	0.5	VCOH	1/1	162.000
SXGA	157.500	91.146	1728	0.5	VCOH	1/1	157.500
	135.000	81.130	1664	0.5	VCOH or VCOL	1/1	135.000
	108.000	64.904	1664	0.5	VCOH or VCOL	1/1	108.000
XGA	94.500	68.677	1376	0.5	VCOH or VCOL	1/1	94.500
	78.750	60.023	1312	0.5	VCOL	1/1	78.750
	75.000	56.476	1328	0.5	VCOH	1/2	150.000
	65.000	48.363	1344	0.5	VCOH or VCOL	1/2	130.000
SVGA	56.250	53.674	1048	0.5	VCOH or VCOL	1/2	112.500
	50.000	48.077	1040	0.5	VCOH or VCOL	1/2	100.000
	49.500	46.875	1056	0.5	VCOH or VCOL	1/2	99.000
	40.000	37.879	1056	0.5	VCOL	1/2	80.000
VGA	36.000	43.269	832	0.5	VCOH	1/4	144.000
	31.500	37.861	832	0.5	VCOH or VCOL	1/4	126.000
	25.175	31.469	800	0.5	VCOH or VCOL	1/4	100.700
	25.149	31.436	800	0.5	VCOH or VCOL	1/4	100.596
PAL	29.375	15.625	1880	0.5	VCOH or VCOL	1/4	117.500
	22.031	15.625	1410	0.5	VCOH or VCOL	1/4	88.125
	14.688	15.625	940	0.5	VCOH or VCOL	1/8	117.500
NTSC	24.545	15.734	1560	0.5	VCOH or VCOL	1/4	98.180
	18.409	15.734	1170	0.5	VCOH	1/8	147.270
	12.273	15.734	780	0.5	VCOH or VCOL	1/8	98.180

VCO select : VCOH (f_{VCO} = 85 MHz to 162 MHz)

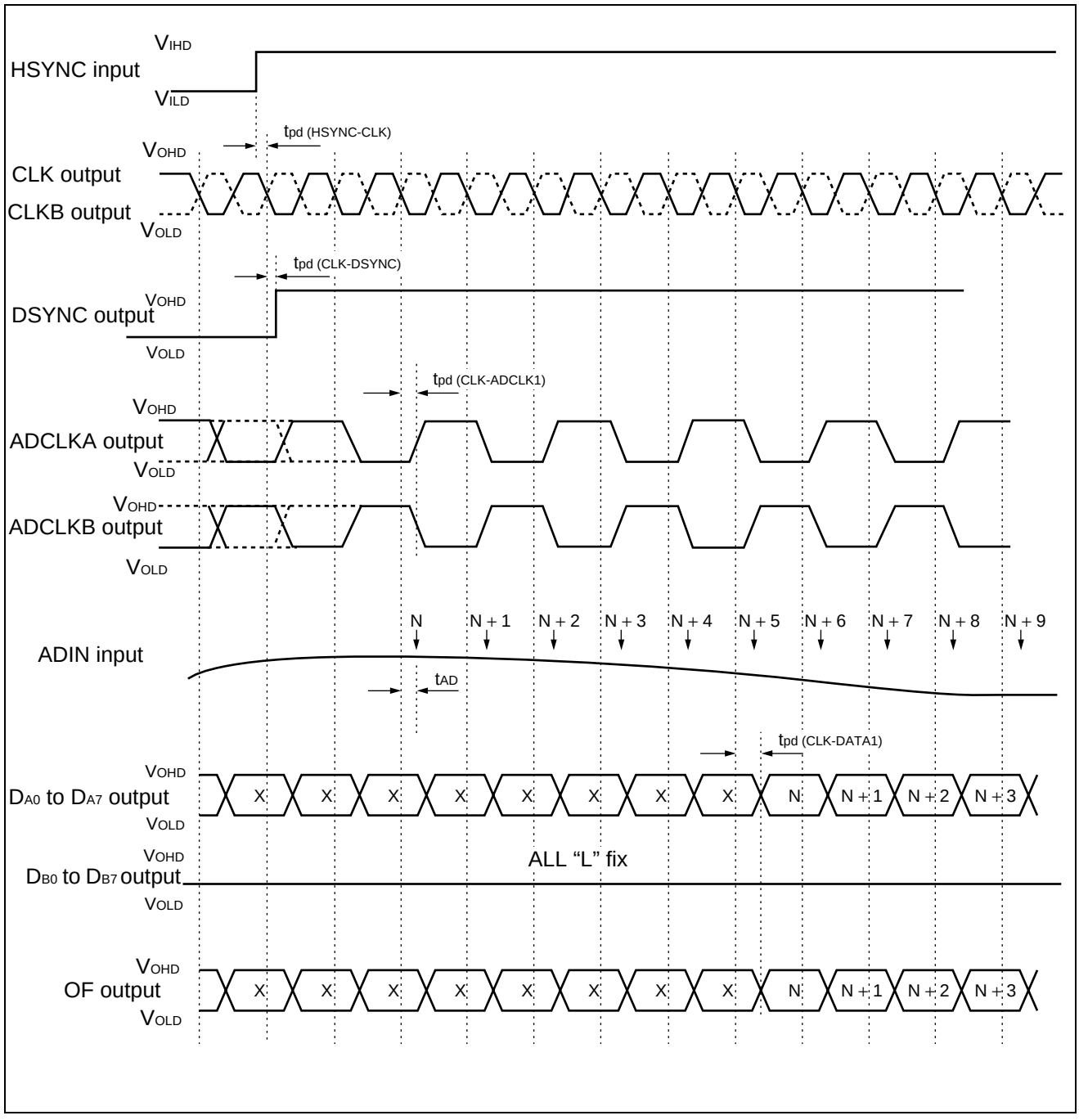
VCOL (f_{VCO} = 75 MHz to 140 MHz)

$f_{CLK} = f_{HSYNC} \times$ Counter

$f_{VCO} = f_{HSYNC} \times$ Counter/Divider

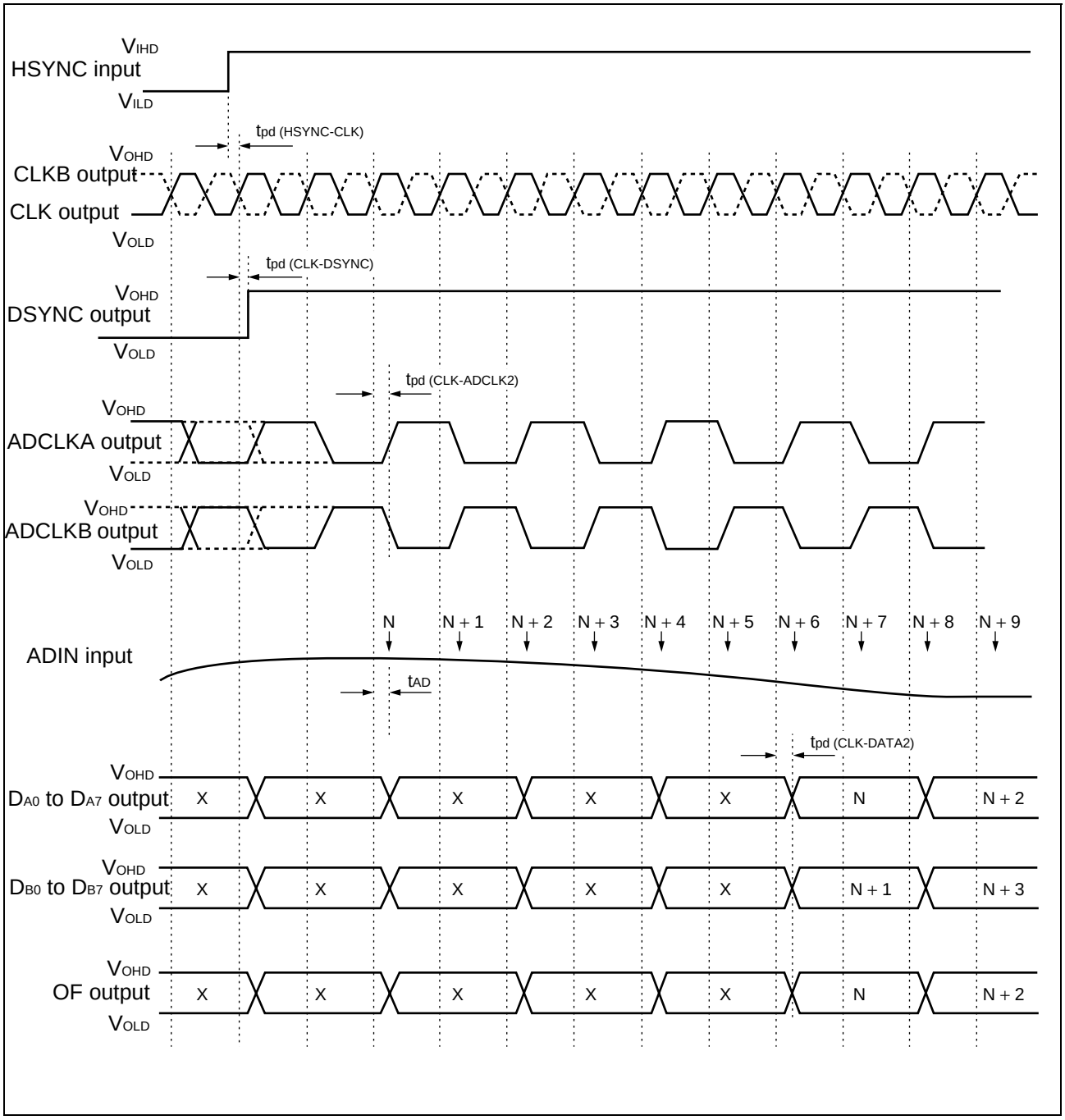
■ TIMING DIAGRAM

- Straight Output Mode (Timing Diagram 1)



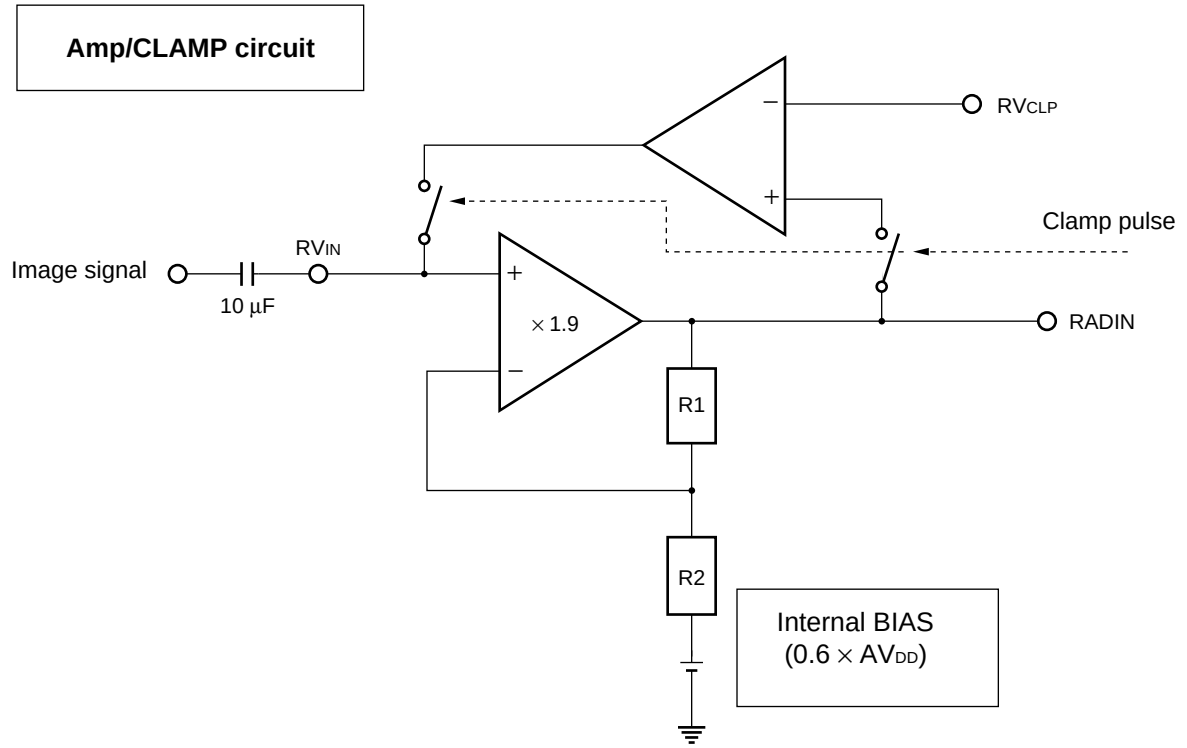
- ADIN input - Sampling at CLK rising (at CLKB falling)
- D_{A0} to D_{A7} - Output (after 5 CLK + t_{pd} ($_{CLK-DATA1}$) from sampling) at CLK rising (at CLKB falling)

- Demultiplex Output (in- phase) Mode (Timing Diagram 2)

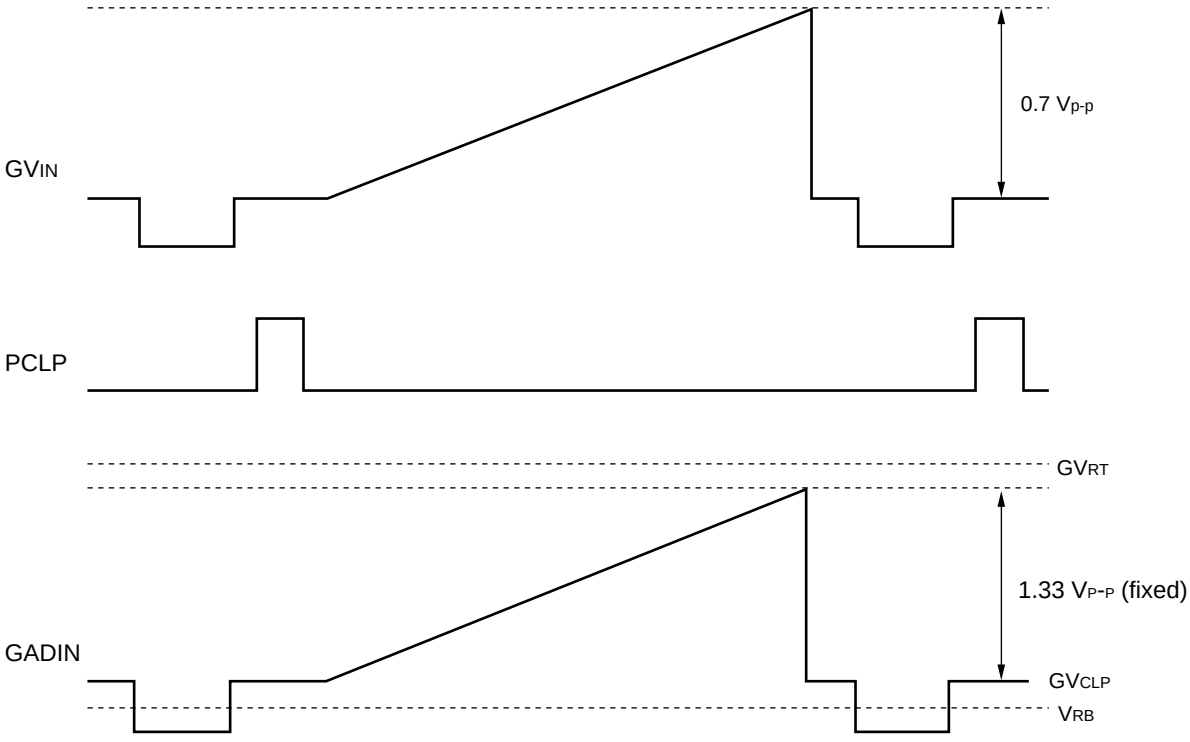


- ADIN input - Sampling at CLK rising (at CLKB falling)
- D_{A0} to D_{A7} - Output (after 6 CLK + t_{pd} ($_{CLK-DATA2}$) from sampling) at CLK rising (at CLKB falling)
- D_{B0} to D_{B7} - Output (after 5 CLK + t_{pd} ($_{CLK-DATA2}$) from sampling) at CLK rising (at CLKB falling)

■ CLAMP and AMP OPERATION

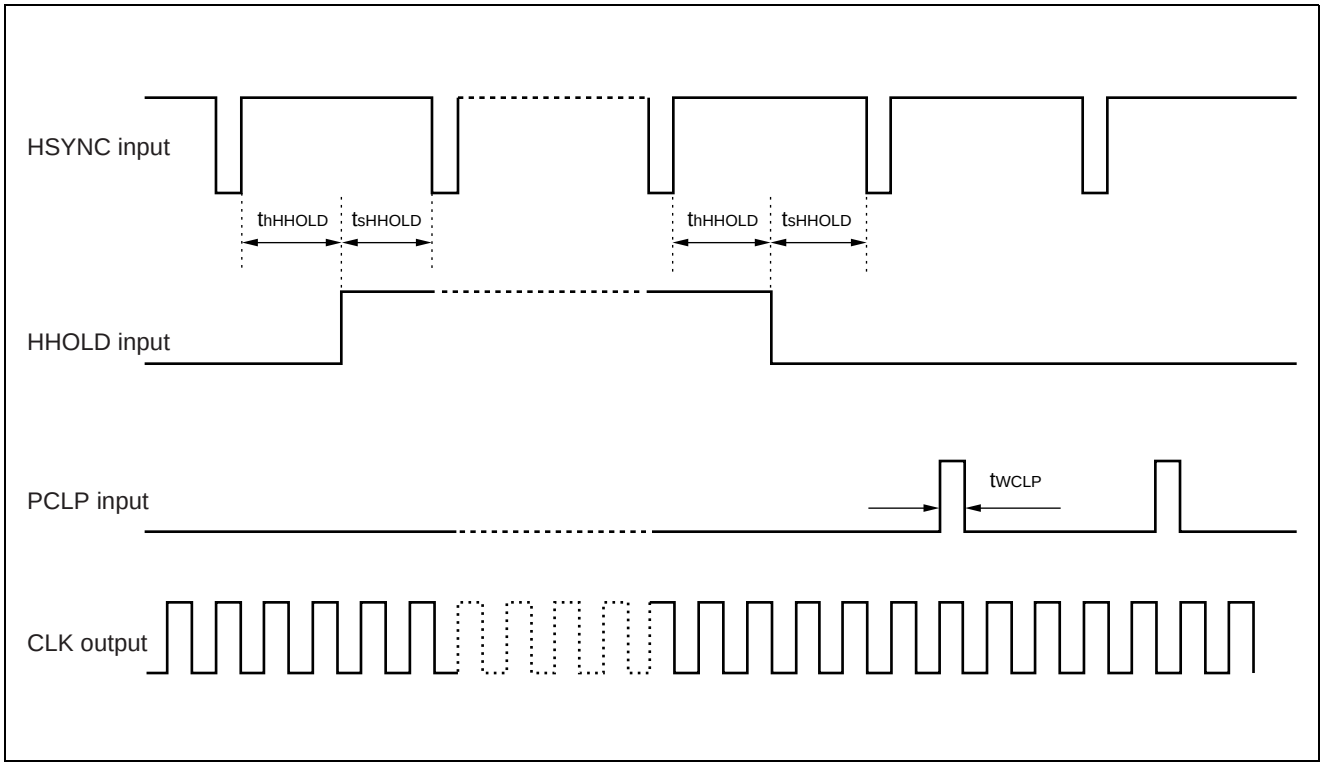


< For example, Sync on G signal input >

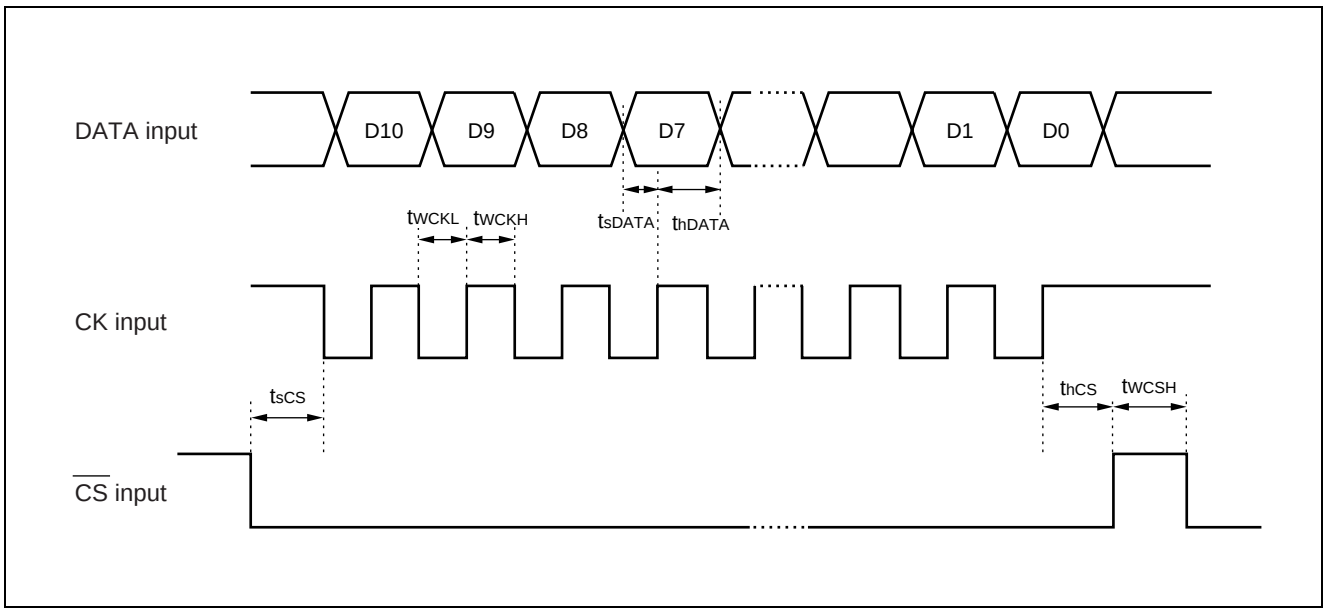


Contrast adjust : controlling the voltage difference between VRT and VRB (typ : $V_{RT} - V_{RB} = 1.33$ V)
Brightness adjust : controlling the voltage difference between VCLP and VRB (typ : $V_{CLP} = V_{RB}$)

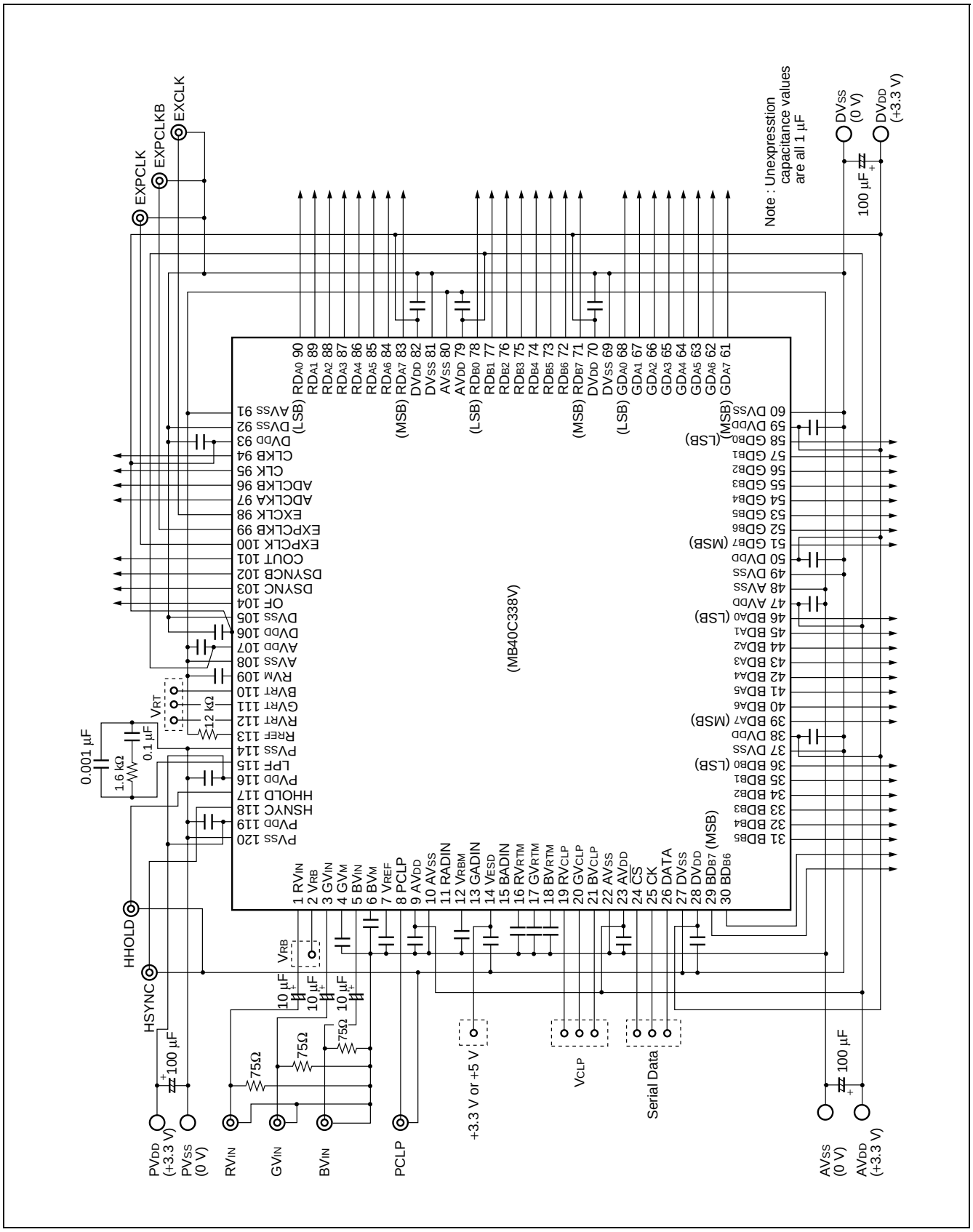
■ CLAMP SIGNAL and HOLD SIGNAL



■ SERIAL DATA TRANSFER TIMING



■ TYPICAL APPLICATION



■ USAGE PRECAUTIONS

Be sure to ground the pins of AV_{DD}, DV_{DD}, PV_{DD}, V_{ESD}, RV_{RTM}, GV_{RTM}, BV_{RTM}, V_{RBM}, RV_{M}, GV_{M}, BV_{M} and V_{REF} via high-frequency capacitor.

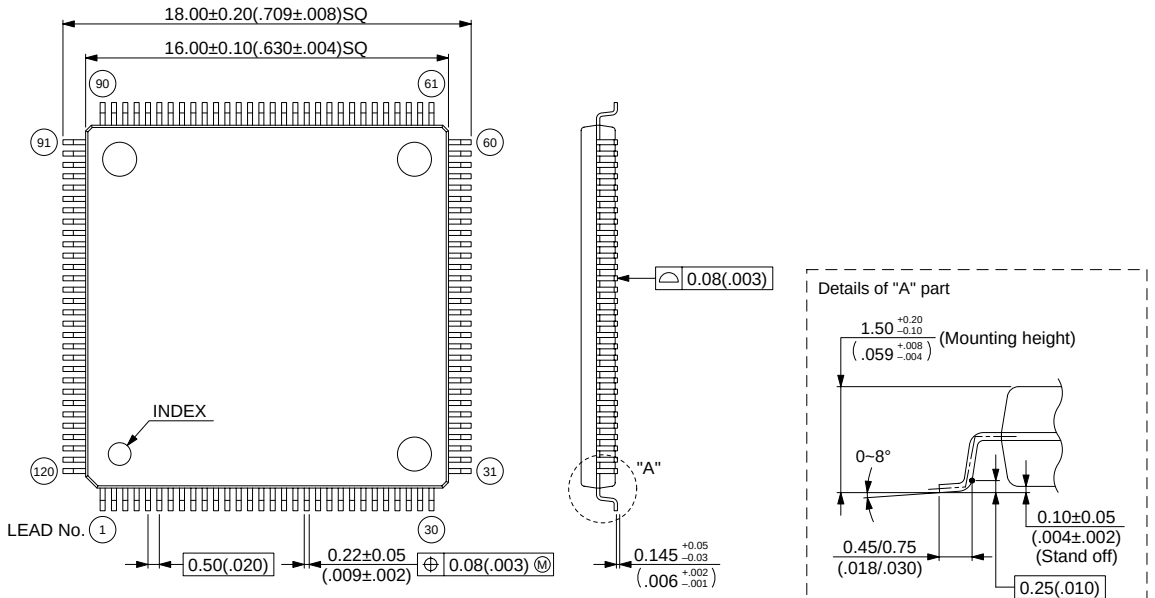
Place the high-frequency capacitor as close as possible to the pin.

■ ORDERING INFORMATION

Part number	Package	Remark
MB40C338VPFV	120-pin plastic LQFP (FPT-120P-M21)	

■ PACKAGE DIMENSION

120-pin plastic LQFP
(FPT-120P-M21)



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Dimension in mm (inches)

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For further information please contact:

Japan

FUJITSU LIMITED
Corporate Global Business Support Division
Electronic Devices
Shinjuku Dai-Ichi Seimei Bldg. 7-1,
Nishishinjuku 2-chome, Shinjuku-ku,
Tokyo 163-0721, Japan
Tel: +81-3-5322-3347
Fax: +81-3-5322-3386

http://www.fujitsu.co.jp/

North and South America

FUJITSU MICROELECTRONICS, INC.
3545 North First Street,
San Jose, CA 95134-1804, U.S.A.
Tel: +1-408-922-9000
Fax: +1-408-922-9179

Customer Response Center
Mon. - Fri.: 7 am - 5 pm (PST)
Tel: +1-800-866-8608
Fax: +1-408-922-9179

http://www.fujitsumicro.com/

Europe

FUJITSU MICROELECTRONICS EUROPE GmbH
Am Siebenstein 6-10,
D-63303 Dreieich-Buchschlag,
Germany
Tel: +49-6103-690-0
Fax: +49-6103-690-122

http://www.fujitsu-fme.com/

Asia Pacific

FUJITSU MICROELECTRONICS ASIA PTE. LTD.
#05-08, 151 Lorong Chuan,
New Tech Park,
Singapore 556741
Tel: +65-281-0770
Fax: +65-281-0220

http://www.fmap.com.sg/

Korea

FUJITSU MICROELECTRONICS KOREA LTD.
1702 KOSMO TOWER, 1002 Daechi-Dong,
Kangnam-Gu,Seoul 135-280
Korea
Tel: +82-2-3484-7100
Fax: +82-2-3484-7111

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«Трейд Электроникс»

Шишлаков Евгений

8 (495)668-30-28 доб 169

manager28@tradeelectronics.ru

http://www.tradeelectronics.ru/