CT1990/1 Series

MIL-STD-1553B Remote Terminal, Bus Controller, or Passive Monitor Hybrid with Status Word Control

Features

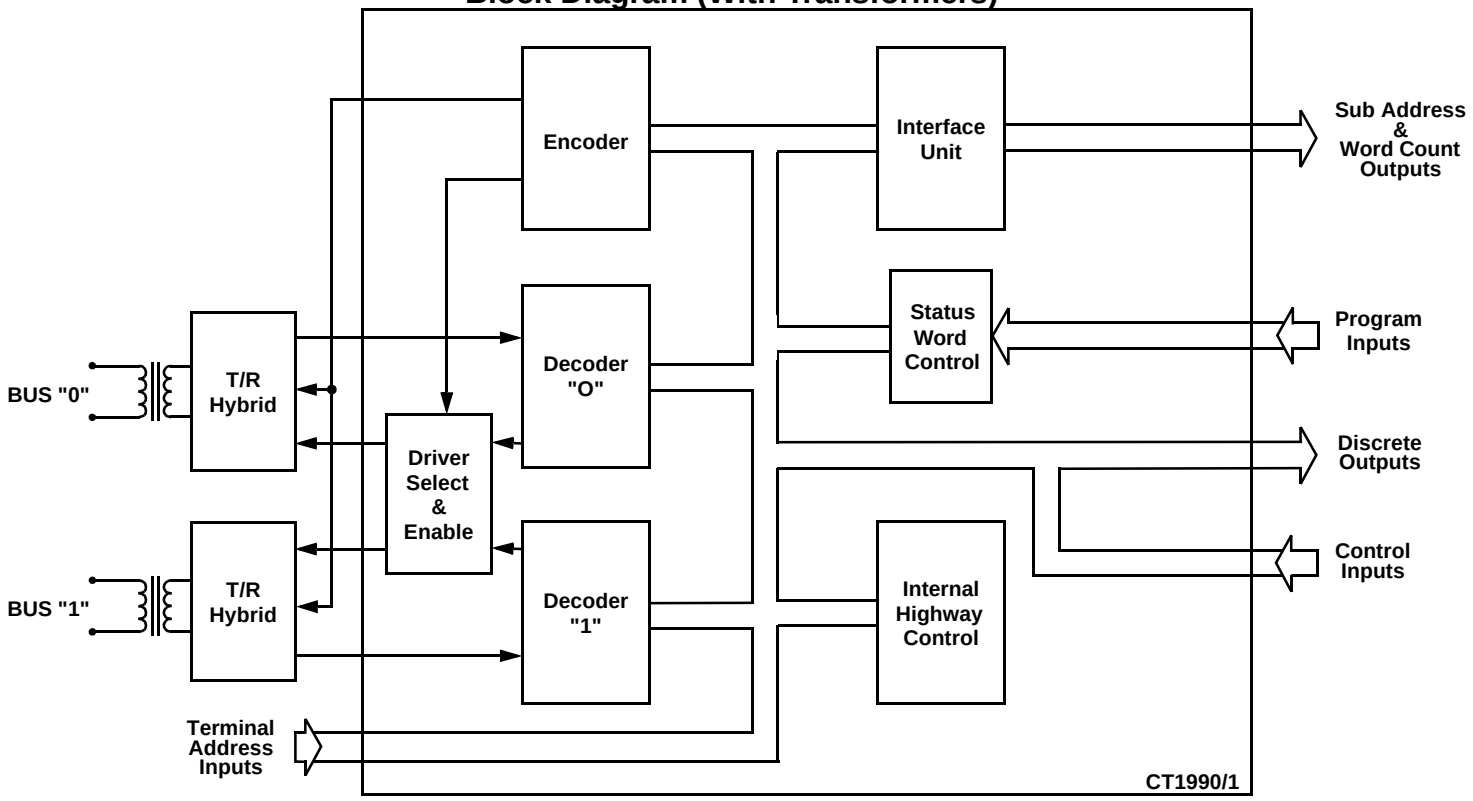
- Performs the Complete Dual-Redundant Remote Terminal, Bus Controller Protocol and Passive Monitor Functions of MIL-STD-1553B
- Automated Self-Test Functions
- Allows setting of the Message Error Bit on illegal commands
- Provides programmable control over Terminal Flag and Subsystem Flag Status Bits
- MIL-PRF-38534 Compliant Circuits Available
- 50 mw Typical Power Consumption
- Small Size
- Available in Ceramic Plug-in Package Configuration
- Compatible with all ACT Driver/Receiver Units
- 5V DC Operation
- Full Military (-55°C to +125°C) Temperature Range
- DESC SMD# 5962–94775: Released CT1990, Pending CT1991

AEROFLEX
CIRCUIT TECHNOLOGY

General Description

The CT1990/1 Series is a monolithic implementation of the MIL-STD-1553B Bus Controller, Remote Terminal and Passive Monitor functions. All protocol functions of MIL-STD-1553B are incorporated and a number of options are included to improve flexibility. These features include programming of the status word, illegalizing specific commands and an independent loop back self-test which is initiated by the subsystem. This unit is directly compatible with all transceivers and microprocessor interfaces such as the CT1611 and CT1800 produced by Aeroflex Incorporated.

Block Diagram (With Transformers)



Absolute Maximum Ratings

Parameter	Range	Units
Supply Voltage (V_{DD})	-0.3 to +7.0	V
Input or Output Voltage at any Pad	-0.3 to (V_{DD} + 0.3)	V
Storage Case Temperature	-65 to +150	°C

Recommended DC Operating Conditions

Parameter	Min	Typ	Max	Unit	Notes
Vcc Power Supply Voltage Vcc	4.5	5.0	5.5	V	-
V_{IH} High Level Input Voltage, Vcc = 5V	2.2			V	1,2
V_{IL} Low Level Input Voltage, Vcc = 5V			0.7	V	1,2

Electrical Characteristics

(T_A = -55°C to +125°C)

Parameter	Test Conditions	Min	Max	Unit	Notes
V_{OH} High Level Output Voltage	Vcc = 4.5V	2.4		V	4
V_{OL} Low Level Output Voltage	Vcc = 4.5V		0.4	V	4
I_{IH} High Level Input Current	Vcc = 5.5V, V_{IN} = 2.4V	-200 -25	-700 -400	µA µA	2 3
I_{IL} Low Level Input Current	Vcc = 5.5V, V_{IN} = 0.4V	-400 -25	-900 -400	µA µA	2 3
I_{CC} Supply Current	Vcc = 5.5V		20	mA	4

Notes:

1. RTAD 0/1/2/3/4 and RTADPAR ONLY.
2. ALL Inputs and Bidirectionals other than those in Note 1.
3. I_{OL} max = 3mA / I_{OH} max = -2mA TX INHIBIT 0/1 and TX DATA/$\overline{DATA}$ ONLY. I_{OL} max = 2mA / I_{OH} max = -1 mA. ALL remaining Outputs and Bidirectionals.
4. Input Clock (running) = 6Mhz, ALL remaining Inputs are Open and ALL Outputs and Bidirectionals have no load.

Clock Requirements

Frequency	6.0 MHz
Stability -55°C to +125°C	±0.01% (100ppm)
Maximum Asymmetry	48 - 52%
Rise/Fall Time	10ns MAX
Output Level	Logic "0" 0.4V MAX Logic "1" 2.4V MIN

REMOTE TERMINAL OPERATION

Receive Data Operation

All valid data words associated with a valid receive data command word for the RT are passed to the subsystem. The RT examines all command words from the bus and will respond to valid (i.e. correct Manchester, parity coding etc.) commands which have the correct RT address (or broadcast address if the RT broadcast option is enabled). When the data words are received, they are decoded and checked by the RT and, if valid, passed to the subsystem on a word by word basis at 20 µs intervals. This applies to receive data words in both Bus Controller to RT and RT to RT messages. When the RT detects that the message has finished, it checks that the correct number of words have been received and if the message is fully valid, then a Good Block Received signal is sent to the subsystem, which must be used by the subsystem as permission to use the data just received.

The subsystem must therefore have a temporary buffer store up to 32 words long into which these data words can be placed. The Good Block Received signal will allow use of the buffer store data once the message has been validated.

If a block of data is not validated, then Good Block Received will not be generated. This may be caused by any sort of message error or by a new valid command for the RT being received on another bus to which the RT must switch.

Transmit Data Operation

If the RT receives a valid transmit data command addressed to the RT, then the RT will request the data words from the subsystem for transmission on a word by word basis. To allow maximum time for the subsystem to collect each data word, the next word is requested by the RT as soon as the transmission of the current word has commenced.

It is essential that the subsystem should provide all the data words requested by the RT once a transmit sequence has been accepted. Failure to do so will be classed by the RT as a subsystem failure and reported as such to the Bus Controller.

Control of Data Transfers

This section describes the detailed operation of the data transfer mechanism between the RT and subsystems. It covers the operations of the signals $\overline{\text{DTRQ}}$, $\overline{\text{DTAK}}$, IUSTB, H/$\overline{\text{L}}$, $\overline{\text{GBR}}$, $\overline{\text{NBGT}}$, TX/$\overline{\text{RX}}$ during receive data and transmit data transfers.

Figure 7 shows the operation of the data handshaking signals during a receive command with two data words. When the RT has fully checked the command word, $\overline{\text{NBGT}}$ is pulsed low, which can be used by the subsystem as an initialization signal. TX/$\overline{\text{RX}}$ will be set low indicating a receive command. When the first data word has been fully validated, $\overline{\text{DTRQ}}$ is set low. The subsystem must then reply within approximately 1.5 µs by setting $\overline{\text{DTAK}}$ low. This indicates to the RT that the subsystem is ready to accept data. The data word is then passed to the subsystem on the internal highway IH08-IH715 in two bytes using IUSTB as a strobe signal and H/$\overline{\text{L}}$ as the byte indicator (high byte first followed by low byte). Data is valid about both edges of IUSTB. Signal timing for this handshaking is shown in Figure 12.

If the subsystem does not declare itself busy, then it must respond to $\overline{\text{DTRQ}}$ going low by setting $\overline{\text{DTAK}}$ low within approximately 1.5 us. Failure to do so will be classed by the RT as a subsystem failure and reported as such to the Bus Controller.

It should be noted that IUSTB is also used for internal working in the RT. $\overline{\text{DTRQ}}$ being low should be used as an enable for clocking data to the subsystem with IUSTB.

Once the receive data block has finished and been checked by the RT, $\overline{\text{GBR}}$ is pulsed low if the block is entirely correct and valid. This is used by the subsystem as permission to make use of the data block. If no $\overline{\text{GBR}}$ signal is generated, then an error has been detected by the RT and the entire data block is invalid and no data words in it may be used.

If the RT is receiving data in an RT to RT transfer, the data handshaking signals will operate in an identical fashion but there will be a delay of approx 70 µs between $\overline{\text{NBGT}}$ going low and $\overline{\text{DTRQ}}$ first going low. See Figure 10.

Figure 6 shows the operation of the data handshaking signals during transmit command with three data words. As with the receive command discussed previously, $\overline{NBGT}$ is pulsed low if the command is valid and for the RT. TX/$\overline{RX}$ will be set high indicating a transmit data command. While the RT is transmitting its status word, it requests the first data word from the subsystem by setting $\overline{DTRQ}$ low. The subsystem must then reply within approximately 13.5 µs by setting $\overline{DTAK}$ low. By setting $\overline{DTAK}$ low, the subsystem is indicating that it has the data word ready to pass to the RT. Once $\overline{DTAK}$ is set low by the subsystem, $\overline{DTRQ}$ should be used together with H/$\overline{L}$ and TX/$\overline{RX}$ to enable first the high byte and then the low byte of the data word onto the internal highway IH08-IH715. The RT will latch the data bytes during IUSTB, and will then return $\overline{DTRQ}$ high. Data for each byte must remain stable until IUSTB has returned low. Signal timing for this handshaking is shown in Figure 11.

Additional Data Information Signals

At the same time as data transfers take place, a number of information signals are made available to the subsystem. These are $\overline{INCMD}$, the subaddress lines SA0-SA4, the word count lines WC0-WC4 and current word count lines CWC0-CWC4. Use of these signals is optional.

$\overline{INCMD}$ will go active low while the RT is servicing a valid command for the RT. The subaddress, transmit/receive bit, and word count from the command word are all made available to the subsystem as SA0-SA4, TX/$\overline{RX}$ and WC0-WC4 respectively. They may be sampled when $\overline{INCMD}$ goes low and will remain valid while $\overline{INCMD}$ is low.

The subaddress is intended to be used by the subsystem as an address pointer for the data block. Subaddress 0 and 31 are mode commands, and there can be no receive or transmit data blocks associated with these. (Any data word associated with a mode command uses different handshaking operations. If the subsystem does not use all the subaddresses available, then some of the subaddress lines may be ignored.

The TX/$\overline{RX}$ signal indicates the direction of data transfer across the RT - subsystem interface. Its use is described in the previous section.

The word count tells the subsystem the number of words to expect to receive or transmit in a message, up to 32 words. A word count of all 0s indicates a count of 32 words.

The current word count is set to 0 at the beginning of a new message and is incremented following each data word transfer across the RT - subsystem interface. (It is clocked on the falling edge of the second IUSTB pulse in each word transfer). It should be noted that there is no need for the subsystem to compare the word count and current word count to validate the number of words in a message. This is done by the RT.

Subsystem Use of Status Bits and Mode Commands

General Description

Use of the status bits and the mode commands is one of the most confusing aspects of MIL-STD-1553B. This is because much of their use is optional, and also because some involve only the RT while others involve both the RT and the subsystem.

The CT1990/1 allows full use to be made of all the Status Bits, and also implements all the Mode Commands. External programming of the Terminal Flag and Subsystem Flag Bits plus setting of the Message Error Bit on reception of an illegal command when externally decoded is available. The subsystem is given the opportunity to make use of Status Bits, and is only involved in Mode Commands which have a direct impact on the subsystem.

The mode commands in which the subsystem may be involved are Synchronize, Sychronize with data word, Transmit Vector Word, Reset and Dynamic Bus Control Acceptance. The Status Bits to which the subsystem has access, or control are Service Request, Busy, Dynamic Bus Control Acceptance, Terminal Flag, Subsystem Flag, and Message Error Bit. Operation of each of these Mode Commands and of the Status Bits is described in the following sections.

All other Mode Commands are serviced internally by the RT. The Terminal Flag and Message Error Status Bits and BIT Word contents are controlled by the RT; however the subsystem has the option to set the Message Error Bit and to control the reset conditions for the Terminal Flag and Subsystem Flag Bits in the Status Word, and the Transmitter Timeout, Subsystem Handshake, and Loop Test Fail Bits in the BIT Word.

Synchronize Mode Commands

Once the RT has validated the command word and checked for the correct address, the SYNC line is set low. The signal WC4 will be set low for a Synchronize mode command (See Figure 16), and high for a Synchronize with data word mode command (See Figure 15). In a Synchronize with data word mode command, SYNC remains low during the time that the data word is received. Once the data word has been validated, it is passed to the subsystem on the internal highway IH08-IH715 in two bytes using IUSTB as a strobe signal and H/L as the byte indicator (high byte first followed by low byte). SYNC being low should be used on the enable to allow IUSTB to clock synchronize mode data to the subsystem.

If the subsystem does not need to implement either of these mode commands, the SYNC signal can be ignored, since the RT requires no response from the subsystem.

Transmit Vector Word Mode Command

Figure 14 illustrates the relevant signal timings for an RT receiving a valid Transmit Vector Word mode command. The RT requests data by setting $\overline{\text{VECTEN}}$ low. The subsystem should use H/$\overline{\text{L}}$ to enable first the high byte and then the low byte of the Vector word onto the internal highway IH08-IH715.

It should be noted that the RT expects the Vector word contents to be already prepared in a latch ready for enabling onto the internal highway when $\overline{\text{VECTEN}}$ goes low. If the subsystem has not been designed to handle the Vector word mode command, it will be the fault of the Bus Controller if the RT receives such a command. Since the subsystem is not required to acknowledge the mode command, the RT will not be affected in any way by Vector word circuitry not being implemented in the subsystem. It will however transmit a data word as the Vector word, but this word will have no meaning.

Reset Mode Command

Figure 8 shows the relevant signal timings for an RT receiving a valid reset mode command. Once the command word has been fully validated and serviced, the $\overline{\text{RESET}}$ signal is pulsed low. This signal may be used as a reset function for subsystem interface circuitry.

Dynamic Bus Allocation

This mode command is intended for use with a terminal which has the capability of configuring itself into a bus controller on command from the bus. The line $\overline{\text{DBCREQ}}$ cannot go true unless the $\overline{\text{DBCACC}}$ line was true at the time of the valid command, i.e. tied low. For terminals acting only as RTs, the signal $\overline{\text{DBCACC}}$ should be tied high (inactive), and the signal $\overline{\text{DBCREQ}}$ should be ignored and left unconnected.

Use of the Busy Status Bit

The Busy Bit is used by the subsystem to indicate that it is not ready to handle data transfers either to or from the RT.

The RT sets the bit to logic one if the $\overline{\text{BUSY}}$ line from the subsystem is active low at the time of the second falling edge of INCLK after $\overline{\text{INCMD}}$ goes low. This is shown in Figure 13. Once the Busy bit is set, the RT will stop all receive and transmit data word transfers to and from the subsystem. The data transfers in the Synchronize with data word and Transmit Vector word mode commands are not affected by the Busy bit and will take place even if it has been set.

It should be noted that a minimum of 0.5 µs subaddress decoding time is given to the subsystem before setting of status bits. This allows the subsystem to selectively set the Busy bit if for instance one subaddress is busy but others are ready. This option will prove useful when an RT is interfacing with multiple subsystems.

Use of the Service Request Status Bit

The Service Request bit is used by the subsystem to indicate to the Bus Controller that an asynchronous service is requested.

The timing of the setting of this bit is the same as the Busy bit and is shown in Figure 13. Use of $\overline{\text{SERVREQ}}$ has no effect on the RT apart from setting the Service Request bit.

It should be noted that certain mode commands require that the last status word be transmitted by the RT

instead of the current one, and therefore a currently set status bit will not be seen by the Bus Controller. Therefore the user is advised to hold $\overline{\text{SERVREQ}}$ low until the requested service takes place.

Use of the Subsystem Status Bit

This status bit is used by the RT to indicate a subsystem fault condition. If the subsystem sets $\overline{\text{SSERR}}$ low at any time, the subsystem fault condition in the RT will be set, and the Subsystem Flag status bit will subsequently be set. The fault condition will also be set if a handshaking failure takes place during a data transfer to or from the subsystem. The fault condition is cleared on power-up or by a Reset mode command.

Dynamic Bus Control Acceptance Status Bit

$\overline{\text{DBCACC}}$, when set true, enables an RT to configure itself into a Bus Controller, if the subsystem has the capability, by allowing $\overline{\text{DBCREQ}}$ to pulse true and BIT TIME 18 to be set in the status response. If Dynamic Bus Control is not required then $\overline{\text{DBCACC}}$ must be tied high. $\overline{\text{DBCACC}}$ tied high inhibits $\overline{\text{DBCREQ}}$ and clears BIT TIME 18 in the status response.

OPTIONAL STATUS WORD CONTROL

Message Error Bit

The CT1990/1 monitors all receptions for errors and sets the Message Error Bit as prescribed in MIL-STD-1553B. The subsystem designer may, however, exercise the option of monitoring for illegal commands and forcing the Message Error Bit to be set.

The word count and subaddress lines for the current command are valid when $\overline{\text{INCMD}}$ goes low. The subsystem must then determine whether or not the word count or subaddress is to be considered illegal by the RT. If either of them is considered illegal, the subsystem must produce a positive-going pulse called MEREQ. The positive-going edge of MEREQ must occur within 500 ns of the falling edge of $\overline{\text{INCMD}}$.

Subsystem Flag and Terminal Flag Bits

The conditions that cause the Subsystem Flag and Terminal Flag Bits in the Status Word to be reset may be controlled by the subsystem using the $\overline{\text{ENABLE}}$, $\overline{\text{BIT DECODE}}$, $\overline{\text{NEXT STATUS}}$, and $\overline{\text{STATUS UPDATE}}$ inputs. If $\overline{\text{ENABLE}}$ is inactive (high), then the Terminal Flag and Subsystem Flag behavior is the same as described below: (i.e. the other three option lines are disabled).

Subsystem Flag Bit

This bit is reset to logic zero by a power up initialization or the servicing of a legal mode command to reset the remote terminal (code 01000).

This bit shall be set in the current status register if the subsystem error line, $\overline{\text{SSERR}}$, from the subsystem ever goes active low. This bit shall also be set if an RT/subsystem handshaking failure occurs. This bit, once set, shall be repeatedly set until the detected error condition is known to be no longer present.

Terminal Flag Bit

This bit is reset to logic zero by a power up initialization or the servicing of a legal mode command to reset the remote terminal (code 01000). This bit can be set to logic one in the current status register in four possible ways:

a) If the RX detects any message encoding error in the terminals transmission. A loop test failure, LTFAIL, will be signalled which shall cause the Terminal Flag to be set and the transmission aborted.
b) If a transmitter timeout occurs while the terminal is transmitting.
c) If a remote terminal self test fails.
d) If there is a parity error in the hard wired address to the RX chip.

This bit, once set, shall be repeatedly set until the detected error condition is known to be no longer present. The transmission of this bit as a logic one can be inhibited a legal mode command to inhibit terminal flag bit (code 00110). Similarly, this inhibit can be removed by a mode command to override inhibit terminal flag bit (code 00111), a power up initialization or a legal mode command to reset remote terminal (code 01000).

If $\overline{\text{ENABLE}}$ is held low, then the three options described below are available and are essentially independent. Any, all, or none may be selected. Also, reporting of faults by the subsystem requires that $\overline{\text{SSERR}}$ be latched (not pulsed) low until the fault is cleared.

Resetting SSF and TF on Receipt of Valid Commands

If $\overline{\text{ENABLE}}$ is selected and the other three option lines are held high, then the Status Word Register will be reset on receipt of any valid command with the exception of Transmit Status and Transmit Last Command. Note that in this mode, the TF will never be seen in the Status Word, and the SSF will only be seen if $\overline{\text{SSERR}}$ is latched low. Also note that the SSF will not be seen in response to Transmit Status or Transmit Last Command if the preceding Status Word was clear, regardless of actions taken on the $\overline{\text{SSERR}}$ line after the clear status transmission.

Status Register Update at Fault Occurrence

If $\overline{\text{STATUS UPDATE}}$ is selected (held low), then the TF or SSF will appear in response to a Transmit Status or Transmit Last Command issued as the first command after the fault occurs. Any other command (except as noted in the Preserving the BIT Word section) will reset the TF and SSF. Repeated Transmit Status or Transmit Last Command immediately following the fault will continue to show the TF and/or SSF in the Status Word. Note that this behavior may not meet the "letter-of-the-spec" as described in MIL-STD-1553B, but is considered the "preferred" behavior by some users.

TF and SSF Reporting in the Next Status Word After the Fault

If $\overline{\text{NEXT STATUS}}$ is selected (held low), then the TF or SSF will appear in response to the very next valid command after the fault except for Transmit Status or Transmit Last Command. The flag(s) will be reset on receipt of any valid command following the status transmission with the flag(s) set except for Transmit Status, Transmit Last Command, or as noted in the following section on Preserving the BIT Word.

Preserving the BIT Word

In order to preserve the Transmitter Timeout Flag, Subsystem Handshake Failure, and Loop Test Failure Bits in the BIT Word, it is necessary to select $\overline{\text{BIT DECODE}}$ (hold it low). This will prevent resetting those bits if the Transmit Bit Word Mode Command immediately follows the fault or follows a Transmit Last Command or Transmit Status immediately following the fault. It will also prevent resetting the TF and SSF Bits in the Status Word. Any other valid commands will cause those BIT Word Bits and the Status Word Bits to be reset.

Bus Driver/Receiver Interface

Receive Data

The decoder chip requires two TTL signals, RXDATA and $\overline{\text{RXDATA}}$, to represent the data coming in from the bus. PDIN should be driven to a logic level ‘1’ when the bus waveform exceeds a specified positive threshold and NDIN should be driven to a logic level ‘1’ when a specified negative threshold is exceeded. During the quiet period on the bus both signals should be at the same logic level. All the bus receivers must be permanently enabled, the selection of the bus in use is controlled within the ASIC.

Transmit Data

The signals generated by the encoder chip, TXDATA and $\overline{\text{TXDATA}}$, are of the same format as the receive data. The only difference is that the TTL signals are negative logic, e.g. the signal is active when on logic level "0". This means that when the encoder is quiet both TXDATA and $\overline{\text{TXDATA}}$ are at logic level "1". Both the signals should be used in conjunction with TXINHIBIT 0 and TXINHIBIT 1. TX INHIBIT 0 and TX INHIBIT 1 enable the appropriate driver when it should be transmitting. Figure 5 shows an example of a typical interface circuit between the CT1990/1 and a driver/receiver unit.

BUS CONTROL OPERATION

To enable its use in a bus controller the ASIC has additional logic within it. This logic can be enabled by pulling the pin labelled RT/$\overline{BC}$ low. Once the ASIC is in bus control mode, all data transfers must be initiated by the bus control processor correctly commanding the ASIC via the subsystem interface. In bus control mode six inputs are activated which in RT mode are inoperative and four signals with dual functions exercise the second function (the first being for the RT operation).

To use the CT1990/1 as a 1553B bus control interface, the bus control processor must be able to carry out four basic bus-related functions. Two inputs, BCOPA and BCOPB allow these four options to be selected. The option is then initiated by sending a negative-going strobe on the $\overline{BCOPSTB}$ input. $\overline{BCOPSTB}$ must only be strobed low when $\overline{NDRQ}$ is high. This is particularly important when two options are required during a single transfer.

With these options all message types and lengths can be handled. Normal BC/RT exchanges are carried out in ASIC option zero. This is selected by setting BCOPA and BCOPB to a zero and strobing $\overline{BCOPSTB}$. On receipt of the strobe, the CT1990/1 loads the command word from an external latch using CWEN and H/L The command word is transmitted down the bus. The TX/$\overline{RX}$ bit is, however, considered by the ASIC as being its inverse and so if a transmit command is sent to a RT (Figure 17), the ASIC in BC mode believes it has been given a receive command. As the RT returns the requested number of data words plus its status, the BC carries out a full validation check and passes the data into the subsystem using $\overline{DTRQ}$, $\overline{DTAK}$, H/$\overline{L}$, IUSTB and CWC as in RT operation. It also supplies $\overline{GBR}$ at the end of a valid transmission. Conversely, a receive command sent down the bus is interpreted by the BC as a transmit command, and so the requisite data words are added to the command word. See Figure 18.

For mode commands, where a single command word is required, option one is selected by strobing $\overline{BCOPSTB}$ when BCOPA is high and BCOPB is low. On receiving the strobe, the command word is loaded from the external latch using $\overline{CWEN}$ and H/$\overline{L}$, the correct sync and parity bits are added and the word transmitted (See Figure 20). Mode commands followed by a data word requires option two. Option two, selected by strobing $\overline{BCOPSTB}$ while BCOPA is low and BCOPB is high, loads a data word via $\overline{DWEN}$ and H/$\overline{L}$, adds sync and parity and transmits them to the bus (See Figure 21). If the mode code transmitted required the RT to return a data word, then selecting option three by strobing $\overline{BCOPSTB}$ when BCOPA and BCOPB are both high will identify that data word and if validated, output it to the subsystem interface using RMDSTB and H/$\overline{L}$. This allows data words resulting from mode codes to be identified differently from ordinary data words and routed accordingly (See Figure 22). All received status words are output to the subsystem interface using STATSTB and H/$\overline{L}$.

In BC option three, if the signal $\overline{PASMON}$ is active, then all data appearing on the selected bus is output to the subsystem using STATSTB for command and status words or RMDSTB for data words.

RT to RT transfers require the transmission of two command words. A receive command to one RT is contiguously followed by a transmit command to the other RT. This can be achieved by selecting option one followed by option zero for the second command. The strobe ($\overline{BCOPSTB}$) for option zero must be delayed until $\overline{NDRQ}$ has gone low and returned high following the strobe for option one. The RT transmissions are checked and transferred in the subsystem interface to the bus control processor (See Figure 19).

Note: For all BC operations, BCOPA and BCOPB must remain valid and stable for a minimum of 1 µs following the leading (negative going) edge of $\overline{BCOPSTB}$.

PASSIVE MONITOR

The Monitor Mode may be utilized to analyze or collect all activities which occur on a selected bus. This is initiated by selecting a bus, placing the unit in BC option three and setting $\overline{PASMON}$ low. All data appearing on the selected bus is output to the subsystem using STATSTB for Command and Status Words or RMDSTB for Data Words.

AUTOMATED SELF-TEST

The CT1991 has been designed to fully support a wrap-around self-test which ensures a high degree of fault coverage. The monolithic circuit includes all circuitry required to perform the self-test.

Self-test can be an on-line or off-line function which is initiated by simple subsystem intervention. The $\overline{\text{DRVINH}}$ signal selects on-line or off-line testing. The circuit accomplishes the on-line test without accessing the MIL-STD-1553 data bus by providing an internal data path which connects the encoder circuitry directly to the decoder circuitry. The transceiver is inhibited during this on-line test. The off-line test is designed to include the transceiver as well as the protocol device. This mode will generally be useful as an off-line card test where no live bus is in use.

To initiate the self-test a word is placed in the Vector Word Latch, Loop Test Enable ($\overline{\text{LTEN}}$) is held low, and the Loop Test Trigger ($\overline{\text{LTTRIG}}$) signal is pulsed low. The primary bus will be tested with the word that resides in the Vector Word Latch, encoded then looped back, decoded and presented to the subsystem as a normal data transfer would be accomplished. The secondary bus is sequentially tested after the primary bus is completed via Request Bus A (REQBUSA) utilizing the same word residing in the Vector Word Latch. Upon completion of each test, pass/fail signals will be asserted reporting the results of the test. This test implementation verifies MIL-STD-1553 protocol compliance; proper sync character, 16 data bits, Manchester II coding, odd parity, contiguous word checking and a bit by bit comparison of the transmitted data. The self-test circuitry increases the fault coverage by insuring that the internal function blocks; encoder, decoder, and internal control circuitry are operating correctly. An effective data pattern to accomplish this is HEX AA55 since each bit is toggled, (8 bit internal highway) on a high/low byte basis. The total time required to complete the self-test cycle is 89 microseconds. The Loop Test Enable signal must remain in the low state throughout the diagnostic cycle.

Pin Description

Signal	Direction	Signal Description
RX DATA 0/1	INPUT	**Positive Data In.** This should be a TTL description of the positive, half of the Manchester code data on the bus. It should be driven to a logic level “1” when a predetermined positive threshold is exceeded on the bus.
RX $\overline{\text{DATA}}$ 0/1	INPUT	**Negative Data In.** This should be a TTL description of the negative half of the Manchester code data on the bus. It should be driven to a logic level “1” when a predetermined negative threshold is exceeded on the bus.
TX INHIBIT 0	OUTPUT	**Transmitter Inhibit Bus 0.** Normally high. Goes low when the transmitter is transmitting. Should be used to Inhibit the bus "0" driver.
TX INHIBIT 1	OUTPUT	**Transmitter Inhibit Bus 1.** Normally high. Goes low when the transmitter is transmitting. Should be used to Inhibit the bus "1" driver.
TX DATA	OUTPUT	**Positive Data Out** - When this signal goes high the bus should be driven positive.
TX $\overline{\text{DATA}}$	OUTPUT	**Negative Data Out** - When this signal goes high the bus should be driven negative.
RTAD 0-4	INPUT	**RT address lines** - These should be hardwired by the user. RTAD4 is the most significant bit.
RTADPAR	INPUT	**RT address parity line** - This must be hardwired by the user to give odd parity.
$\overline{\text{BIT DECODE}}$	INPUT	**Built-In Test Decode** - When held low, prevents resetting TXTO Bit, HSFAIL Bit, and LTFAIL Bit in the BIT Word (as well as TF and SSF Bits in the Status Word) upon receipt of a Transmit Bit Word Mode Command.
BCSTEN 0/1	INPUT	**Broadcast command enable Bus 0/1** - When low the recognition of broadcast command is prevented on both Bus 0 and 1. *CT1991 only.*
BCSTEN 0	INPUT	**Broadcast command enable Bus 0** - When low the recognition of broadcast command is prevented on Bus 0. *CT1990 only.*
BCSTEN 1	INPUT	**Broadcast command enable Bus 1** - When low the recognition of broadcast command is prevented on Bus 1. *CT1990 only.*
6MCK	INPUT	**6 Megahertz master clock.**
IH 08 (LSB) IH 19 IH 210 IH 311 IH 412 IH 513 IH614 IH715 (MSB)	BI-DIRECTIONAL	**Internal Highway** - Bi-directional 8 bit highway on which 16 bit words are passed in two bytes. IH 715 is the most significant bit of each byte, the most significant byte being transferred first. The highway should only be driven by the subsystem when data is to be transferred to the RT.
$\overline{\text{DTRQ}}$	OUTPUT	**Data Transfer Request** - Goes low to request a data transfer between the ASIC and subsystem. Goes high at the end of the transfer.
$\overline{\text{DTAK}}$	INPUT	**Data Transfer Acknowledge** - Goes low to indicate that the subsystem is ready for the data transfer.
IUSTB	OUTPUT	**Interface Unit Strobe** - This is a double pulse strobe used to transfer the two bytes of data
H/$\overline{\text{L}}$	OUTPUT	**High/Low** - Indicates which byte of data is on the internal highway. Logic level "0" for least significant byte.
$\overline{\text{GBR}}$	OUTPUT	**Good Block Received** - Pulses low for 500ns when a block of data has been received by the ASIC and has passed all the validity and error checks.

Pin Description (Cont.)

Signal	Direction	Signal Description
$\overline{\text{NBGT}}$	OUTPUT	**New Bus Grant** - Pulses low whenever a new command is accepted by the ASIC.
MEREQ	INPUT	**Message Error Request** - Positive-going edge will cause Message Error Bit in Status Word to be set.
TX/$\overline{\text{RX}}$	OUTPUT	**Transmit/Receive** - The state of this line informs the subsystem whether it is to transmit or receive data The signal is valid while $\overline{\text{INCMD}}$ is low.
$\overline{\text{INCMD}}$	OUTPUT	**In Command** - Goes low when the RT is servicing a valid command. The subaddress and word count lines are valid while the signal is low.
WC0-WC4	OUTPUT	**Word Count** - These five lines specify the requested number of data words to be received or transmitted. Valid when $\overline{\text{INCMD}}$ is low.
SA0-SA4	OUTPUT	**Sub Address** - These five lines are a label for the data being transferred. Valid when INCMD is low.
CWC0-CWC4	OUTPUT	**Current Word Count** - These five lines define which data word in the message is currently being transferred.
$\overline{\text{SYNC}}$	OUTPUT	**Synchronize** - Goes low when a synchronize mode code is being serviced.
$\overline{\text{VECTEN}}$/$\overline{\text{DWEN}}$	OUTPUT	**Vector Word Enable/DataWord Enable** - In the RT mode, this signal is provided to enable the contents of the vector word latch (which is situated in the subsystem) onto the ASIC's internal highway. This signal, when in the Bus Controller mode, is used to enable mode code data from the subsystem onto the internal highway.
$\overline{\text{RESET}}$	OUTPUT	**Reset** - This line pulses low for 500ns on completion of the servicing of a valid and legal mode command to reset remote terminal.
$\overline{\text{SSERR}}$	INPUT	**Subsystem Error** - By taking this line low, the subsystem can set the Subsystem Flag in the Status Word.
$\overline{\text{BUSY}}$	INPUT	**Busy** - This signal should be driven low if the subsystem is not ready to perform a data transfer to or from the ASIC.
$\overline{\text{SERVREQ}}$	INPUT	**Service Request** - This signal should be driven low to request an asynchronous transfer and left low until the transfer has taken place.
INCLK	OUTPUT	**Internal Clock (2 MHz)** - This is made available for synchronization use by the subsystem if required. However, many of the outputs to the subsystem are asynchronous.
$\overline{\text{EOT}}$	OUTPUT	**End of Transmission** - Goes low if a valid sync plus two data bits do not appear in time to be contiguous with preceding word.
$\overline{\text{RTADER}}$	OUTPUT	**Remote Terminal Address Error** - This line goes low if an error is detected in the RT address parity of the selected receiver. Any receiver detecting an error in the RT address will turn itself off.
$\overline{\text{HSFAIL}}$	OUTPUT	**Handshake Failure** - This line pulses low if the allowable time for $\overline{\text{DTAK}}$ response has been exceeded during the ASIC/subsystem data transfer handshaking.
$\overline{\text{LSTCMD}}$/$\overline{\text{CWEN}}$	OUTPUT	**Last Command/Command Word Enable** - This line pulses low when servicing a valid and legal mode command to transmit last command. When in RT mode this line must not be used to enable data from the subsystem. This line also pulses low, when in the Bus Control mode, when a command word is required for transmission.

Pin Description (Cont.)

Signal	Direction	Signal Description
$\overline{\text{STATEN}}$/ STATSTB	OUTPUT	**Status Enable/Status Strobe** - This line pulses low to enable the status word onto the internal highway for transmission. When in RT mode this line must not be used to enable data from the subsystem. This line also pulses high, when in the Bus Control mode, to strobe received status words into the subsystem. When $\overline{\text{PASMON}}$ is true this line pulses high for Command and Status words.
$\overline{\text{STAT UPDATE}}$	INPUT	**Status Update** - When held low, causes TF or SSF to appear in Status Word response to Transmit Status or Transmit Last Command issued immediately after fault occurrence
$\overline{\text{BITEN}}$/ RMDSTB	OUTPUT	**Built In Test Enable/Receive Mode Data Strobe** - This line pulses low when servicing a valid and legal mode command to transmit the internal BIT word. This signal is for information only and must not be used to enable data from the subsystem. This line also pulses high when in the Bus Control mode when mode data is received to be passed to the subsystem and when data is passed to the subsystem during $\overline{\text{PASMON}}$.
$\overline{\text{DWSYNC}}$	OUTPUT	**Data Word Sync** - This line goes low if a data word sync and two Manchester biphase bits are valid. *CT1990 only.*
$\overline{\text{ENABLE}}$	INPUT	**Enable** - When held low, enables Bit Decode, Next Status, and Status Update program lines.
$\overline{\text{CMSYNC}}$	OUTPUT	**Command Word Sync** - This line goes low if a command word sync and two Manchester biphase bits are valid. *CT1990 only.*
$\overline{\text{NDRQ}}$	OUTPUT	**No Data Required** - This line goes low if the encoder transmit buffer is full i.e. another word is going to be transmitted. This signal is for information only and must not be used to enable data from the subsystem.
$\overline{\text{NEXT STAT}}$	INPUT	**Next Status** - When held low, causes TF or SSF to appear in very next Status Word after fault occurrence (except for Transmit Status or Transmit Last Command).
$\overline{\text{PASMON}}$	INPUT	**Passive Monitor** - When functioning as a Bus Controller this line acts as a passive monitor select. The active going edge of this line will cause the REQBUS lines to be latched and that bus, now selected will be monitored so long as $\overline{\text{PASMON}}$ remains low. All traffic on the bus will be handed, after validation, to the subsystem via STATSTB for status and commands words, and RMDSTB for data words.
$\overline{\text{BCOPSTB}}$	INPUT	**Bus Controller Operation Strobe** - When functioning as a Bus Controller a low going pulse on this line will initiate the selected bus controller operation on the requested bus, using BCOPA&B and REQBUSA&B.
RMDSTB		**See $\overline{\text{BITEN}}$/RMDSTB.**
BCOPA	INPUT	**Bus Control Operation A** - Least significant bit of the bus controller operation select lines.
BCOPB	INPUT	**Bus Control Operation B** - Most significant bit of the bus controller operation select lines.
REQBUS A	BI-DIRECTIONAL	**Request Bus A** - This line, when in RT mode, is the least significant bit of the bus request lines which specify the origin of the command, i.e. they are sources. When in BC mode these lines are sinks and specify which bus is to be used for the next command.
REQBUS B	BI-DIRECTIONAL	**Request Bus B** - Most significant bit of the bus request lines. (See above for description.)

Pin Description (Cont.)

Signal	Direction	Signal Description
RT/$\overline{BC}$	INPUT	**Remote Terminal/Bus Control** - This line when high causes the ASIC to function as a remote terminal. When low the ASIC functions as a bus controller or passive monitor.
$\overline{DBCACC}$	INPUT	**Dynamic Bus Control Accept** - This line should be permanently tied low if a subsystem is able to accept control of the bus if offered.
$\overline{LTFAIL}$	OUTPUT	**Loop Test Fail** - This line goes low if any error in the transmitted waveform is detected or if any parity error in the hardwired RT address is detected.
$\overline{ERROR}$	OUTPUT	**Error** - This line latches low if a Manchester or parity error is detected. It is reset by the next $\overline{CMSYNC}$ (RT mode) and also by $\overline{RTO}$ in the BC mode.
$\overline{RTO}$	OUTPUT	**Reply Time Out** - This signal will pulse low whenever the reply time for a transmitting terminal has been exceeded. This line is intended for the bus controller use.
$\overline{TXTO}$	OUTPUT	**Transmitter Time Ou**t - This line goes true if the transmitter time out limits are exceeded.
$\overline{PARER}$	OUTPUT	**Parity Error** - This line will pulse low if a parity error is detected by the decoder.
$\overline{MANER}$	OUTPUT	**Manchester Error** - This line will pulse low if a Manchester error is detected by the decoder.
$\overline{DBCREQ}$	OUTPUT	**Dynamic Bus Control Request** - This line will pulse low when the status reply for a mode code Dynamic Bus Control has finished where the accept bit was set.
$\overline{VALD}$	OUTPUT	**Valid Data** - This line will pulse low when a valid data word is received.
$\overline{DRVINH}$	INPUT	**Driver Inhibit** - Selects on-line or off-line testing during automated self test. When high self test is on-line. Must be high when $\overline{LTEN}$ is high. *CT1991 only.*
$\overline{LTEN}$	INPUT	**Loop Test Enable** - Enables automated self-test when low. Normally high. *CT1991 only.*
$\overline{LTTRIG}$	INPUT	**Loop Test Trigger** - When pulsed low while $\overline{LTEN}$ is low automated self-test is initiated. $\overline{LTEN}$ pulse width should be 100ns $\leq$ PW $\leq$ 5µs. *CT1991 only.*

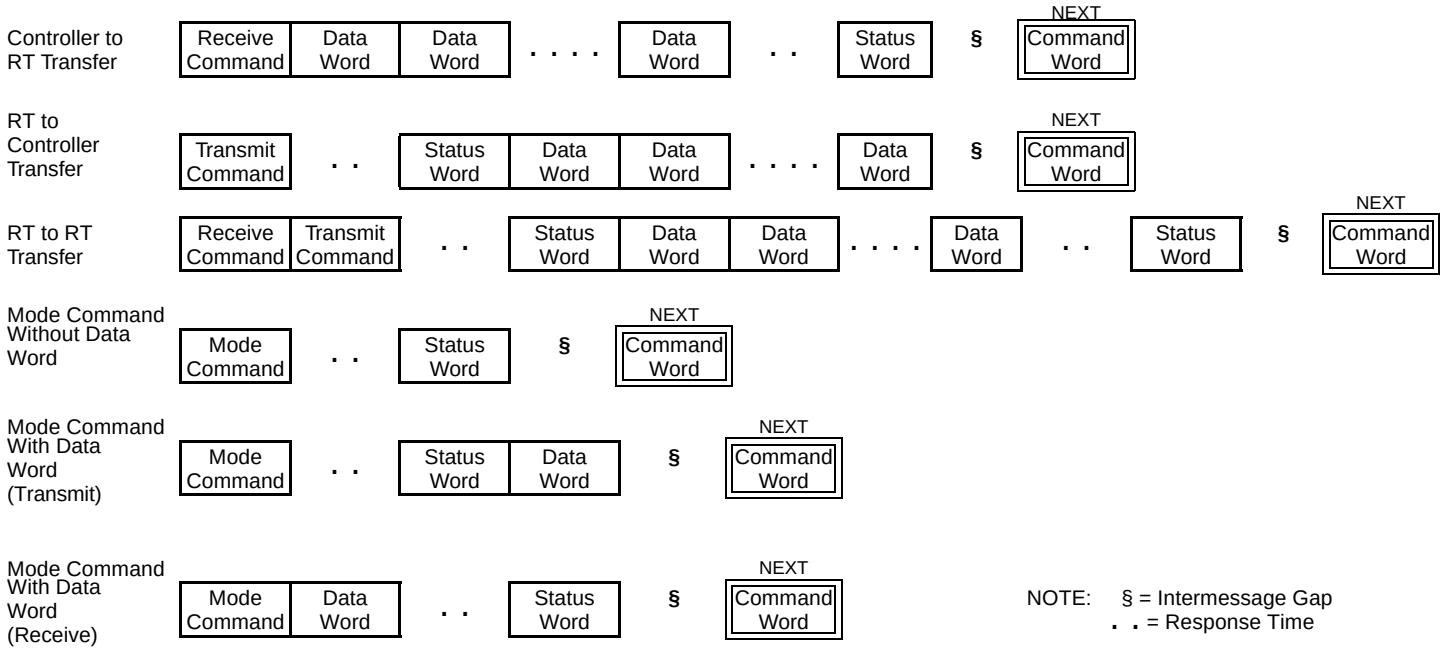
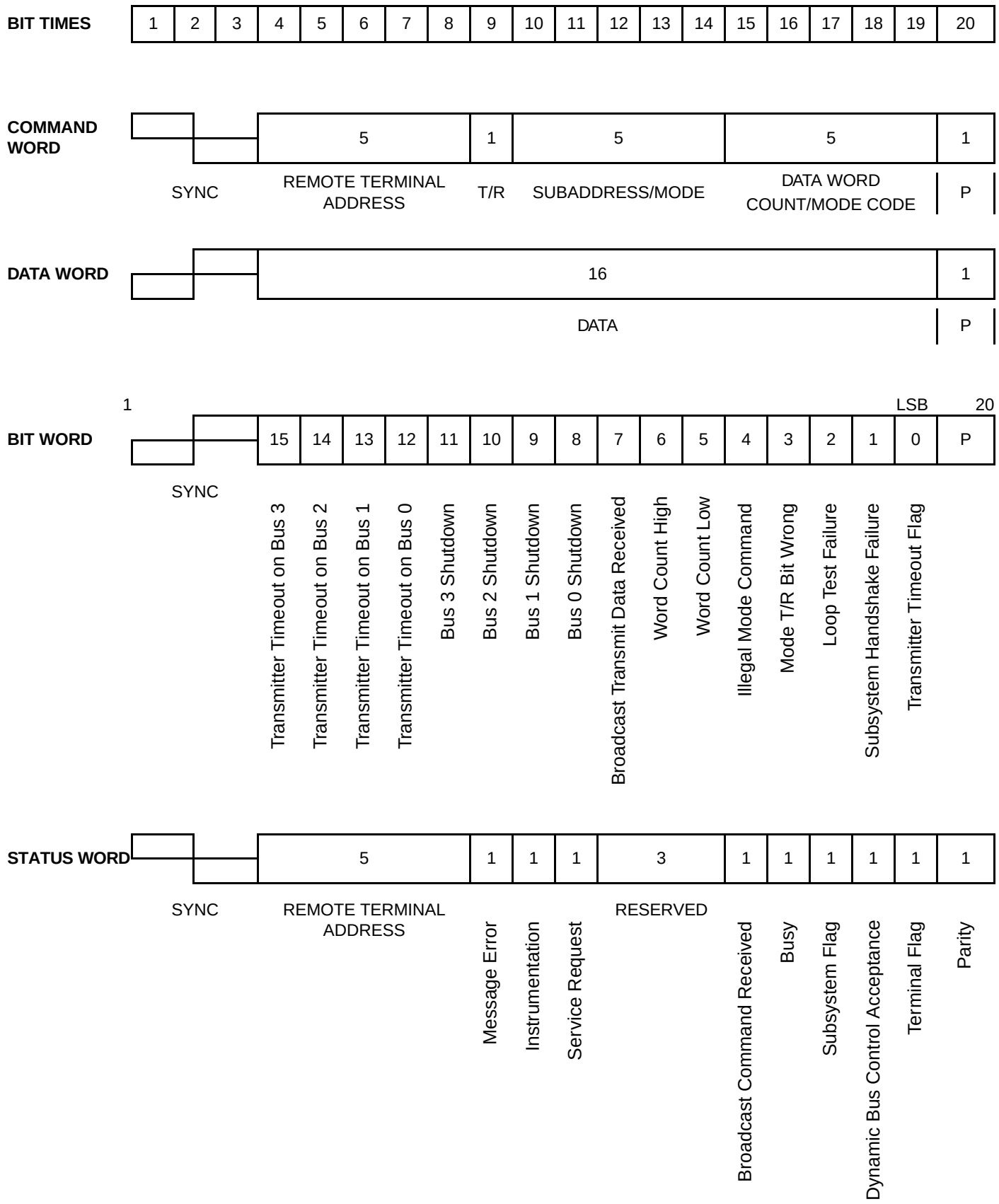


Figure 1 – Typical Message Formats

T/R Bit	Mode Code	Function	Associated Data Word	Broadcast Command Allowed
1	00000	Dynamic Bus Control	No	No
1	00001	Synchronize	No	Yes
1	00010	Transmit Status Word	No	No
1	00011	Initiate Self Test	No	Yes
1	00100	Transmitter Shutdown	No	Yes
1	00101	Override Transmitter Shutdown	No	Yes
1	00110	Inhibit Terminal Flag Bit	No	Yes
1	00111	Override Inhibit Terminal Flag Bit	No	Yes
1	01000	Reset Remote Terminal	No	Yes
1	01001	Reserved	No	TBD
	↓	↓	↓	↓
1	01111	Reserved	No	TBD
1	10000	Transmit Vector Word	Yes	No
0	10001	Synchronize	Yes	Yes
1	10010	Transmit Last Command	Yes	No
1	10011	Transmit BITWord	Yes	No
0	10100	Selected Transmitter Shutdown	Yes	Yes
0	10101	Override Selected Transmitter Shutdown	Yes	Yes
1 or 0	10110	Reserved	Yes	TBD
	↓	↓	↓	↓
1 or 0	11111	Reserved	Yes	TBD

Figure 2 – Assigned Mode Codes



Note: T/R – Transmit/Receive
P – Parity

Figure 3 – Word Count

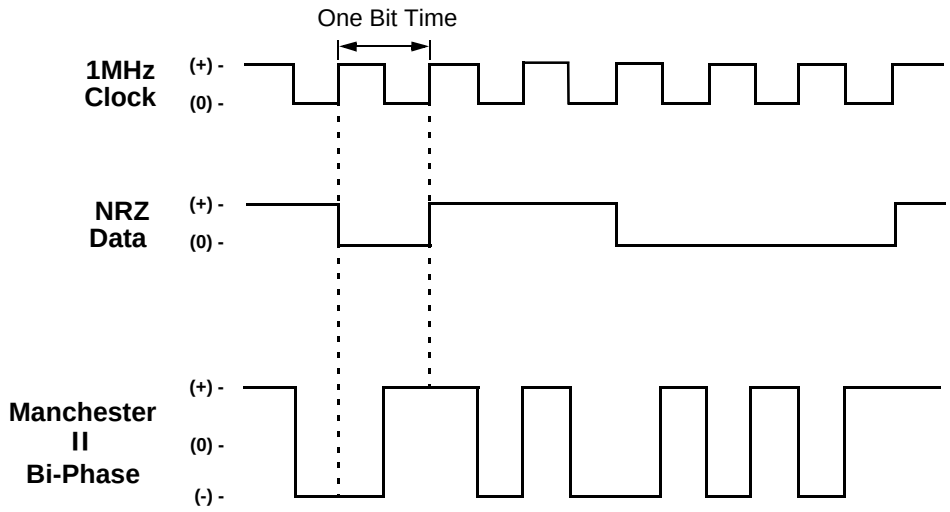


Figure 4 – Data Encoding

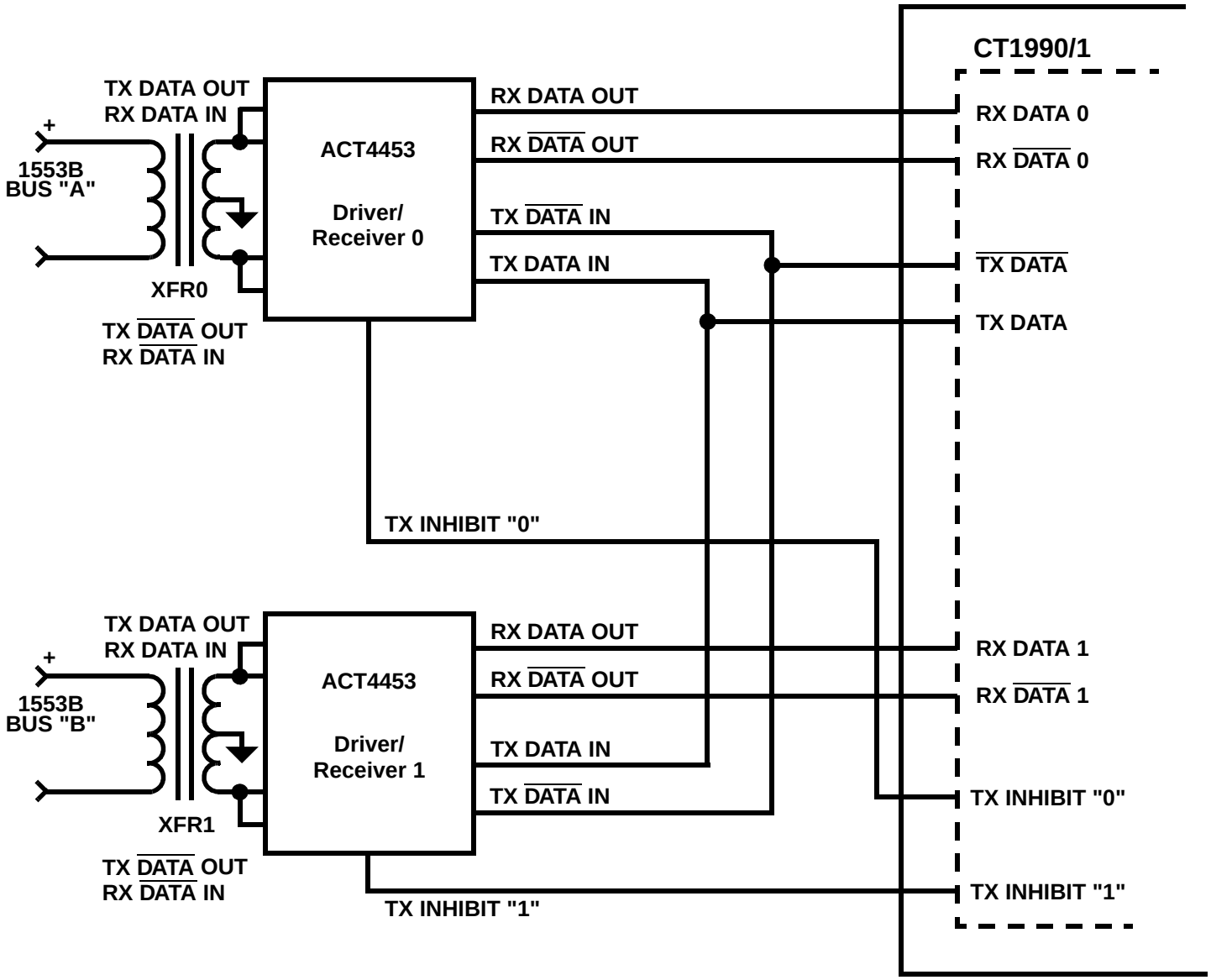


Figure 5 – Example of an Interface between the CT1990/1 and Driver/Receiver

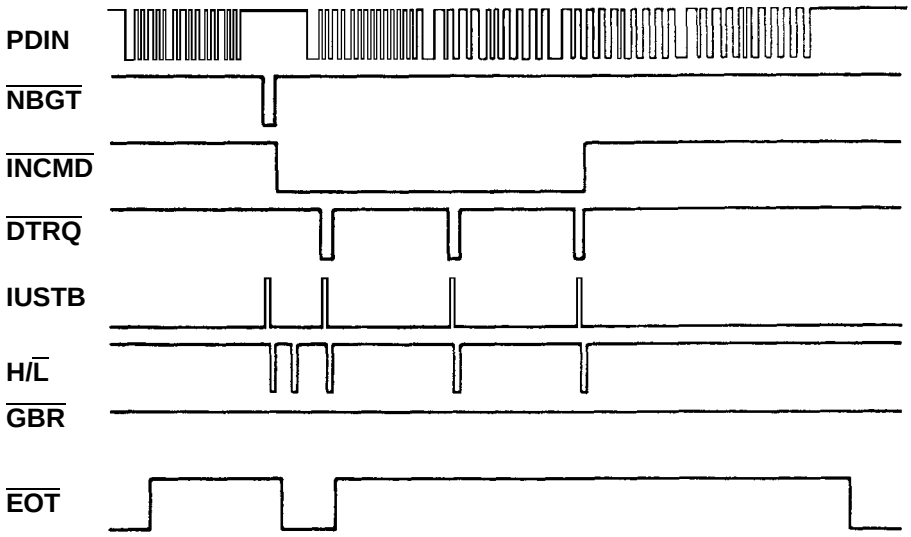


Figure 6 – Transfer of three Data Words from RT 03 to BC

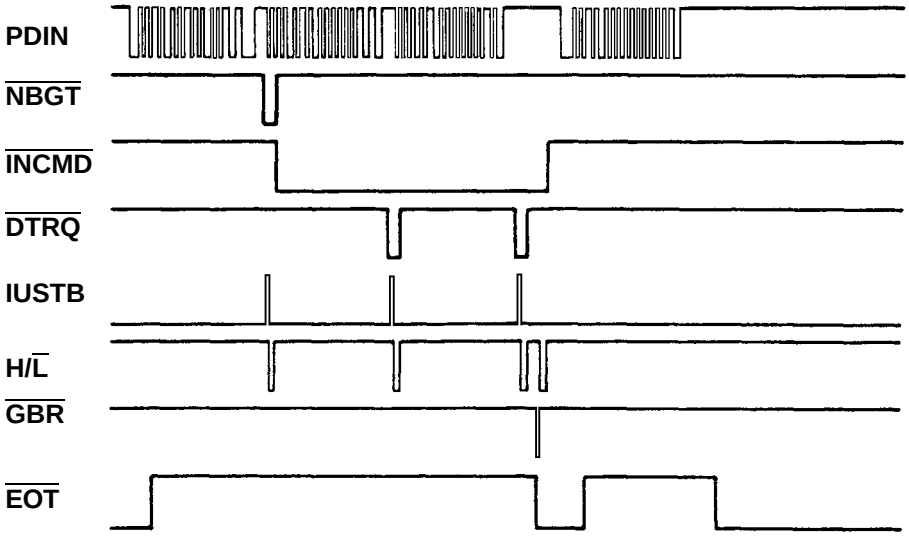


Figure 7 – Transfer of two Data Words from BC to RT 03

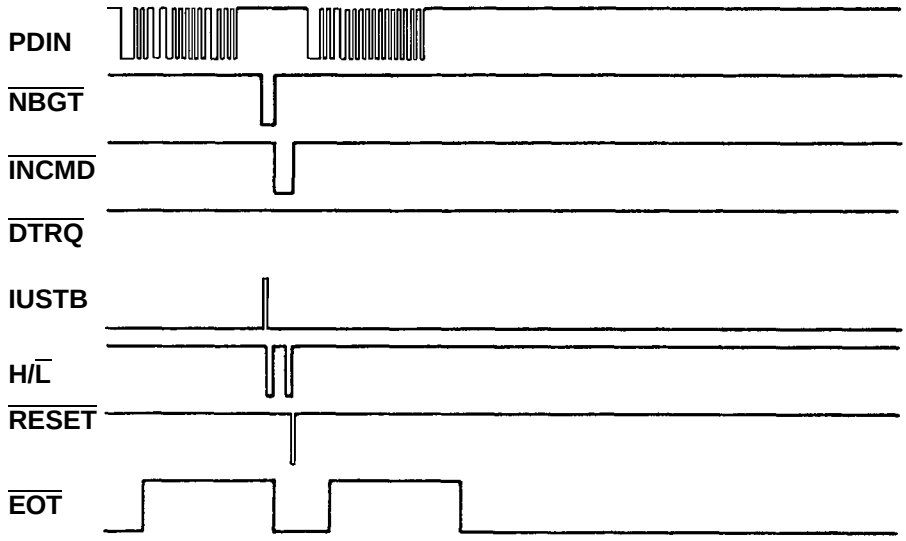


Figure 8 – Mode Command Reset Remote Terminal

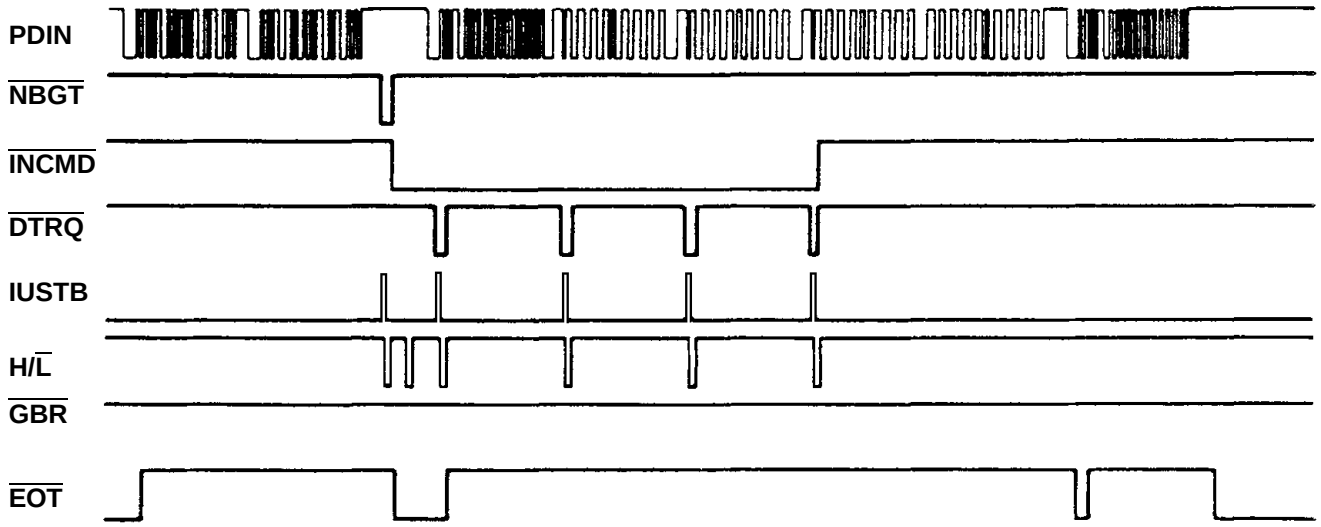


Figure 9 – RT to RT transfer of four data words (This RT sending the data)

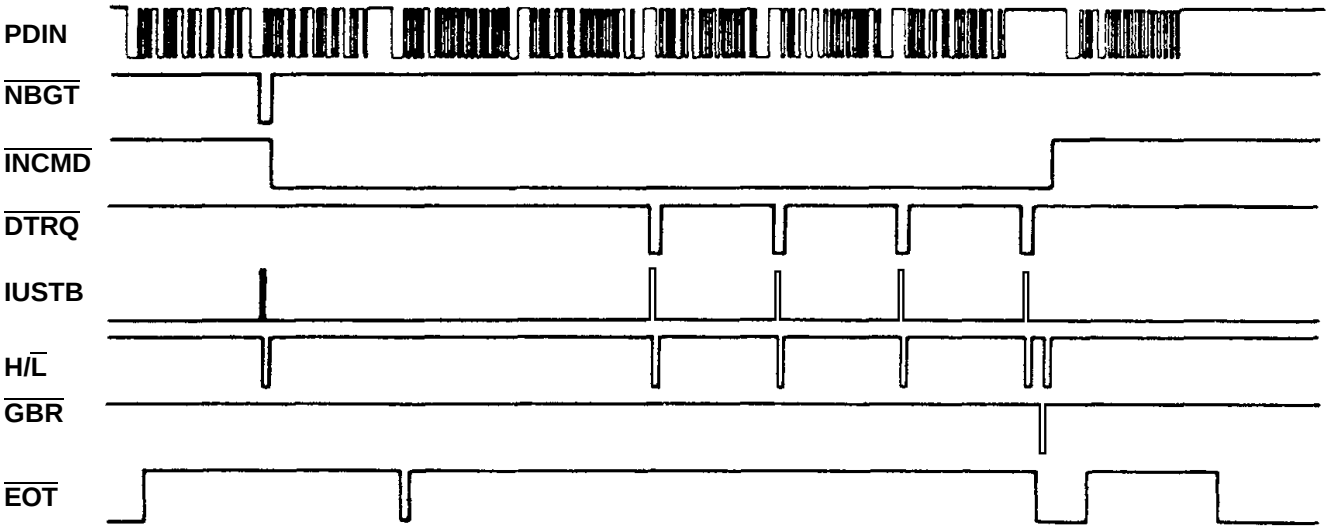


Figure 10 – RT to RT transfer of four data words (This RT receiving the data)

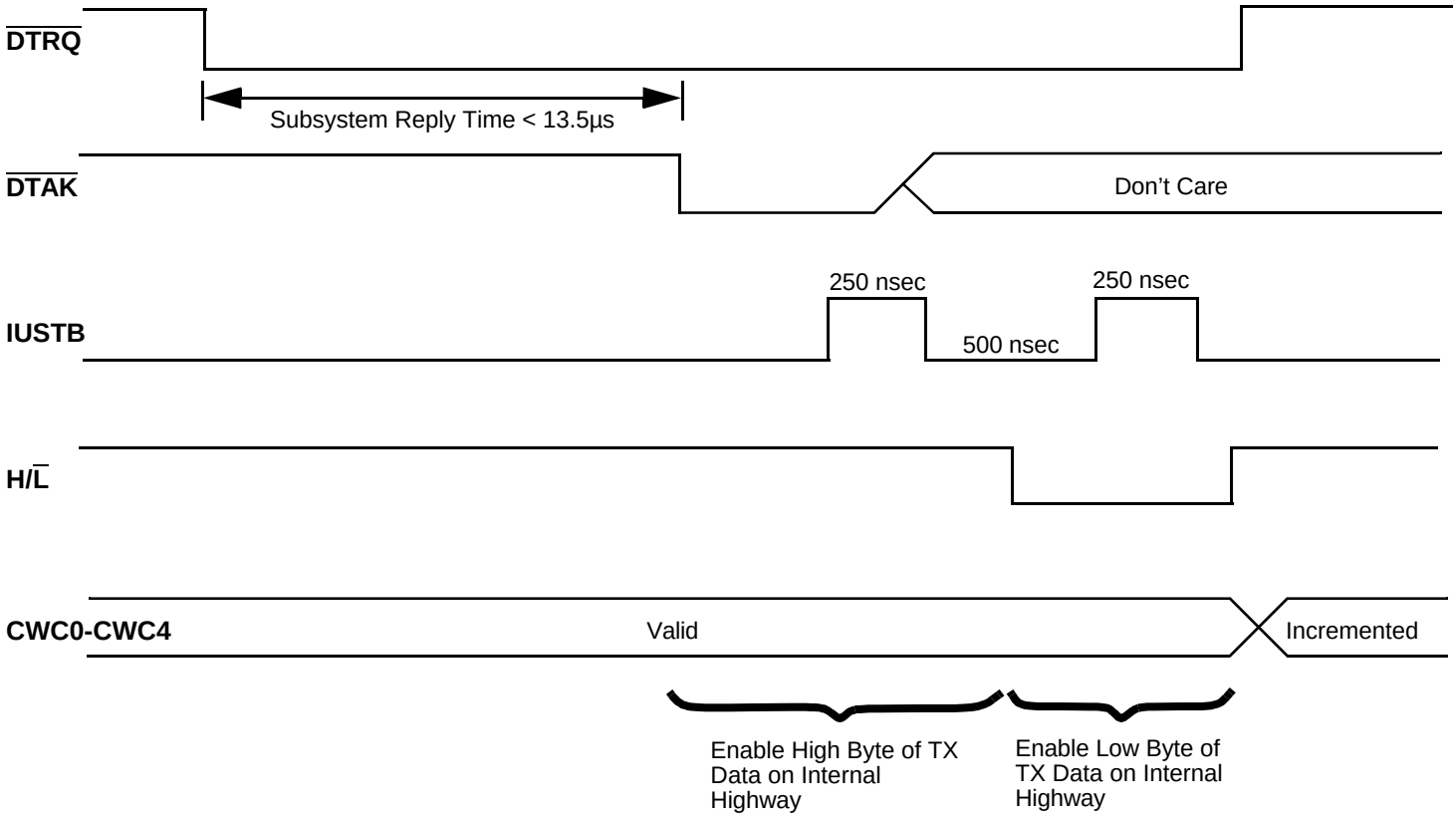


Figure 11 – Handshaking for Tx Data Transfers

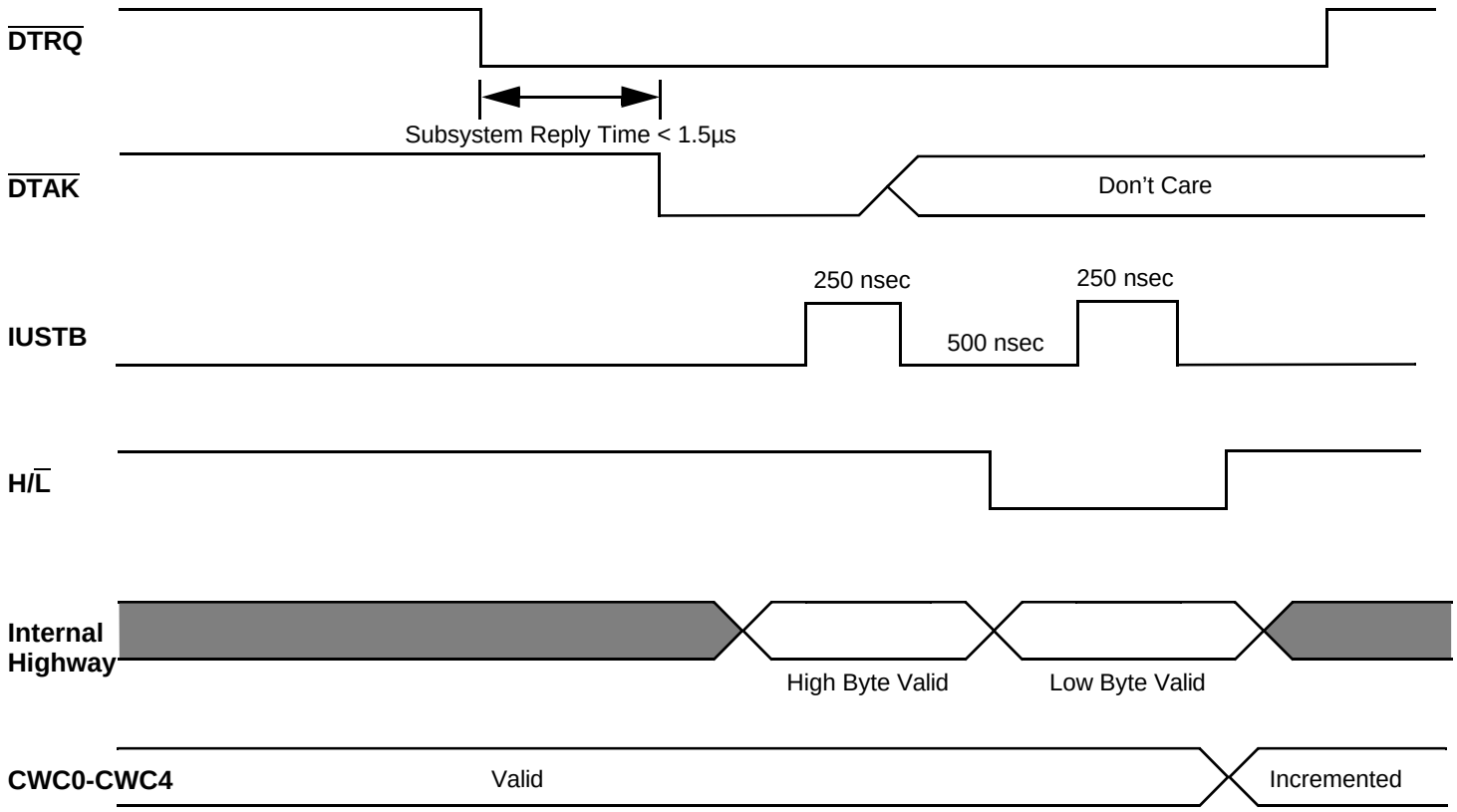


Figure 12 – Handshaking for Rx Data Transfers

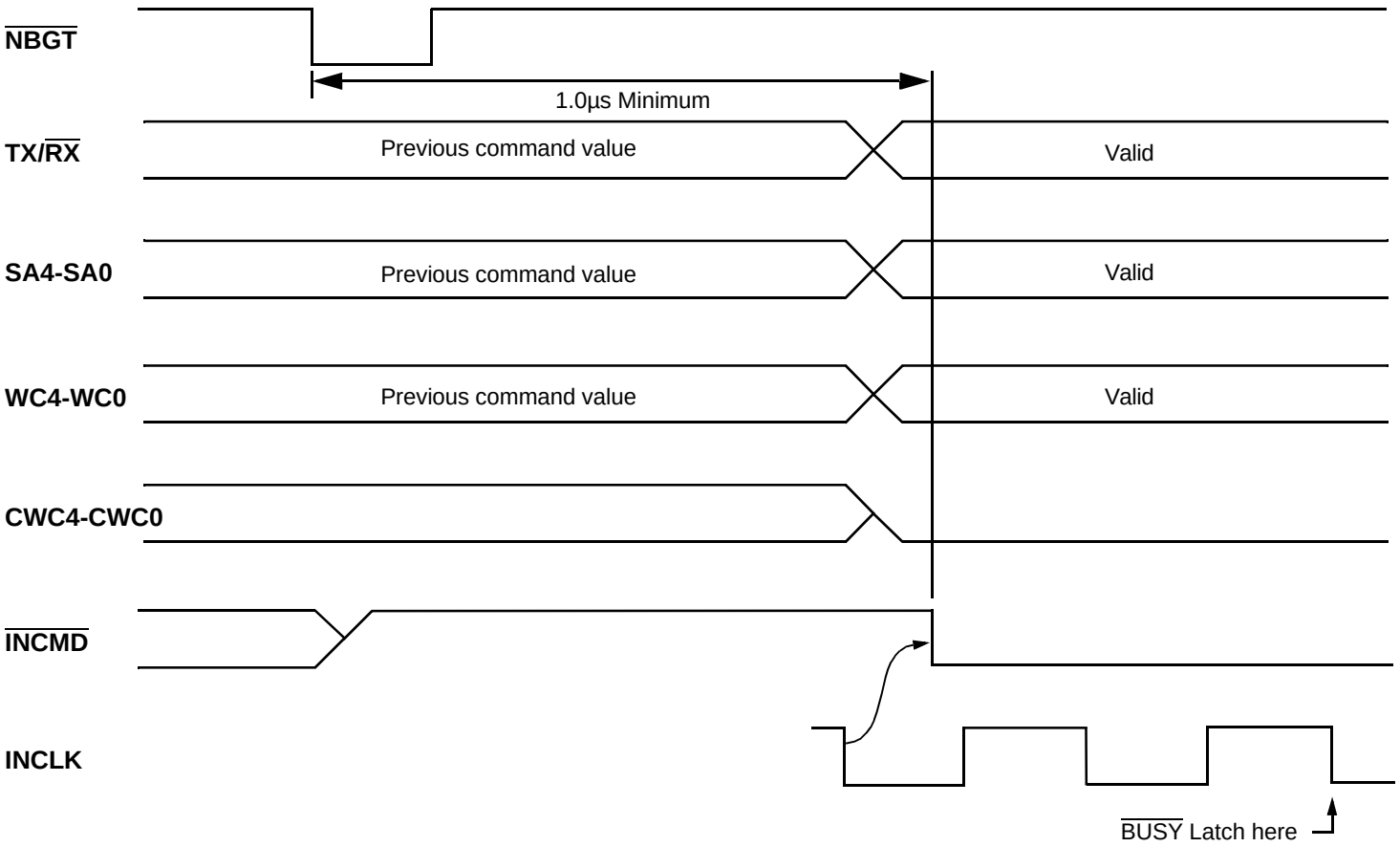


Figure 13 – New Command Initialization

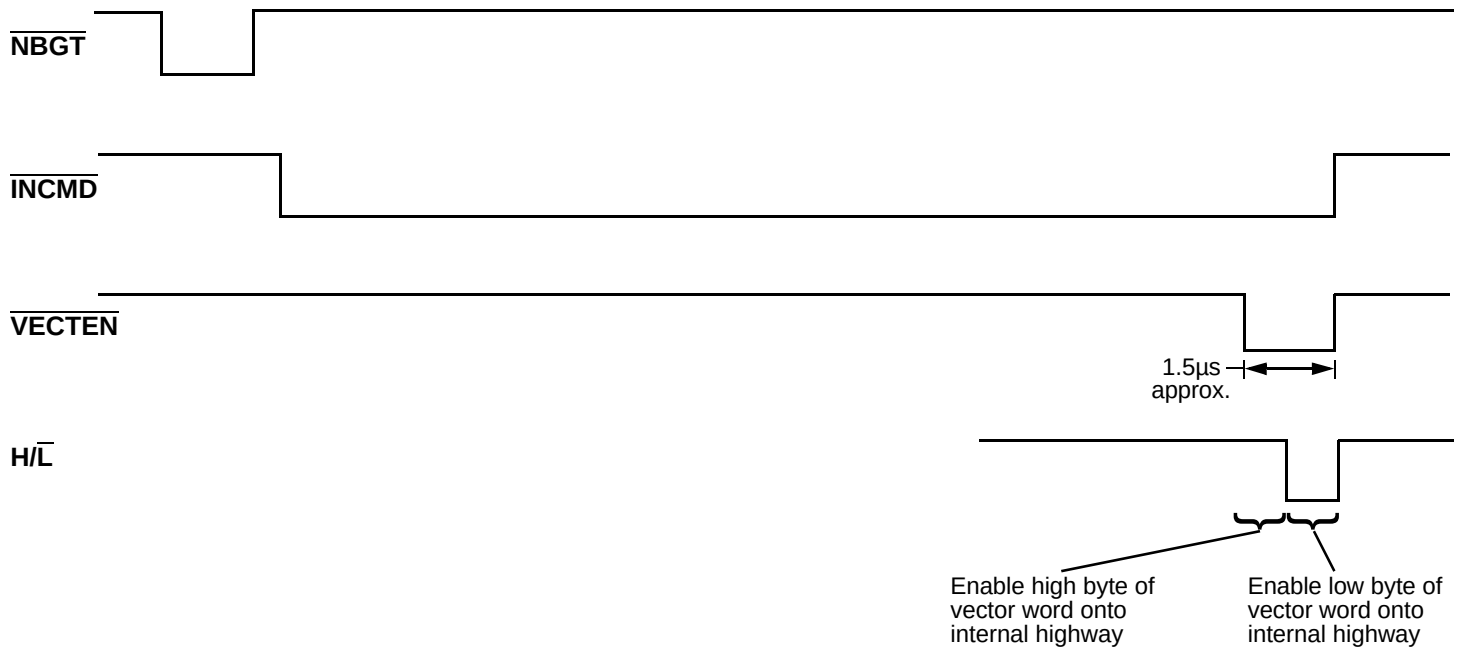


Figure 14 – Transmit Vector Word Command

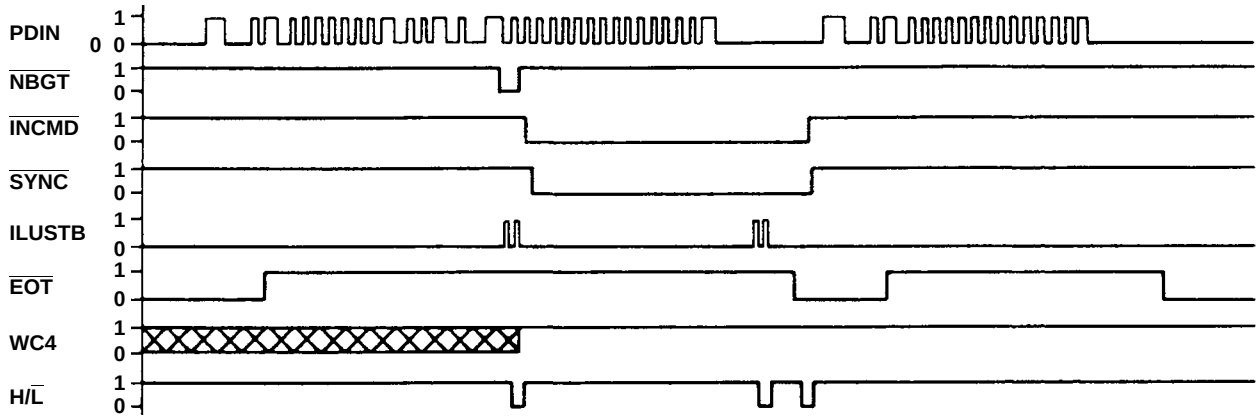


Figure 15 – Synchronize (with data) mode command

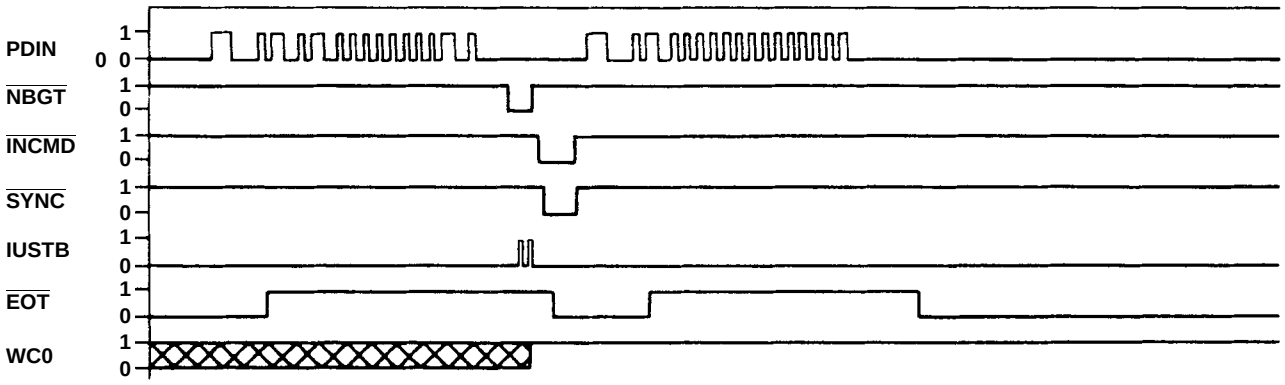


Figure 16 – Synchronize (no data) mode command

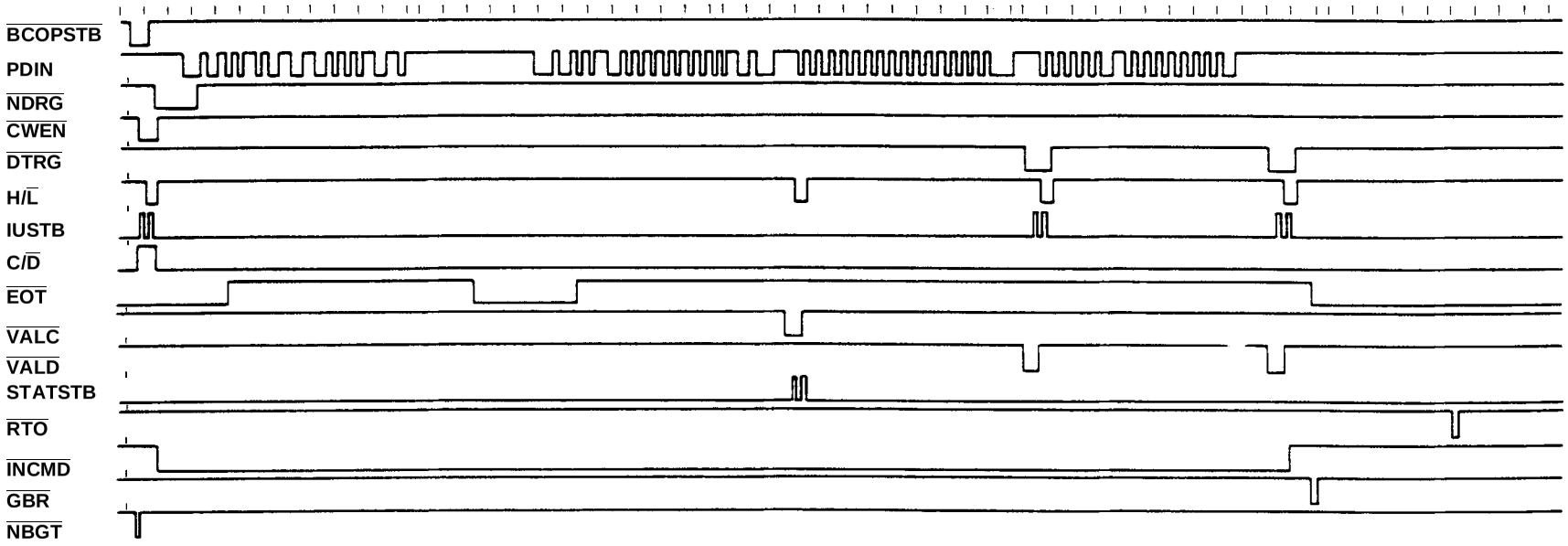


Figure 17 – BUS Controller sending command to RT 10001 to transmit two data words

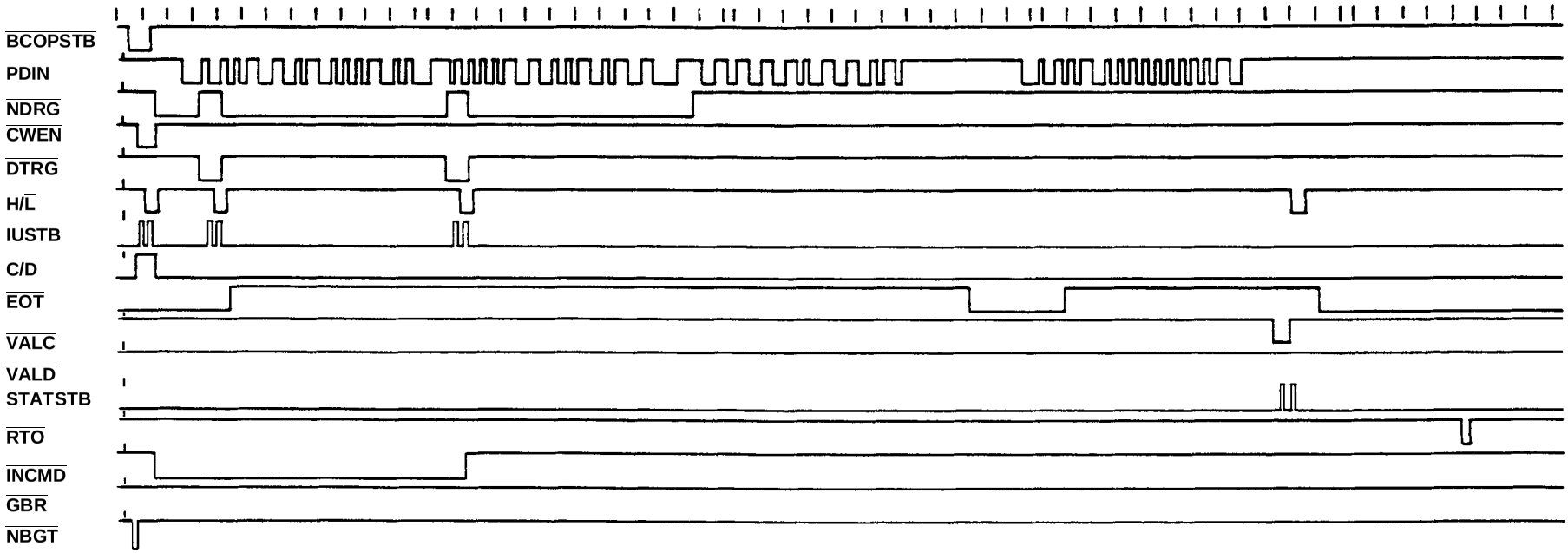


Figure 18 – BUS Controller sending command to RT 10001 to receive two data words

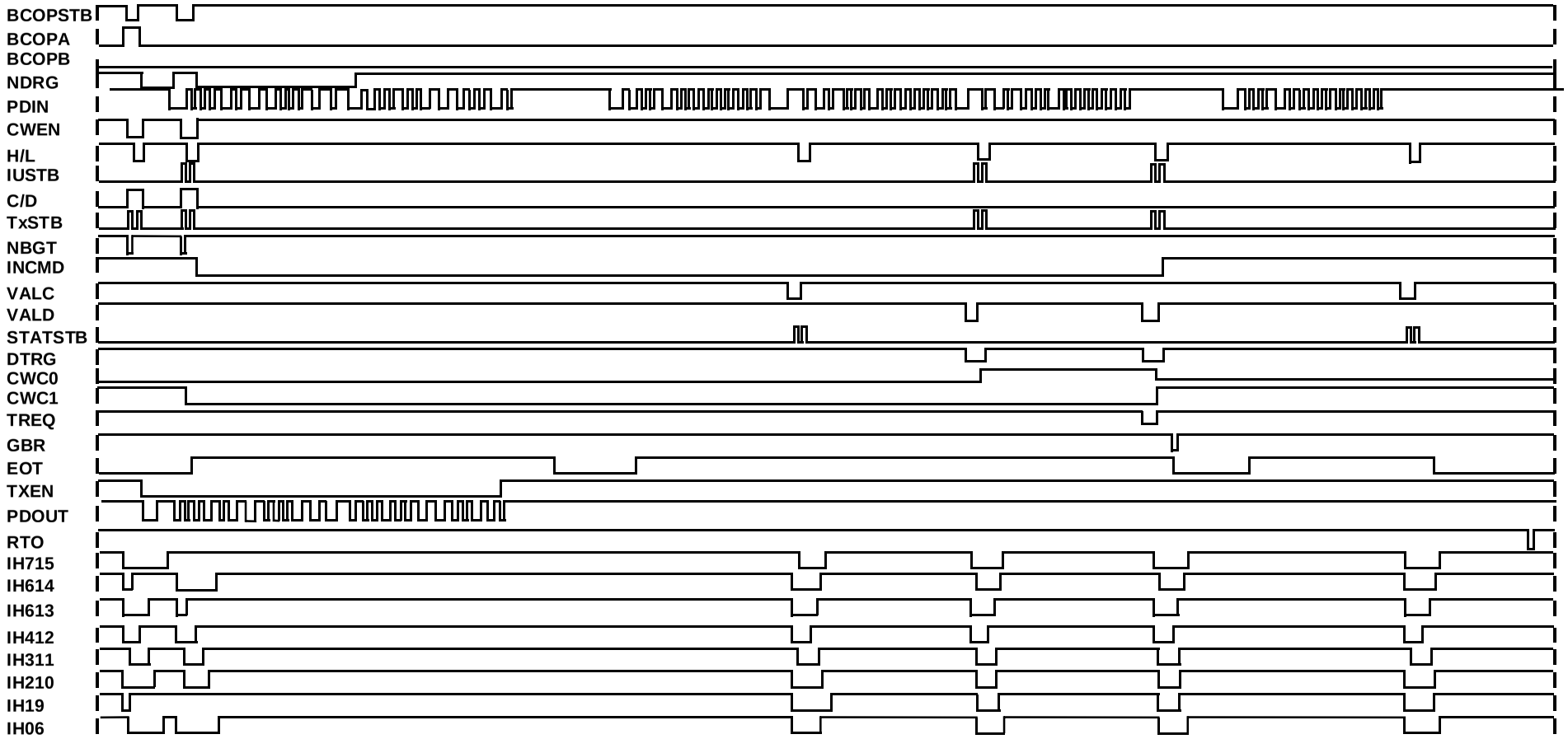


Figure 19 – BUS Controller commanding RT 10001 to transmit two data words at RT 00001

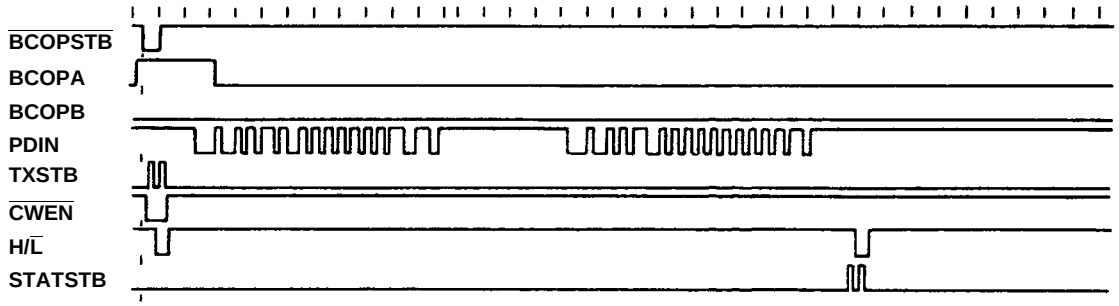


Figure 20 – BUS Controller sending mode command transmit status word mode code 00010

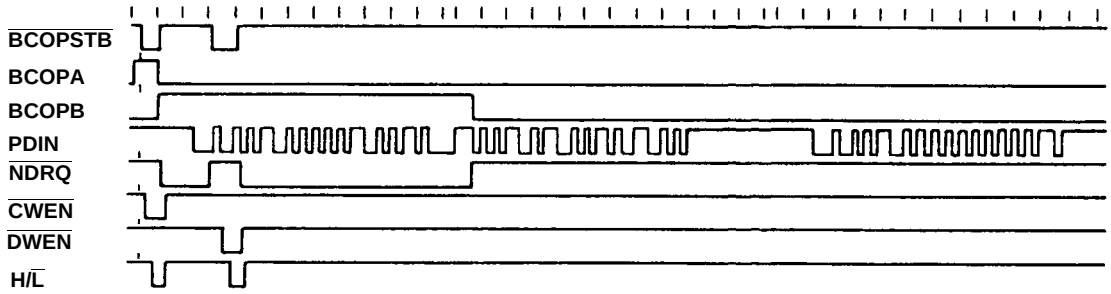


Figure 21 – BUS Controller sending mode command synchronize mode code 10001

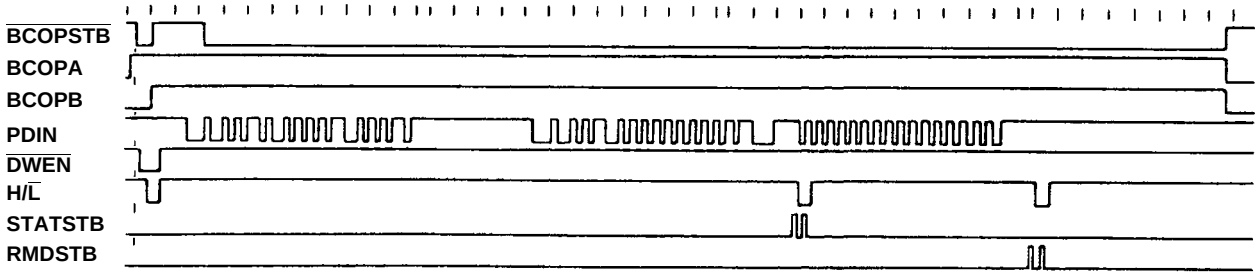


Figure 22 – BUS Controller sending mode command transmit vector mode code 10000

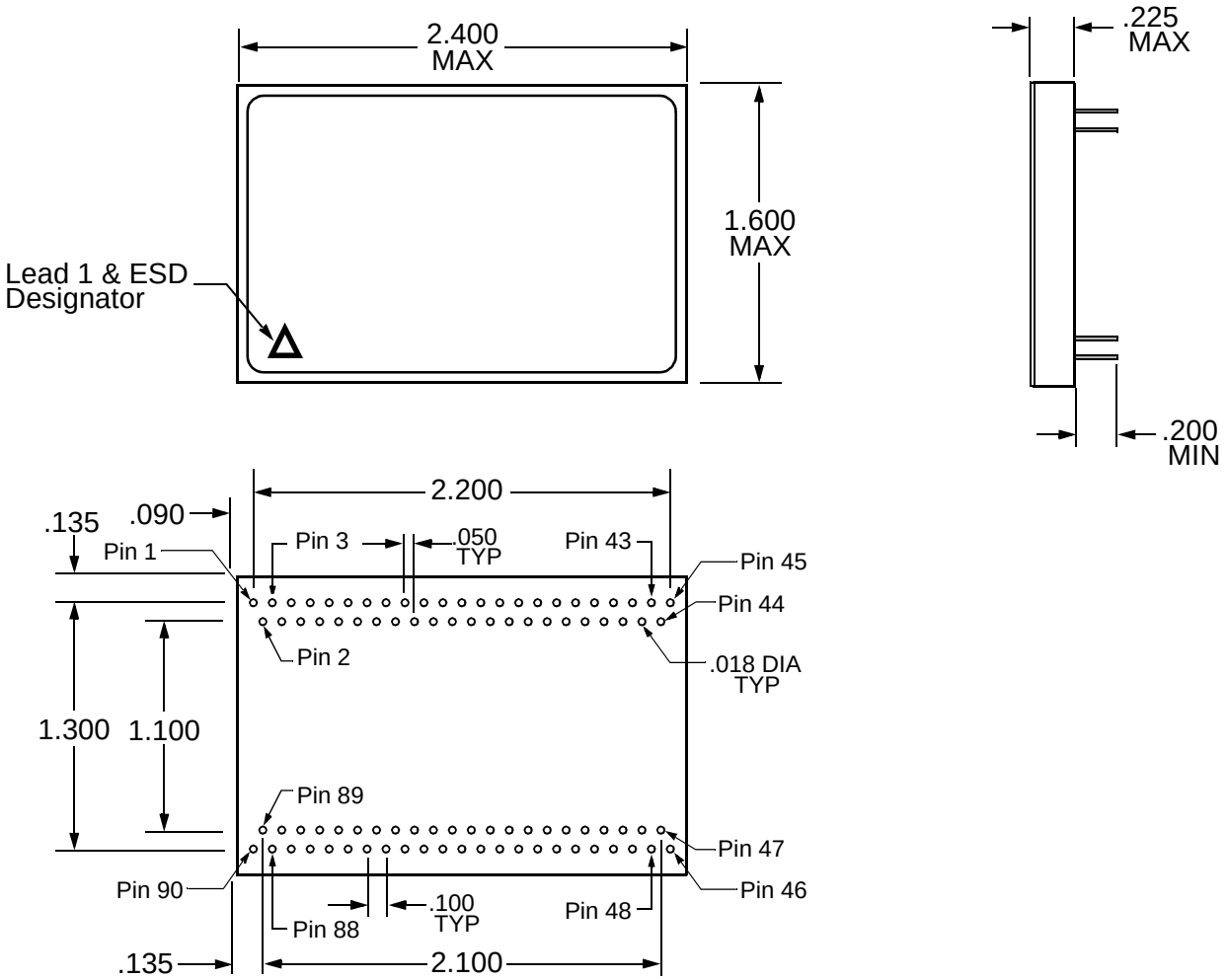
Pin Out Description - CT1990

Pin #	Function	Pin #	Function	Pin #	Function
1	$\overline{\text{BIT DECODE}}$	31	REQBUSB	61	$\overline{\text{ERROR}}$
2	CWC0 (LSB)	32	REQBUSA	62	$\overline{\text{LTFAIL}}$
3	SA4 (MSB)	33	COMMON & CASE	63	$\overline{\text{MANER}}$
4	SA3	34	$\overline{\text{ENABLE}}$	64	$\overline{\text{PARER}}$
5	SA2	35	$\overline{\text{STAT UPDATE}}$	65	$\overline{\text{VALD}}$
6	CWC4 (MSB)	36	MEREQ	66	$\overline{\text{RTADER}}$
7	CWC3	37	IH 08 (LSB)	67	RX DATA 1
8	CWC2	38	IH19	68	RX $\overline{\text{DATA}}$ 1
9	CWC1	39	IH210	69	+5 VIN
10	$\overline{\text{GBR}}$	40	IH311	70	TX INHIBIT 1
11	H/$\overline{\text{L}}$	41	IH412	71	TX INHIBIT 0
12	$\overline{\text{STATEN}}$/STATSTB	42	IH513	72	TX DATA
13	$\overline{\text{EOT}}$	43	IH614	73	TX $\overline{\text{DATA}}$
14	SA1	44	IH715 (MSB)	74	$\overline{\text{SERVREQ}}$
15	SA0 (LSB)	45	NC	75	$\overline{\text{TXTO}}$
16	$\overline{\text{INCMD}}$	46	NC	76	$\overline{\text{DBCACC}}$
17	TX/$\overline{\text{RX}}$	47	RTADPAR	77	$\overline{\text{RESET}}$
18	$\overline{\text{DTRQ}}$	48	RTAD0 (LSB)	78	RT/$\overline{\text{BC}}$
19	$\overline{\text{VECTEN}}$/$\overline{\text{DWEN}}$	49	RTAD1	79	$\overline{\text{DBCREQ}}$
20	$\overline{\text{NBGT}}$	50	RTAD2	80	$\overline{\text{HSFAIL}}$
21	$\overline{\text{SYNC}}$	51	RTAD3	81	$\overline{\text{LSTCMD}}$/$\overline{\text{CWEN}}$
22	INCLK	52	RTAD4 (MSB)	82	$\overline{\text{BITEN}}$/$\overline{\text{RMDSTB}}$
23	IUSTB	53	$\overline{\text{CMSYNC}}$	83	$\overline{\text{BUSY}}$
24	$\overline{\text{NEXT STAT}}$	54	$\overline{\text{DWSYNC}}$	84	WC4 (MSB)
25	$\overline{\text{DTAK}}$	55	BCSTEN 0	85	WC3
26	BCOPA	56	RX DATA 0	86	WC0 (LSB)
27	$\overline{\text{BCOPSTB}}$	57	RX $\overline{\text{DATA}}$ 0	87	$\overline{\text{SSERR}}$
28	BCOPB	58	BCSTEN 1	88	WC2
29	$\overline{\text{PASMON}}$	59	$\overline{\text{RTO}}$	89	WC1
30	$\overline{\text{NDRQ}}$	60	6 MCK	90	NC

Pin Out Description - CT1991

Pin #	Function	Pin #	Function	Pin #	Function
1	$\overline{\text{BIT DECODE}}$	31	REQBUSB	61	$\overline{\text{ERROR}}$
2	CWC0 (LSB)	32	REQBUSA	62	$\overline{\text{LTFAIL}}$
3	SA4 (MSB)	33	COMMON & CASE	63	$\overline{\text{MANER}}$
4	SA3	34	$\overline{\text{ENABLE}}$	64	$\overline{\text{PARER}}$
5	SA2	35	$\overline{\text{STAT UPDATE}}$	65	$\overline{\text{VALD}}$
6	CWC4 (MSB)	36	MEREQ	66	$\overline{\text{RTADER}}$
7	CWC3	37	IH 08 (LSB)	67	RX DATA 1
8	CWC2	38	IH19	68	RX $\overline{\text{DATA}}$ 1
9	CWC1	39	IH210	69	+5 VIN
10	$\overline{\text{GBR}}$	40	IH311	70	TX INHIBIT 1
11	H/$\overline{\text{L}}$	41	IH412	71	TX INHIBIT 0
12	$\overline{\text{STATEN}}$/STATSTB	42	IH513	72	TX DATA
13	$\overline{\text{EOT}}$	43	IH614	73	TX $\overline{\text{DATA}}$
14	SA1	44	IH715 (MSB)	74	$\overline{\text{SERVREQ}}$
15	SA0 (LSB)	45	NC	75	$\overline{\text{TXTO}}$
16	$\overline{\text{INCMD}}$	46	NC	76	$\overline{\text{DBCACC}}$
17	TX/$\overline{\text{RX}}$	47	RTADPAR	77	$\overline{\text{RESET}}$
18	$\overline{\text{DTRQ}}$	48	RTAD0 (LSB)	78	RT/$\overline{\text{BC}}$
19	$\overline{\text{VECTEN}}$/$\overline{\text{DWEN}}$	49	RTAD1	79	$\overline{\text{DBCREQ}}$
20	$\overline{\text{NBGT}}$	50	RTAD2	80	$\overline{\text{HSFAIL}}$
21	$\overline{\text{SYNC}}$	51	RTAD3	81	$\overline{\text{LSTCMD}}$/$\overline{\text{CWEN}}$
22	INCLK	52	RTAD4 (MSB)	82	$\overline{\text{BITEN}}$/$\overline{\text{RMDSTB}}$
23	IUSTB	53	$\overline{\text{LTEN}}$	83	$\overline{\text{BUSY}}$
24	$\overline{\text{NEXT STAT}}$	54	$\overline{\text{LTTRIG}}$	84	WC4 (MSB)
25	$\overline{\text{DTAK}}$	55	BCSTEN 0/1	85	WC3
26	BCOPA	56	RX DATA 0	86	WC0 (LSB)
27	$\overline{\text{BCOPSTB}}$	57	RX $\overline{\text{DATA}}$ 0	87	$\overline{\text{SSERR}}$
28	BCOPB	58	$\overline{\text{DRVINH}}$	88	WC2
29	$\overline{\text{PASMON}}$	59	$\overline{\text{RTO}}$	89	WC1
30	$\overline{\text{NDRQ}}$	60	6 MCK	90	NC

Ceramic CoFired Plug In Package Outline



Ordering Information

Model Number	DESC Part Number	Package
CT1990-1-20	5962-9477501	1.6" x 2.4" Ceramic Plug In
CT1991-1-20	Pending	1.6" x 2.4" Ceramic Plug In

Aeroflex Circuit Technology
35 South Service Road
Plainview New York 11830

Telephone: (516) 694-6700
FAX: (516) 694-6715
Toll Free Inquiries: 1-(800)THE-1553

Specifications subject to change without notice.

О компании

ООО "ТрейдЭлектроникс" - это оперативные поставки широкого спектра электронных компонентов отечественного и импортного производства напрямую от производителей и с крупнейших мировых складов. Реализуемая нашей компанией продукция насчитывает более полумиллиона наименований.

Благодаря этому наша компания предлагает к поставке практически не ограниченный ассортимент компонентов как оптовыми, мелкооптовыми партиями, так и в розницу.

Наличие собственной эффективной системы логистики обеспечивает надежную поставку продукции по конкурентным ценам в точно указанные сроки.

Срок поставки со стоков в **Европе и Америке – от 3 до 14 дней.**

Срок поставки из **Азии – от 10 дней.**

Благодаря развитой сети поставщиков, помогаем в поиске и приобретении экзотичных или снятых с производства компонентов.

Предоставляем спец цены на элементы для создания инженерных сэмплов.

Упорный труд, качественный результат дают нам право быть уверенными в себе и надежными для наших клиентов.

Наша компания это:

- Гарантия качества поставляемой продукции
- Широкий ассортимент
- Минимальные сроки поставок
- Техническая поддержка
- Подбор комплектации
- Индивидуальный подход
- Гибкое ценообразование

Наша организация особенно сильна в поставках модулей, микросхем, пассивных компонентов, ксайленсах (XC), EPF, EPM и силовой электроники.

Большой выбор предлагаемой продукции, различные виды оплаты и доставки, позволят Вам сэкономить время и получить максимум выгоды от сотрудничества с нами!

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гарантия бесперебойности производства и качества выпускаемой продукции

Перечень производителей, продукцию которых мы поставляем на российский рынок

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гарантия бесперебойности производства и качества выпускаемой продукции

С удовольствием будем прорабатывать для Вас поставки всех необходимых компонентов по текущим запросам для скорейшего выявления групп элементов, по которым сотрудничество именно с нашей компанией будет для Вас максимально выгодным!

С уважением,

Менеджер отдела продаж ООО

«Трейд Электроникс»

Шишлаков Евгений

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