IR3623MPbF

HIGH FREQUENCY 2-PHASE, SINGLE OR DUAL OUTPUT SYNCHRONOUS STEP DOWN CONTROLLER WITH OUTPUT TRACKING AND SEQUENCING

Features

- Dual Synchronous Controller with 180º Out of Phase Operation
- Configurable to 2-Independent Outputs or Current Share Single Output
- Output Voltage Tracking
- Power up /down Sequencing
- Current Sharing Using Inductor's DCR
- +/-1% Accurate Reference Voltage
- Programmable Switching Frequency up 1200kHz
- Programmable Over Current Protection
- Hiccup Current Limit Using MOSFET $R_{DS(on)}$ sensing
- Latched Overvoltage Protection
- Dual Programmable Soft-Starts
- Enable
- Pre-Bias Start-up
- Dual Power Good Outputs
- On Board Regulator
- External Frequency Synchronization
- Thermal Protection
- 32-Lead MLPQ Package

Applications

- Embedded Telecom Systems
- Distributed Point of Load Power Architectures
- Computing Peripheral Voltage Regulator
- Graphics Card
- General DC/DC Converters

Description

The IR3623 IC is a high performance Synchronous Buck PWM Controller that can be configured for two independent outputs or as a current sharing single output. Since the IC does not contain integrated MOSFET drivers it is ideal for controlling iPOWIR™ integrated power stage modules such as the iP2005 series of products.

IR3623 enables output tracking and sequencing of multiple rails in either ratiometric or simultaneous fashion. The IR3623 features 180º out of phase operation which reduces the required input/output capacitance. The switching frequency is programmable from 200kHz to 1200kHz per phase by use of an external resistor or the switching frequency can be synchronized to an external clock signal. Other key features offered by the IR3623 include; two independent programmable soft starts, two independent power good outputs, precision enable input and under voltage lockout. The current limit is provided by sensing the low side MOSFET's on-resistance for optimum cost and performance. The output voltages are monitored through dedicated pins to protect against open circuit and to improve response time to an overvoltage event.

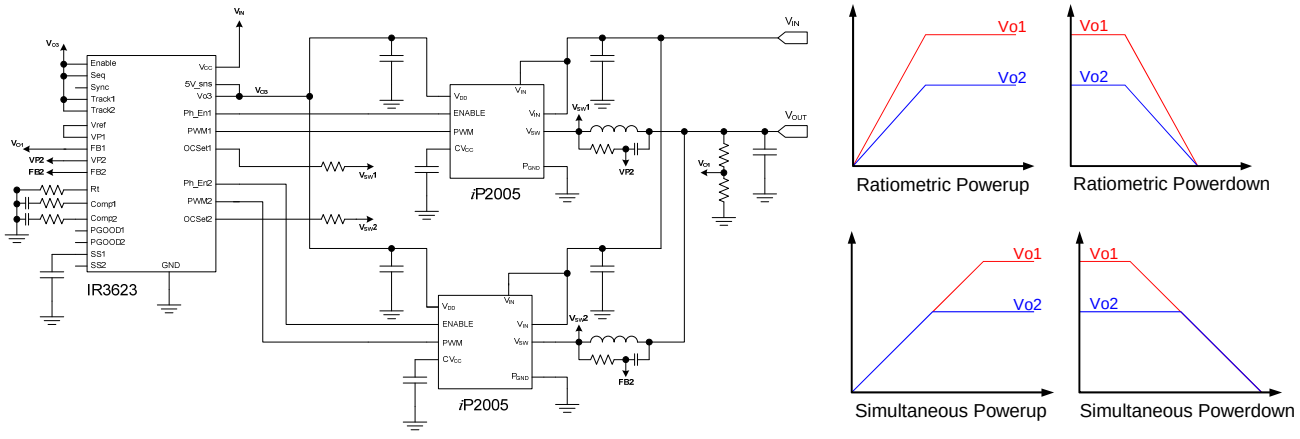


Fig. 1: Power Up /Down Sequencing

ORDERING INFORMATION

PKG DESIG	PACKAGE DESCRIPTION	PIN COUNT	PARTS PER TUBE	PARTS PER REEL	T&R ORIANTAION
M	IR3623MPbF	32	73	-------	Fig A
M	IR3623MTRPbF	32	--------	3000	

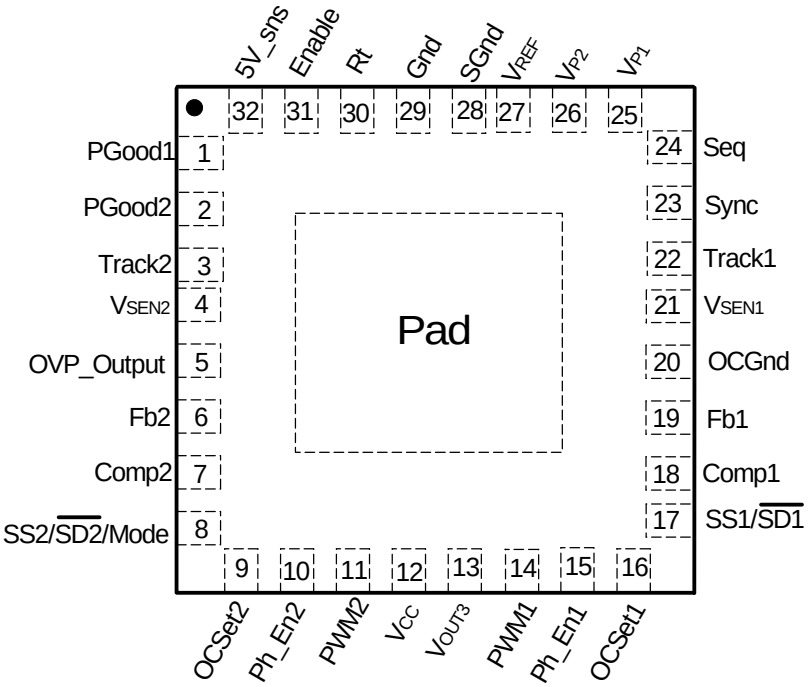
ABSOLUTE MAXIMUM RATINGS

(Voltages referenced to GND)

- Vcc Supply Voltage ..... -0.5V to 16V
- PWM1, PWM2 ..... -0.5V to 16V
- PGood ..... -0.5V to 16V
- Gnd to SGnd ..... +/- 0.3V
- Storage Temperature Range ..... -65°C To 150°C
- Operating Junction Temperature Range ..... -40°C To 125°C
- ESD Classification ..... JEDEC, JESD22-A114

Caution: *Stresses above those listed in "Absolute Maximum Rating" may cause permanent damage to the device. These are stress ratings only and function of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to "Absolute Maximum Rating" conditions for extended periods may affect device reliability.*

Package Information



Θ_{JA} = 36° C/W
Θ_{JC} = 1° C/W

**Exposed pad on underside is connected to a copper pad through vias for 4-layer PCB board design*

Recommended Operating Conditions

Symbol	Definition	Min	Max	Units
Vcc	Supply Voltage	8.5	14.5	V
Fs	Operating frequency	200	1200	kHz
Tj	Junction temperature	-40	125	^{o}C

Electrical Specifications

Unless otherwise specified, these specification apply over Vcc=12V, 0^{o}C<Tj<105^{o}C

Parameter	SYM	Test Condition	Min	TYP	MAX	Units
Output Voltage Accuracy						
FB1, FB2 Voltage	V_{FB}			0.8		V
Accuracy			-1		+1	%
		-40^{o}C<Tj< 125^{o}C, *Note2*	-2.5		+1.35	%
Supply Current						
V_{CC} Supply Current (Static)	I_{CC} (Static)	SS=0V, No Switching	-	10	17	mA
Under Voltage Lockout						
V_{CC}-Threshold	V_{CC}_UVLO(R)	Supply ramping up	7.6	8.00	8.4	V
	V_{CC}_UVLO(F)	Supply ramping down	6.9	7.4	7.9	V
V_{CC}-Hysteresis	Vcc-Hyst	Supply ramping up / down	400	600	800	mV
Enable-Threshold	En_UVLO(R)	Supply ramping up	1.2		1.4	V
	En_UVLO(F)	Supply ramping down	1.0	1.2	1.35	V
Enable-Hysteresis	En_Hyst	Supply ramping up / down		100		mV
5V_sns-Threshold	5V_sns_UVLO(R)	Supply ramping up	4.55		4.85	V
	5V_sns_UVLO(F)	Supply ramping down	4.3	4.6	4.8	V
5V_sns_Hysteresis	5V_sns_Hyst	Supply ramping up / down		100		mV
Ph_En, PWM 1,2						
Drive Current	I(drive)			10		mA
Input Voltage High				V_{out3} -1		V
Input Voltage Low					0.8	V
Internal Regulator						
Output Accuracy	V_{out3}	7.6V<Vcc<14.5V Isource=0 to 200mA	4.9	5.15	5.4	V
Output Curret	Io		200			mA
Oscillator						
Frequency	F_S	Rt=62K	510	617	690	kHz
Frequency Range	Fs(range)	See Figure 16	200		1200	kHz
Ramp Amplitude	Vramp	*Note1*		1.25		V
Min Duty Cycle	Dmin	Fb=1V			0	%
Min Pulse Width	Dmin(ctrl)	F_S=300kHz, *Note1*			150	ns
Max duty Cycle	Dmax	F_S=300kHz, Fb=0.6V	85			%
Sync Frequency Range		20% above free running Freq			2400	kHz
Sync Pulse Duration			200	300		ns
Sync High Level Threshold		*Note1*	2			V
Sync Low Level Threshold		*Note1*			0.8	V

Electrical Specifications

Parameter	SYM	Test Condition	Min	TYP	MAX	Units
Error Amplifier						
Fb Voltage Input Bias Current	IFB	SS=3V		-0.1	-0.5	µA
E/A Source/Sink Current	$I_{(source/Sink)}$		120	200	280	µA
Transconductance	gm1,2		2800		4400	µmho
Input offset Voltage	Voffset	Fb to Vref	-3		+3	mV
VP Voltage Range	VP	*Note1*	0		V_{CC}-2	V
Track Voltage Range	Track	*Note1*	0		V_{CC}-2	V
Soft Start/SD						
Soft Start Current	ISS	Source / Sink	17	22	27	µA
Shutdown Output Threshold	SD				0.25	V
Over Current Protection						
OCSET Current	I_{OCSET}		17	22	27	µA
Hiccup Current	IHiccup	*Note1*		3		uA
Hiccup Duty Cycle	Hiccup(duty)	I_{Hiccup}/I_{OCSET}, *Note1*		15		%
Over Voltage Protection						
OVP Trip Threshold	OVP(trip)		1.1Vref	1.15Vref	1.2Vref	V
OVP Fault Prop Delay	OVP(delay)	Output Forced to 1.125Vref			5	µS
OVP_Output Current			10	20		mA
Thermal Shutdown						
Thermal shutdown		*Note1*	135			°C
Thermal shutdown Hysteresis				20		°C
Seq Input						
Seq Threshold	Seq	On Off	2.0		 0.3	V
Power Good						
Vsen Lower Trip point	Vsen(trip)	Vsen Ramping Down	0.8Vref	0.9Vref	0.95Vref	V
PGood Output Low Voltage	PG(voltage)	I_{PGood}=2mA		0.1	0.5	V

Note1: Guaranteed by design but not test in production

Note2: Cold temperature performance is guaranteed via correlation using statistical quality control. Not tested in production

Pin#	Pin Name	Description
1	PGood1	Power Good pin out put for channel 1, open collector. This pin needs to be externally pulled high
2	PGood2	Power Good pin out put for channel 2, open collector. This pin needs to be externally pulled high
3	Track2	Sets the type of power up / down sequencing (ratiometric or simultaneously). If it is not used connect this pin to Vout3.
4	V_{SEN2}	Sense pin for OVP2 and Power Good 2, Channel 2. If it is not used connect this pin to Gnd.
5	OVP-Output	OVP output, goes high when OVP condition occurs
6	Fb2	Inverting inputs to the error amplifier2. If it is not used connect this pin to Gnd
7	Comp2	Compensation pin for the error amplifier2
8	SS2/SD2/Mode	Soft start for channel 2, can be used as SD pin. Float this pin for current share single output application. If it is not used connect this pin to Gnd.
9	OCSet2	Current limit set point for channel2
10	Ph_En2	Phase Enable pin for channel2
11	PWM2	PWM output for channel2
12	Vcc	Supply Voltage for the internal blocks of the IC
13	V_{out3}	Output of the internal regulator
14	PWM1	PWM output for channel1
15	Ph_En1	Phase Enable pin for channel1
16	OCSet1	Current limit set point for Channel 1
17	SS1/SD1	Soft start for channel 1, can be used as SD pin
18	Comp1	Compensation pin for the error amplifier1
19	Fb1	Inverting input to the error amplifier1
20	OCGnd	Ground connection for OCset circuit
21	V_{SEN1}	Sense pin for OVP1 and Power Good, Channel 1
22	Track1	Sets the type of power up / down sequencing (ratiometric or simultaneously). If it is not used connect this pin to Vout3.
23	Sync	External synchronization pin
24	Seq	Enable pin for tracking and sequencing
25	V_{P1}	Non inverting input of error amplifier1
26	V_{P2}	Non inverting input of error amplifier2. If it is not used connect this pin to Gnd.
27	V_{REF}	Reference Voltage
28	SGnd	Signal Ground
29	Gnd	IC's Ground
30	Rt	Connecting a resistor from this pin to ground sets the Switching frequency
31	Enable	Enable pin, recycling this pin will rest OV, SS and Prebias latch
32	5V_sns	Sensing either external 5V or the Vout3

Block Diagram

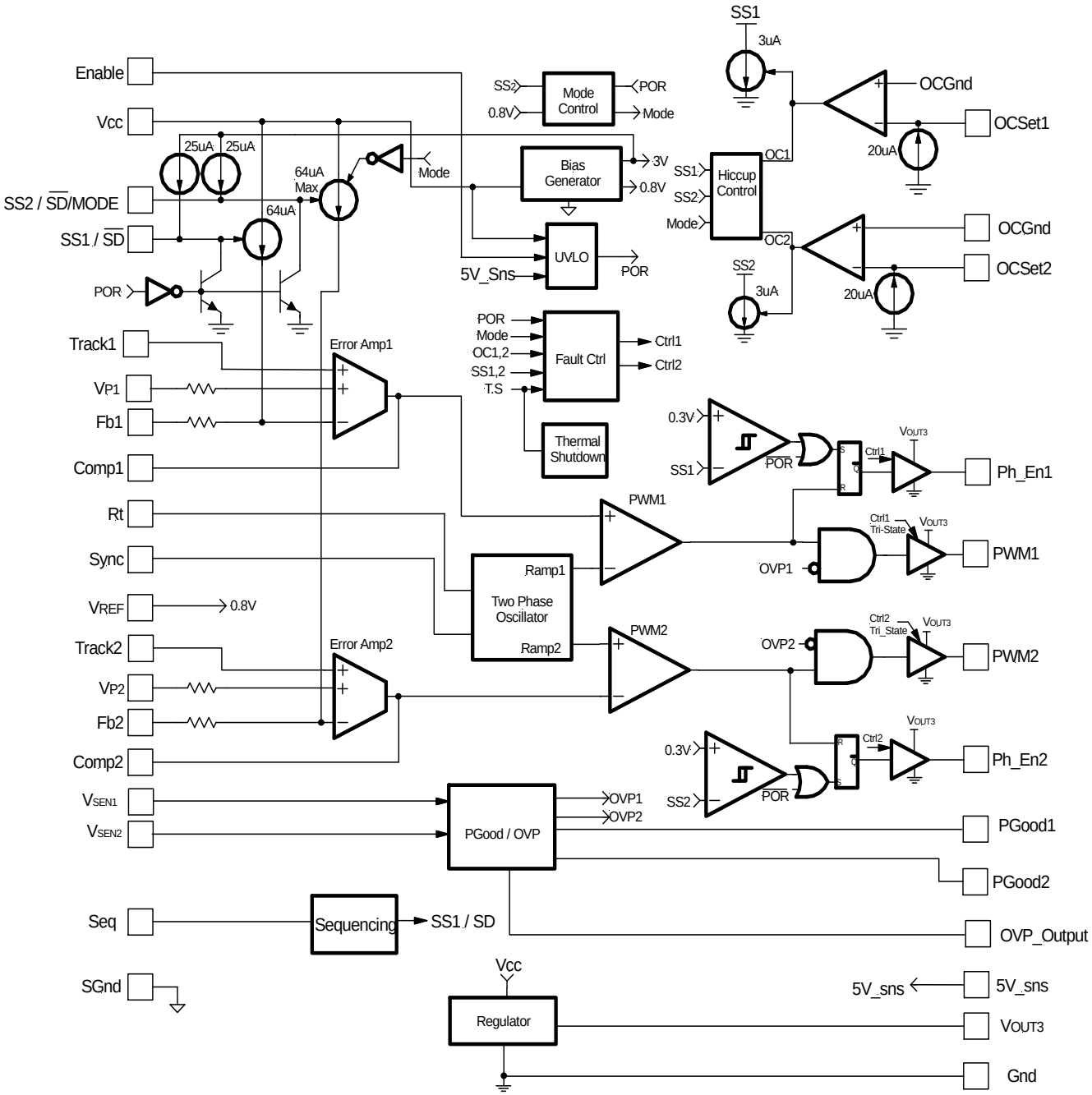
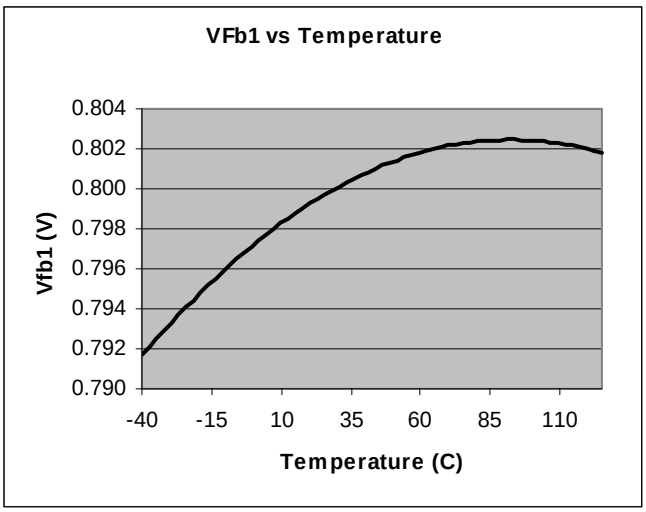
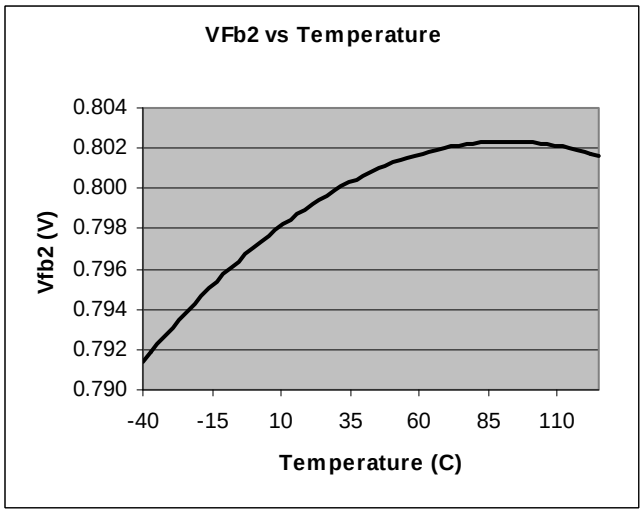
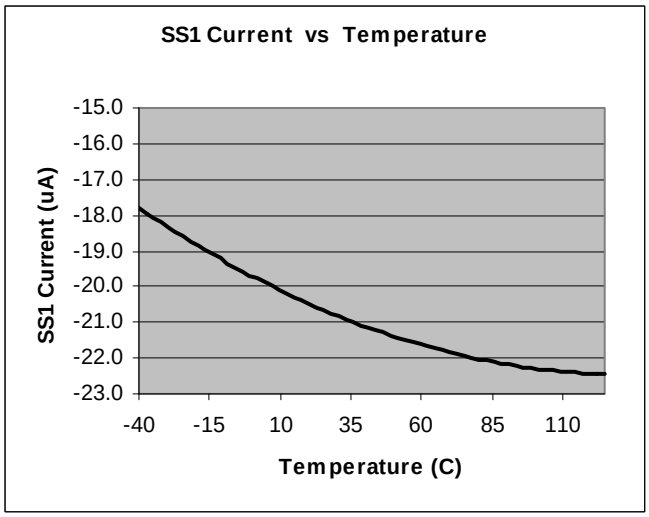


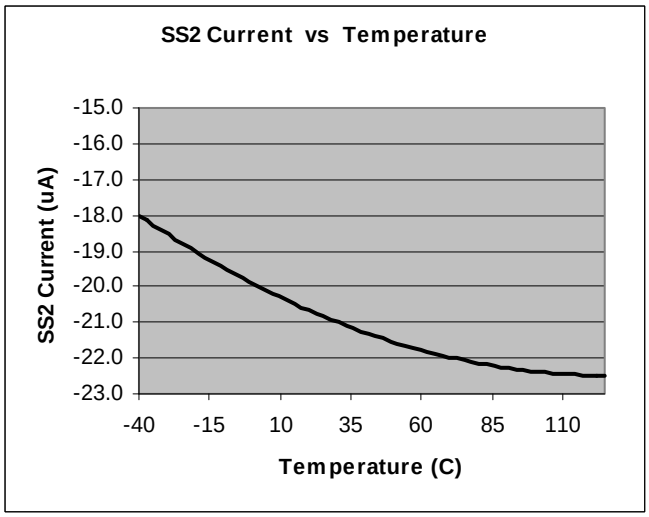
Fig. 2: Simplified block diagram of the IR3623

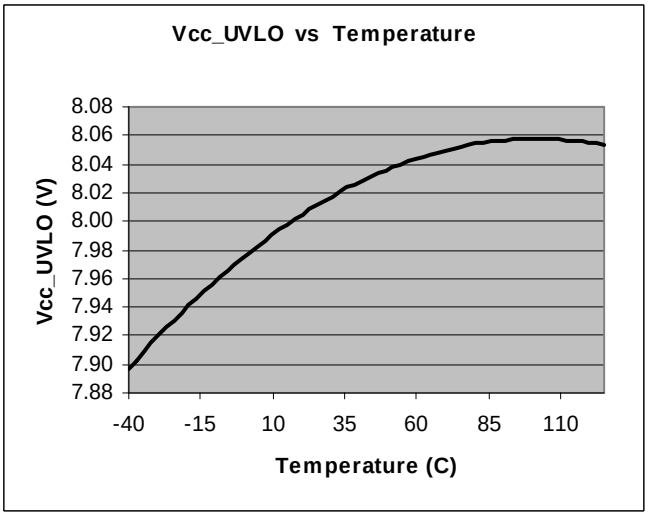
TYPICAL OPERATING CHARACTERISTICS

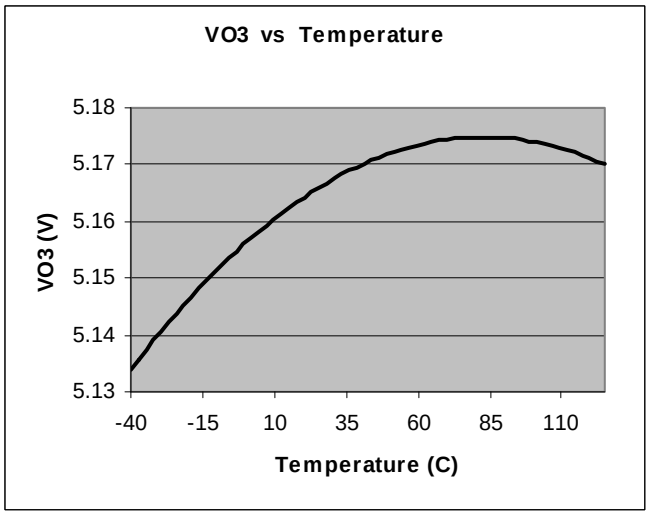












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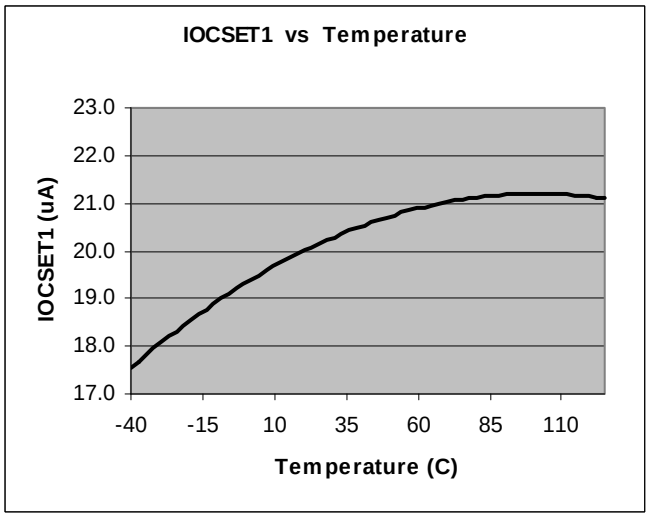
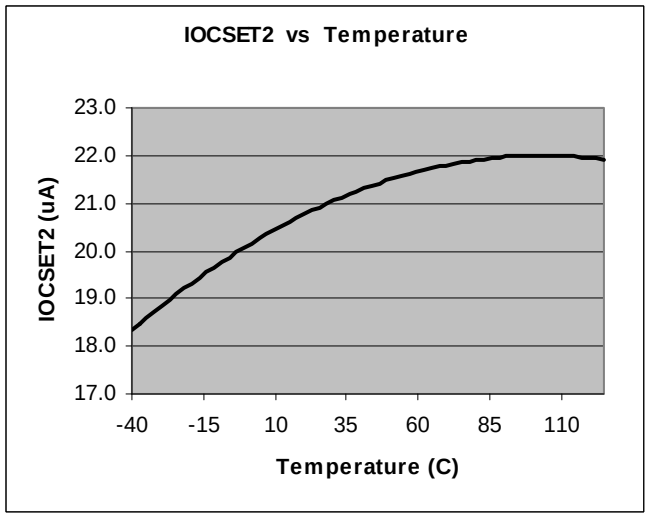
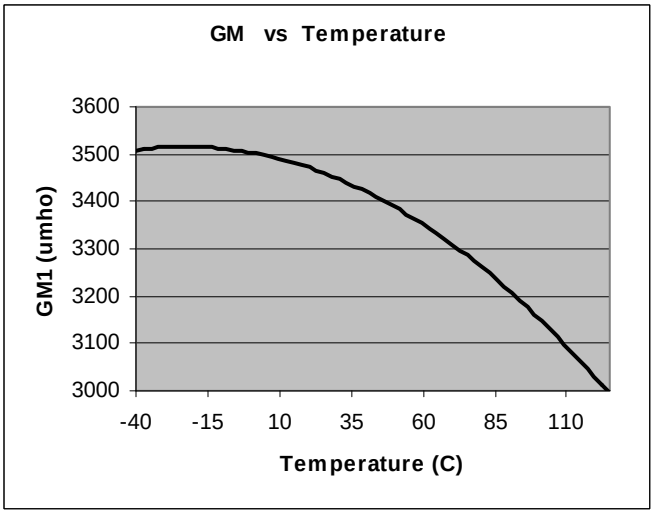
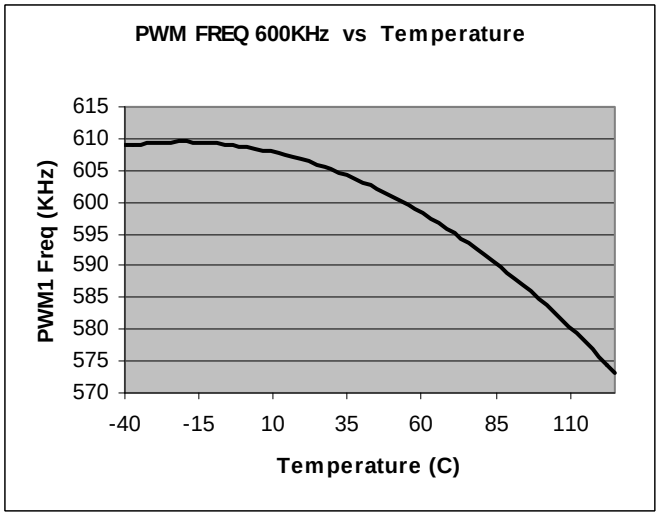
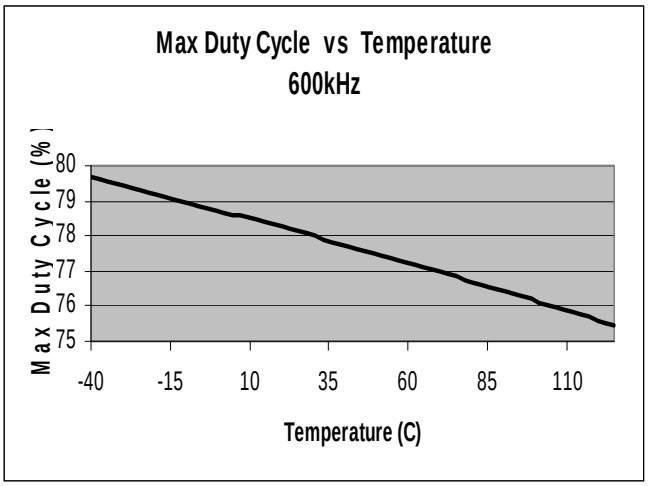
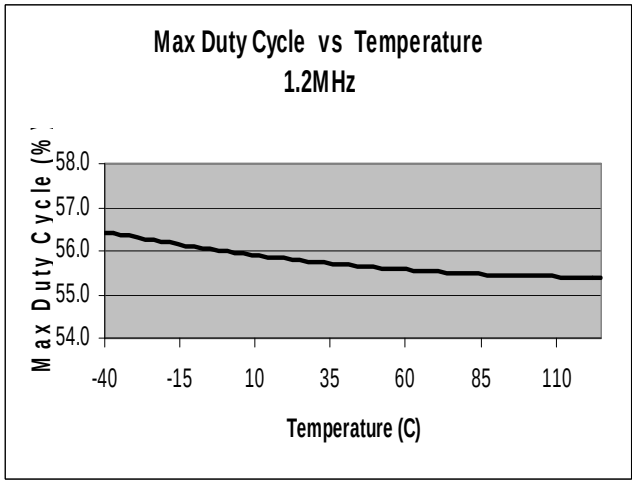












Circuit Description

THEORY OF OPEARTION

Introduction

The IR3623 is a versatile device for high performance buck converters. It consists of two synchronous buck controllers which can be operated either in two independent outputs mode or in current share single output mode for high current applications.

The timing of the IC is provided by an internal oscillator circuit which generates two-180°-out-of-phase clock that can be externally programmed up to 1200kHz per phase.

The IR3623 when combined with IR's iPOWIR power stage modules offers a compact and efficient solution where integration and power density are desired.

Under-Voltage Lockout

The under-voltage lockout circuit monitors three signals (Vcc, Enable and 5V_sns). This ensures the correct operation of the converter during power up and power down sequence. The PWM outputs remain in the off state whenever one of these signals drop below set thresholds. Normal operation resumes once these signals rise above the set values. Figure 3 shows a typical start up sequence.

5V_sns

IR3623 integrates an internal LDO for powering the external module without need for an external supply. For a correct start up sequence the external module needs to be biased first prior to the controller IC. The V_{out3} ramps up as soon as Vcc is applied but the POR (Power On Ready) is not enabled until the V_{out3} reached the 5V threshold set by 5V_sns pin.

Enable

The enable features another level of flexibility for start up. The Enable has precise threshold which is internally monitored by under-voltage lockout circuit.

It's threshold can be externally programmed to desired level by using two external resistors, so the converter doesn't start up until the input voltage is sufficiently high.

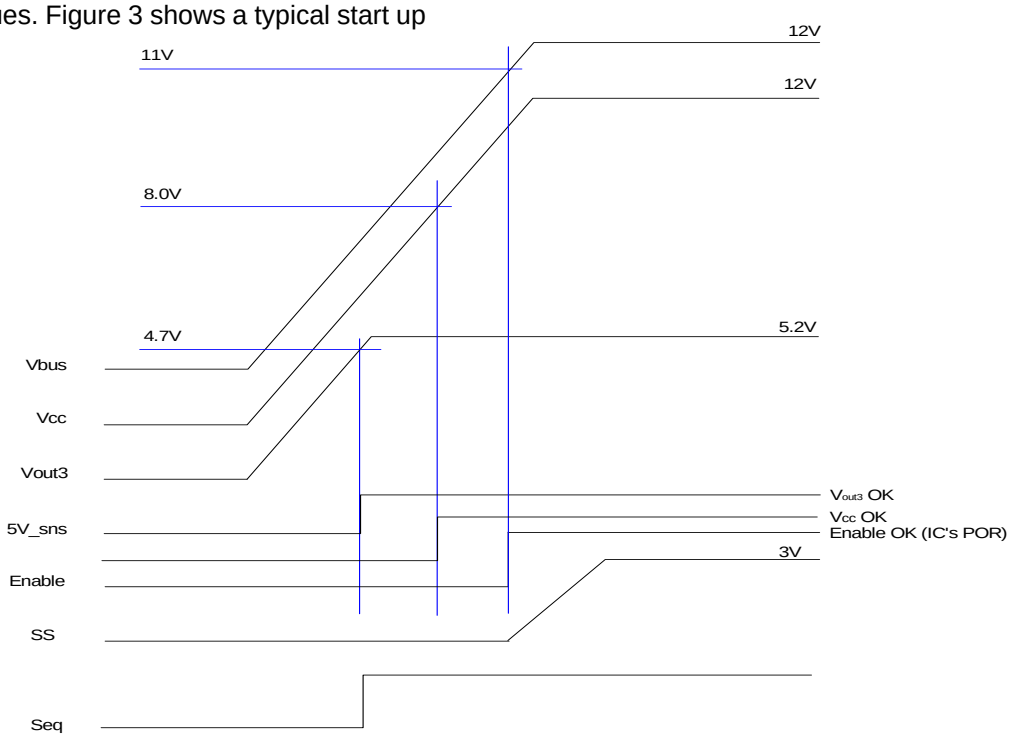


Fig. 3: Normal Start up, Enable threshold is externally set to 11V

Internal Regulator

IR3623 features an on-board regulator capable of sourcing current up to 200mA. This integrated regulator can be used to generate bias voltage an example of how this can be used to power the iP2005A is shown in figure 22.
The output of regulator is protected for short circuit and thermal shutdown.

Out-of-Phase Operation

The IR3623 drives its two output stages 180º out-of-phase. In current share mode single output, the two inductor ripple currents cancel each other and result in a reduction of the output current ripple and yield a smaller output capacitor for the same ripple voltage requirement. Figure 4 shows two channels inductor current and the resulting voltage ripple at output.

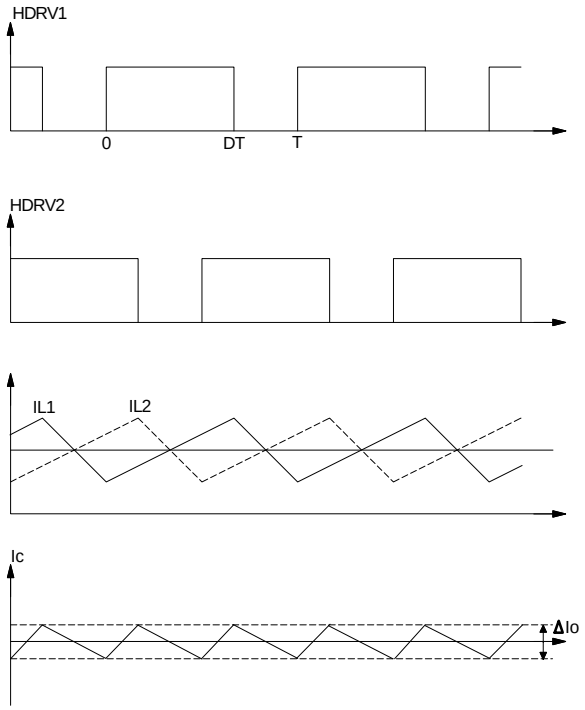


Fig. 4: Current ripple cancellation for output

In addition, the 180º out of phase contributes to input current cancellation. This result in much smaller input capacitor's RMS current and reduces the input capacitor quantity. Figure 5 shows the equivalent RMS current.

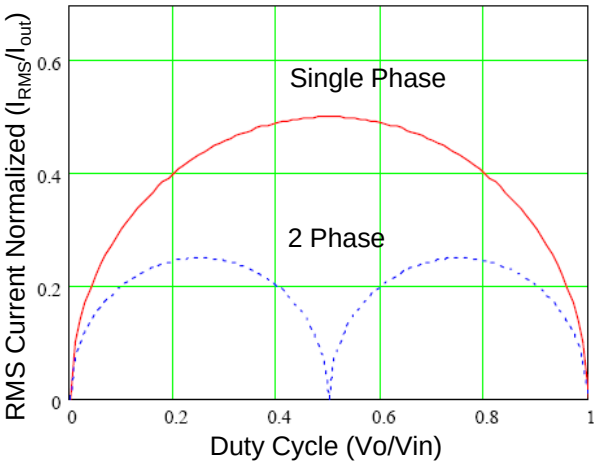


Fig. 5: Input RMS value vs. Duty Cycle

Mode Selection

The IR3623 can operate as a dual output independently regulated buck converter, or as a 2 phase single output buck converter (current share mode). The SS2 pin is used for mode selection. In current share mode this pin should be floating and in dual output mode a soft start capacitor must be connected from this pin to ground to program the start time for the second output.

Independent Mode

In this mode the IR3623 provides control to two independent output power supplies with either common or different input voltages. The output voltage of each individual channel is set and controlled by the output of the error amplifier, which is the amplified error signal from the sensed output voltage and the reference voltage. The error amplifier output voltage is compared to the ramp signal thus generating fixed frequency pulses of variable duty-cycle, (PWM) which are applied to the external MOSEFT drivers. Figure 23 shows a typical schematic for such application.

Current Share Mode

This feature allows to connect both outputs together to increase current handling capability of the converter to support a common load. In current sharing mode, error amplifier 1 becomes the master which regulates the common output voltage and the error amplifier 2 performs the current sharing function, figure 6 shows the configuration of error amplifiers.

In this mode IR3623 make sure the master channel starts first followed by slave channel to prevent any glitch during start up. This is done by clamping the output of slave's error amplifier until the master channel generates the first PWM signal.

At no load condition the slave channel may be kept off depends on the offset of error amplifier.

Lossless Inductor Current Sensing

The IR3623 uses a lossless current sensing for current share purposes. The inductor current is sensed by connecting a series resistor and a capacitor network in parallel with inductor and measuring the voltage across the capacitor, this voltage is proportional to the inductor current. As shown in figure 6 the voltage across the inductor's DCR can be expressed by:

$$V_{RL1}(s) = (V_{in} - V_{out}) * \frac{R_{L1}}{R_{L1} * sL_1} \qquad ----(1)$$

$$V_{RL1}(s) = I_{L1} * R_{L1} \qquad ----(2)$$

The voltage across the C_1 can expressed by:

$$V_{C1}(s) = (V_{in} - V_{out}) * \frac{1/sC_1}{R_1 * 1/sC_1} \qquad ----(3)$$

Combining equations (1),(2) and (3) result to the following expression for V_{C1}:

$$V_{C1}(s) = I_{L1} * \frac{R_{L1} + sL_1}{1 + sR_1 * C_1} \qquad ----(4)$$

Usually the resistor R_1 and C_1 are chosen so that the time constant of R_1 and C_1 equals the time constant of the inductor which is the inductance L_1 over the inductor's DCR (R_{L1}). If the two time constants match, the voltage across C_1 is proportional to the current through L_1, and

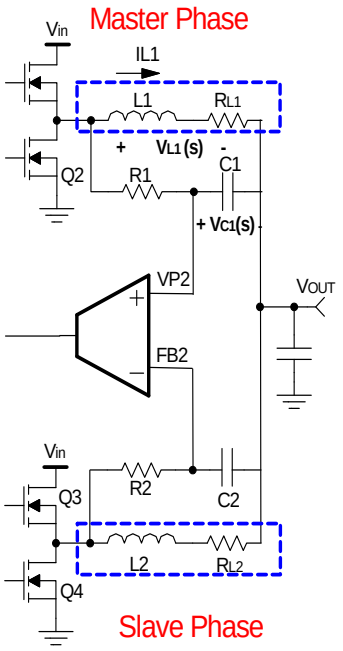


Fig. 6: Loss Less inductor current sensing and current sharing

the sense circuit can be treated as if only a sense resistor with the value R_{L1} was used.

$$If: R_1 * C_1 = \frac{L_1}{R_{L1}}$$

$$V_C(s) \approx I_{L1} * R_{L1}$$

The mismatch of the time constant does not affect the measurements of inductor DC current, but affects the AC component of the inductor current.

Soft-Start

The IR3623 has programmable soft-start to control the output voltage rise and limit the inrush current during start-up. It provides a separate Soft-start function for each outputs. This will enable to sequence the outputs by controlling the rise time of each outputs through selection of different value soft-start capacitors.

To ensure correct start-up, the soft-start sequence initiates when the Vcc, Enable and 5V_sns rise above their threshold and generate the Power On Reset (POR) signal. Soft-start function operates by sourcing an internal current to charge an external capacitor to about 3V. Initially, the soft-start function clamps the error amplifier's output of the PWM converter.

Soft-Start (cont.)

During power up, the converter output starts at zero and thus the voltage at Fb is about 0V. A current (64uA) injects into the Fb pin and generates a voltage about 1.6V (64ux25K) across the negative input of error amplifier, see figure 7.

The magnitude of this current is inversely proportional to the voltage at soft-start pin. The 28uA current source starts to charge up the external capacitor. In the mean time, the soft-start voltage ramps up, the current flowing into Fb pin starts to decrease linearly and so does the voltage at negative input of error amplifier.

When the soft-start capacitor is around 1V, the voltage at the negative input of the error amplifier is approximately 0.8V.

As the soft-start capacitor voltage charges up, the current flowing into the Fb pin keeps decreasing.

The feedback voltage increases linearly as the injecting current goes down. The injecting current drops to zero when soft-start voltage is around 1.8V and the output voltage goes into steady state. Figure 8 shows the theoretical operational waveforms during soft-start.

The output start-up time is the time period when soft-start capacitor voltage increases from 1V to 2V. The start-up time will be dependent on the size of the external soft-start capacitor. The start-up time can be estimated by:

$$28\mu A * \frac{T_{start}}{C_{ss}} = 1.8V - 1V$$

For a given start up time, the soft-start capacitor (nF) can be estimated as:

$$C_{SS} \cong \frac{20(\mu A) * T_{start}(ms)}{0.8(V)} \qquad ----(5)$$

For normal start up the **Seq** pin should be pulled high (usually can be connected to Vout3).

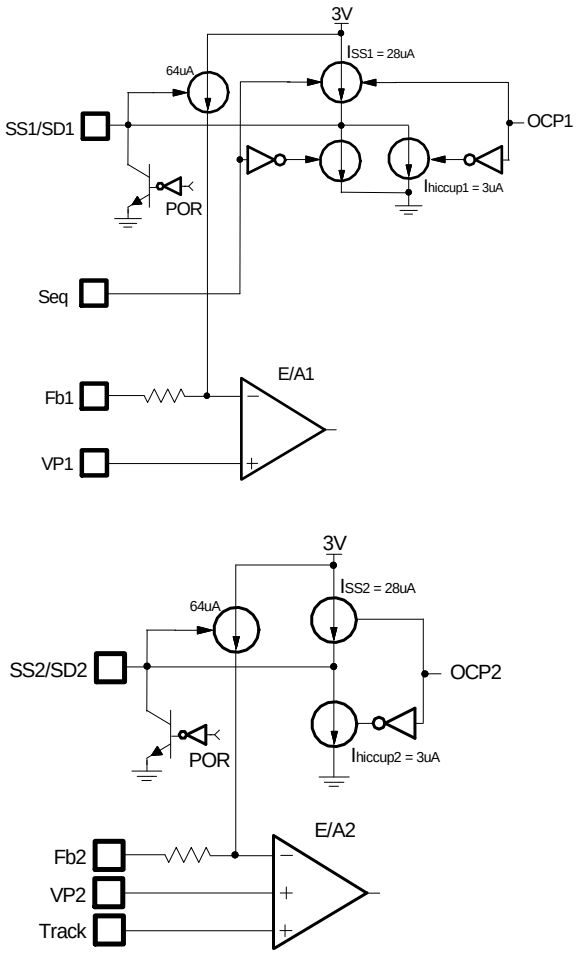


Fig. 7: Soft-Start circuit for IR3623

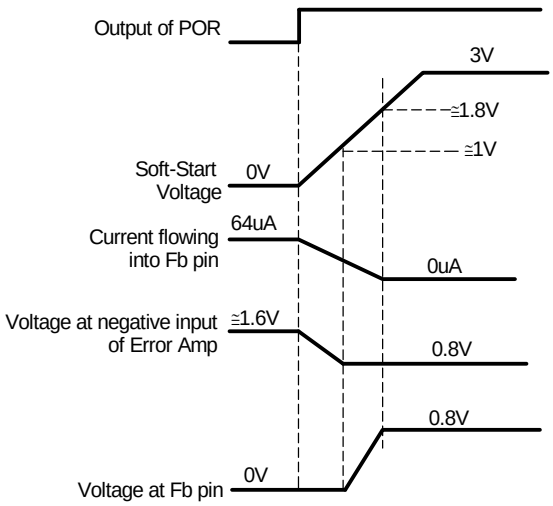


Fig. 8: Theoretical operation waveforms during soft-start

Output Voltage Tracking and Sequencing

The IR3623 can accommodate a full spectrum of user programmable tracking and sequencing options using Track, Seq, Enable and Power Good pins.

Through these pins both simple voltage tracking such as that required by the DDR memory application or more sophisticated sequencing such ratiometric or simultaneously can be implemented.

The Seq pin controls the internal current sources to set the power up or down sequencing, toggle this pin high for power up and toggle this pin low for power down.

The Track pin is used to determine the second channel output for either ratiometric or simultaneously by using two external resistors. Figure 9 shows how these pins are configured for different sequencing mode.

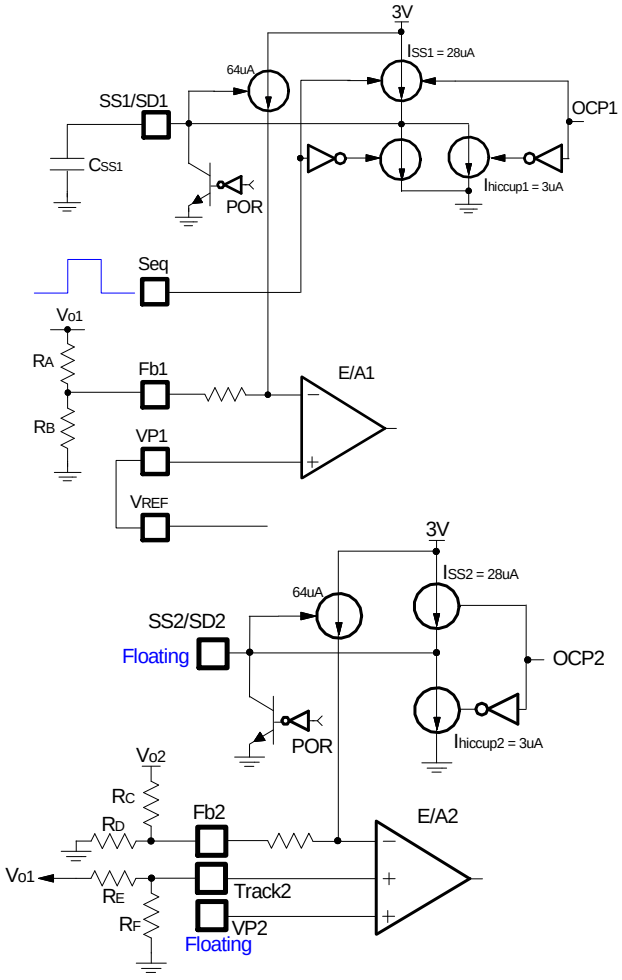


Fig. 9: Sequencing using Track pin

In general the R_A and R_B set the output voltage for the first output and R_C and R_D set the output voltage for the second output.

For simultaneously vs. ratiometric, RE and RF can be selected according to the table below:

Track Pin	simultaneously	ratiometric
R_E	R_C	R_A
R_F	R_D	R_B

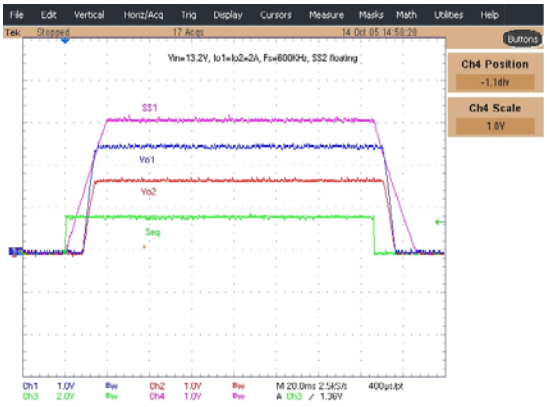


Fig. 10: Ratiometric Power up /down

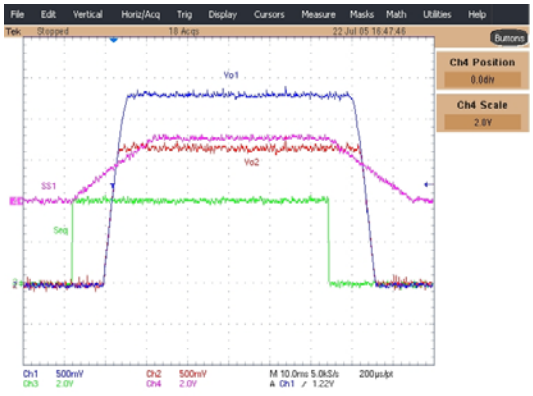


Fig. 11: Simultaneously Power Up / down

The Track pin must be connected to Vout3 if it is not used. For current share mode, high output voltage application (e.g. 5V) this pin needs to be connected to Vcc.

Fault Protection

The IR3623 monitors the output voltage for over voltage protection and power good indication. It senses the $R_{ds(on)}$ of low side MOSFET for over current protection. It also protects the output for prebias conditions. Figure below shows the IC's operating waveforms under different fault conditions.

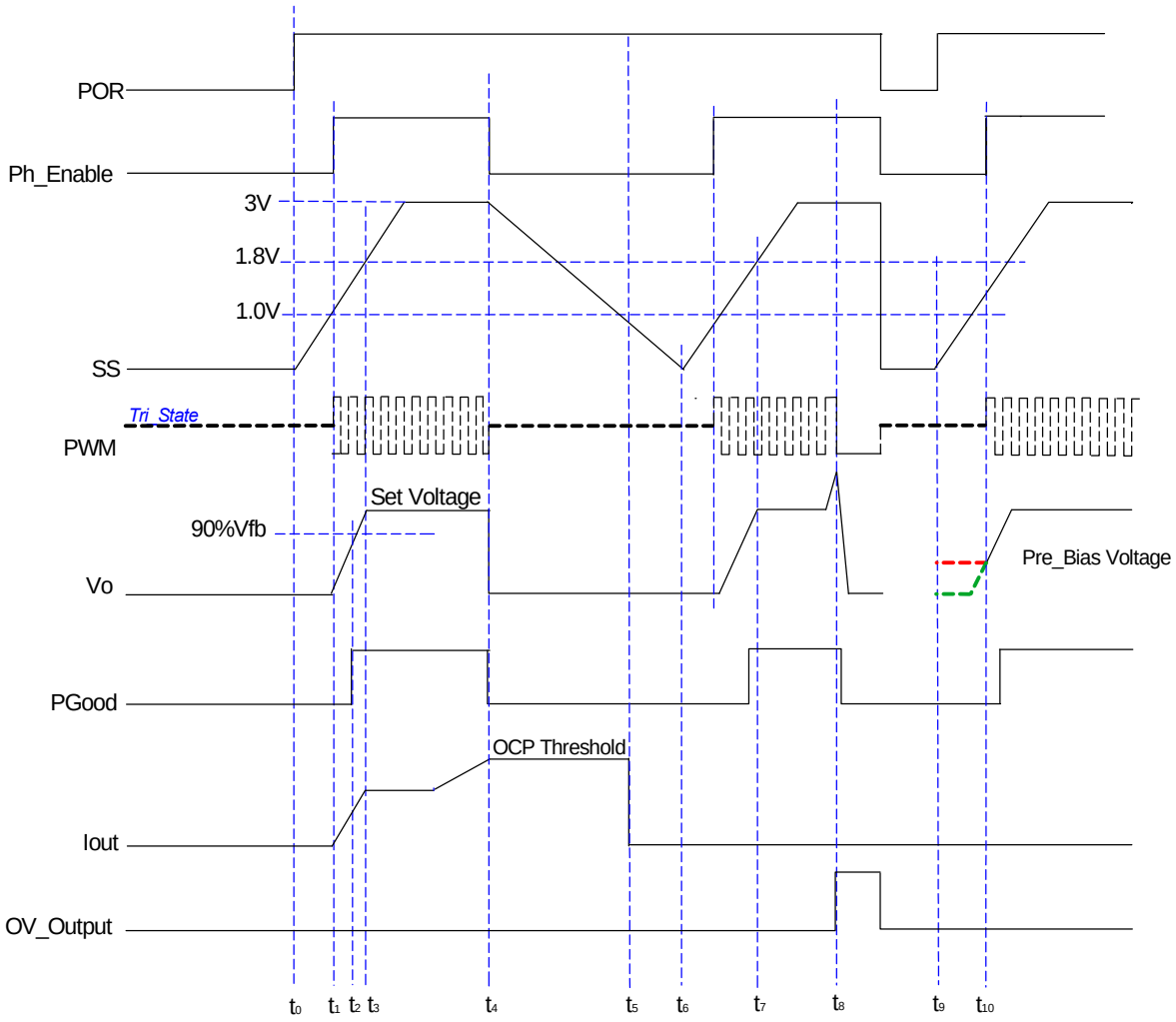


Fig. 12: Fault Conditions

t_0 – t_1: Vcc, 5V_sns and Enable signals passed their respective UVLO threshold. Ph_Enable goes high and PWM switches high from tri-state. Soft start sequence starts.

t_1 – t_2: Power Good signal flags high.

t_1 – t_3: Output voltage ramps up and reaches the set voltage.

t_4 – t_5: OC event, SS ramps down, Ph-Enable pulls low and PWM tri-states. IC in Hiccup mode.

t_5– t_6: OC is removed, recovery sequence, fresh SS.

t_6 –t_7: Ph_Enable goes high and PWM switches high from tri-state. Output voltage reaches the set voltage.

t_8: OVP event. Ph_Enable is kept high and PWM is pulled low. OVP-Output flags high to indicate OV event.

t_9 –t_{10}: Manually recycled the Vcc after latched OVP. PreBias start up. The Ph_Enable goes high after first internal PWM pulse is generated. The PWM output is kept in tri-state until Ph-Enable goes high.

Over-Current Protection

The over current protection is performed by sensing current through the $R_{DS(on)}$ of low side MOSFET. This method enhances the converter's efficiency and reduce cost by eliminating a current sense resistor. As shown in figure 13, an external resistor (R_{SET}) is connected between OCSet pin and the drain of low side MOSFET (Q2) which sets the current limit set point.

The internal current source develops a voltage across R_{SET}. When the low side MOSFET is turned on, the inductor current flows through the Q2 and results a voltage which is given by:

$$V_{OCSet} = (I_{OCSet} * R_{OCSet}) - (R_{DS(on)} * I_L) \quad ----(6)$$

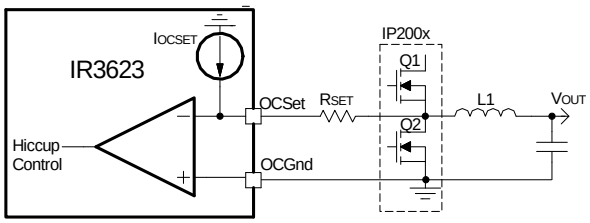


Fig. 13: Connection of over current sensing resistor

The critical inductor current can be calculated by setting:

$$V_{OCSet} = (I_{OCSet} * R_{OCSet}) - (R_{DS(on)} * I_L) = 0$$

$$I_{SET} = I_{L(critical)} = \frac{R_{OCSet} * I_{OCSet}}{R_{DS(on)}} \quad ----(7)$$

An over current is detected if the OCSet pin goes below ground. This trips the OCP comparator and cycles the soft start function in hiccup mode.

The hiccup is performed by charging and discharging the soft-start capacitor in certain slope rate. As shown in figure 14 a 3uA current source is used to discharge the soft-start capacitor.

The OCP comparator resets after every soft start cycles, the converter stays in this mode until the overload or short circuit is removed. The converter will automatically recover.

During this fault condition the Ph_En signal is low and PWM output is on Tri-state, see figure 12.

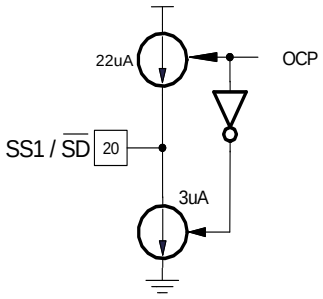


Fig. 14: 3uA current source for discharging soft-start capacitor during hiccup

The OCP circuit starts sampling current 200ns (typical) after PWM signal goes high. The OCSet pin is internally clamped to prevent false trigging, figure 15 shows the OCSet pin during one switching cycle.

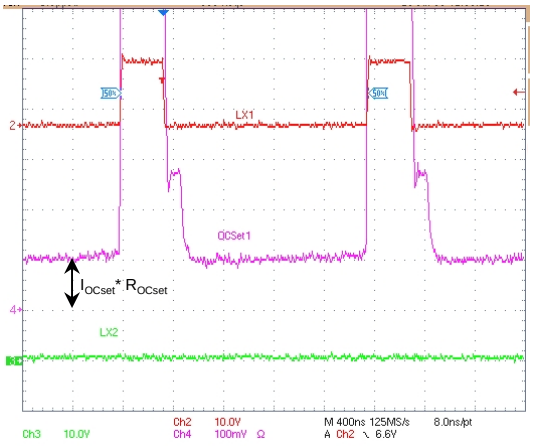


Fig. 15: OCset pin during normal condition
Ch1: Inductor point, Ch2:Ldrv, Ch3:OCSet

The value of R_{SET} should be checked in an actual circuit to ensure that the over current protection circuit activates as expected. The IR3623 current limit is designed primarily as disaster preventing, "no blow up" circuit, and doesn't operate as a precision current regulator.
When the SS2 is floating over current on either phase would result to hiccup of output voltage.

Ph_En and Pre-Bias

For a correct start up the driver section needs to be powered up before the PWM signal is applied. IR3623 features a dedicated pin (Ph_En) which can be used for this purposes. Figure 22 shows how this pin is used to enable power stage modules. During normal start up the PWM is in Tri-state mode until the Ph_En goes high, each channel has it's own Ph_En pins.

During the Pre-Bias start up the Ph_En is kept low and the PWM output is in Tri-state mode. The Ph_En will be enabled as soon as the internal PWM signal is generated.

Over Voltage Protection

Over-voltage is sensed through two dedicated sense pins V_{SEN1}, V_{SEN2}. A separate OVP circuit is provided for each channel.

The OVP threshold is user programmable and can be set by two external resistors. Upon over-voltage condition of either one of the outputs, the OVP forces a latched shutdown on the fault output and pulls low the PWM signal.

IR3623 features an OVP output signal, high status of this pin indicates the OVP event for either of the channels. This pin has 10mA current capability which can be used to drive an external switch.

Reset is performed by recycling the Vcc or Enable.

Power Good

The IR3623 provides two separate open collector power good signals which report the status of the outputs. The outputs are sensed through the two dedicated V_{SEN1} and V_{SEN2} pins.

Once the IR3623 is enabled and the outputs reach the set value (90% of set value) the power good signals go open and stay open as long as the outputs stay within the set values.

These pins need to be externally pulled high.

Shutdown using Soft Start pins

The outputs can be shutdown by pulling the soft-start pin below 0.3V. This can be easily done by using an external small signal transistor. During shutdown both MOSFET drivers will be turned off. Normal operation will resume by cycling soft start pin.

Operating Frequency Selection

The switching frequency is determined by connecting an external resistor (Rt) to ground. Figure 16 provides a graph of oscillator frequency versus Rt. The maximum recommended channel frequency is 1.2MHz.

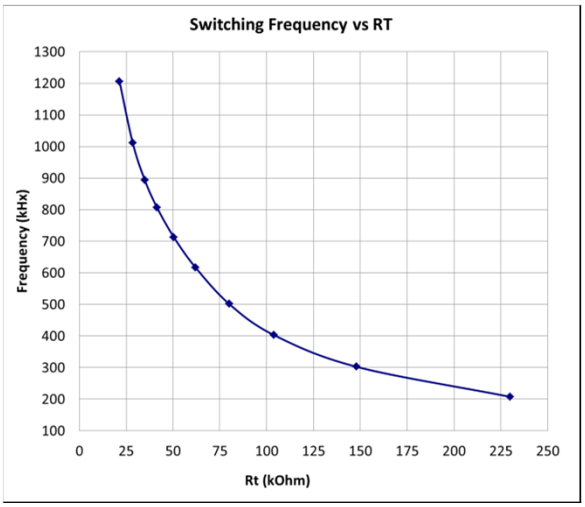


Fig. 16: Switching Frequency vs. External Resistor (R_t)

Frequency Synchronization

The IR3623 is capable of accepting an external digital synchronization signal. Synchronization will be enabled by the rising edge at an external clock. Per –channel switching frequency is set by external resistor (Rt). The free running frequency oscillator frequency is twice the per-channel frequency. During synchronization, Rt is selected such that the free running frequency is 20% below the synchronization frequency. Synchronization capability is provided for both single output current share mode and dual output configuration. When unused, the sync pin will remain floating and is noise immune.

Applying the external signal to the Sync input changes the effective value of the ramp signal (Vramp/Vosc).

$$V_{ocs(eff)} = 1.25 * f_{Free\_Run} / f_{Sync} \qquad ----(8)$$

Equation (8) shows that the effective amplitude of the ramp ($V_{osc(eff)}$) is reduced after the external Sync signal is applied. More difference between the frequency of the Sync (f_{Sync}) and the free-running frequency (f_{Free_Run}) results in more change in the effective amplitude of the ramp signal.

Therefore, since the ramp amplitude takes part in calculating the loop-gain and bandwidth of the regulator, it is recommended not to use a Sync frequency which is much higher than the free-running frequency. In addition, the effective value of the ramp signal, given by equation (8), should be used when the compensator is designed for the regulator.

Thermal Shutdown

Temperature sensing is provided inside IR3623. The trip threshold is typically set to 135°C. When trip threshold is exceeded, thermal shutdown turns off both MOSFETs. Thermal shutdown is not latched and automatic restart is initiated when the sensed temperature drops to normal range. There is a 20°C hysteresis in the shutdown threshold.

Application Information

Design Example:

The following example is a typical application for IR3623. The application circuit is shown in page25.

$V_{in} = 12V$,(13.2V,max)
$V_o = 1.8V$
$I_o = 40A$
$\Delta V_o \leq 30mV$
$F_s = 600kHz$

Output Voltage Programming

Output voltage is programmed by reference voltage and external voltage divider. The Fb pin is the inverting input of the error amplifier, which is internally referenced to 0.8V. The divider is ratioed to provide 0.8V at the Fb pin when the output is at its desired value. The output voltage is defined by using the following equation:

$$V_o = V_{REF} * \left(1 + \frac{R_6}{R_5}\right) \quad ----(9)$$

When an external resistor divider is connected to the output as shown in figure 17.

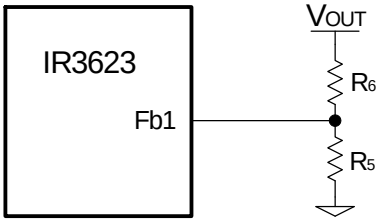


Fig. 17: Typical application of the IR3623 for programming the output voltage

Equation (9) can be rewritten as:

$$R_5 = R_6 * \left(\frac{V_{ref}}{V_o - V_{ref}}\right) \quad ----(10)$$

For the calculated values of R_5 and R_6 see feedback compensation section.

Soft-Start Programming

The soft-start timing can be programmed by selecting the soft-start capacitance value. The start-up time of the converter can be calculated by using:

$$C_{SS} \cong 20\mu A * T_{start} \quad ----(11)$$

Where T_{start} is the desired start-up time (ms)
For a start-up time of 5ms, the soft-start capacitor will be 0.1uF. Choose a ceramic capacitor at 0.1uF.

Input Capacitor Selection

The 180º out of phase will reduce the RMS value of the ripple current seen by input capacitors. This reduces numbers of input capacitors. The input capacitors must be selected that can handle both the maximum ripple RMS at highest ambient temperature as well as the maximum input voltage. The RMS value of current ripple for duty cycle under 50% is expressed by:

$$I_{RMS} = \sqrt{\left(I_1^2 D_1(1-D_1) + I_2^2 D_2(1-D_2) - 2I_1 I_2 D_1 D_2\right)} \quad --(12)$$

Where:
-I_{RMS} is the RMS value of the input capacitor current
-D_1 and D_2 are the duty cycle for each channel
-I_1 and I_2 are the output current for each channel

For Io=40A and D=0.13, the I_{RMS}= 17.8A.

Ceramic capacitors are recommended due to their peak current capabilities, they also feature low ESR and ESL at higher frequency which enhance better efficiency,
Use 15x22uF, 16V ceramic capacitor from TDK (C3225X5R1C226M).

For the single output application when the duty cycle is larger than 50% the following equation can be used to calculate the total RMS value input capacitor current:

$$I_{RMS} = I_o \sqrt{(2D(1-D) + (2-2D))} \qquad D > 0.5$$

Inductor Selection

The inductor is selected based on output power, operating frequency and efficiency requirements. Low inductor value causes large ripple current, resulting in the smaller size, faster response to a load transient but poor efficiency and high output noise. Generally, the selection of inductor value can be reduced to desired maximum ripple current in the inductor (Δi) . The optimum point is usually found between 20% and 50% ripple of the output current.

For the buck converter, the inductor value for desired operating ripple current can be determined using the following relation:

$$V_{in} - V_o = L * \frac{\Delta i}{\Delta t};\ \ \Delta t = D * \frac{1}{F_s}$$

$$L = (V_{in} - V_o) * \frac{V_o}{V_{in} * \Delta i * F_s} \quad \text{----(13)}$$

Where:

V_{in} = *Maximum input voltage*

V_o = *Output Voltage*

Δi = *Inductor ripple current*

F_s = *Switching frequency*

Δt = *Turn on time*

D = *Duty cycle*

For 2-phase single output application the inductor ripple current is chosen between 10-40% of maximum phase current

If $\Delta i \approx 35\%(I_o)$, then the output inductor will be:

L = 0.37uH

The Panasonic ETQP4LR36WFC (L_1=0.34uH, 24A, R_{L1}=1.1mOhm) provides a low profile inductor suitable for this application.
Use the following equation to calculate C_{12} and R_{12} for current sensing:

$$R_{12} * C_{12} = \frac{L_1}{R_{L1}}$$

This results to C_{12}=0.33uF and R_{12}=1.1K

Output Capacitor Selection

The voltage ripple and transient requirements determines the output capacitors types and values. The criteria is normally based on the value of the Effective Series Resistance (ESR). However the actual capacitance value and the Equivalent Series Inductance (ESL) are other contributing components, these components can be described as:

$$\Delta V_o = \Delta V_{o(ESR)} + \Delta V_{o(ESL)} + \Delta V_{o(C)}$$

$$\Delta V_{o(ESR)} = \Delta I_L * ESR \quad \text{----(14)}$$

$$\Delta V_{o(ESL)} = \left(\frac{V_{in}}{L}\right) * ESL$$

$$\Delta V_{o(C)} = \frac{\Delta I_L}{8 * C_o * F_s}$$

ΔV_o = Output voltage ripple

ΔI_L = Inductor ripple current

Since the output capacitor has major role in overall performance of converter and determine the result of transient response, selection of capacitor is critical. The IR3623 can perform well with all types of capacitors.

As a rule the capacitor must have low enough ESR to meet output ripple and load transient requirements, yet have high enough ESR to satisfy stability requirements.

The goal for this design is to meet the voltage ripple requirement in smallest possible capacitor size. Therefore ceramic capacitor is selected due to low ESR and small size.

Panasonic ECJ2FB0J226M (22uF, 6.3V, X5R and EIA 0805 case size) is a good choice.

In the case of tantalum or low ESR electrolytic capacitors, the ESR dominates the output voltage ripple, equation (14) can be used to calculate the required ESR for the specific voltage ripple.

Feedback Compensation

The IR3623 is a voltage mode controller; the control loop is a single voltage feedback path including error amplifier and error comparator. To achieve fast transient response and accurate output regulation, a compensation circuit is necessary. The goal of the compensation network is to provide a closed loop transfer function with the highest 0dB crossing frequency and adequate phase margin (greater than 45º).

The output LC filter introduces a double pole, –40dB/decade gain slope above its corner resonant frequency, and a total phase lag of 180º (see figure 18). The resonant frequency of the LC filter expressed as follows:

$$F_{LC} = \frac{1}{2*\pi\sqrt{L_o * C_o}} \quad \text{----(15)}$$

figure 16 shows gain and phase of the LC filter. Since we already have 180º phase shift just from the output filter, the system risks being unstable.

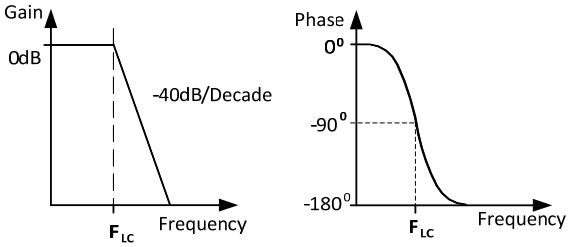


Fig. 18: Gain and Phase of LC filter

The IR3623's error amplifier is a differential-input transconductance amplifier. The output is available for DC gain control or AC phase compensation.

The E/A can be compensated either in type II or typeIII compensation. When it is used in typeII compensation the transconductance properties of the E/A become evident and can be used to cancel one of the output filter poles. This will be accomplished with a series RC circuit from Comp pin to ground as shown in figure 19.

This method requires that the output capacitor should have enough ESR to satisfy stability requirements. In general the output capacitor's ESR generates a zero typically at 5kHz to 50kHz which is essential for an acceptable phase margin. The ESR zero of the output capacitor expressed as follows:

$$F_{ESR} = \frac{1}{2*\pi*ESR*C_o} \quad \text{----(16)}$$

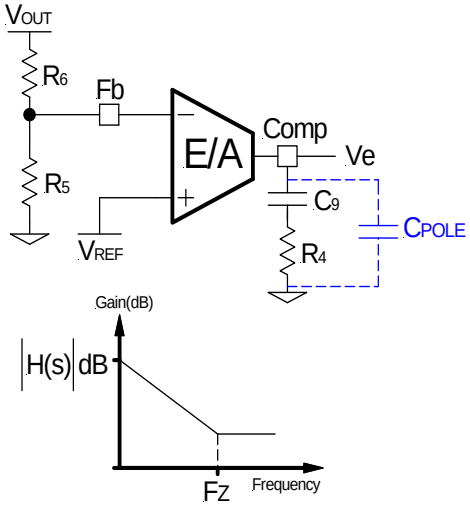


Fig. 19: TypeII compensation network and its asymptotic gain plot

The transfer function (Ve/Vo) is given by:

$$H(s) = \left(g_m * \frac{R_5}{R_5 + R_6}\right) * \frac{1 + sR_4C_9}{sC_9} \quad \text{----(17)}$$

The (s) indicates that the transfer function varies as a function of frequency. This configuration introduces a gain and zero, expressed by:

$$[H(s)] = \left(g_m * \frac{R_5}{R_5 + R_6}\right) * R_4 \quad \text{----(18)}$$

$$F_z = \frac{1}{2\pi * R_4 * C_9} \quad \text{----(19)}$$

The gain is determined by the voltage divider and E/A's transconductance gain.
First select the desired zero-crossover frequency (Fo):

$$F_o > F_{ESR} \text{ and } F_o \le (1/5 \sim 1/10) * F_s$$

Use the following equation to calculate R_4:

$$R_4 = \frac{V_{osc} * F_o * F_{ESR} * (R_5 + R_6)}{V_{in} * F_{LC}^2 * R_5 * g_m} \quad \text{----(20)}$$

Where:
V_{in} = Maximum Input Voltage
V_{osc} = Oscillator Ramp Voltage
F_o = Crossover Frequency
F_{ESR} = Zero Frequency of the Output Capacitor
F_{LC} = Resonant Frequency of the Output Filter
g_m = Error Amplifier Transconductance

To cancel one of the LC filter poles, place the zero before the LC filter resonant frequency pole:

$$F_z = 75\% F_{LC}$$

$$F_z = 0.75 * \frac{1}{2\pi\sqrt{L_o * C_o}} \quad \text{----(21)}$$

Using equations (19) and (21) to calculate C9.

$$C_9 = \frac{1}{2\pi * R_4 * F_z}$$

One more capacitor is sometimes added in parallel with C_9 and R_4. This introduces one more pole which is mainly used to suppress the switching noise.
The additional pole is given by:

$$F_P = \frac{1}{2\pi * R_4 * \frac{C_9 * C_{POLE}}{C_9 + C_{POLE}}}$$

The pole sets to one half of switching frequency which results in the capacitor C_{POLE}:

$$C_{POLE} = \frac{1}{\pi * R_4 * F_s - \frac{1}{C_9}} \cong \frac{1}{\pi * R_4 * F_s}$$

$$For\ F_P << \frac{F_s}{2}$$

For a general solution for unconditionally stability for any type of output capacitors, in a wide range of ESR values we should implement local feedback with a compensation network (typeIII). The typically used compensation network for voltage-mode controller is shown in figure 20.

In such configuration, the transfer function is given by:

$$\frac{V_e}{V_o} = \frac{1 - g_m Z_f}{1 + g_m Z_{IN}}$$

The error amplifier gain is independent of the transconductance under the following condition:

$$g_m * Z_f >> 1 \text{ and } g_m * Z_{in} >> 1 \quad \text{----(22)}$$

By replacing Z_{in} and Z_f according to figure 15, the transformer function can be expressed as:

$$H(s) = \frac{1}{sR_6(C_{11} + C_{12})} * \frac{(1 + sR_7C_{11}) * [1 + sC_{10}(R_6 + R_8)]}{\left[1 + sR_7\left(\frac{C_{11} * C_{12}}{C_{11} + C_{12}}\right)\right] * (1 + sR_8C_{10})}$$

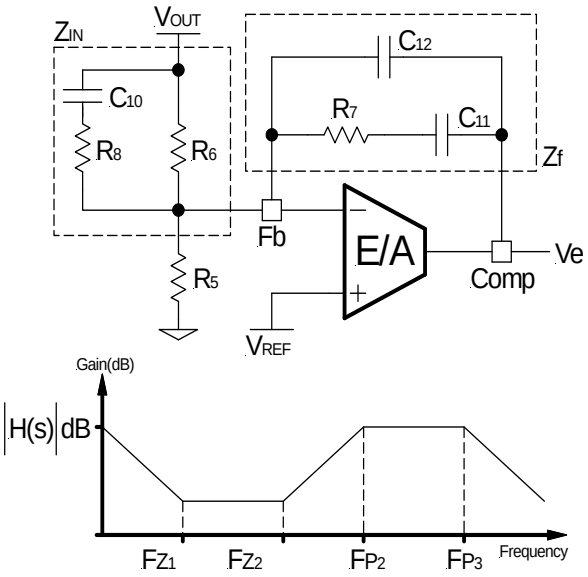


Fig. 20: Compensation network with local feedback and its asymptotic gain plot

As known, transconductance amplifier has high impedance (current source) output, therefore, consider should be taken when loading the E/A output. It may exceed its source/sink output current capability, so that the amplifier will not be able to swing its output voltage over the necessary range.

The compensation network has three poles and two zeros and they are expressed as follows:

$$F_{P1} = 0$$

$$F_{P2} = \frac{1}{2\pi * R_8 * C_{10}}$$

$$F_{P3} = \frac{1}{2\pi * R_7\left(\frac{C_{11} * C_{12}}{C_{11} + C_{12}}\right)} \cong \frac{1}{2\pi * R_7 * C_{12}}$$

$$F_{z1} = \frac{1}{2\pi * R_7 * C_{11}}$$

$$F_{z2} = \frac{1}{2\pi * C_{10} * (R_6 + R_8)} \cong \frac{1}{2\pi * C_{10} * R_6}$$

Cross over frequency is expressed as:

$$F_o = R_7 * C_{10} * \frac{V_{in}}{V_{osc}} * \frac{1}{2\pi * L_o * C_o}$$

Based on the frequency of the zero generated by output capacitor and its ESR versus crossover frequency, the compensation type can be different. The table below shows the compensation types and location of crossover frequency.

Compensator type	F_{ESR} vs. F_o	Output capacitor
TypII(PI)	$F_{LC}<F_{ESR}<F_o<F_{s/2}$	Electrolytic , Tantalum
TypeIII(PID) **Method A**	$F_{LC}<F_o<F_{ESR}<F_{s/2}$	Tantalum, ceramic
TypeIII(PID) **Method B**	$F_{LC}<F_o<F_{s/2}<F_{ESR}$	Ceramic

Table1- The compensation type and location of F_{ESR} versus F_o

The details of these compensation types are discussed in application note AN-1043 which can be downloaded from IR Web-Site.

For this design we have:

V_{in}=13.2V
V_o=1.8V
V_{osc}=1.25V
V_{ref}=0.8V
g_m=2800umoh
L_o=0.34uH, DCR=1.1mOhm
C_o=15x22uF, ESR= 0.33mOhm
F_s=600kHz

These result to:

F_{LC}=15kHz
F_{ESR}=1.46MHz
$F_{s/2}$=300kHz

Select crossover frequency:

$$F_o < F_{ESR} \text{ and } F_o \le (1/5 \sim 1/10) * F_s$$

F_o=100kHz

Since: $F_{LC}<F_o<F_{s/2}<F_{ESR}$, typeIII method B is selected to place the pole and zeros.

The following design rules will give a crossover frequency approximately one-sixth of the switching frequency. The higher the band width, the potentially faster the load transient response. The DC gain will be large enough to provide high DC-regulation accuracy (typically -5dB to -12dB). The phase margin should be greater than 45º for overall stability.
Desired Phase Margin: $\Theta_{max} = \frac{\pi}{3}$

$$F_{Z2} = F_o * \sqrt{\frac{1-Sin\Theta}{1+Sin\Theta}}$$
$$F_{Z2} = 26.79kHz$$

$$F_{P2} = F_o * \sqrt{\frac{1+Sin\Theta}{1-Sin\Theta}}$$
$$F_{P2} = 373.21kHz$$

$$Select:\ F_{Z1} = 0.5 * F_{Z2} \quad and \quad F_{P3} = 0.5 * F_s$$

$$R_7 \ge \frac{2}{g_m};\ R_7 \ge 0.72K\Omega;\quad Select: R_7 = 10K\Omega$$

$$Calculate\ C_{11}, C_{12}\ and\ C_{10}:$$

$$C_{11} = \frac{1}{2\pi * F_{Z1} * R_7};\ C_{11} = 1.19nF,\ Select:\ C_{11} = 1.2nF$$

$$C_{12} = \frac{1}{2\pi * F_{P3} * R_7};\ C_{12} = 53pF,\quad Select: C_{12} = 47pF$$

$$C_{10} = \frac{2\pi * F_o * L_o * C_o * V_{osc}}{R_7 * V_{in}};\ C_{10} = 0.67nF,$$

$$Select: C_{10} = 0.68nF$$

$$Calculate\ R_8, R_6\ and\ R_5:$$

$$R_8 = \frac{1}{2\pi * C_{10} * F_{P2}};\ R_8 = 0.63K\Omega,\quad Select: R_8 = 0.68K\Omega$$

$$R_6 = \frac{1}{2\pi * C_{10} * F_{Z2}} - R_8;\ R_6 = 8.05K\Omega,\quad Select: R_6 = 8.06K\Omega$$

$$R_5 = \frac{V_{ref}}{V_o - V_{ref}} * R_6;\ R_5 = 6.45K\Omega,\quad Select: R_5 = 6.49K\Omega$$

Compensation for Current Loop (slave channel)

The slave error amplifier is differential transconductance amplifier, in 2-phase configuration the main goal for the slave channel feedback loop is to control the inductor current to match the master channel inductor current as well provides highest bandwidth and adequate phase margin for overall stability. The following analysis is valid for both using external current sense resistors and using DCR of inductor.
The transfer function of power stage is expressed by:

$$G(s) = \frac{I_{L2}(s)}{V_e} = \frac{V_{in}}{sL_2 * V_{osc}} \quad \text{----(23)}$$

Where:
V_{in}=Input voltage
L_2=Output inductor
V_{osc}=Oscillator Peak Voltage

As shown the G(s) is a function of inductor current. The transfer function for compensation network is given by equation (24), when using a series RC circuit as shown in figure21.

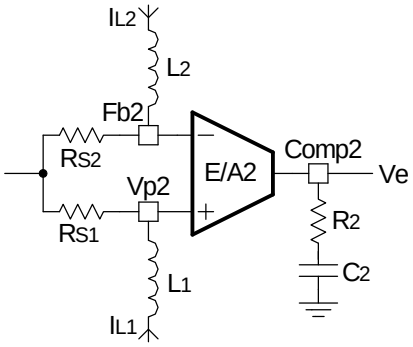


Fig. 21: The Compensation network for current loop

$$D(s) = \frac{V_e(s)}{R_{s2}} = \left(g_m * \frac{R_{s1}}{R_{s2}}\right) * \left(\frac{1 + sC_2R_2}{sC_2}\right) \quad \text{----(24)}$$

The loop gain function is:

$$H(s) = [G(s) * D(s) * R_{s2}]$$

$$H(s) = R_{s2} * \left(g_m * \frac{R_{s1}}{R_{s2}}\right) * \left(\frac{1 + sR_2C_2}{sC_2}\right) * \left(\frac{V_{in}}{sL_2 * V_{osc}}\right)$$

Select a zero frequency for current loop (F_{o2}) 1.25 times larger than zero cross frequency for voltage loop (F_{o1}).

$$F_{O2} \cong 1.25 * F_{O1}$$

$$H(F_{O2}) = g_m * R_{s1} * R_2 * \frac{V_{in}}{2\pi * F_{O2} * L_2 * V_{osc}} = 1 \quad \text{----(25)}$$

From (25), R2 can be expressed as:

$$R_2 = \frac{1}{g_m * R_{s1}} * \frac{2\pi * F_{O2} * L_2 * V_{osc}}{V_{in}} \quad \text{----(26)}$$

V_{in}=13.2V
V_{osc}=1.25V
g_m=2800umoh
L_2=0.34uH
R_{s1}=DCR=1.1mOhm
F_{o2}=125kHz

This results to : R_2=8.2K

The power stage of current loop has a dominant pole (Fp) at frequency expressed by:

$$F_P = \frac{R_{eq}}{2\pi * L_2}$$

Where R_{eq} is the total resistance of the power stage which includes the $R_{ds(on)}$ of MOSFET switches, the DCR of inductor and shunt resistance (if it used).

$$R_{eq} = R_{ds(on)} + R_L + R_s$$

R_{eq}=9.4mOhm

Set the zero of compensator at 10 times the dominant pole frequency F_P, the compensator capacitor, C2 can be expressed as:

$$F_z = 10 * F_P$$

$$C_2 = \frac{1}{2\pi * R_2 * F_z}$$

C_2=0.47nF

All design should be tested for stability to verify the calculated values.

Programming the Current-Limit

The Current-Limit threshold can be set by connecting a resistor (R_{SET}) from drain of low side MOSFET to the OCSet pin. The resistor can be calculated by using equation (7).

The $R_{DS(on)}$ has a positive temperature coefficient and it should be considered for the worse case operation. This resistor must be placed close to the IC, place a small ceramic capacitor from this pin to ground for noise rejection purposes.

$$I_{SET} = I_{L(critical)} = \frac{R_{OCSet} * I_{OCSet}}{R_{DS(on)}} \quad ----(7)$$

$$R_{DS(on)} = 2.3m\Omega * 1.5 = 3.45m\Omega$$

$$I_{SET} \cong I_{o(LIM)} = 20A * 1.5 = 30A$$

(50% over nominal output current)

$$R_{OCSet} = R_3 = R_4 = 5.11K\Omega$$

Layout Consideration

The layout is very important when designing high frequency switching converters. Layout will affect noise pickup and can cause a good design to perform with less than expected results.

Start to place the power components, make all the connection in the top layer with wide, copper filled areas. The inductor, output capacitor should be close to each other as possible. This helps to reduce the EMI radiated by the power traces due to the high switching currents through them. Place input capacitors as close as possible to the power module's input pin. Add capacitors as necessary to reduce the ESR to desired levels. The feedback part of the system should be kept away from the inductor and other noise sources, and be placed close to the IC. In multilayer PCB use one layer as power ground plane and have a control circuit ground (analog ground), to which all signals are referenced. The goal is to localize the high current path to a separate loop that does not interfere with the more sensitive analog control function. These two grounds must be connected together on the PC board layout at a single point. The exposed pad of IC should be connected to analog ground. Layout guidelines for IP2005A can be found in the product data sheet.

Typical Application

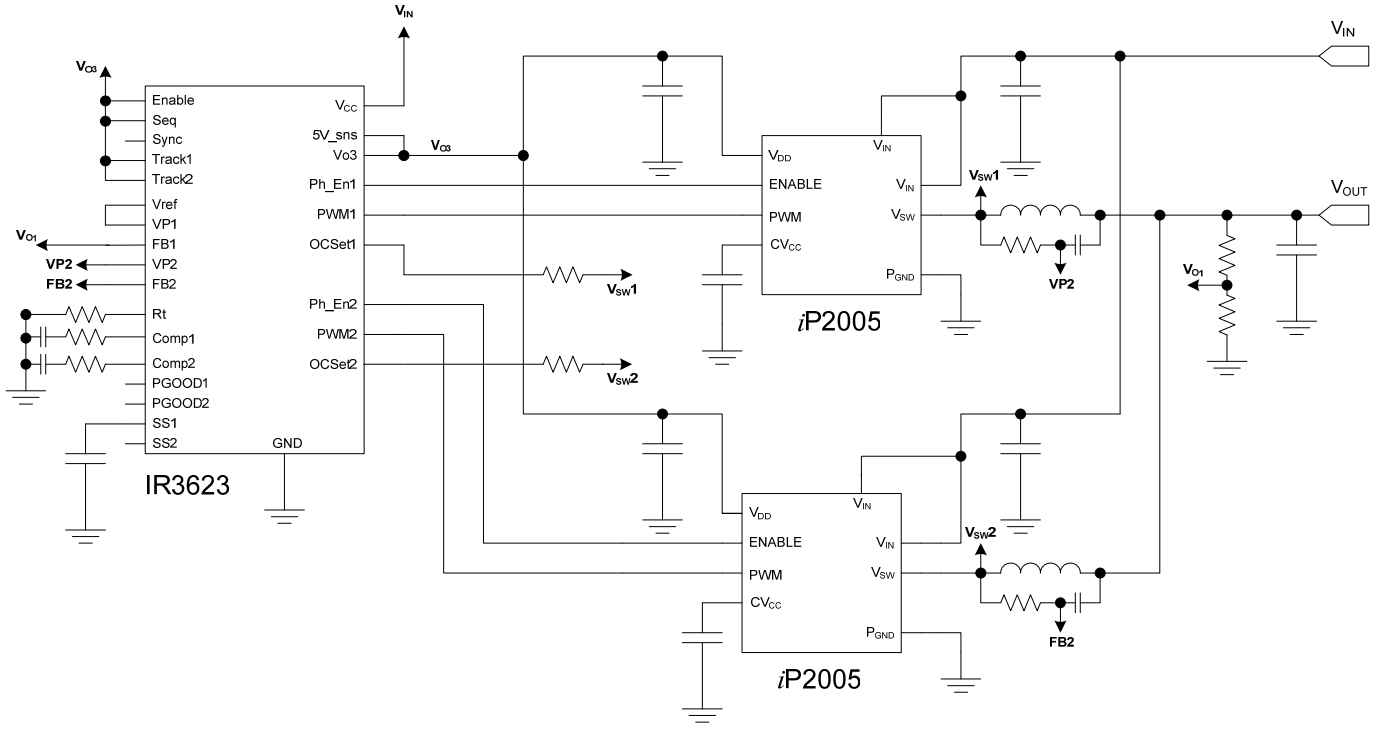


Fig. 22: Application circuit for Single Output

Typical Application

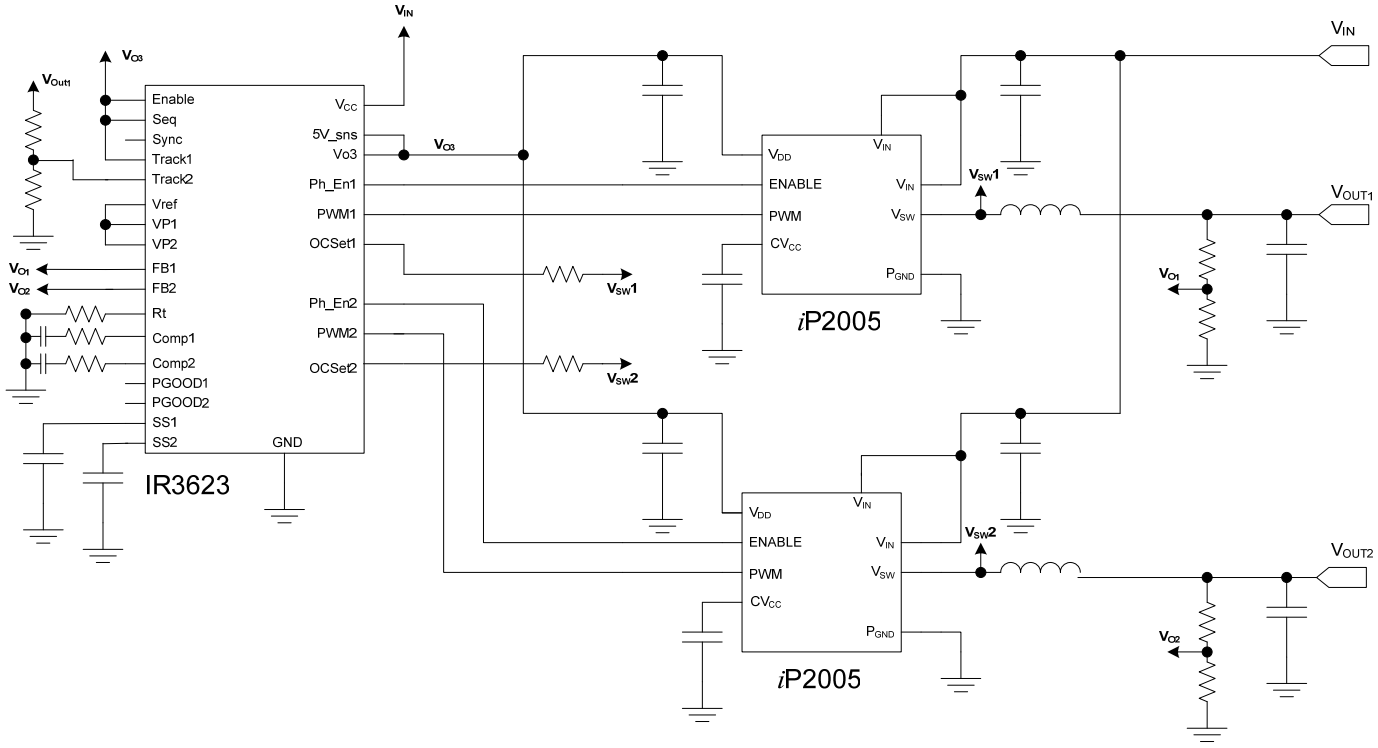
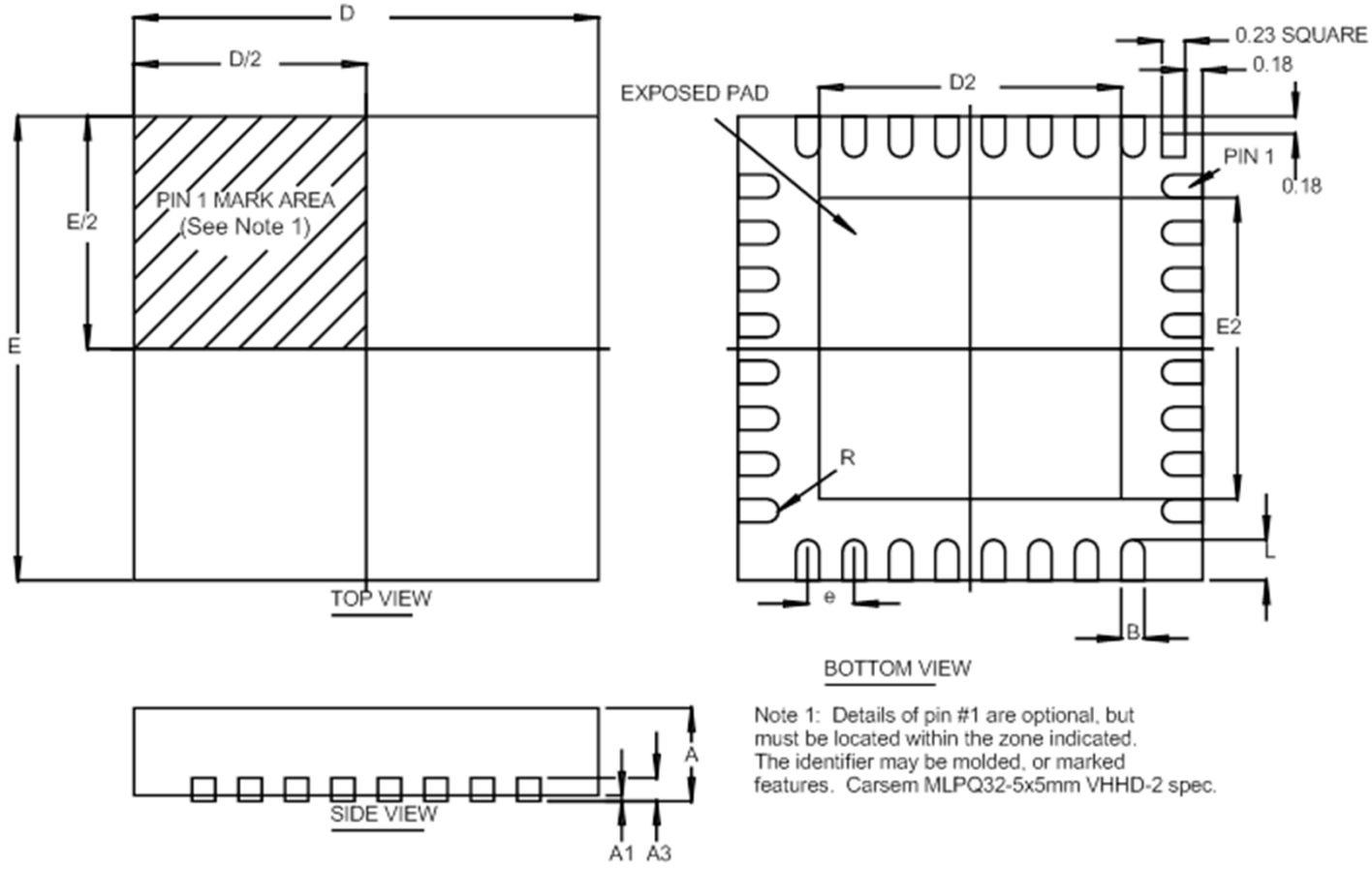


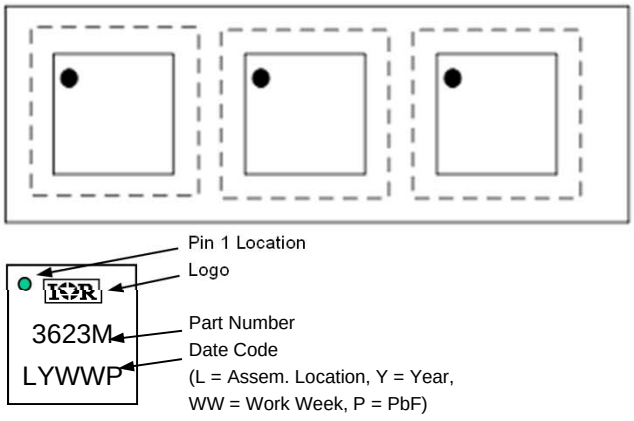
Fig. 23: Application circuit for Dual Output

(IR3623M) MLPQ Package; 5x5-32 Lead



Note 1: Details of pin #1 are optional, but must be located within the zone indicated. The identifier may be molded, or marked features. Carsem MLPQ32-5x5mm VHHD-2 spec.

SYMBOL	32 PIN 5X5 MM		
DESIGN	MIN	NOM	MAX
A	0.80	0.90	1.00
A1	0.00	0.02	0.05
A3		0.20 REF	
B	0.18	0.23	0.30
D		5.00 BSC	
D2	3.00	3.15	3.25
E		5.00 BSC	
E2	3.00	3.15	3.25
e		0.50 BSC	
L	0.30	0.40	0.50
R	0.09	---	---



Part Marking

International
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