

## Features

- Designed to Store Configurator Programs for Field Programmable System Level Integrated Circuits (FPSLICs)
- In-System Programmable (ISP) via 2-wire Bus
- Spare Memory Available for System Parameters Storage
- Low-power CMOS EEPROM Process
- Available in 6 mm x 6 mm x 1 mm 8-lead LAP Package (Pin Compatible Across Product Family)
- Emulation of Atmel's AT24CXXX Serial EEPROMs
- Available in 3.3V  $\pm$  10% LV
- Low-power Standby Mode
- High-reliability
  - Endurance: 100,000 Write Cycles
  - Data Retention: 90 Years for Industrial Parts (at 85°C) and 190 Years for Commercial Parts (at 70°C)

## Description

The FPSLIC Support Devices provide an easy-to-use, cost-effective configuration memory for programming Field Programmable System Level Integrated Circuits by using a simple serial-access procedure to configure one or more FPSLIC devices. See Table 1 for a list of supported FPSLIC devices.

The FPSLIC Support Device can be programmed with industry-standard programmers, Atmel's ATDH2200E Programming Kit or Atmel's ATDH2225 ISP Cable.

**Table 1.** ATFS FPSLIC Support Devices

| FPSLIC Device | FPSLIC Support Device | Configuration Data | Spare Memory |
|---------------|-----------------------|--------------------|--------------|
| AT94K05       | ATFS05                | 226520 Bits        | 35624 Bits   |
| AT94K10       | ATFS10                | 430488 Bits        | 93800 Bits   |
| AT94K40       | ATFS40                | 815382 Bits        | 233194 Bits  |

## Pin Configurations

### 8-lead LAP

|          |   |   |          |
|----------|---|---|----------|
| DATA     | 1 | 8 | VCC      |
| CLK      | 2 | 7 | SER_EN   |
| RESET/OE | 3 | 6 | CEO (A2) |
| CE       | 4 | 5 | GND      |



## Support Device

**ATFS05**

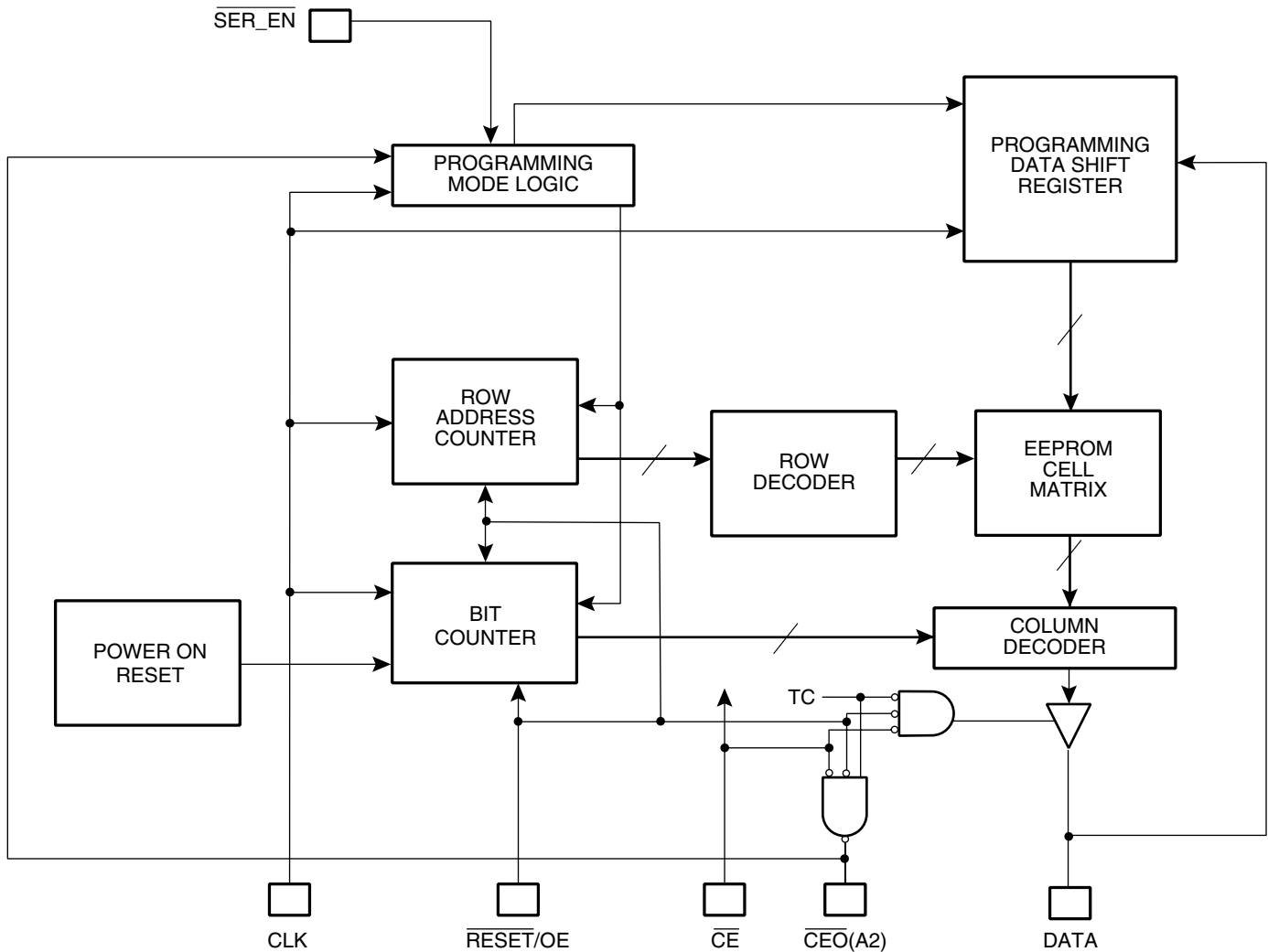
**ATFS10**

**ATFS40**

## Advance Information



## Block Diagram



## Device Description

The control signals for the FPSLIC Support Device ( $\overline{CE}$ ,  $\overline{RESET/OE}$  and CCLK) interface directly with the FPSLIC control signals. All FPSLIC devices can control the entire configuration process and retrieve data from the FPSLIC Support Device without requiring an external intelligent controller.

The  $\overline{RESET/OE}$  and  $\overline{CE}$  pins control the tri-state buffer on the DATA output pin and enable the address counter. When  $\overline{RESET/OE}$  is driven Low, the configuration EEPROM resets its address counter and tri-states its DATA pin. The  $\overline{CE}$  pin also controls the output of the FPSLIC Support Device. If  $\overline{CE}$  is held High after the  $\overline{RESET/OE}$  reset pulse, the counter is disabled and the DATA output pin is tri-stated. When OE is subsequently driven High, the counter and the DATA output pin are enabled. When  $\overline{RESET/OE}$  is driven Low again, the address counter is reset and the DATA output pin is tri-stated, regardless of the state of  $\overline{CE}$ .

When the FPSLIC Support Device has driven out all of its data and  $\overline{CEO}$  is driven Low, the device tri-states the DATA pin to avoid contention with other FPSLIC Support Devices. Upon power-up, the address counter is automatically reset.

## Pin Description

| 8 LAP Pin | Name                         | I/O | Description                                                                                                                                                                                                                                                                                                                                                                                                               |
|-----------|------------------------------|-----|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 1         | DATA                         | I/O | Tri-state DATA output for configuration. Open-collector bi-directional pin for programming.                                                                                                                                                                                                                                                                                                                               |
| 2         | CLK                          | I   | Clock input. Used to increment the internal address and bit counter for reading and programming.                                                                                                                                                                                                                                                                                                                          |
| 3         | $\overline{\text{RESET/OE}}$ | I   | Output Enable (active High) and RESET (active Low) when $\overline{\text{SER\_EN}}$ is High. A Low level on $\overline{\text{RESET/OE}}$ resets both the address and bit counters. A High level (with $\overline{\text{CE}}$ Low) enables the data output driver.                                                                                                                                                         |
| 4         | $\overline{\text{CE}}$       | I   | Chip Enable input (active Low). A Low level (with OE High) allows DCLK to increment the address counter and enables the data output driver. A High level on $\overline{\text{CE}}$ disables both the address and bit counters and forces the device into a low-power standby mode. Note that this pin will <i>not</i> enable/disable the device in the 2-wire Serial Programming mode ( $\overline{\text{SER\_EN}}$ Low). |
| 5         | GND                          |     | Ground pin. A 0.2 $\mu\text{F}$ decoupling capacitor between $V_{\text{CC}}$ and GND is recommended.                                                                                                                                                                                                                                                                                                                      |
| 6         | A2                           | I   | Device selection input, A2. This is used to enable (or select) the device during programming (i.e., when $\overline{\text{SER\_EN}}$ is Low). A2 has an internal pull-down resistor.                                                                                                                                                                                                                                      |
| 7         | $\overline{\text{SER\_EN}}$  | I   | Serial enable must be held High during FPSLIC loading operations. Bringing $\overline{\text{SER\_EN}}$ Low enables the 2-wire Serial Programming Mode. For non-ISP applications, $\overline{\text{SER\_EN}}$ should be tied to $V_{\text{CC}}$ .                                                                                                                                                                          |
| 8         | $V_{\text{CC}}$              |     | +3.3V power supply pin                                                                                                                                                                                                                                                                                                                                                                                                    |

## FPSLIC Master Serial Mode Summary

The I/O and logic functions of the FPSLIC devices are established by a configuration program. The program is loaded either automatically upon power-up, or on command, depending on the state of the mode pins. In Master Mode, the FPSLIC automatically loads the configuration program from an external memory. The FPSLIC Support Device has been designed for compatibility with the Master Mode.

## Control of Configuration

Most connections between the FPSLIC device and the FPSLIC Support Device are simple and self-explanatory:

- The DATA output of the FPSLIC Support Device drives DIN of the FPSLIC devices.
- The master FPSLIC CCLK output drives the CLK input of the FPSLIC Support Device.
- $\overline{\text{SER\_EN}}$  must be connected to  $V_{CC}$  (except during ISP).

## Programming Mode

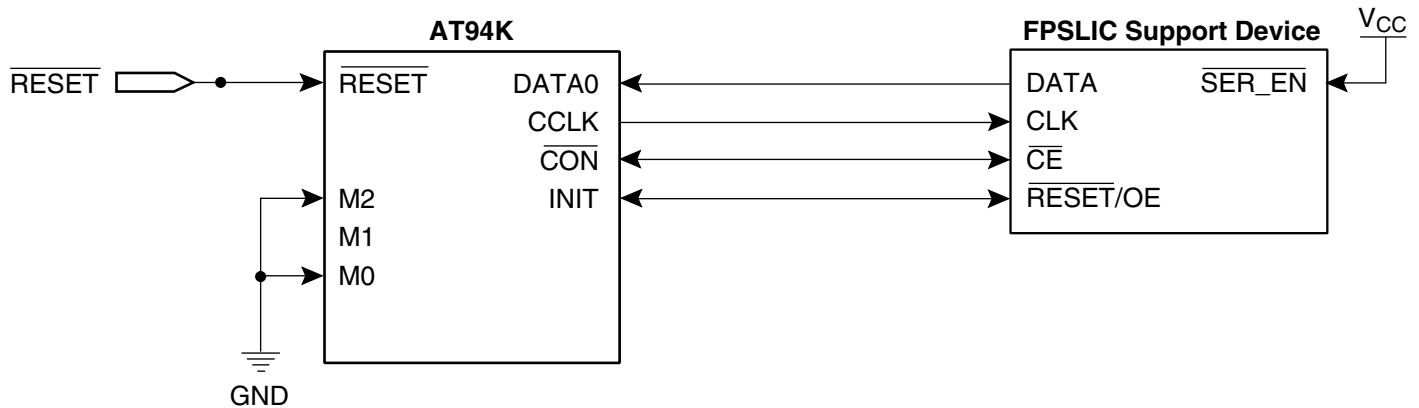
The programming mode is entered by bringing  $\overline{\text{SER\_EN}}$  Low. In this mode the chip can be programmed by the 2-wire serial bus. The programming is done at  $V_{CC}$  supply only. Programming super voltages are generated inside the chip.

## Standby Mode

The FPSLIC Support Device enters a low-power standby mode whenever  $\overline{\text{CE}}$  is asserted High. In this mode, the ATFS05 consumes less than 50  $\mu\text{A}$  of current at 3.3V. The output remains in a high-impedance state regardless of the state of the  $\overline{\text{OE}}$  input.

## Example Circuits

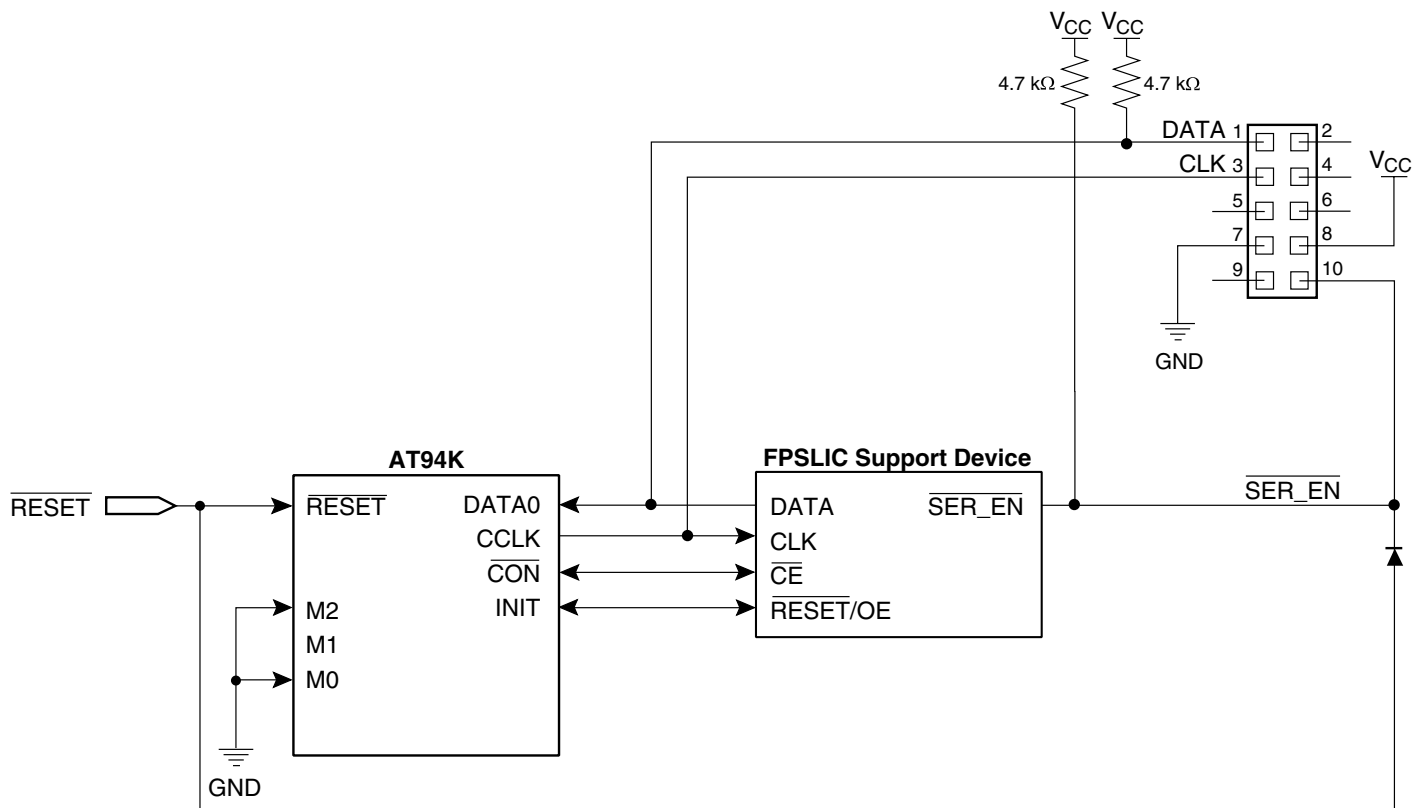
**Figure 1.** FPSLIC Support Device for Programming FPSLIC Devices



The FPSLIC's bi-directional  $\overline{\text{CON}}$  pin drives the  $\overline{\text{CE}}$  input of the FPSLIC Support Device, while the  $\overline{\text{RESET/OE}}$  input is driven by the FPSLIC's bi-directional  $\overline{\text{INIT}}$  pin. This connection works under all normal circumstances, even when the user aborts the configuration before  $\overline{\text{CON}}$  has gone High. A Low level on the  $\overline{\text{RESET/OE}}$  input, during FPSLIC reset, clears the FPSLIC Support Device's internal address pointer so that the reconfiguration starts at the beginning.

The spare memory can be accessed by in-system programming the ATFS through a two-wire serial interface built in the FPSLIC device. For more information, refer to the "C Code for Interfacing the FPSLIC AVR Core to AT17 Series Configuration Memories" application note, available on the Atmel web site ([www.atmel.com](http://www.atmel.com)).

**Figure 2.** In-System Programming of FPSLIC Support Devices



## Absolute Maximum Ratings\*

|                                                    |                          |
|----------------------------------------------------|--------------------------|
| Operating Temperature .....                        | -55°C to +125°C          |
| Storage Temperature .....                          | -65°C to +150°C          |
| Voltage on Any Pin<br>with Respect to Ground ..... | -0.1V to $V_{CC} + 0.5V$ |
| Supply Voltage ( $V_{CC}$ ) .....                  | -0.5V to +7.0V           |
| Maximum Soldering Temp. (10 sec. @ 1/16 in.) ..... | 260°C                    |
| ESD ( $R_{ZAP} = 1.5K$ , $C_{ZAP} = 100$ pF) ..... | 2000V                    |

\*NOTICE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those listed under operating conditions is not implied. Exposure to Absolute Maximum Rating conditions for extended periods of time may affect device reliability.

## Operating Conditions

| Symbol   | Description |                                                  | ATFS05/10/40 |     | Units |
|----------|-------------|--------------------------------------------------|--------------|-----|-------|
|          |             |                                                  | Min          | Max |       |
| $V_{CC}$ | Commercial  | Supply voltage relative to GND<br>-0°C to +70°C  | 3.0          | 3.6 | V     |
|          | Industrial  | Supply voltage relative to GND<br>-40°C to +85°C | 3.0          | 3.6 | V     |

## DC Characteristics – ATFS05

$V_{CC} = 3.3V \pm 10\%$

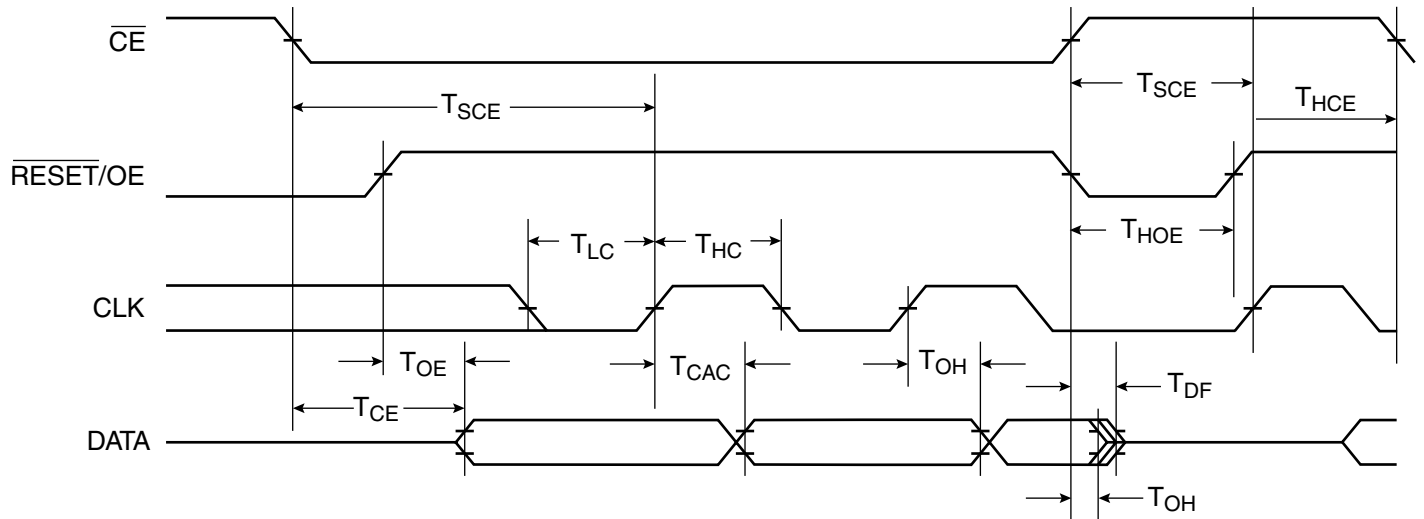
| Symbol    | Description                                                 |            | Min | Max      | Units         |
|-----------|-------------------------------------------------------------|------------|-----|----------|---------------|
| $V_{IH}$  | High-level Input Voltage                                    |            | 2.0 | $V_{CC}$ | V             |
| $V_{IL}$  | Low-level Input Voltage                                     |            | 0   | 0.8      | V             |
| $V_{OH}$  | High-level Output Voltage ( $I_{OH} = -2.5\text{ mA}$ )     | Commercial | 2.4 |          | V             |
| $V_{OL}$  | Low-level Output Voltage ( $I_{OL} = +3\text{ mA}$ )        |            |     | 0.4      | V             |
| $V_{OH}$  | High-level Output Voltage ( $I_{OH} = -2\text{ mA}$ )       | Industrial | 2.4 |          | V             |
| $V_{OL}$  | Low-level Output Voltage ( $I_{OL} = +3\text{ mA}$ )        |            |     | 0.4      | V             |
| $I_{CCA}$ | Supply Current, Active Mode                                 |            |     | 5        | mA            |
| $I_L$     | Input or Output Leakage Current ( $V_{IN} = V_{CC}$ or GND) |            | -10 | 10       | $\mu\text{A}$ |
| $I_{CCS}$ | Supply Current, Standby Mode                                | Commercial |     | 50       | $\mu\text{A}$ |
|           |                                                             | Industrial |     | 100      | $\mu\text{A}$ |

## DC Characteristics – ATFS10/40

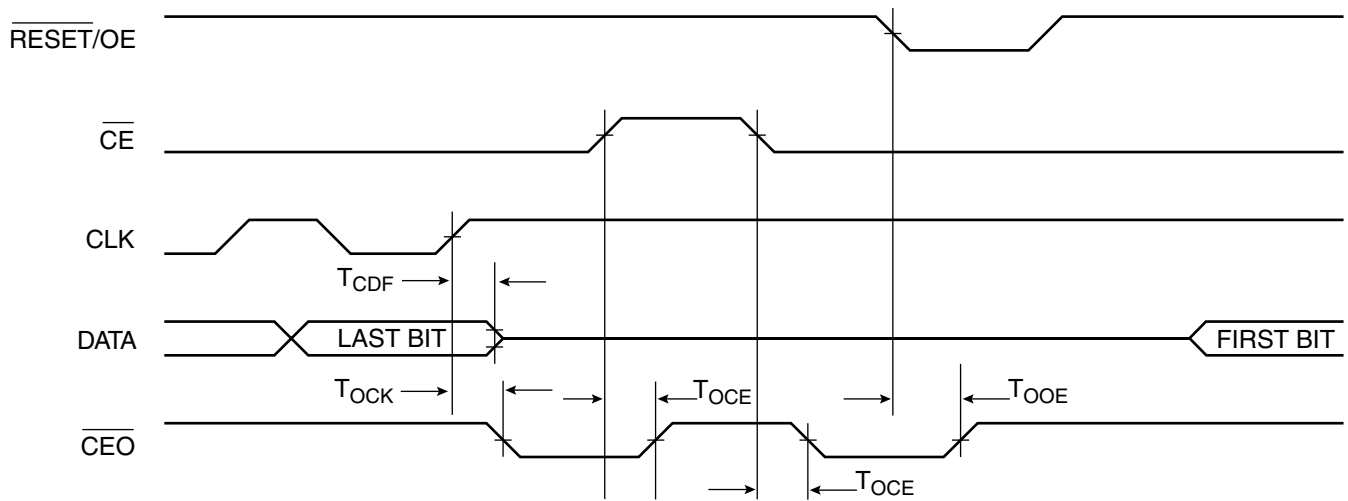
$V_{CC} = 3.3V \pm 10\%$

| Symbol    | Description                                                 |            | Min | Max      | Units         |
|-----------|-------------------------------------------------------------|------------|-----|----------|---------------|
| $V_{IH}$  | High-level Input Voltage                                    |            | 2.0 | $V_{CC}$ | V             |
| $V_{IL}$  | Low-level Input Voltage                                     |            | 0.0 | 0.8      | V             |
| $V_{OH}$  | High-level Output Voltage ( $I_{OH} = -2.5\text{ mA}$ )     | Commercial | 2.4 |          | V             |
| $V_{OL}$  | Low-level Output Voltage ( $I_{OL} = +3\text{ mA}$ )        |            |     | 0.4      | V             |
| $V_{OH}$  | High-level Output Voltage ( $I_{OH} = -2\text{ mA}$ )       | Industrial | 2.4 |          | V             |
| $V_{OL}$  | Low-level Output Voltage ( $I_{OL} = +3\text{ mA}$ )        |            |     | 0.4      | V             |
| $I_{CCA}$ | Supply Current, Active Mode                                 |            |     | 5        | mA            |
| $I_L$     | Input or Output Leakage Current ( $V_{IN} = V_{CC}$ or GND) |            | -10 | 10       | $\mu\text{A}$ |
| $I_{CCS}$ | Supply Current, Standby Mode                                | Commercial |     | 100      | $\mu\text{A}$ |
|           |                                                             | Industrial |     | 100      | $\mu\text{A}$ |

## AC Characteristics



## AC Characteristics When Cascading



## AC Characteristics for ATFS05

$V_{CC} = 3.3V \pm 10\%$

| Symbol          | Description                                                       | Commercial |     | Industrial |     | Units |
|-----------------|-------------------------------------------------------------------|------------|-----|------------|-----|-------|
|                 |                                                                   | Min        | Max | Min        | Max |       |
| $T_{OE}^{(1)}$  | $\overline{OE}$ to Data Delay                                     |            | 50  |            | 55  | ns    |
| $T_{CE}^{(1)}$  | $\overline{CE}$ to Data Delay                                     |            | 60  |            | 60  | ns    |
| $T_{CAC}^{(1)}$ | CLK to Data Delay                                                 |            | 75  |            | 80  | ns    |
| $T_{OH}$        | Data Hold from $\overline{CE}$ , $\overline{OE}$ , or CLK         | 0          |     | 0          |     | ns    |
| $T_{DF}^{(2)}$  | $\overline{CE}$ or $\overline{OE}$ to Data Float Delay            |            | 55  |            | 55  | ns    |
| $T_{LC}$        | CLK Low Time                                                      | 25         |     | 25         |     | ns    |
| $T_{HC}$        | CLK High Time                                                     | 25         |     | 25         |     | ns    |
| $T_{SCE}$       | $\overline{CE}$ Setup Time to CLK (to guarantee proper counting)  | 35         |     | 60         |     | ns    |
| $T_{HCE}$       | $\overline{CE}$ Hold Time from CLK (to guarantee proper counting) | 0          |     | 0          |     | ns    |
| $T_{HOE}$       | $\overline{OE}$ High Time (guarantees counter is reset)           | 25         |     | 25         |     | ns    |
| $F_{MAX}$       | Maximum Input Clock Frequency                                     | 10         |     | 10         |     | MHz   |

Notes: 1. AC test lead = 50 pF.  
2. Float delays are measured with 5 pF AC loads. Transition is measured  $\pm 200$  mV from steady-state active levels.

## AC Characteristics for ATFS05 when Cascading

$V_{CC} = 3.3V \pm 10\%$

| Symbol          | Description                   | Commercial |     | Industrial |     | Units |
|-----------------|-------------------------------|------------|-----|------------|-----|-------|
|                 |                               | Min        | Max | Min        | Max |       |
| $T_{CDF}^{(1)}$ | CLK to Data Float Delay       |            | 60  |            | 60  | ns    |
| $F_{MAX}$       | Maximum Input Clock Frequency | 8          |     | 8          |     | MHz   |

Note: 1. Float delays are measured with 5 pF AC loads. Transition is measured  $\pm 200$  mV from steady state active levels.

## AC Characteristics for ATFS10/40

$V_{CC} = 3.3V \pm 10\%$

| Symbol          | Description                                                       | Commercial |     | Industrial |     | Units |
|-----------------|-------------------------------------------------------------------|------------|-----|------------|-----|-------|
|                 |                                                                   | Min        | Max | Min        | Max |       |
| $T_{OE}^{(1)}$  | $\overline{OE}$ to Data Delay                                     |            | 50  |            | 55  | ns    |
| $T_{CE}^{(1)}$  | $\overline{CE}$ to Data Delay                                     |            | 55  |            | 60  | ns    |
| $T_{CAC}^{(1)}$ | CLK to Data Delay                                                 |            | 55  |            | 60  | ns    |
| $T_{OH}$        | Data Hold From $\overline{CE}$ , $\overline{OE}$ , or CLK         | 0          |     | 0          |     | ns    |
| $T_{DF}^{(2)}$  | $\overline{CE}$ or $\overline{OE}$ to Data Float Delay            |            | 50  |            | 50  | ns    |
| $T_{LC}$        | CLK Low Time                                                      | 25         |     | 25         |     | ns    |
| $T_{HC}$        | CLK High Time                                                     | 25         |     | 25         |     | ns    |
| $T_{SCE}$       | $\overline{CE}$ Setup Time to CLK (to guarantee proper counting)  | 30         |     | 35         |     | ns    |
| $T_{HCE}$       | $\overline{CE}$ Hold Time from CLK (to guarantee proper counting) | 0          |     | 0          |     | ns    |
| $T_{HOE}$       | $\overline{OE}$ High Time (guarantees counter is reset)           | 25         |     | 25         |     | ns    |
| $F_{MAX}$       | MAX Input Clock Frequency                                         | 15         |     | 10         |     | MHz   |

Notes: 1. AC test load = 50 pF.  
2. Float delays are measured with 5 pF AC loads. Transition is measured  $\pm 200$  mV from steady state active levels.

## AC Characteristics for ATFS10/40 when Cascading

$V_{CC} = 3.3V \pm 10\%$

| Symbol          | Description               | Commercial |     | Industrial |     | Units |
|-----------------|---------------------------|------------|-----|------------|-----|-------|
|                 |                           | Min        | Max | Min        | Max |       |
| $T_{CDF}^{(1)}$ | CLK to Data Float Delay   |            | 50  |            | 50  | ns    |
| $F_{MAX}$       | MAX Input Clock Frequency | 12.5       |     | 10         |     | MHz   |

Note: 1. Float delays are measured with 5 pF AC loads. Transition is measured  $\pm 200$  mV from steady state active levels.

## Thermal Resistance Coefficients<sup>(1)</sup>

| Device    | Package Type                 |      | $\theta_{JC}$ [°C/W] | $\theta_{JA}$ [°C/W] |
|-----------|------------------------------|------|----------------------|----------------------|
|           |                              |      |                      | Airflow = 0 ft/min   |
| ATFS05    | Leadless Array Package (LAP) | 8CN4 | 45                   | 115.71               |
| ATFS10/40 | Leadless Array Package (LAP) | 8CN4 | 45                   | 135.71               |

Note: 1. For more information refer to the “Thermal Characteristics of Atmel’s Packages” application note, available on the Atmel web site.



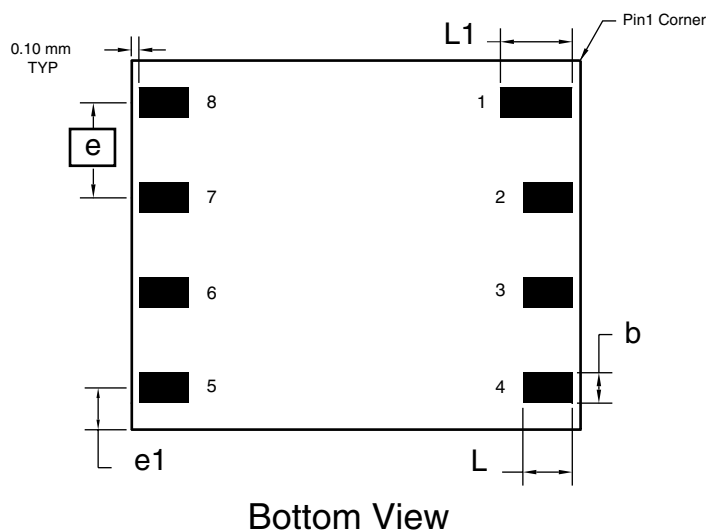
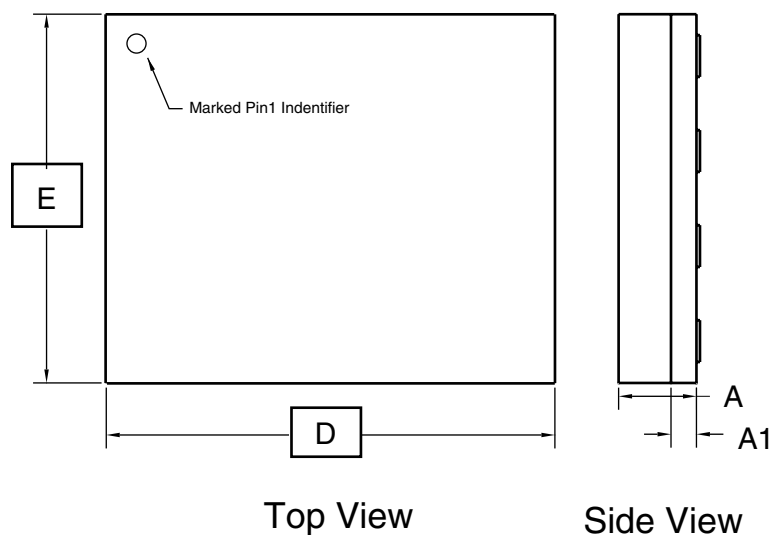
## Ordering Information

| Ordering Code                       | Package              | Operation Range               |
|-------------------------------------|----------------------|-------------------------------|
| ATFS05-CC<br>ATFS10-CC<br>ATFS40-CC | 8CN4<br>8CN4<br>8CN4 | Commercial<br>(0°C to 70°C)   |
| ATFS05-CI<br>ATFS10-CI<br>ATFS40-CI | 8CN4<br>8CN4<br>8CN4 | Industrial<br>(-40°C to 85°C) |

| Package Type |                                                                                 |
|--------------|---------------------------------------------------------------------------------|
| 8CN4         | 8-lead (6 x 6 x 1.04 mm Body), Lead Pitch 1.27 mm, Leadless Array Package (LAP) |

## Packaging Information

### 8CN4 – LAP



**COMMON DIMENSIONS**  
(Unit of Measure = mm)

| SYMBOL | MIN      | NOM  | MAX  | NOTE |
|--------|----------|------|------|------|
| A      | 0.94     | 1.04 | 1.14 |      |
| A1     | 0.30     | 0.34 | 0.38 |      |
| b      | 0.45     | 0.50 | 0.55 | 1    |
| D      | 5.89     | 5.99 | 6.09 |      |
| E      | 4.89     | 5.99 | 6.09 |      |
| e      | 1.27 BSC |      |      |      |
| e1     | 1.10 REF |      |      |      |
| L      | 0.95     | 1.00 | 1.05 | 1    |
| L1     | 1.25     | 1.30 | 1.35 | 1    |

Note: 1. Metal Pad Dimensions.

11/14/01



2325 Orchard Parkway  
San Jose, CA 95131

#### TITLE

**8CN4**, 8-lead (6 x 6 x 1.04 mm Body), Lead Pitch 1.27 mm,  
Leadless Array Package (LAP)

#### DRAWING NO.

8CN4

#### REV.

A





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Большой выбор предлагаемой продукции, различные виды оплаты и доставки, позволят Вам сэкономить время и получить максимум выгоды от сотрудничества с нами!

## Перечень производителей, продукцию которых мы поставляем на российский рынок





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С удовольствием будем прорабатывать для Вас поставки всех необходимых компонентов по текущим запросам для скорейшего выявления групп элементов, по которым сотрудничество именно с нашей компанией будет для Вас максимально выгодным!

С уважением,

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