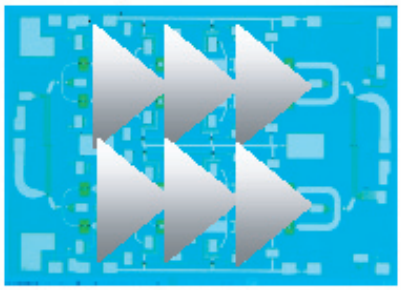
AMMC - 6430
25 - 33 GHz Power Amplifier

Data Sheet



Chip Size: 2500 x 1750 µm (100 x 69 mils)
Chip Size Tolerance: ± 10µm (±0.4 mils)
Chip Thickness: 100 ± 10µm (4 ± 0.4 mils)
Pad Dimensions: 100 x 100 µm (4 ± 0.4 mils)

Description

The AMMC-6430 MMIC is a broadband nearly 1W power amplifier designed for use in transmitters that operate in various frequency bands between 25GHz and 33GHz. This MMIC optimized for linear operation with an output third order intercept point (OIP3) of 37dBm. At 30GHz it provides 29dBm of output power (P-1dB) and 17dB of gain. The device has input and output matching circuitry for use in 50 Ω environments. The AMMC-6430 also integrates a temperature compensated RF power detection circuit that enables power detection of 0.3V/W. DC bias is simple and the device operates on widely available 5.5V for current supply (negative voltage only needed for Vg). It is fabricated in a PHEMT process for exceptional power and gain performance. For improved reliability and moisture protection, the die is passivated at the active areas.

Features

- Wide frequency range: 25 - 33 GHz
- High gain: 17 dB
- Power: @30 GHz, P-1dB=29 dBm
- Highly linear: OIP3=37dBm
- Integrated RF power detector
- 5.5 Volt, -0.7 Volt, 900mA operation

Applications

- Microwave Radio systems
- Satellite VSAT and DBS systems
- LMDS & Pt-Pt mmW Long Haul
- 802.16 & 802.20 WiMax BWA
- WLL and MMDS loops
- Can be driven by AMMC-6345, increasingluding overall gain.

AMMC-6430 Absolute Maximum Ratings[1]

Symbol	Parameters/Conditions	Units	Min.	Max.
V_d	Positive Drain Voltage	V		7
V_g	Gate Supply Voltage	V	-3	0.5
I_{dq}	Drain Current	mA		1500
P_{in}	CW Input Power	dBm		23
T_{ch}	Operating Channel Temp.	°C		+150
T_{stg}	Storage Case Temp.	°C	-65	+150
T_{max}	Maximum Assembly Temp (60 sec max)	°C		+300

Note:
1. Operation in excess of any one of these conditions may result in permanent damage to this device.



Note: These devices are ESD sensitive. The following precautions are strongly recommended. Ensure that an ESD approved carrier is used when dice are transported from one destination to another. Personal grounding is to be worn at all times when handling these devices

AMMC-6430 DC Specifications/Physical Properties [1]

Symbol	Parameters and Test Conditions	Units	Min.	Typ.	Max.
I_{dq}	Drain Supply Current (under any RF power drive and temperature) (V_d=5.0 V, V_g set for I_d Typical)	mA		900	1000
V_g	Gate Supply Operating Voltage ($I_{d(Q)}$ = 900 (mA))	V	-0.9	-0.7	-0.55
θ_{ch-b}	Thermal Resistance[2] (Backside temperature, T_b = 25°C)	°C/W		9	

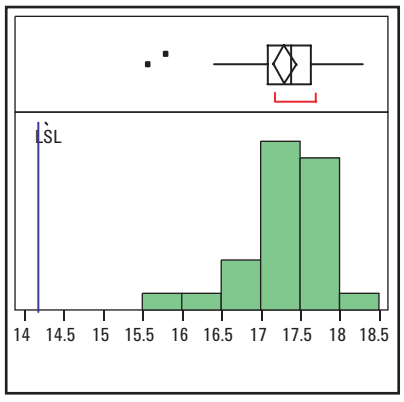
Notes:
1. Ambient operational temperature T_A=25°C unless otherwise noted.
2. Channel-to-backside Thermal Resistance (θ_{ch-b}) = 10°C/W at $T_{channel}$ (T_c) = 107°C as measured using infrared microscopy. Thermal Resistance at backside temperature (T_b) = 25°C calculated from measured data.

AMMC-6430 RF Specifications [3, 4, 5]

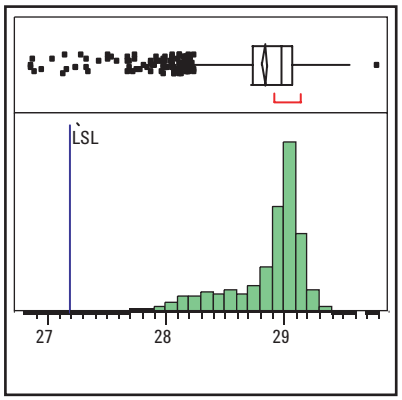
T_A= 25°C, V_d=5.5V, $I_{d(Q)}$=900 mA, Z_o=50 Ω

Symbol	Parameters and Test Conditions	Units	Minimum	Typical	Maximum	Sigma
Gain	Small-signal Gain[4]	dB	14	17		0.5
P_{-1dB}	Output Power at 1dB Gain Compression	dBm	27	28.5		0.38
P_{-3dB}	Output Power at 3dB Gain Compression	dBm		29		0.35
OIP3	Third Order Intercept Point; Δf=100MHz; Pin=-20dBm	dBm		37		0.8
RLin	Input Return Loss[4]	dB		-15		0.92
RLout	Output Return Loss[4]	dB		-15		0.63
Isolation	Min. Reverse Isolation	dB		-43		1.8

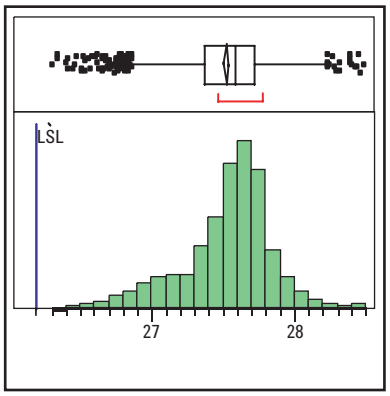
Notes:
3. Small/Large -signal data measured in wafer form T_A = 25°C.
4. 100% on-wafer RF test is done at frequency = 27, 29, and 32 GHz. Statistics based on 1500 part sample
5. Specifications are derived from measurements in a 50 Ω test environment. Aspects of the amplifier performance may be improved over a more narrow bandwidth by application of additional conjugate, linearity, or power matching.



Gain at 29 GHz



P-1dB at 29 GHz



P-1dB at 33 GHz

Typical distribution of Small Signal Gain and Output Power @P-1dB. Based on 1500 part sampled over several production lots.

AMMC-6430 Typical Performances (T_A = 25°C, V_d =5.5 V, I_{dq} = 900 mA, Z_{in} = Z_{out} = 50 Ω)

NOTE: These measurements are in a 50 Ω test environment. Aspects of the amplifier performance may be improved over a more narrow bandwidth by application of additional conjugate, linearity, or power matching.

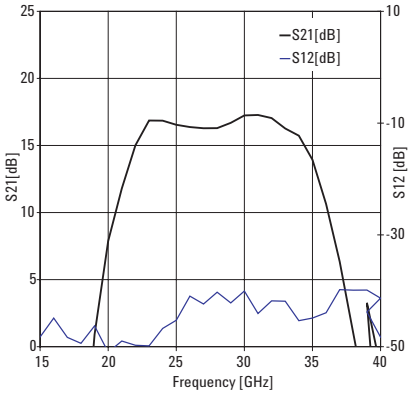


Figure 1. Typical Gain and Reverse Isolation

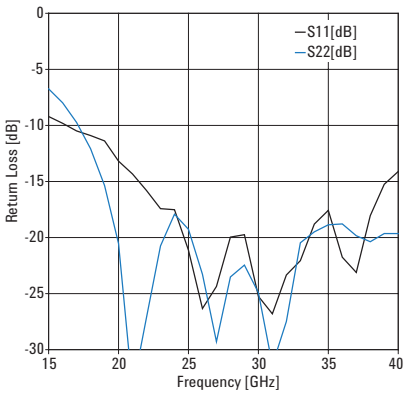


Figure 2. Typical Return Loss (Input and Output)

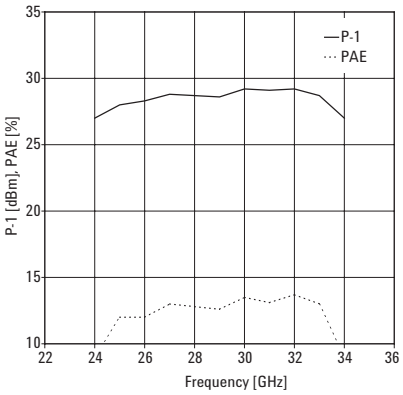


Figure 3. Typical Output Power (@P-1dB) and PAE

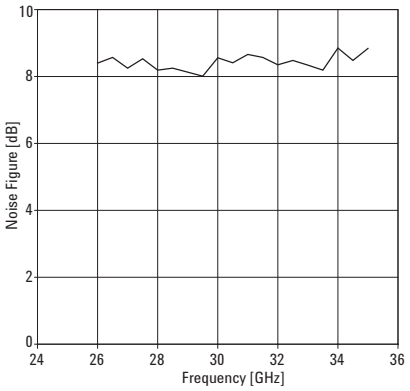


Figure 4. Typical Noise Figure

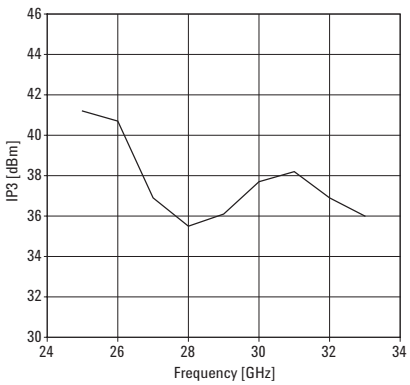


Figure 5. Typical Output 3rd Order Intercept Pt.

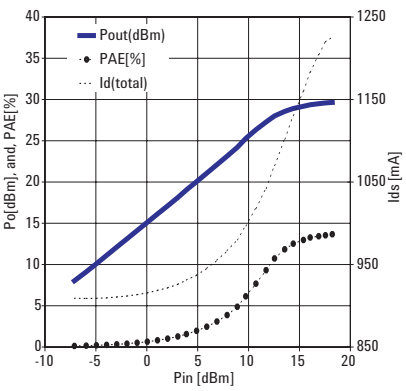


Figure 6. Typical Output Power, PAE, and Total Drain Current versus Input Power at30GHz

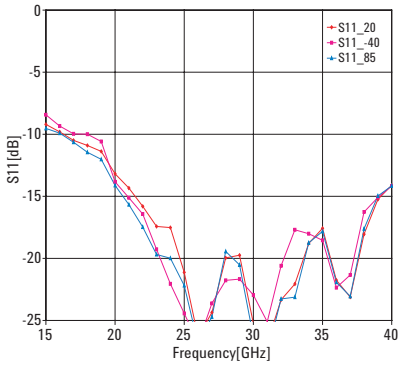


Figure 7. Typical S11 over temperature

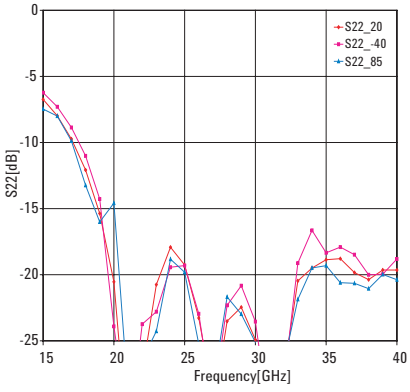


Figure 8. Typical S22 over temperature

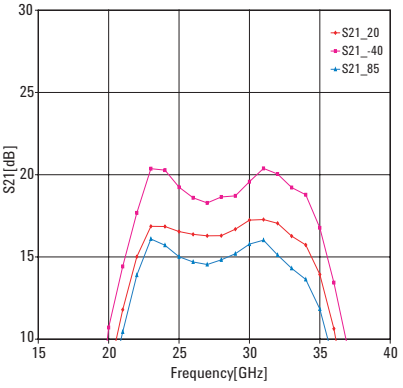


Figure 9. Typical Gain over temperature

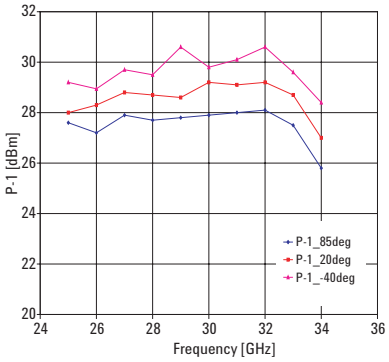


Figure 10. Typical One dB Compression over temperature

Typical Scattering Parameters [1], ($T_A = 25°C$, $V_d = 5.5$ V, $I_{dq} = 900$ mA, $Z_{in} = Z_{out} = 50\ \Omega$)

	S11			S21			S12			S22		
Freq GHz	**dB**	**Mag**	**Phase**	**dB**	**Mag**	**Phase**	**dB**	**Mag**	**Phase**	**dB**	**Mag**	**Phase**
10	-5.91	0.51	165.15	-38.73	0.01	-150.08	-46.83	4.56E-03	-163.93	-4.57	0.59	164.28
11	-6.57	0.47	148.07	-38.15	0.01	177.71	-47.99	3.99E-03	161.86	-5.15	0.55	144.68
12	-7.18	0.44	132.45	-38.84	0.01	159.58	-45.28	5.44E-03	162.25	-5.83	0.51	125.30
13	-7.75	0.41	116.37	-38.40	0.01	144.22	-44.76	5.78E-03	127.45	-7.10	0.44	109.48
14	-8.35	0.38	102.02	-35.23	0.02	127.82	-48.37	3.82E-03	114.36	-5.96	0.50	93.30
15	-9.21	0.35	89.97	-35.73	0.02	131.62	-48.26	3.86E-03	99.54	-6.74	0.46	66.48
16	-9.81	0.32	76.63	-35.32	0.02	174.87	-44.88	5.70E-03	76.35	-7.98	0.40	42.81
17	-10.49	0.30	65.83	-21.06	0.09	-173.40	-48.33	3.83E-03	66.69	-9.74	0.33	19.70
18	-10.90	0.29	53.72	-8.97	0.36	146.31	-49.40	3.39E-03	62.63	-12.08	0.25	-2.59
19	-11.38	0.27	38.47	0.91	1.11	86.03	-46.28	4.85E-03	90.04	-15.37	0.17	-23.98
20	-13.19	0.22	26.38	7.87	2.48	12.36	-50.99	2.82E-03	85.49	-20.54	0.09	-43.76
21	-14.34	0.19	19.22	11.79	3.89	-59.81	-48.99	3.55E-03	59.91	-33.57	0.02	-36.06
22	-15.81	0.16	11.11	15.01	5.63	-128.14	-49.75	3.26E-03	65.89	-27.13	0.04	58.91
23	-17.43	0.13	8.99	16.86	6.97	160.79	-49.86	3.21E-03	101.47	-20.75	0.09	56.63
24	-17.52	0.13	-4.76	16.85	6.96	96.24	-46.73	4.61E-03	79.40	-17.92	0.13	20.33
25	-21.12	0.09	-14.59	16.54	6.72	39.34	-45.27	5.45E-03	80.30	-19.27	0.11	-3.94
26	-26.33	0.05	-16.19	16.37	6.59	-11.71	-40.96	8.96E-03	82.13	-23.28	0.07	-27.01
27	-24.36	0.06	37.91	16.28	6.52	-61.96	-42.37	7.62E-03	68.87	-29.28	0.03	-9.02
28	-19.96	0.10	25.90	16.29	6.53	-110.13	-40.26	9.71E-03	49.68	-23.52	0.07	26.76
29	-19.75	0.10	16.45	16.69	6.83	-159.96	-42.17	7.79E-03	47.32	-22.46	0.08	16.30
30	-25.24	0.05	8.60	17.24	7.28	145.89	-40.05	9.95E-03	32.17	-24.92	0.06	-25.48
31	-26.81	0.05	19.45	17.27	7.31	92.90	-44.07	6.26E-03	27.80	-31.37	0.03	-70.15
32	-23.34	0.07	52.06	17.04	7.11	34.67	-41.80	8.13E-03	27.52	-27.49	0.04	124.04
33	-22.06	0.08	55.38	16.27	6.51	-21.77	-41.87	8.07E-03	29.56	-20.47	0.09	87.29
34	-18.80	0.11	38.20	15.73	6.12	-80.57	-45.35	5.40E-03	9.23	-19.49	0.11	57.42
35	-17.57	0.13	22.77	13.93	4.97	-147.31	-44.88	5.70E-03	28.68	-18.86	0.11	45.83
36	-21.76	0.08	12.34	10.64	3.40	147.08	-43.93	6.36E-03	69.74	-18.79	0.12	42.27
37	-23.11	0.07	58.33	6.34	2.08	87.01	-39.80	1.02E-02	47.20	-19.84	0.10	33.52
38	-18.05	0.13	65.65	0.98	1.12	33.30	-39.89	1.01E-02	23.04	-20.37	0.10	37.79
39	-15.25	0.17	48.45	-4.18	0.62	-13.03	-39.87	1.02E-02	16.72	-19.65	0.10	38.29
40	-14.11	0.20	38.60	-9.56	0.33	-54.38	-41.33	8.59E-03	38.69	-19.65	0.10	41.26

Note:
1. Data obtained from on-wafer measurements.

Biasing and Operation

The recommended quiescent DC bias condition for optimum efficiency, performance, and reliability is Vd=5 volts with Vg set for Id=950 mA. Minor improvements in performance are possible depending on the application. The drain bias voltage range is 3 to 5.5V. A single DC gate supply connected to Vg will bias all gain stages. Muting can be accomplished by setting Vg and /or Vg to the pinch-off voltage Vp.

An optional output power detector network is also provided. The differential voltage between the Det-Ref and Det-Out pads can be correlated with the RF power emerging from the RF output port. The detected voltage is given by :

$$V = (V_{ref} - V_{\det}) - V_{ofs}$$

where V_{ref} is the voltage at the DET_R port, $V_{\det}$ is a voltage at the DET_O port, and V_{ofs} is the zero-input-power offset voltage. There are three methods to calculate :

1. V_{ofs} can be measured before each detector measurement (by removing or switching off the power source and measuring). This method gives an error due to temperature drift of less than 0.01dB/50°C.
2. V_{ofs} can be measured at a single reference temperature. The drift error will be less than 0.25dB.
3. V_{ofs} can either be characterized over temperature and stored in a lookup table, or it can be measured at two temperatures and a linear fit used to calculate at any temperature. This method gives an error close to the method #1.

The RF ports are AC coupled at the RF input to the first stage and the RF output of the final stage. No ground wired are needed since ground connections are made with plated through-holes to the backside of the device.

Assembly Techniques

The backside of the MMIC chip is RF ground. For microstrip applications the chip should be attached directly to the ground plane (e.g. circuit carrier or heatsink) using electrically conductive epoxy [1,2].

For best performance, the topside of the MMIC should be brought up to the same height as the circuit surrounding it. This can be accomplished by mounting a gold plate metal shim (same length and width as the MMIC) under the chip which is of correct thickness to make the chip and adjacent circuit the same height. The amount of epoxy used for the chip and/or shim attachment should be just enough to provide a thin fillet around the bottom perimeter of the chip or shim. The ground plain should be free of any residue that may jeopardize electrical or mechanical attachment.

The location of the RF bond pads is shown in Figure 12. Note that all the RF input and output ports are in a Ground-Signal configuration.

RF connections should be kept as short as reasonable to minimize performance degradation due to undesirable series inductance. A single bond wire is normally sufficient for signal connections, however double bonding with 0.7 mil gold wire or use of gold mesh is recommended for best performance, especially near the high end of the frequency band.

Thermosonic wedge bonding is preferred method for wire attachment to the bond pads. Gold mesh can be attached using a 2 mil round tracking tool and a tool force of approximately 22 grams and a ultrasonic power of roughly 55 dB for a duration of 76 +/- 8 mS. The guided wedge at an untrasonic power level of 64 dB can be used for 0.7 mil wire. The recommended wire bond stage temperature is 150 +/- 2°C.

Caution should be taken to not exceed the Absolute Maximum Rating for assembly temperature and time.

The chip is 100um thick and should be handled with care. This MMIC has exposed air bridges on the top surface and should be handled by the edges or with a custom collet (do not pick up the die with a vacuum on die center).

This MMIC is also static sensitive and ESD precautions should be taken.

Notes:
1. Ablebond 84-1 LM1 silver epoxy is recommended.
2. Eutectic attach is not recommended and may jeopardize reliability of the device.

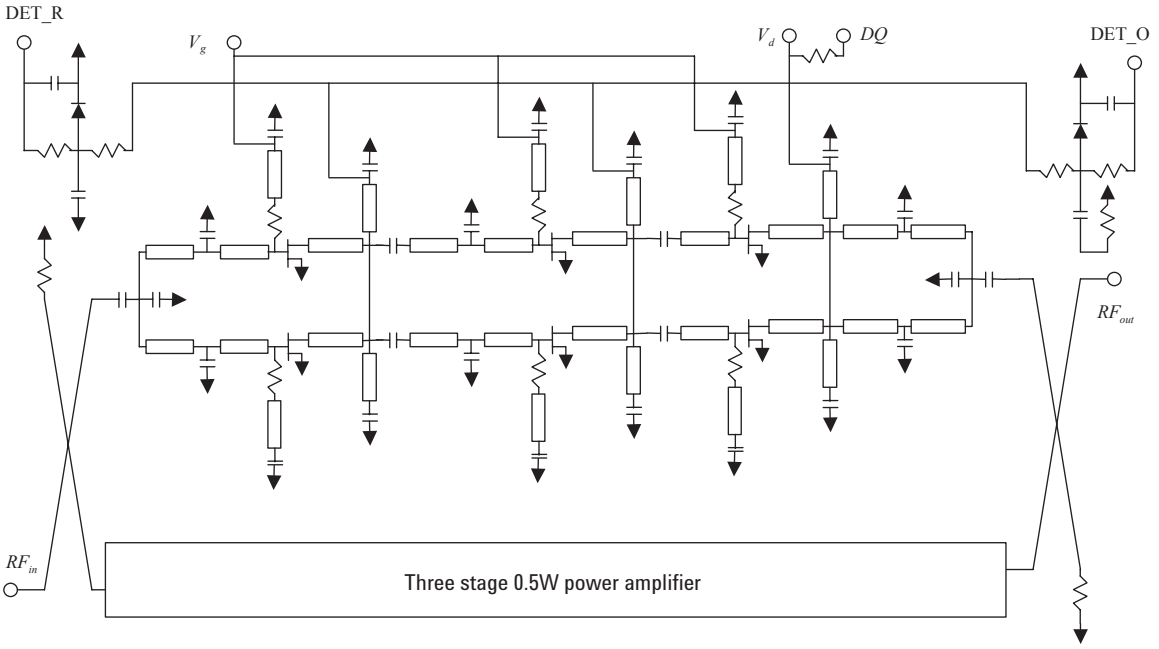


Figure 11. AMMC-6430 Schematic

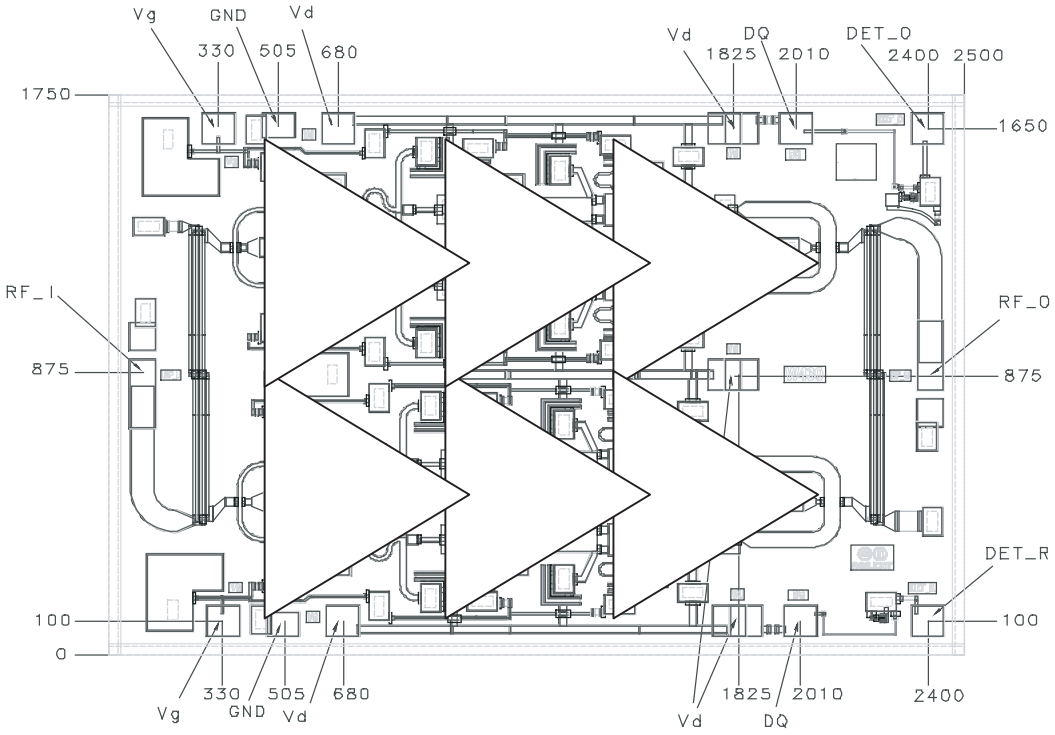


Figure 12. AMMC-6430 Bonding pad locations

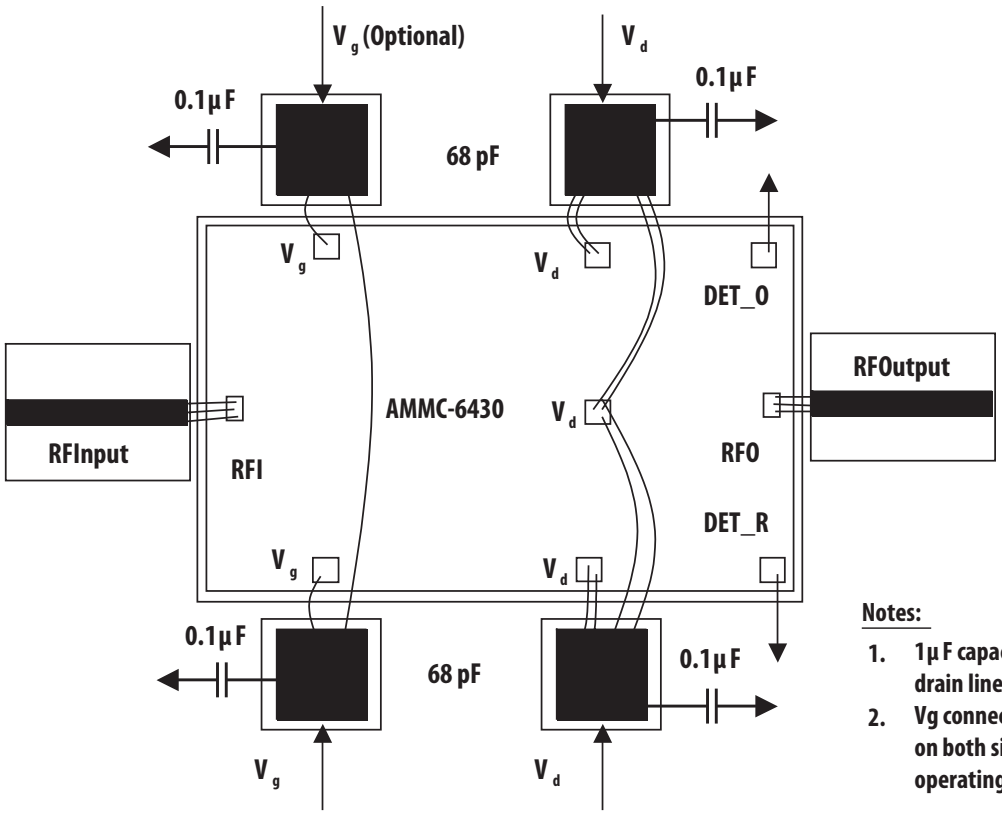


Figure 13. AMMC-6430 Assembly diagram

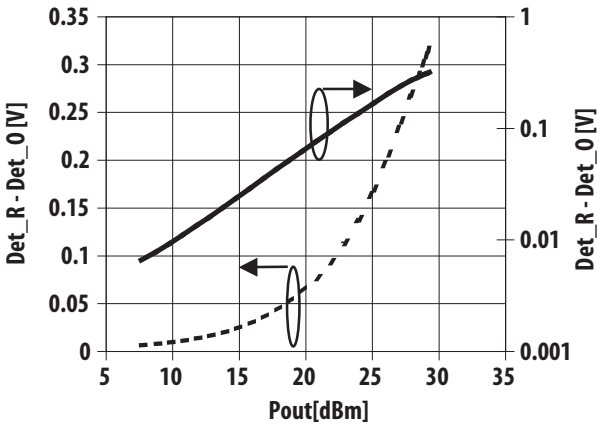


Figure 14. AMMC-6430 Typical Detector Voltage and Output Power, Freq=30 GHz

Ordering information:

AMMC-6430-W10 = 10 devices per tray

AMMC-6430-W50 = 50 devices per tray

For product information and a complete list of distributors, please go to our web site: **www.avagotech.com**

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