Data Sheet | March 2004 | FN9002.3

USB Dual Port Power Supply Controller

The ISL6119 is a USB dual port power controller, fully independent overcurrent (OC) fault protection IC. Operational over the +2.5V to +5.5V range, this device features internal current monitoring, accurate current limiting, integrated power switches and current limited delay to latch-off for system protection.

The ISL6119 current sense and limiting circuitry sets the current limit to a nominal 1A, making this device well suited for the USB port power management application. The ISL6119 provides OC fault notification, accurate current limiting and a consistent timed latch-off thus isolating and protecting the voltage bus in the presence of an OC event or short circuit. The 12ms time to latch-off is independent of the adjoining switch's electrical or thermal condition and the OC response time is inversely related to the OC magnitude.

Each ISL6119 incorporates in a single 8 lead SOIC package two 80mΩ N-channel MOSFET power switches for power control. Each switch is driven by a constant current source giving a controlled ramp up of the output voltage. This provides a soft start turn-on eliminating bus voltage drooping caused by inrush current while charging heavy load capacitances. Independent enabling inputs and fault reporting outputs for each channel are compatible with 3V and 5V logic to allow external control and monitoring.

The ISL6119 undervoltage lockout feature prevents turn-on of the outputs unless the correct ENABLE state and VIN > 2.5V are present. During initial turn-on the ISL6119 prevents fault reporting by blanking the fault signal. Rising and falling outputs are current limited voltage ramps so that both the inrush current and voltage slew rate are limited, independent of load. This reduces supply droop due to surge and eliminates the need for external EMI filters. During operation, once an OC condition is detected the appropriate output is current limited for 12ms to allow transient conditions to pass. If still in current limit after the current limit period has elapsed, the output is then latched off and the fault is reported by pulling the corresponding $\overline{\text{FAULT}}$ low. The $\overline{\text{FAULT}}$ signal is latched low until reset by the ENABLE signal being de-asserted at which time the $\overline{\text{FAULT}}$ signal will clear.

Features

- 80mΩ Integrated Power N-channel MOSFET Switches
- Accurate Current Sensing and 1A Current Limiting
- 12ms Fault Delay to Latch-Off, No Thermal Dependency
- 2.5V to 5.5V Operating Range
- Disabled Output Internally Pulled Low
- Undervoltage Lockout
- Controlled Turn-on Ramp Time
- Channel Independent Fault Output Signals
- Compatible with 3.3V and 5V Logic Families
- Channel Independent Logic Level Enable High Inputs (ISL6119H) or Enable Low Inputs (ISL6119L)
- Pb-Free Package Options
- Available in Tape & Reel with '-T' Part Number Suffix

Applications

- USB Port Power Management
- Electronic Circuit Limiting and Breaker

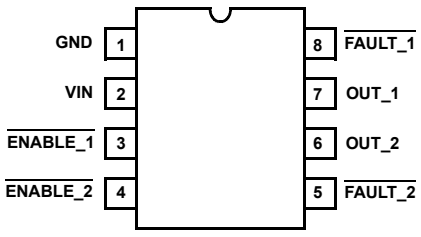
Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. DWG. #
ISL6119LIB	-40 to 85	8 Lead SOIC	M8.15
ISL6119LIBZA (Note)	-40 to 85	8 Lead SOIC (Pb-free)	M8.15
ISL6119HIB	-40 to 85	8 Lead SOIC	M8.15
ISL6119HIBZA (Note)	-40 to 85	8 Lead SOIC (Pb-free)	M8.15
ISL6119EVAL1	Evaluation Platform		
ISL6119USBEVAL1	USB Dual Port Evaluation Platform		

NOTE: Intersil Pb-free products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which is compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J Std-020B.

Pinout

ISL6119 (SOIC)
TOP VIEW



CAUTION: These devices are sensitive to electrostatic discharge; follow proper IC Handling Procedures.
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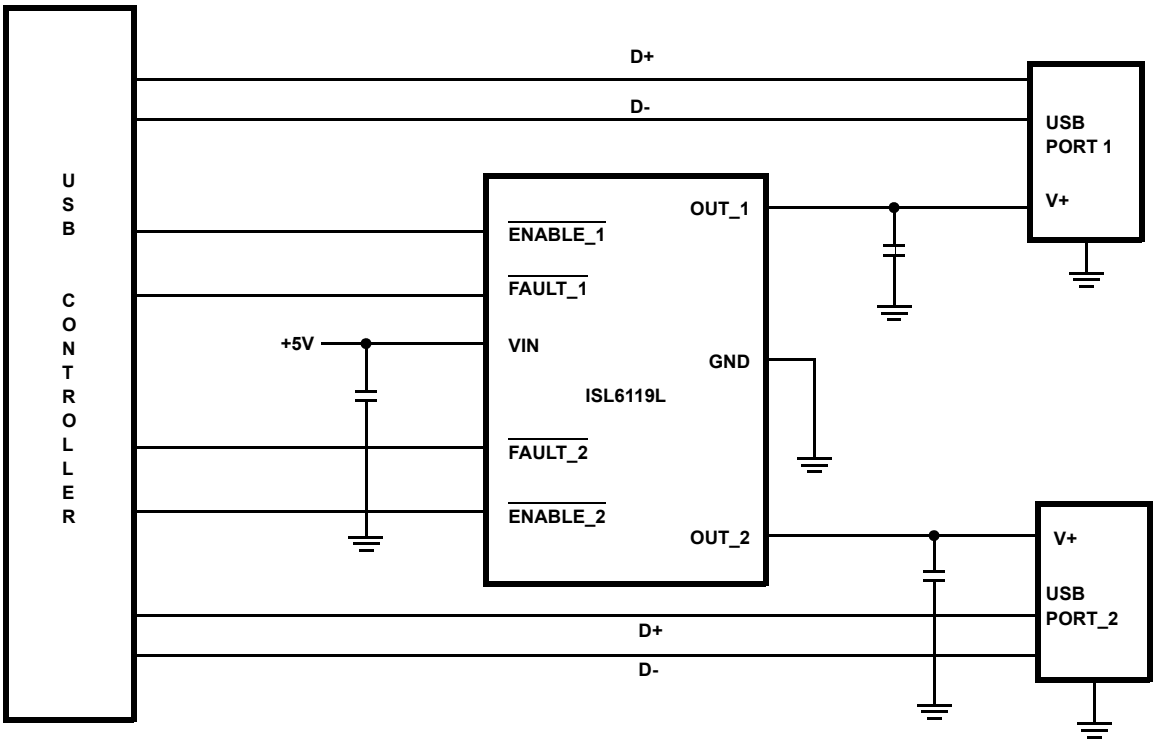
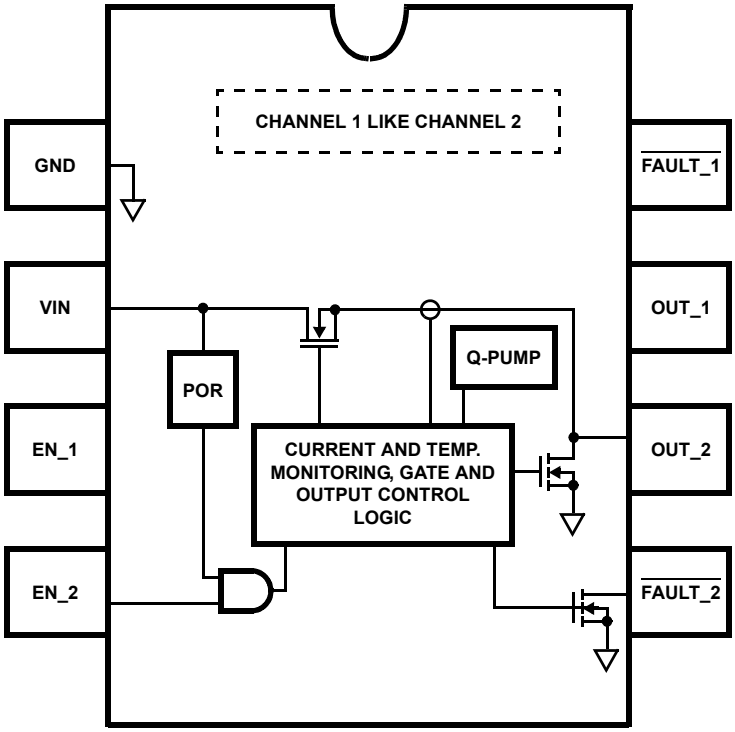
Typical Application: Dual USB Port Power



Simplified Block Diagram



Pin Descriptions

PIN NO.	DESIGNATOR	FUNCTION	DESCRIPTION
1	GND	IC Reference	
2	VIN	Chip bias, Controlled Supply Input, Undervoltage lock-out	VIN provides chip bias voltage. At VIN < 2.5V chip functionality is disabled, $\overline{\text{FAULT}}$ latch is cleared and floating and OUT is held low.
3, 4	ENABLE_1, 2/ $\overline{\text{ENABLE_1, 2}}$	Channel Enable/ Enable Not Inputs	Enables/Disables switch.
5, 8	$\overline{\text{FAULT_2, 1}}$	Channel 2, 1 Over Current Fault Not Indicator	Channel overcurrent fault indicator. $\overline{\text{FAULT}}$ floats and is disabled until VIN >2.5V. This output is pulled low after the OC timeout period has expired and stays latched until ENABLE is deasserted.
6, 7	OUT_2, 1	Channel 2,1 Controlled Supply Output	Channel voltage output, connect to load to protect. Upon an OC condition I_{OUT} is current limited to 1A. Current limit response time is within 200µs. This output will remain in current limit for a nominal 12ms before being latched off.

Absolute Maximum Ratings

Supply Voltage (VIN to GND). 6.0V
EN, FAULT . . . . . -0.3V to 6V
OUT . . . . . GND -0.3V to VIN 0.3V
Output Current . . . . . Short Circuit Protected
ESD Rating
Human Body Model (Per MIL-STD-883 Method 3015.7) 3KV

Thermal Information

Thermal Resistance (Typical, Note 1) θ_{JA} (°C/W)
8 Lead SOIC Package 96
Maximum Junction Temperature . . . . . 150°C
Maximum Storage Temperature Range . . . . . -65°C to 150°C
Maximum Lead Temperature (Soldering 10s) . . . . . 300°C
(SOIC - Lead Tips Only)

Operating Conditions

Temperature Range . . . . . -40°C to 85°C
Supply Voltage Range (Typical). . . . . 2.7V to 5.5V

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTES:

1. θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air. See Tech Brief TB379 for details.
2. All voltages are relative to GND, unless otherwise specified.

Electrical Specifications

Supply Voltages = 5V, $T_A = T_J$ = -40 to 85°C, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
POWER SWITCH						
ISL6119 On Resistance at 2.7V	$r_{DS(ON)_27}$	VIN = 2.7V I_{OUT} = 0.7A $T_A = T_J$ = 25°C	-	90	105	mΩ
		$T_A = T_J$ = 85°C	-	115	130	mΩ
ISL6119 On Resistance at 3.3V	$r_{DS(ON)_33}$	VIN = 3.3V, I_{OUT} = 0.7A $T_A = T_J$ = 25°C	-	80	100	mΩ
		$T_A = T_J$ = 85°C	-	115	130	mΩ
ISL6119 On Resistance at 5.0V	$r_{DS(ON)_50}$	VIN = 5V, I_{OUT} = 0.7A $T_A = T_J$ = 25°C	-	80	95	mΩ
		$T_A = T_J$ = 85°C	-	115	130	mΩ
Disabled Output Voltage	V_{OUT_DIS}	VIN = 5V, Switch Disabled, 50µA Load	-	300	450	mV
Vout Rising Rate	t_vout_rt	R_L = 10Ω, C_L = 0.1µF, 10%-90%	-	10	-	V/ms
Slow Vout Turn-off Rate	t_svout_offt	R_L = 10Ω, C_L = 0.1µF, 90%-10%	-	10	-	V/ms
Fast Vout Turn-off Rate	t_fvout_offt	R_L = 1Ω, C_L = 0.1µF, 90%-10%	-	4	-	V/µs
CURRENT CONTROL						
Current Limit, VIN = 3.3V - 5V	Ilim	Vout = 0.8V	0.75	1	1.25	A
OC Regulation Settling Time	$tsett_{Ilim}$	R_L = 5Ω, C_L = 0.1µF to Within 10% of CR	-	2	-	ms
Severe OC Regulation Settling Time	$tsett_{Ilim_sev}$	R_L< 1Ω, C_L = 0.1µF to Within 10% of CR	-	100	-	µs
Over Current Latch-off Time	t_{OC_loff}	ISL6119X, Tj = +25°C	-	10	-	ms
I/O PARAMETERS						
Fault Output Voltage	Vfault_hi	Fault I_{OUT} = 10mA	-	-	0.4	V
ENABLE High Threshold	Ven_vih	VIN = 5.5V	2.0	-	-	V
ENABLE Low Threshold at 2.7V	Ven_vil	VIN = 2.7V	-	-	0.6	V
ENABLE Low Threshold at 5.5V	Ven_vil	VIN = 5.5V	-	-	0.8	V
ENABLE Input Current	Ien_i	ENABLE = 0V to 5V, VIN = 5V, T_J > 25°C	-0.5	-	0.5	µA
BIAS PARAMETERS						
Enabled VIN Current	I_{VDD}	Switches Closed, OUTPUT = OPEN, T_J > 0°C	-	120	200	µA
Disabled VIN Current	I_{VDD}	Switches Open, OUTPUT = OPEN	-	1	5	µA
Undervoltage Lockout Threshold	V_{UVLO}	VIN Rising, Switch Enabled	1.7	2.25	2.5	V
UV Hysteresis	UV_{HYS}		50	100	-	mV
Over Temperature Disable	Temp_dis		-	150	-	°C

Introduction

The ISL6119 is a fully independent dual channel overcurrent (OC) fault protection IC for the +2.5V to +5.5V environment. Each ISL6119 incorporates in a single 8 lead SOIC package two 80mW N-channel MOSFET power switches for power control. Independent enabling inputs and fault reporting outputs compatible with 3V and 5V logic allows for external control and monitoring. This device features internal current monitoring, accurate current limiting, integrated power switches and current limited timed delay to latch-off for system protection. See Figure 1 for typical operational waveforms including both under and overcurrent situations.

Key Feature Description and Operation

UV Lock Out

The ISL6119 undervoltage lockout feature prevents functionality of the device unless the correct ENABLE state and VIN > 2.5V are present.

Soft Start

A constant 500nA current source ramps up the switch's gate causing a voltage follower effect on the output voltage. This provides a soft start turn-on eliminating bus voltage drooping caused by in-rush current charging heavy load capacitances. Rising and falling outputs are current limited voltage ramps so that both the inrush current and voltage slew rate are limited, independent of load. This reduces supply droop due to surge and also eliminates the need for EMI filters necessary on other IC products.

Fault Blanking On Start-Up

During initial turn-on the ISL6119 prevents nuisance faults being reported to the system controller by blanking the fault signal for 12ms. This blanking eliminates the need for external RC filters necessary for other vendor products that assert a fault signal upon initial turn-on into a temporary high current condition. See Figures 10 through 12 for waveform examples.

Current Regulation

The ISL6119 has integrated current sensing on the power MOSFET that allows for rapid control of OC events. Once an OC is detected the ISL6119 goes into its current regulation (CR) control mode. The ISL6119 CR level is set to a nominal 1A. This current regulation is ±25% over the full operating temperature and voltage bias range. See Figures 4 and 5 for illustrative curves. The speed of this control is inversely related to the magnitude of the OC fault. Thus a hard overcurrent is more quickly controlled than a marginal OC condition. See Figure 6 for waveforms illustrating this and Figure 7 for an accompanying graph.

Over Temperature Shutdown

Although the ISL6119 has a thermal shutdown feature, because of the 12ms timed shutdown this will only be invoked in extremely high ambient temperatures

Latch-Off Time Delay

The primary function of any OC protection device is to quickly isolate the voltage bus from a faulty load. Unlike many other IC products that sense the IC thermal condition (the monitored IC junction temperature depends on a number of factors the most important of which are power dissipation of the faulted and adjacent switches and package temp) to isolate a faulty load, the ISL6119 uses an internal 12ms timer that starts upon OC detection. Once an OC condition is detected the appropriate output is current limited for a maximum of 12ms to allow transient conditions to pass before latch-off. This time to latch-off is independent of device thermal or adjacent switch condition. See Figure 18 for waveforms illustrating independent latch-off.

If, after the ISL6119 has latched off, and the fault has asserted and, the enable is not deasserted but the OC condition still exists, the ISL6119 unlike other IC devices does not send to the controller a continuous string of fault pulses. The ISL6119's single fault signal is sent at the time of latch-off unlike other devices.

Slow And Fast Shutdown

The ISL6119 has two shutdown modes. When turned off with a load current less than the current regulation (CR) level the ISL6119 shuts down in a controlled manner using a 500nA constant current source controlled ramp. When latched off due to CR and the timer has expired, the ISL6119 quickly pulls down the output thereby quickly removing the faulted load from the voltage bus. See Figures 8 and 9 for waveforms of each mode.

Active Output Pulldown

Another unique ISL6119 feature is the active pull down on the outputs to 300mV above GND when the device is disabled. Competitors' parts' switch leakage causes the output voltage to drift up to VIN voltage even when the part is supposed to be disabled.

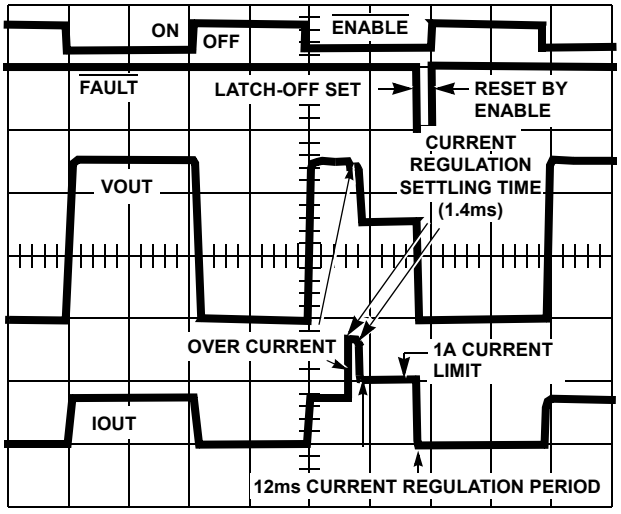


FIGURE 1. TYPICAL OPERATIONAL WAVEFORMS

Typical Performance Curves

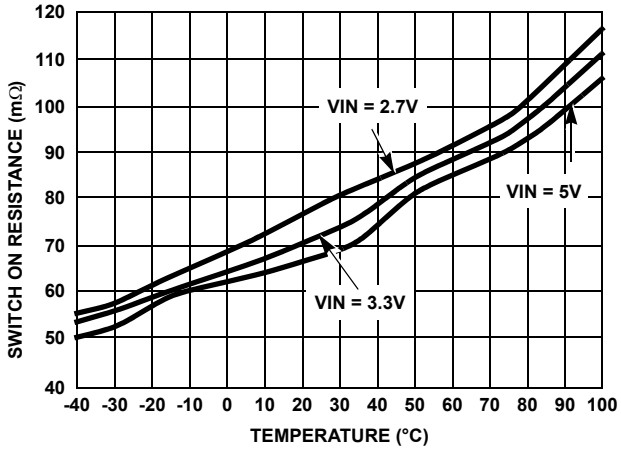


FIGURE 2. SWITCH ON RESISTANCE AT 0.7A

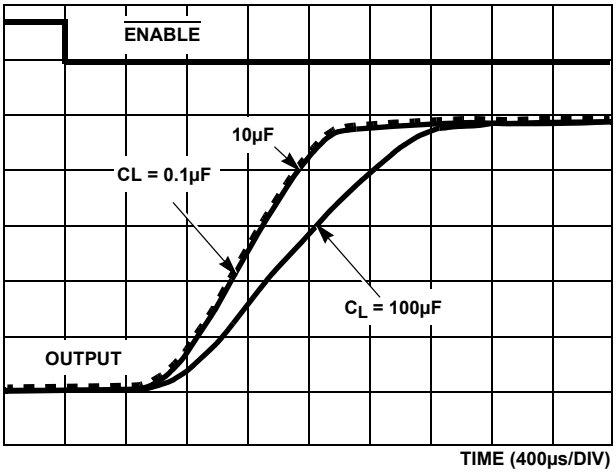


FIGURE 3. VOUT SOFT START vs C_{LOAD}, RI = 10Ω

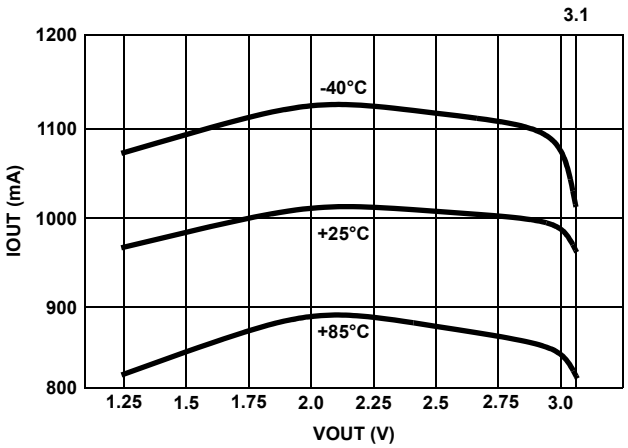


FIGURE 4. CURRENT REGULATION vs Vout (VIN = 3.3V)

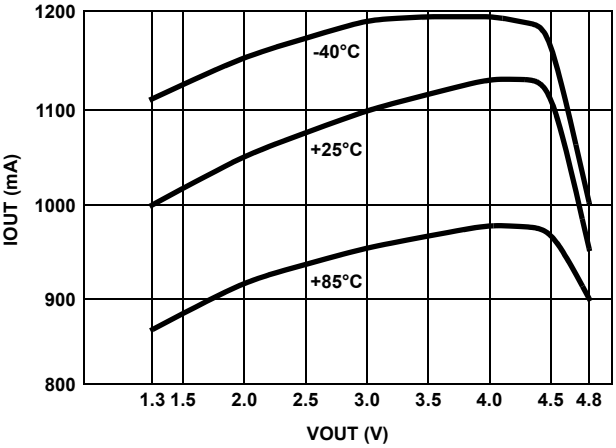


FIGURE 5. CURRENT REGULATION vs VOUT (VIN = 5.0V)

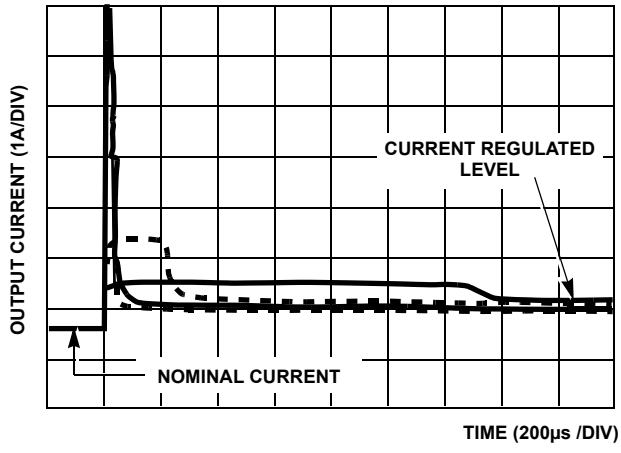


FIGURE 6. OC TO CR SETTLING TIME WAVEFORMS

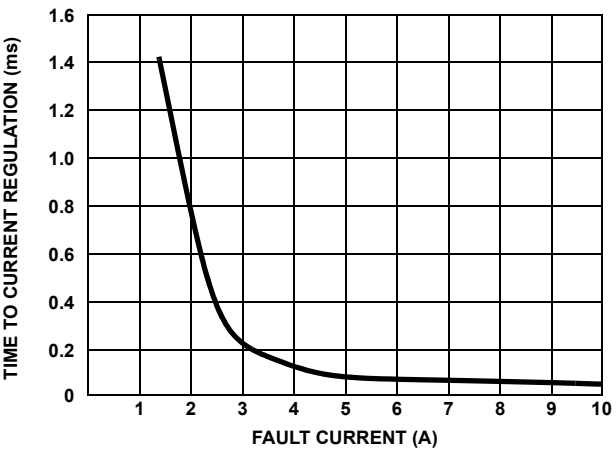


FIGURE 7. CR SETTLING TIME vs FAULT CURRENT

Typical Performance Curves (Continued)

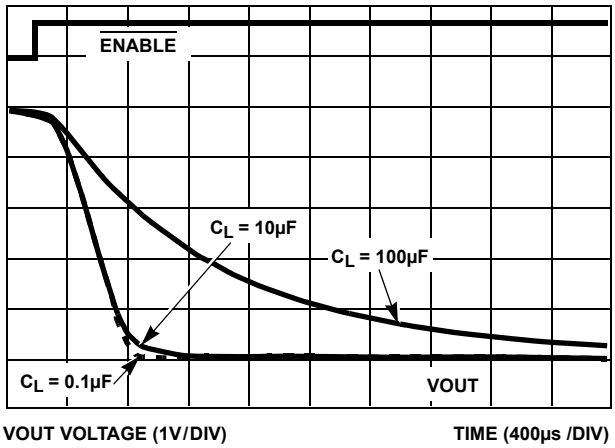


FIGURE 8. SLOW TURN -OFF vs C_{LOAD}, RI = 10Ω

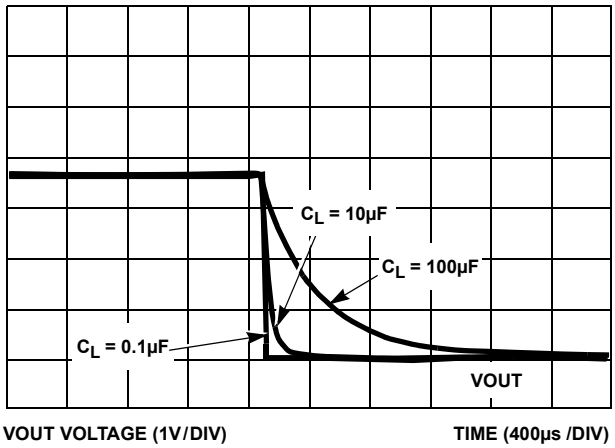


FIGURE 9. FAST TURN-OFF vs C_{LOAD}

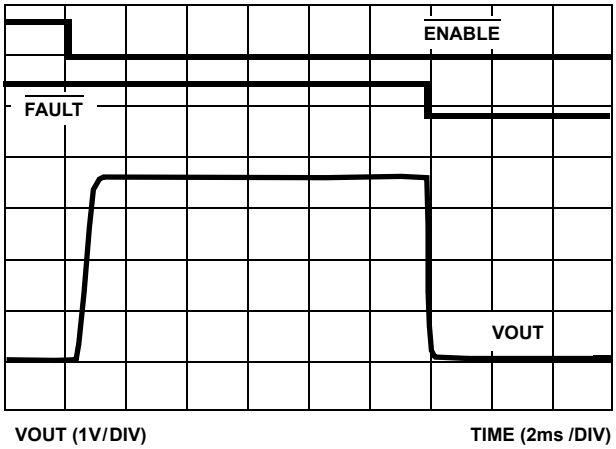


FIGURE 10. ISL6119L TURN-ON INTO 1.5A OCS

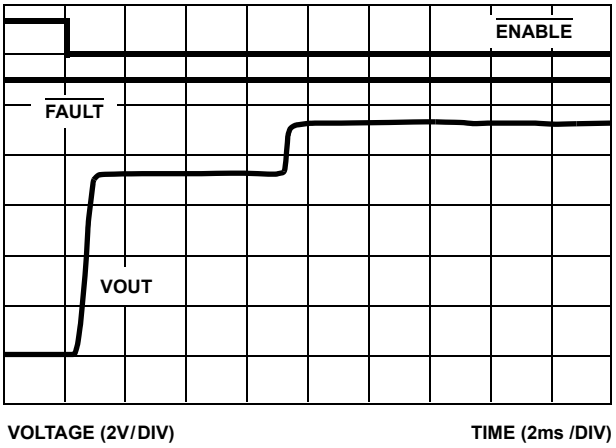


FIGURE 11. ISL6119L TURN-ON INTO 1.5A MOMENTARY OC

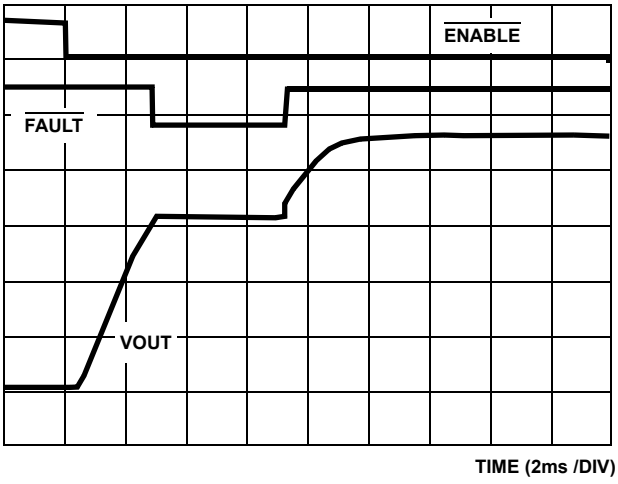


FIGURE 12. VENDOR IC TURN-ON INTO MOMENTARY OC

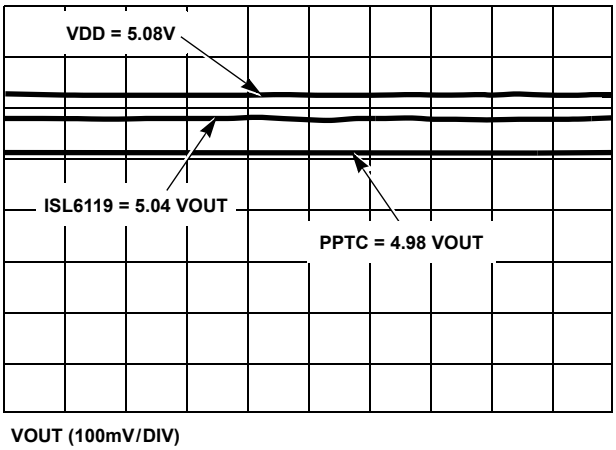


FIGURE 13. ISL6119 vs PPTC INTO 500mA LOAD

Typical Performance Curves (Continued)

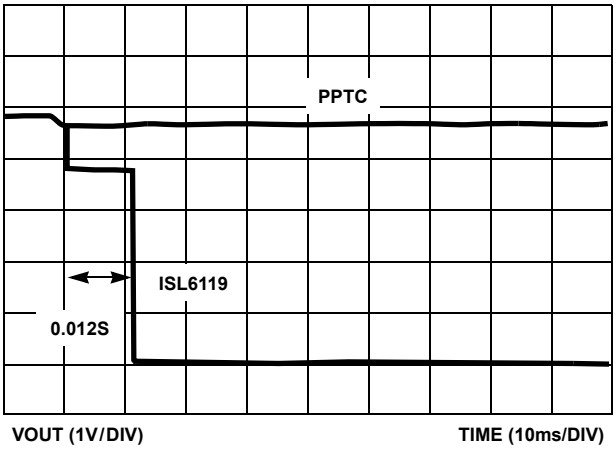


FIGURE 14. ISL6119 vs PPTC PLUGGED ONTO 1.5A LOAD

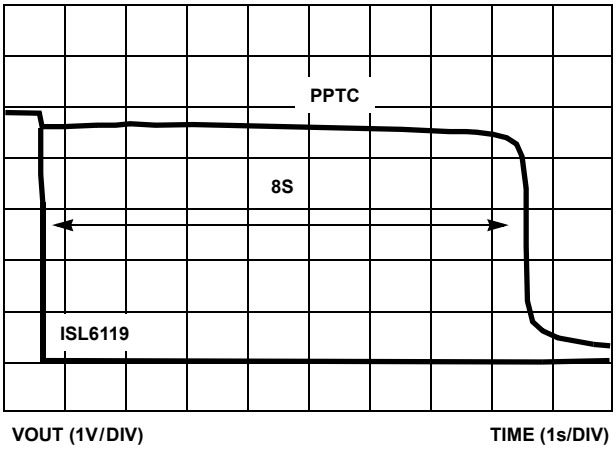


FIGURE 15. ISL6119 vs PPTC WITH EXTENDED 1.5A LOAD

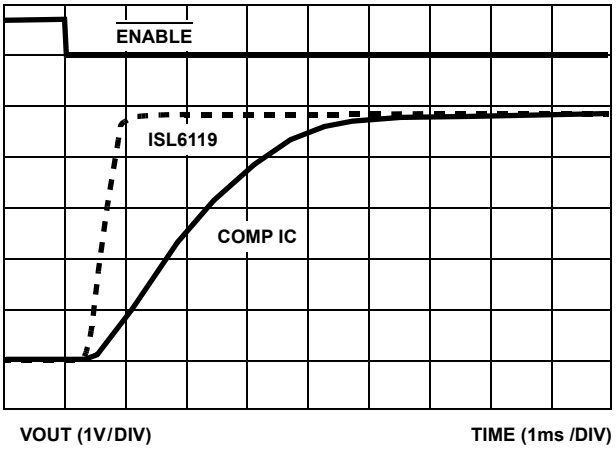


FIGURE 16. COMPARATIVE TURN-ON WAVEFORMS, RI = 10Ω

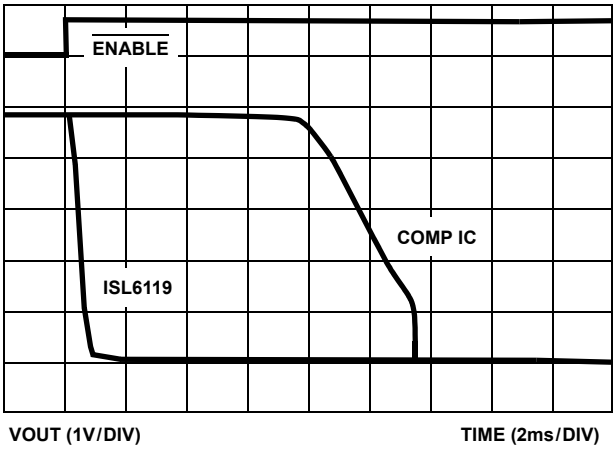


FIGURE 17. I COMPARATIVE TURN-OFF WAVEFORMS

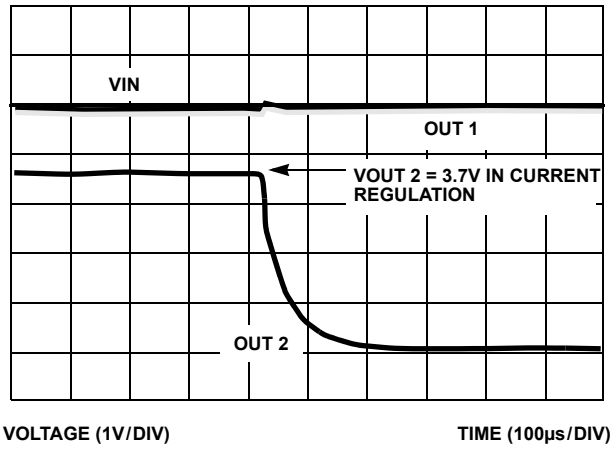


FIGURE 18. SWITCH FAULT INDEPENDENCE

Using the ISL6119EVAL1 Platform

General and Biasing Information

The ISL6119EVAL1 platform, Figure 19, allows evaluation of the ISL6119 dual power supply control IC and comparison against a suitably sized PPTC component.

The evaluation platform is biased and monitored through numerous test points (TP#). See Table 1 for test point assignments and descriptions.

TABLE 1. ISL6119EVAL1 TEST POINT ASSIGNMENTS

TP #	DESCRIPTION
TP1	Eval Board and IC Gnd
TP2	Eval Bd +5V Bias
TP3	Enable Switch 1
TP4	Enable Switch 2
TP5	Switch 2 Fault
TP6	Switch Out 2
TP7	Switch Out 1
TP8	Switch 1 Fault
TP9	IC VIN Pin
TP10	PPTC Load Side
TP11	Invoke Over Current

Upon proper bias the PPTC, F1 has a nominal 500mA load current passing through it which is the hold current rating for that particular device. Removal of the PPTC is necessary to isolate the ISL6119 as the PPTC load current is common to the ISL6119EVAL1 bias connections.

By enabling either or both of the ISL6119L switches by signaling TP3 and/or TP4 low (<0.6V) these switches are also loaded with a nominal 500mA current. See Figures 3 and 8 for typical ISL6119 turn-on and off waveforms.

Provided test points enable the evaluation of voltage loss across the PPTC (TP9 - TP10) and the ISL6119 enabled switches (TP9 - TP6 and TP7). Expect to see 50% - 300% greater voltage loss across typical PPTC devices than the ISL6119. See Figure 13 for a voltage loss comparison across ISL6119 and PPTC device.

An overcurrent (OC) condition can be invoked on both the ISL6119 and the PPTC by driving TP11 to +6V, causing SW1 to close and a nominal 1.5A load is imposed. This represents a current over load to the ISL6119 and is thus quickly current regulated to the 1A limit. If the OC duration extends beyond the nominal 12ms of the internal ISL6119L timer then the output is latched off and the fault output is asserted by being pulled low turning on the appropriate FAULT LED, see Figure 10. (Please note: the labeling for FAULT-1 and FAULT-2 is reversed). The eval board is designed to only invoke an OC condition on channel 2 (TP4) so that a channel to channel isolation evaluation in the presence of an OC condition can be evaluated. See Figure 18.

The primary function of any OC protection device is to quickly isolate the voltage bus from a faulty load. Unlike the PPTC and other vendor available IC products, the ISL6119 internal timer that starts upon OC detection provides consistent protection that is not temperature dependent. See Figures 14 and 15 for a comparison of the time to protection offered by the ISL6119 vs the PPTC. Figure 14 illustrates the ISL6119 timed latch-off of 12ms with a 1.5A load and Figure 15 shows the 8 second latch-off of the PPTC at approximately its trip current rating of 1.5A.

Using the ISL6119USBEVAL1 Platform

General and Biasing Information

The ISL6119USBEVAL1 platform, Figure 20, allows evaluation of the ISL6119 dual power supply control IC in a USB environment.

The evaluation platform is biased and monitored through numerous test points (TP#). See Table 2 for test point assignments and descriptions.

TABLE 2. ISL6119USBEVAL1 TEST POINT ASSIGNMENTS

TP #	DESCRIPTION
TP1	Eval Board and IC Gnd
TP2	Eval Bd +5V Bias
TP3	Enable Switch 1
TP4	Enable Switch 2
TP5	Switch 1 Fault
TP8	Switch 2 Fault

Upon proper bias the ISL6119L is held off through pull up resistors on the enable pins and is enabled by signaling either or both of the ISL6119L switches TP3, and/or TP4 low (<0.6V).

The USB connector is provided so that either test loads or USB peripherals can be powered. In addition, differential signalling (D+ and D-) access points are provided for each output port so that I/O activity can also be conducted in a prototype environment.

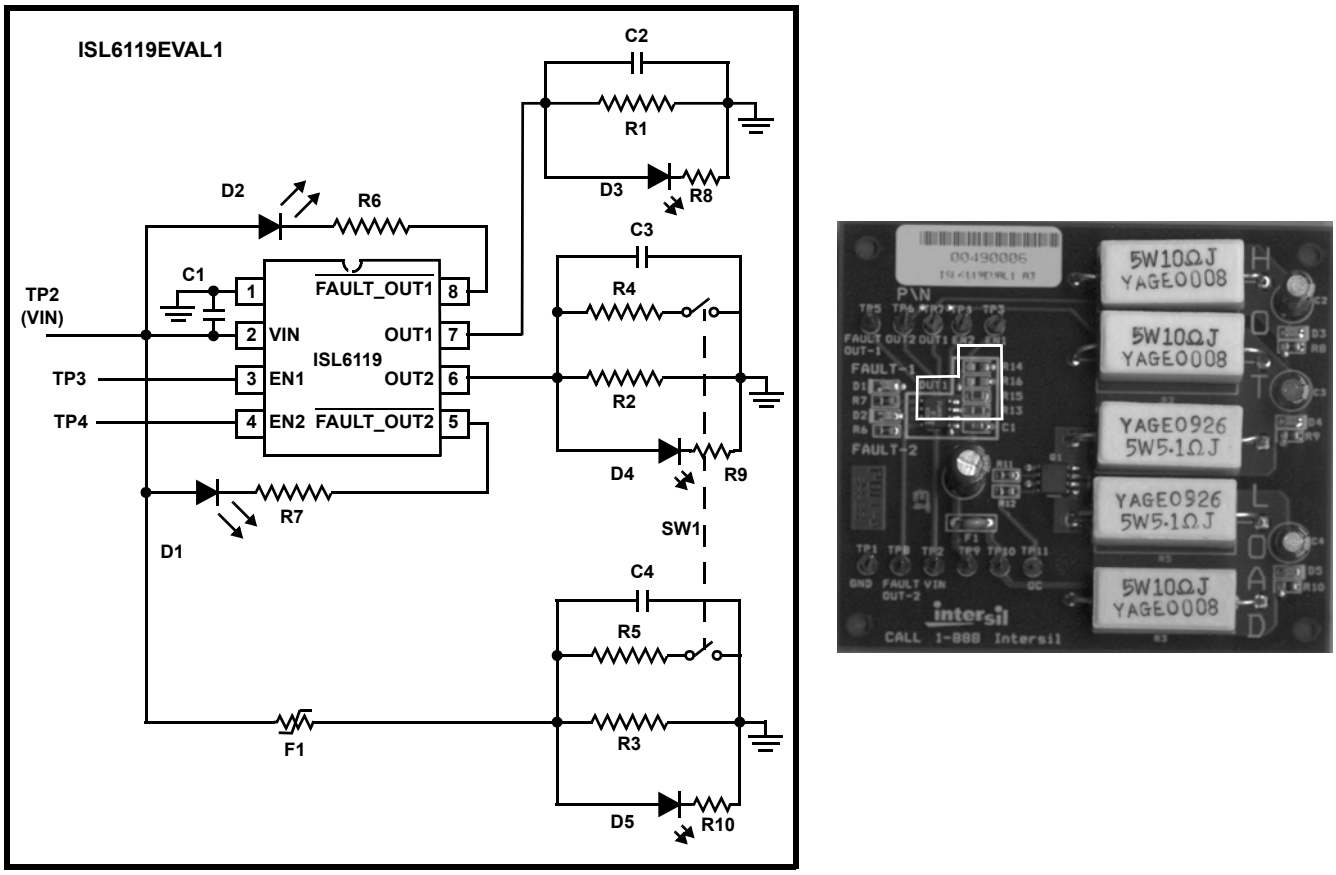


FIGURE 19. ISL6119EVAL1 BOARD SCHEMATIC AND PHOTOGRAPH

TABLE 3. ISL6119EVAL1 BOARD COMPONENT LISTING

COMPONENT DESIGNATOR	COMPONENT FUNCTION	COMPONENT DESCRIPTION
DUT1	ISL6119	Intersil, ISL6119LIB 3.3V Aux HotPlug Controller
R1 - R3	500mA Nominal Load Resistors	YAGEO, 10Ω, 5%, 5W, 10W-5-ND
R4 - R5	1.5A Current Over Load Resistors	YAGEO, 5Ω, 5%, 5W, 5W-5-ND
R6 - R10	LED Current Limiting Resistor	470Ω, 0805
C1	Decoupling Capacitor	0.1μF, 0805
C2 - C4	Load Capacitor	10μF 16V Electrolytic, Radial Lead
D1 - D5	Indicating LEDs	0805, SMD LEDs Red
F1	PPTC (Polymer Positive Temperature Coefficient)	Raychem, Poly Switch, RXE075 or Equivalent
SW1 (Q1)	Current Over Load Invoking Switch Access TP11	Intersil, ITF86110DK8T, 7.5A, 30V, 0.025Ω, Dual N-channel, Logic Level Power MOSFET

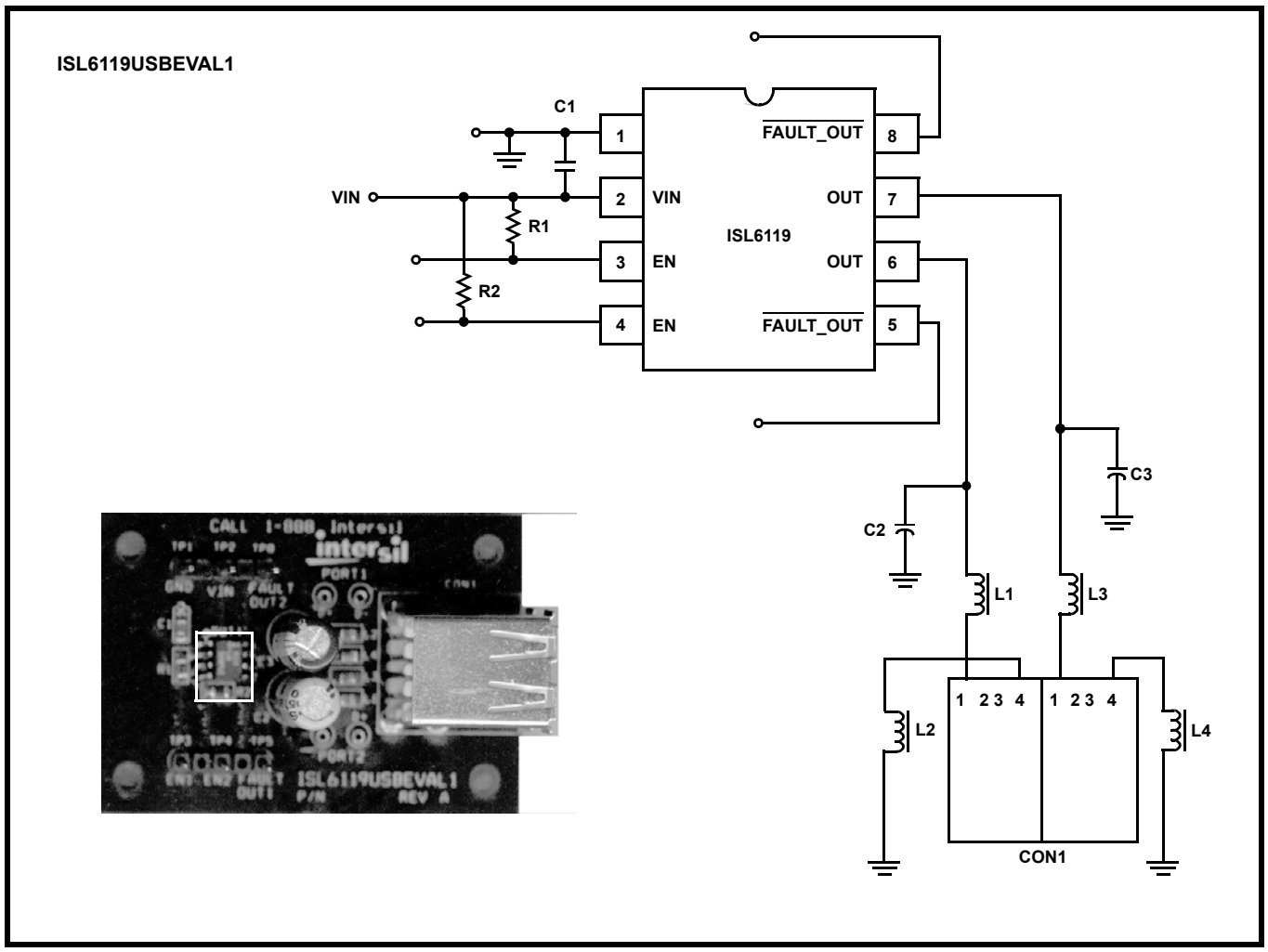


FIGURE 20. ISL6119USBEVAL BOARD

TABLE 4.

COMPONENT DESIGNATOR	COMPONENT NAME	COMPONENT DESCRIPTION
ISL6119USBEVAL1		
DUT1	ISL6119L	Intersil, ISL6119L 5V USB HotPlug Controller
C1	Chip Decoupling Capacitor	0.1µF, 0805
C2 - C3	V+ Decoupling Capacitors	100µF 16V Electrolytic, Radial Lead
L1 - L4	V+ And GND Stability Inductors	220nH, 0805 (OPTIONAL FOR IMPLEMENTATION)
CON1	Dual Stacked USB Type A Connector	ASSMANN, AU-Y1008 or Equiv
R1 - R2	Pull-Up Resistors	1.2Ωk, 0805

Implementing Autoreset on the ISL6119 Hot Swap Controller

Abstract

In applications where the cost, complexity or requirement for a system controller is avoided and an autonomous power control function is desired, a device that can monitor and protect against excessive current failures is needed. This tech brief shows how to implement such an autonomous controller using the ISL6119HIB. This application works only with the ‘H’ version of this device. The ‘H’ version refers to the enable function being asserted upon a high input.

Introduction

The ISL6118, ISL6119 and ISL6121 are all 2.5V to 5V power supply controllers, each having a different level of current regulation (CR). The ISL6118 and ISL6119 have 2 independent controllers with CR levels of 0.6A and 1.0A respectively whereas the ISL6121 is a single supply controller with a 2A CR level. Each of these devices features integrated power switch(es) for power control. Each switch is driven by a constant current source giving a controlled ramp up of the output voltage. This provides a soft start turn-on eliminating bus voltage drooping caused by in-rush current while charging heavy load capacitances. The independent enabling inputs and fault reporting outputs for each channel are available and necessary for the autonomous autoreset application.

The undervoltage (UV) feature prevents turn-on of the outputs unless the ENABLE pin and VIN are > 2.5V. During initial turn-on the ISL6119 prevents fault reporting by blanking the fault signal. Rising and falling outputs are current-limited voltage ramps so that both the inrush current and voltage slew rate are limited, independent of load. This reduces supply droop due to surge and eliminates the need for external EMI filters. During operation, once an OC condition is detected the appropriate output is current limited to the appropriate level for 10ms to allow transient conditions to pass. If still in current limit after the current limit period has elapsed, the output is latched off and the fault is reported by pulling the corresponding $\overline{\text{FAULT}}$ low. The $\overline{\text{FAULT}}$ signal is latched low until reset by the ENABLE signal being de-asserted at which time the $\overline{\text{FAULT}}$ signal will clear.

It is this described sequence of events that allows for the autoreset function to be implemented in a cost efficient manner requiring the addition of only an RC network per channel to the typical application.

Figure 21 illustrates the RC network needed with suggested component values and the configuration of the relevant pins for each autoreset channel.

Description of Operation

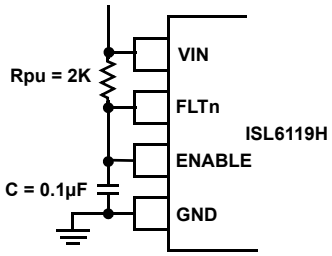


FIGURE 21.

Initially as voltage is applied to VIN, the pull up resistor (Rpu) provides for pull up to VIN on both the ENABLE pin asserting the output once VIN > 2.5V and on the FLTn pin. Once turned on and an overcurrent (OC) condition occurs the IC provides CR protection for 10ms and then the FLTn pin pulls low through Rpu and also pulling the ENABLE low thus resetting the device fault condition. At this time the Rpu charges the cap and the voltage on the ENABLE/FLTn node rises until the ENABLE > 2.0 and the output is asserted on once again. This automatic reset cycle will continue until the OC fault no longer exists on the output. After several seconds in this mode of operation the IC thermal protection invokes adjusting the timing of the on-off cycle to prevent excessive thermal dissipation in the power switch protecting itself and surrounding circuitry. See Figure 22 for operation waveform.

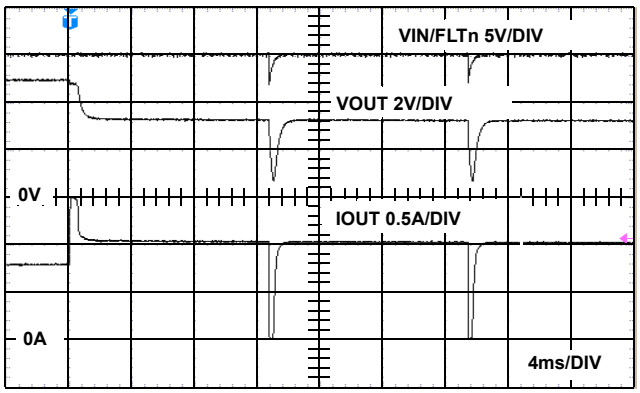
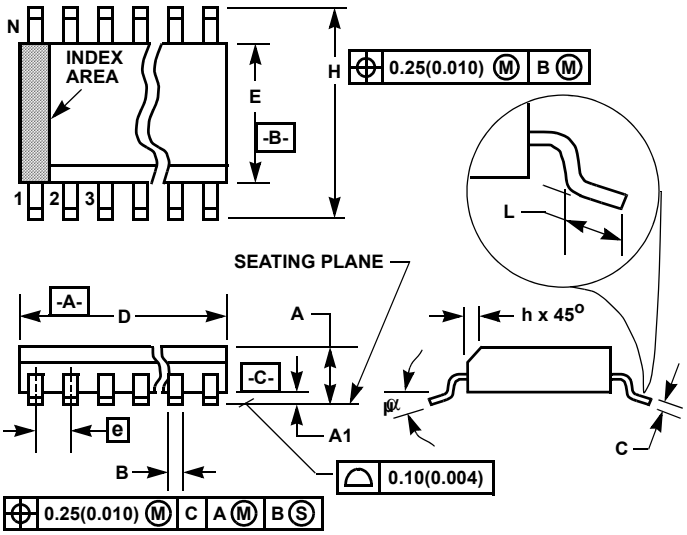


FIGURE 22. AUTO RESET OPERATION

Applications

- USB
- 2.5V to 5V up to 10W power port protection

Small Outline Plastic Packages (SOIC)



NOTES:

1. Symbols are defined in the “MO Series Symbol List” in Section 2.2 of Publication Number 95.
2. Dimensioning and tolerances per ANSI Y14.5M-1982.
3. Dimension “D” does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension “E” does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. “L” is the length of terminal for soldering to a substrate.
7. “N” is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. The lead width “B”, as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch).
10. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.

M8.15 (JEDEC MS-012-AA ISSUE C)
8 LEAD NARROW BODY SMALL OUTLINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.0532	0.0688	1.35	1.75	-
A1	0.0040	0.0098	0.10	0.25	-
B	0.013	0.020	0.33	0.51	9
C	0.0075	0.0098	0.19	0.25	-
D	0.1890	0.1968	4.80	5.00	3
E	0.1497	0.1574	3.80	4.00	4
e	0.050 BSC		1.27 BSC		-
H	0.2284	0.2440	5.80	6.20	-
h	0.0099	0.0196	0.25	0.50	5
L	0.016	0.050	0.40	1.27	6
N	8		8		7
α	0°	8°	0°	8°	-

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