Multichannel, 24-Bit, 192 kHz, Σ-Δ DAC

AD1833

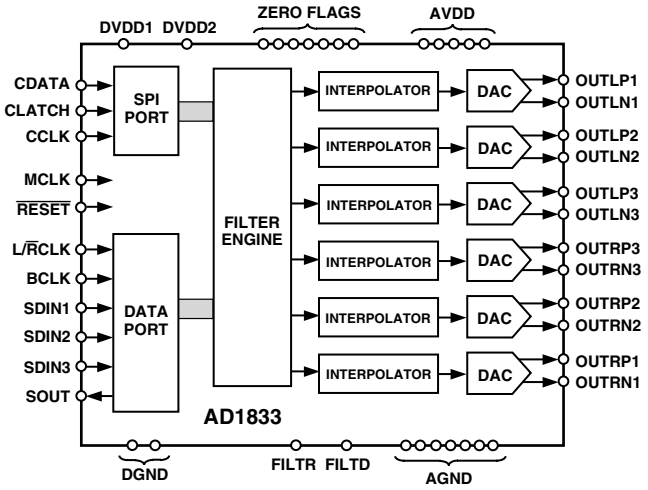
FEATURES

- 5 V Stereo Audio System with 3.3 V Tolerant Digital Interface
- Supports 96 kHz Sample Rates on Six Channels and 192 kHz on 2 Channels
- Supports 16-/20-/24-Bit Word Lengths
- Multibit Sigma-Delta Modulators with "Perfect Differential Linearity Restoration" for Reduced Idle Tones and Noise Floor
- Data Directed Scrambling DACs—Least Sensitive to Jitter
- Differential Output for Optimum Performance
- DACs Signal-to-Noise and Dynamic Range: 110 dB
- –94 dB THD + N—6-Channel Mode
- –95 dB THD + N—2-Channel Mode
- On-Chip Volume Control Per Channel with 1024-Step Linear Scale
- Software Controllable Clickless Mute
- Digital De-Emphasis Processing
- Supports 256 × f_S, 512× f_S, and 768× f_S Master Clock Modes
- Power-Down Mode Plus Soft Power-Down Mode
- Flexible Serial Data Port with Right-Justified, Left-Justified, I^2S-Compatible and DSP Serial Port Modes
- Supports Packed Data Mode (TDM) for DACs
- 48-Lead LQFP Plastic Package

APPLICATIONS

- DVD Video and Audio Players
- Home Theatre Systems
- Automotive Audio Systems
- Set-Top Boxes
- Digital Audio Effects Processors

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD1833 is a complete, high-performance, single-chip, multichannel, digital audio playback system. It features six audio playback channels each comprising a high-performance digital interpolation filter, a multibit sigma-delta modulator featuring Analog Devices patented technology and a continuous-time voltage-out analog DAC section. Other features include an on-chip clickless attenuator and mute capability, per channel, programmed through an SPI-compatible serial control port.

The AD1833 is fully compatible with all known DVD formats, catering for up to 24-bit word lengths at sample rates of 48 kHz and 96 kHz on all six channels while supporting a 192 kHz sample rate on two channels. It also provides the "Redbook" standard 50 µs/15 µs digital de-emphasis filters at sample rates of 32 kHz, 44.1 kHz, and 48 kHz.

The AD1833 has a very flexible serial data input port that allows for glueless interconnection to a variety of ADCs, DSP chips, AES/EBU receivers, and sample rate converters. The AD1833 can be configured in left-justified, I^2S, right-justified, or DSP serial port compatible modes. The AD1833 accepts serial audio data in MSB first, two's complement format. While the AD1833 can be operated from a single 5 V power supply, it also features a separate supply pin for its digital interface which allows the device to be interfaced to devices using 3.3 V power supplies.

It is fabricated on a single monolithic integrated circuit and is housed in a 48-lead LQFP package for operation over the temperature range –40°C to +85°C.

REV. 0

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AD1833–SPECIFICATIONS

TEST CONDITIONS UNLESS OTHERWISE NOTED

Supply Voltages (AV_{DD}, DV_{DD})	5.0 V
Ambient Temperature	25°C
Input Clock	12.288 MHz, (256 × f_S Mode)
Input Signal	Nominally 1 kHz, 0 dBFS (Full Scale)
Input Sample Rate	48 kHz
Measurement Bandwidth	20 Hz to 20 kHz
Word Width	24 Bits
Load Capacitance	500 pF
Load Impedance	10 kΩ

NOTES
Performance of all channels are identical (exclusive of the Interchannel Gain Mismatch and Interchannel Phase Deviation specifications).
Specifications subject to change without notice.

Parameter	Min	Typ	Max	Unit	Test Conditions
ANALOG PERFORMANCE					
DIGITAL-TO-ANALOG CONVERTERS					
Dynamic Range (20 Hz to 20 kHz, –60 dBFS Input)					
With A-Weighted Filter	106.5	110		dB	
		110.5		dB	f_S = 96 kHz
Total Harmonic Distortion + Noise		–95	–89	dB	Two Channels Active
		–94		dB	Six Channels Active
		–95		dB	96 kHz, Two Channels Active
		–94		dB	96 kHz, Six Channels Active
SNR		110		dB	
Interchannel Isolation		108		dB	
DC Accuracy					
Gain Error		±3.0		%	
Interchannel Gain Mismatch		0.2		%	
Gain Drift		80		ppm/°C	
Interchannel Crosstalk (EIAJ Method)		–120		dB	
Interchannel Phase Deviation		±0.1		Degrees	
Volume Control Step Size (1023 Linear Steps)		0.098		%	
Volume Control Range (Max Attenuation)		63.5		dB	
Mute Attenuation		–120		dB	
De-Emphasis Gain Error		±0.1		dB	
Full-Scale Output Voltage at Each Pin (Single-Ended)		1.0 (2.8)		V rms (V p-p)	
Output Resistance Measured Differentially		150		Ω	
Common-Mode Output Volts		2.2		V	
DAC INTERPOLATION FILTER—48 kHz					
Pass Band			20	kHz	
Pass Band Ripple		±0.01		dB	
Stop Band	24			kHz	
Stop Band Attenuation	70			dB	
Group Delay		510		µs	
DAC INTERPOLATION FILTER—96 kHz					
Pass Band			37.7	kHz	
Pass Band Ripple		±0.03		dB	
Stop Band	55.034			kHz	
Stop Band Attenuation	70			dB	
Group Delay		160		µs	
DAC INTERPOLATION FILTER—192 kHz					
Pass Band			89.954	kHz	
Pass Band Ripple		±1		dB	
Stop Band	104.85			kHz	
Stop Band Attenuation	70			dB	
Group Delay		140		µs	

Parameter	Min	Typ	Max	Unit	Test Conditions
DIGITAL I/O					
Input Voltage HI	3.0			V	
Input Voltage LO			0.8	V	
Output Voltage HI	$DV_{DD2} - 0.4$			V	
Output Voltage LO			0.4	V	
POWER SUPPLIES					
Supply Voltage (AV_{DD} and DV_{DD1})	4.5	5.0	5.5	V	
Supply Voltage (DV_{DD2})	3.3		DV_{DD1}	V	
Supply Current I_{ANALOG}		38.5	42	mA	
Supply Current $I_{DIGITAL}$		42	45.5	mA	Active
		2		mA	Power-Down
Power Supply Rejection Ratio					
1 kHz 300 mV p-p Signal at Analog Supply Pins		–60		dB	
20 kHz 300 mV p-p Signal at Analog Supply Pins		–50		dB	

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*
(T_A = 25°C unless otherwise noted)

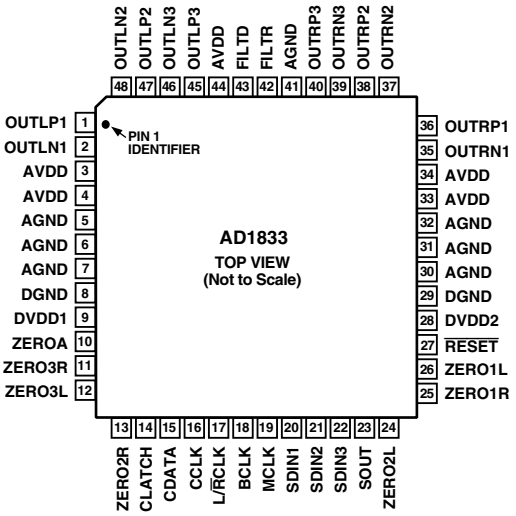
AV_{DD}, DV_{DDx} to AGND, DGND . . . . . –0.3 V to +6.5 V
AGND to DGND . . . . . –0.3 V to +0.3 V
Digital I/O Voltage to DGND . . . . . –0.3 V to DV_{DD2} + 0.3 V
Analog I/O Voltage to AGND . . . . . –0.3 V to AV_{DD} + 0.3 V
Operating Temperature Range
Industrial (A Version) . . . . . –40°C to +85°C
Storage Temperature Range . . . . . –65°C to +150°C
Maximum Junction Temperature . . . . . 150°C
LQFP, θ_{JA} Thermal Impedance . . . . . 91°C/W
Lead Temperature, Soldering
Vapor Phase (60 sec) . . . . . 215°C
Infrared (15 sec) . . . . . 220°C

*Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Only one absolute maximum rating may be applied at any one time.

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
AD1833AST	–40°C to +85°C	Thin Plastic Quad Flatpack	ST-48
EVAL-AD1833EB		Evaluation Board	

PIN CONFIGURATION



CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD1833 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high-energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

DIGITAL TIMING (Guaranteed over –40°C to +85°C, AV_{DD} = DV_{DD} = 5.0 V ± 10%)

		Min	Unit
t_{DML}	MCLK LO Pulsewidth (All Modes)	15	ns
t_{DMH}	MCLK HI Pulsewidth (All Modes)	15	ns
t_{DBH}	BCLK HI Pulsewidth	15	ns
t_{DBL}	BCLK LO Pulsewidth	15	ns
t_{DLS}	LRCLK Setup	5	ns
t_{DLH}	LRCLK Hold (DSP Serial Port Mode Only)	10	ns
t_{DDS}	SDATA Setup	5	ns
t_{DDH}	SDATA Hold	15	ns
t_{PDRP}	PD/RST LO Pulsewidth	10	ns
t_{CCH}	CCLK HI Pulsewidth	10	ns
t_{CCL}	CCLK LO Pulsewidth	10	ns
t_{CSU}	CDATA Setup Time	5	ns
t_{CHD}	CDATA Hold Time	10	ns
t_{CLH}	CLATCH HI Pulsewidth	10	ns

Specifications subject to change without notice.

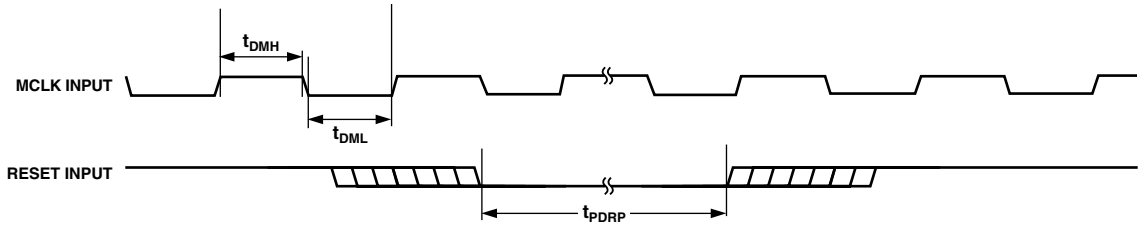


Figure 1. MCLK and $\overline{RESET}$ Timing

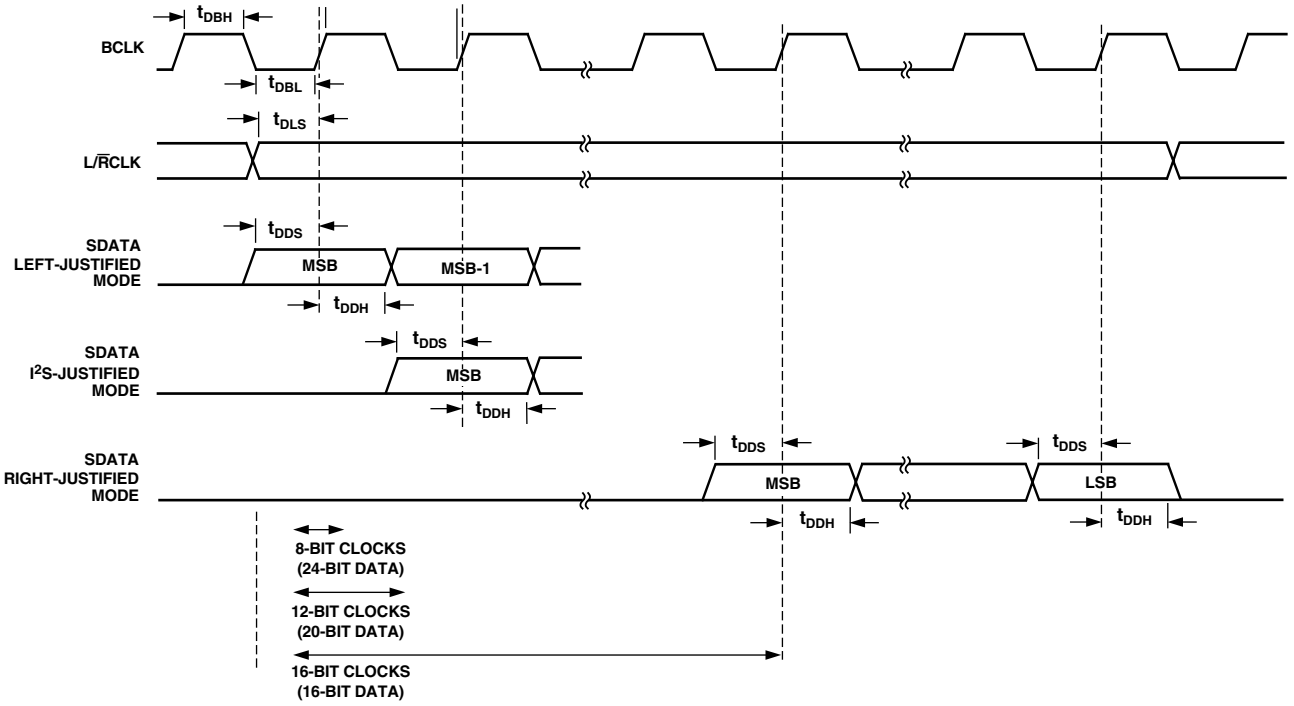


Figure 2. Serial Data Port Timing

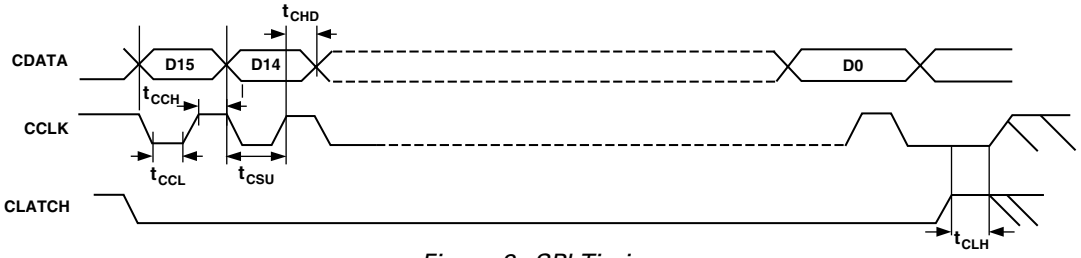
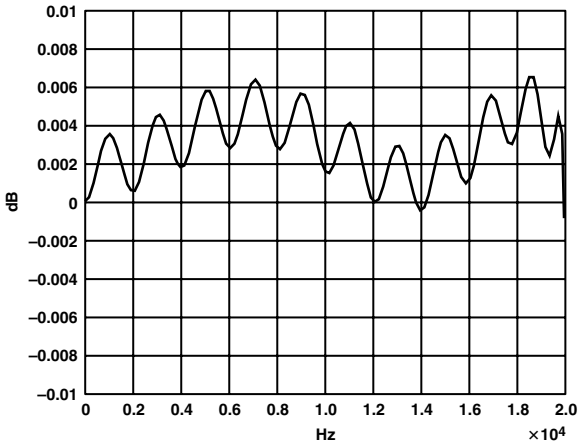


Figure 3. SPI Timing

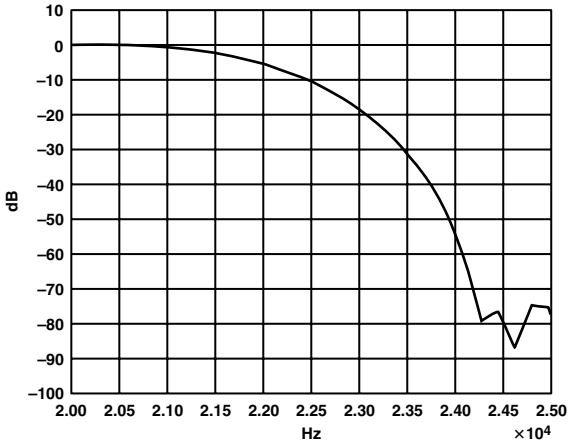
PIN FUNCTION DESCRIPTIONS

Pin	Mnemonic	IN/OUT	Description
1	OUTLP1	O	DAC 1 Left Channel Positive Output.
2	OUTLN1	O	DAC 1 Left Channel Negative Output.
3, 4, 33, 34, 44	AVDD		Analog Supply.
5, 6, 7, 30, 31, 32, 41	AGND		Analog Ground.
8, 29	DGND		Digital Ground.
9	DVDD1		Digital Supply to Core Logic.
10	ZEROA	O	Flag to Indicate Zero Input on All Channels.
11	ZERO3R	O	Flag to Indicate Zero Input on Channel 3 Right.
12	ZERO3L	O	Flag to Indicate Zero Input on Channel 3 Left.
13	ZERO2R	O	Flag to Indicate Zero Input on Channel 2 Right.
14	CLATCH	I	Latch Input for Control Data (SPI Port).
15	CDATA	I	Serial Control Data Input (SPI Port).
16	CCLK	I	Clock Input for Control Data (SPI Port).
17	L/$\overline{R}$CLK	I/O	Left/Right Clock for DAC Data Input (FSTDM Output in TDM Mode).
18	BCLK	I/O	Bit Clock for DAC Data Input (BCLKTDM Output in TDM Mode).
19	MCLK	I	Master Clock Input.
20	SDIN1	I	Data Input for Channel 1 Left/Right (Data Stream Input in TDM and Packed Modes).
21	SDIN2	I/O	Data Input for Channel 2 Left/Right (L/$\overline{R}$CLK Output to Auxiliary DAC in TDM Mode).
22	SDIN3	I/O	Data Input for Channel 3 Left/Right (BCLK Output to Auxiliary DAC in TDM Mode).
23	SOUT	O	Auxiliary I^2S Output (Available in TDM Mode).
24	ZERO2L	O	Flag to Indicate Zero Input on Channel 2 Left.
25	ZERO1R	O	Flag to Indicate Zero Input on Channel 1 Right.
26	ZERO1L	O	Flag to Indicate Zero Input on Channel 1 Left.
27	$\overline{RESET}$	I	Power-Down and Reset Control.
28	DVDD2		Power Supply to External Interface Logic.
35	OUTRN1	O	DAC 1 Right Channel Negative Output.
36	OUTRP1	O	DAC 1 Right Channel Positive Output.
37	OUTRN2	O	DAC 2 Right Channel Negative Output.
38	OUTRP2	O	DAC 2 Right Channel Positive Output.
39	OUTRN3	O	DAC 3 Right Channel Negative Output.
40	OUTRP3	O	DAC 3 Right Channel Positive Output.
42	FILTR		Reference/Filter Capacitor Connection. Recommend 10 µF/100 µF Decouple to Analog Ground.
43	FILTD		Filter Capacitor Connection. Recommend 10 µF/100 µF Decouple to Analog Ground.
45	OUTLP3	O	DAC 3 Left Channel Positive Output.
46	OUTLN3	O	DAC 3 Left Channel Negative Output.
47	OUTLP2	O	DAC 2 Left Channel Positive Output.
48	OUTLN2	O	DAC 2 Left Channel Negative Output.

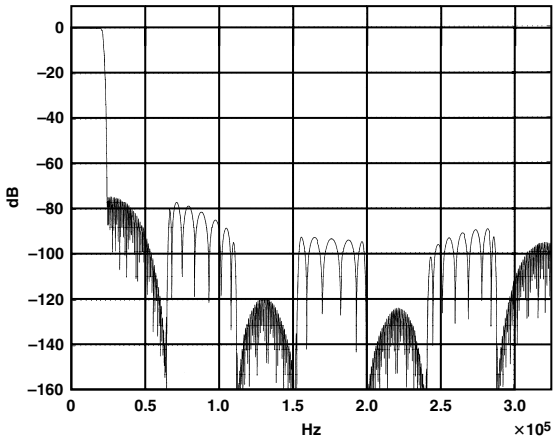
AD1833–Typical Performance Characteristics



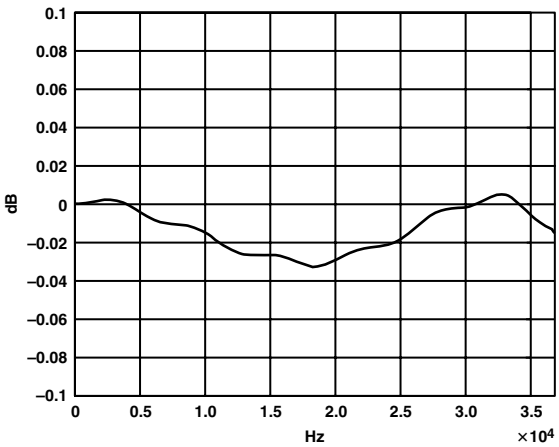
TPC 1. Pass Band Response, 8× Mode



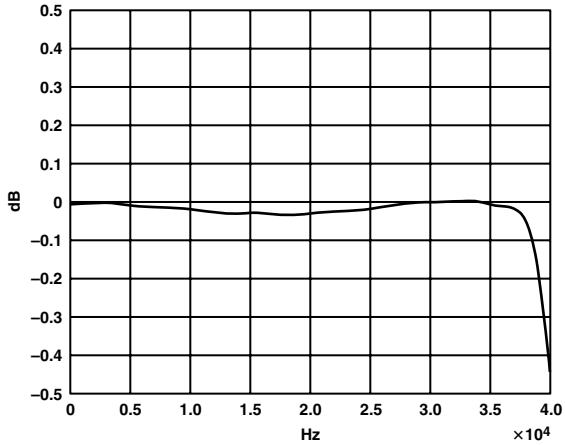
TPC 2. Transition Band Response, 8× Mode



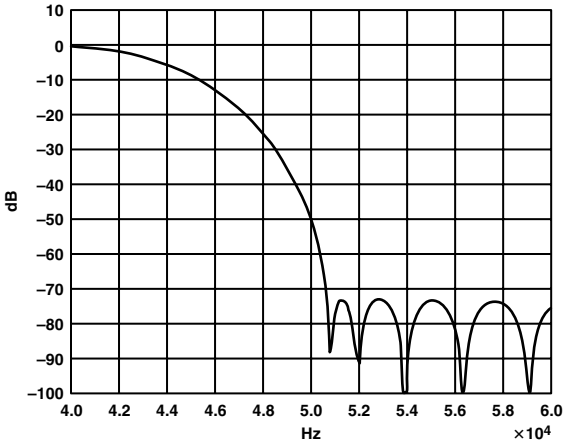
TPC 3. Complete Response, 8× Mode



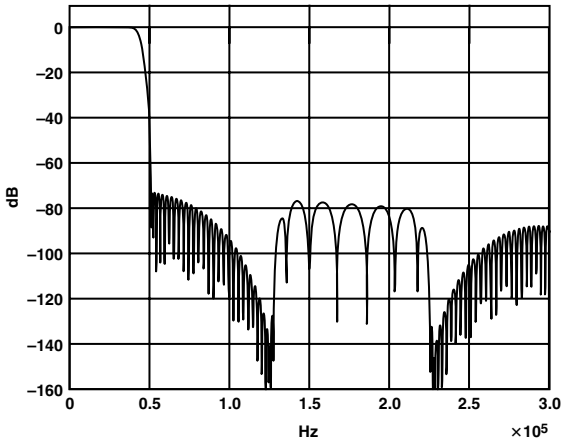
TPC 4. Pass Band Response, 4× Mode



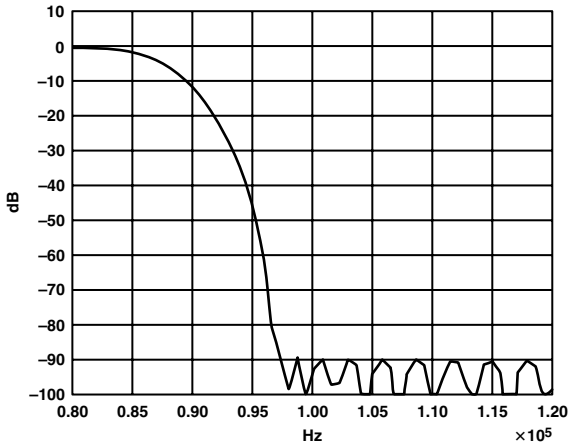
TPC 5. 40 kHz Pass Band Response, 4× Mode



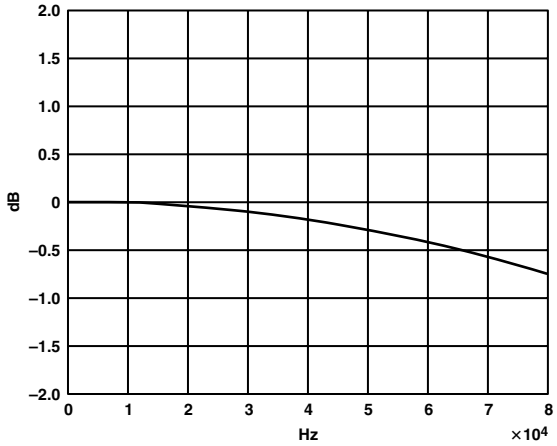
TPC 6. Transition Band Response, 4× Mode



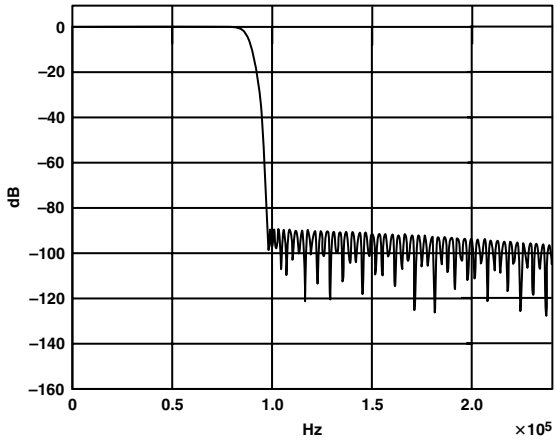
TPC 7. Complete Response, 4× Mode



TPC 9. Transition Band Response, 2× Mode



TPC 8. 80 kHz Pass Band Response, 2× Mode



TPC 10. Complete Response, 2× Mode

FUNCTIONAL DESCRIPTION

Device Architecture

The AD1833 is a 6-channel audio DAC featuring multibit Sigma-Delta (Σ-Δ) technology. The AD1833 features three stereo converters (giving six channels) where each stereo channel is controlled by a common bit-clock (BCLK) and synchronization signal (L/$\overline{R}$CLK).

Interpolator

The interpolator consists of up to three stages of sample rate doubling and half-band filtering followed by a 16 sample zero order hold. The sample rate doubling is achieved by zero stuffing the input samples, and a digital half band filter is then used to remove any images above the band of interest and to bring the zero samples to their correct values.

By selecting different input sample rates, one, two, or all three stages of doubling may be switched in. This allows for three different sample rate inputs. All three doubling stages are used with the 48 kHz input sample rate, with the 96 kHz input sample rate only two doubling stages are used, and with the 192 kHz input sample rate only one doubling stage is used. In each case the input sample frequency is increased to 384 kHz. The Zero-Order Hold (ZOH) holds the interpolator samples for upsampling by the modulator. This is done at a rate 16 times the interpolator output sample rate.

Modulator

The modulator is a 6-bit, second-order implementation and uses data scrambling techniques to achieve perfect linearity. The modulator samples the output of the interpolator stage(s) at a rate of 6.144 MHz.

OPERATING FEATURES

SPI Register Definitions

The SPI port allows flexible control of the devices' programmable functions. It is organized around nine registers; six individual channel VOLUME registers and three CONTROL registers. Each WRITE operation to the AD1833 SPI control port requires 16 bits of serial data in MSB-first format. The four most significant bits are used to select one of nine registers (seven register addresses are reserved), and the bottom 10 bits are then written to that register. This allows a write to one of the nine registers in a single 16-bit transaction. The SPI CCLK signal is used to clock in the data. The incoming data should change on the falling edge of this signal and remain valid during the rising edge. At the end of the 16 CCLK periods, the CLATCH signal should rise to latch the data internally into the AD1833. See Figure 2.

The serial interface format used on the Control Port utilizes a 16-bit serial word as shown in Table I. The 16-bit word is divided into several fields: Bits 15–12 define the register address, Bits 11 and 10 are reserved and must be programmed to 0, and Bits 9–0 are the data field (which has specific definitions, depending on the register selected).

Table I. Control Port Map

Register Address				Reserved[1]		Data Field									
15[2]	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

NOTES
[1]Must be programmed to zero.
[2]Bit 15 = MSB

Bit 15	Bit 14	Bit 13	Bit 12	Register Function
0	0	0	0	DAC Control I
0	0	0	1	DAC Control II
0	0	1	0	DAC Volume 1
0	0	1	1	DAC Volume 2
0	1	0	0	DAC Volume 3
0	1	0	1	DAC Volume 4
0	1	1	0	DAC Volume 5
0	1	1	1	DAC Volume 6
1	0	0	0	DAC Control III
1	0	0	1	Reserved
1	0	1	0	Reserved
1	0	1	1	Reserved
1	1	0	0	Reserved
1	1	0	1	Reserved
1	1	1	0	Reserved
1	1	1	1	Reserved

Table II. DAC Control I

Address	Reserved*		De-Emphasis	Function			
				Serial Mode	Data Word Width	Power-Down RESET	Interpolator Mode
15–12	11	10	9–8	7–5	4–3	2	1–0
0000	0	0	00 = None 01 = 44.1 kHz 10 = 32.0 kHz 11 = 48.0 kHz	000 = I^2S 001 = RJ 010 = DSP 011 = LJ 100 = Pack Mode 1 (256) 101 = Pack Mode 2 (128) 110 = AUX Mode 111 = Reserved	00 = 24 Bits 01 = 20 Bits 10 = 16 Bits 11 = Reserved	0 = Normal 1 = PWRDWN	00 = 8× (48 kHz) 01 = 2× (192 kHz) 10 = 4× (96 kHz) 11 = Reserved

*Must be programmed to zero.

DAC CONTROL REGISTER I

De-Emphasis

The AD1833 has a built-in de-emphasis filter that can be used to decode CDs that have been encoded with the standard "Redbook" 50 µs/15 µs emphasis response curve. Three curves are available; one each for 32 kHz, 44.1 kHz, and 48 kHz sampling rates. The filters may be selected by writing to Control Bits 9 and 8 in DAC Control Register I, see Table III.

Table III. De-Emphasis Settings

Bit 9	Bit 8	De-Emphasis
0	0	Disabled
0	1	44.1 kHz
1	0	32 kHz
1	1	48 kHz

Data Serial Interface Mode

The AD1833's serial data interface is designed to accept data in a wide range of popular formats including I^2S, right justified (RJ), left justified (LJ) and flexible DSP modes. The L/$\overline{R}$CLK pin acts as the word clock (or Frame Sync) to indicate sample interval boundaries. The BCLK defines the serial data rate while the data is input on the SDIN1-3 pins. The serial mode settings may be selected by writing to Control Bits 7 through 5 in DAC Control Register I, see Table IV.

Table IV. Data Serial Interface Mode Settings

Bit 7	Bit 6	Bit 5	Serial Mode
0	0	0	I^2S
0	0	1	Right Justify
0	1	0	DSP
0	1	1	Left Justify
1	0	0	Packed Mode 1 (256)
1	0	1	Packed Mode 2 (128)
1	1	0	AUX Mode
1	1	1	Reserved

DAC Word Width

The AD1833 will accept input data in three separate word-lengths—16, 20, and 24 bits. The word-length may be selected by writing to Control Bits 4 and 3 in DAC Control Register I, see Table V.

Table V. Word Length Settings

Bit 4	Bit 3	Word Length
0	0	24 Bits
0	1	20 Bits
1	0	16 Bits
1	1	Reserved

Power-Down Control

The AD1833 can be powered down by writing to Control Bit 2 in DAC Control Register I, see Table VI. The power-down/reset bit is not latched when the CLATCH is brought high to latch the entire word, but only after the following low-to-high CLATCH transition. Therefore, to put the part in power-down, or to bring it back up from power-down, the command should be written twice.

Table VI. Power-Down Control

Bit 2	Power-Down Setting
0	Normal Operation
1	Power-Down Mode

Interpolator Mode

The AD1833's DAC interpolators can be operated in one of three modes—8×, 4×, or 2× corresponding with 48 kHz, 96 kHz, and 192 kHz modes respectively. The Interpolator Mode may be selected by writing to Control Bits 1 and 0 in DAC Control Register I, see Table VII.

Table VII. Interpolator Mode Settings

Bit 1	Bit 0	Interpolator Mode
0	0	8× (48 kHz)
0	1	2× (192 kHz)
1	0	4× (96 kHz)
1	1	Reserved

Table VIII. DAC Control II

Address	Reserved*		Function						
			Reserved*	Mute Control					
15–12	11	10	9–6	5	4	3	2	1	0
0001	0	0	0	Channel 6 0 = Mute Off 1 = Mute On	Channel 5 0 = Mute Off 1 = Mute On	Channel 4 0 = Mute Off 1 = Mute On	Channel 3 0 = Mute Off 1 = Mute On	Channel 2 0 = Mute Off 1 = Mute On	Channel 1 0 = Mute Off 1 = Mute On

*Must be programmed to zero.

DAC CONTROL REGISTER II

DAC Control Register II contains individual channel mute controls for each of the 6 DACs. Default operation (bit = 0) is muting off. Bits 9 through 6 of Control Register II are reserved and should be programmed to zero, see Table VIII.

Table IX. Muting Control

Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Muting
X	X	X	X	X	1	Mute Channel 1
X	X	X	X	1	X	Mute Channel 2
X	X	X	1	X	X	Mute Channel 3
X	X	1	X	X	X	Mute Channel 4
X	1	X	X	X	X	Mute Channel 5
1	X	X	X	X	X	Mute Channel 6

DAC CONTROL REGISTER III

Stereo Replicate

The AD1833 allows the stereo information on Channel 1 (SDIN1—Left 1 and Right 1) to be copied to Channels 2 and 3 (Left/Right 2 and Left/Right 3). These signals can be used in an external summing amplifier to increase potential signal SNR. Stereo Replicate mode can be enabled by writing to Control Bit 5, see Table XI. Note that replication is not reflected in the zero flag status.

Table XI. Stereo Replicate

Bit 5	Stereo Mode
0	Normal
1	Channel 1 Data Replicated on Channels 2 and 3

Table X. DAC Control III

Address	Reserved*		Reserved*	Function			
				Stereo Replicate (192 kHz)	MCLK Select	Zero Detect	Reserved
15–12	11	10	9–6	5	4–3	2	1–0
1000	0	0	0	0 = Normal 1 = Replicate	00 = 256 × f_S (MCLK × 2) 01 = 512 × f_S (MCLK Straight Through) 10 = 768 × f_S (MCLK × 2/3)	0 = Active High 1 = Active Low	

*Must be programmed to zero.

MCLK Select

The AD1833 allows the matching of available external MCLK frequencies to the required sample rate. The oversampling rate can be selected from $256 \times f_S$, $512 \times f_S$ or $768 \times f_S$ by writing to Bit 4 and Bit 3. Internally the AD1833 requires an MCLK of $512 \times f_S$; therefore, in the case of $256 \times f_S$ mode, a clock doubler is used, whereas in $768 \times f_S$ mode, a divide-by-3 block (/3) is first implemented, followed by a clock doubler. See Table XII.

Table XII. MCLK Settings

Bit 4	Bit 3	Oversample Ratio
0	0	$256 \times f_S$ (MCLK × 2 Internally)
0	1	$512 \times f_S$
1	0	$768 \times f_S$ (MCLK × 2/3 Internally)
1	1	Reserved

Channel Zero Status

The AD1833 provides individual logic output status indicators when zero data is sent to a channel for 1024 or more consecutive sample periods. There is also a global zero flag that indicates all channels contain zero data. The polarity of the active zero signal is programmable by writing to Control Bit 2, see Table XIII. The six individual channel flags are best used as three stereo zero flags by combining pairs of them through suitable logic gates. Then, when both the left and right input are zero for 1024 clock cycles, i.e., a stereo zero input for 1024 sample periods, the combined result of the two individual flags will go active indicating a stereo zero.

Table XIII. Zero Detect

Bit 2	Channel Zero Status
0	Active High
1	Active Low

DAC Volume Control Registers

The AD1833 has six volume control registers, one each for the six DAC channels. Volume control is exercised by writing to the relevant register associated with each DAC. This setting is used to attenuate the DAC output. Full-scale setting (all 1s) is equivalent to zero attenuation. See Table XV.

Table XIV. MCLK vs. Sample Rate Selection

Sampling Rate f_S (kHz)	Interpolator Mode	MCLK (MHz)		
		256 f_S	512 f_S	768 f_S
32 64 128	8× (Normal) 4× (Double) 2× (4 Times)	8.192	16.384	24.576
44.1 88.2 176.4	8× (Normal) 4× (Double) 2× (4 Times)	11.2896	22.5792	33.8688
48 96 192	8× (Normal) 4× (Double) 2× (4 Times)	12.288	24.576	36.864

Table XV. Volume Control Registers

Address	Reserved*		Volume Control
15–12	11	10	9–0
0 0 1 0	0	0	Channel 1 Volume Control (OUTL1)
0 0 1 1			Channel 2 Volume Control (OUTR1)
0 1 0 0			Channel 3 Volume Control (OUTL2)
0 1 0 1			Channel 4 Volume Control (OUTR2)
0 1 1 0			Channel 5 Volume Control (OUTL3)
0 1 1 1			Channel 6 Volume Control (OUTR3)

*Must be programmed to zero.

I²S Timing

I²S timing uses an L/$\overline{R}$CLK to define when the data being transmitted is for the left channel and when it is for the right channel. The L/$\overline{R}$CLK is low for the left channel and high for the right channel. A bit clock running at $64 \times f_S$ is used to clock in the data. There is a delay of one bit clock from the time the L/$\overline{R}$CLK signal changes state to the first bit of data on the SDINx lines. The data is written MSB first and is valid on the rising edge of bit clock.

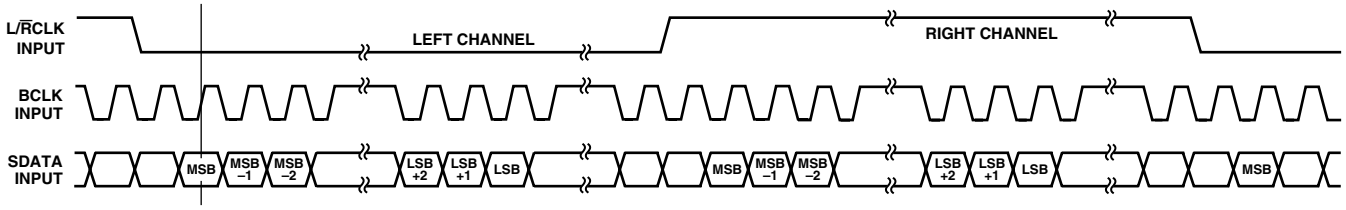


Figure 4. I²S Timing Diagram

Left Justified Timing

Left Justified (LJ) timing uses an L/$\overline{R}$CLK to define when the data being transmitted is for the left channel and when it is for the right channel. The L/$\overline{R}$CLK is high for the left channel and low for the right channel. A bit clock running at $64 \times f_S$ is used to clock in the data. The first bit of data appears on the SDINx lines at the same time the L/$\overline{R}$CLK toggles. The data is written MSB first and is valid on the rising edge of bit clock.

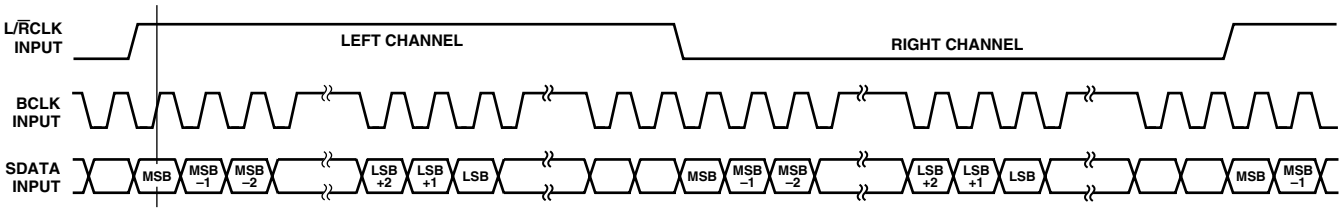


Figure 5. Left-Justified Timing Diagram

Right Justified Timing

Right Justified (RJ) timing uses an L/$\overline{R}$CLK to define when the data being transmitted is for the left channel and when it is for the right channel. The L/$\overline{R}$CLK is high for the left channel and low for the right channel. A bit clock running at $64 \times f_S$ is used to clock in the data. The first bit of data appears on the SDINx 8-bit clock periods (for 24-bit data) after L/$\overline{R}$CLK toggles. In RJ mode the LSB of data is always clocked by the last bit clock before L/$\overline{R}$CLK transitions. The data is written MSB first and is valid on the rising edge of bit clock.

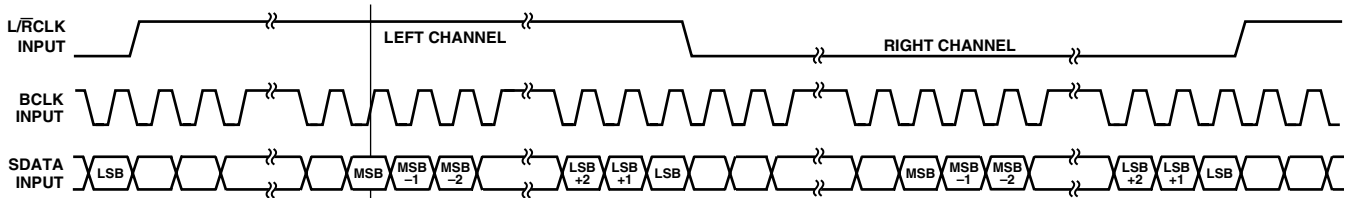


Figure 6. Right-Justified Timing Diagram

AUX-Mode Timing—Interfacing to a SHARC®

In AUX mode, the AD1833 is the master and generates a frame sync signal (FSTDM) on its L/$\overline{R}$CLK pin, and a bit clock (BCLKTDM) on its BCLK pin, both of which are used to control the data transmission from the SHARC. The bit clock runs at a frequency of $256 \times f_S$. In this mode all data is written on the rising edge of the bit clock and read on the falling edge of the bit clock. The AD1833 starts the frame by raising a frame sync on the rising edge of bit clock. The SHARC recognizes this on the following falling edge of bit clock, and is ready to start outputting data on the next rising edge of bit clock. Each channel is given a 32-bit clock slot, the data is left justified and uses 16, 20, or 24 of the 32 bits. An enlarged diagram (see Figure 6) is provided detailing this. The data is sent from the SHARC to the AD1833 on the SDIN1 pin and is provided in the following order, MSB first—Internal DACL0, Internal DACL1, Internal DACL2, AUX DACL0, Internal DACR0, Internal DACR1, Internal DACR2 and AUX DACR0. The data is written on the rising edge of bit clock and read by the AD1833 on the falling edge of bit clock. The left and right data destined for the auxiliary DAC is sent to it in standard I^2S format in the next frame using the SDIN2, SDIN3, and SOUT pins as the L/$\overline{R}$CLK, BCLK, and SDIN pins respectively for communicating with the auxiliary DAC.

DSP Mode Timing

DSP Mode Timing uses the rising edge of the frame sync signal on the L/$\overline{R}$CLK pin to denote the start of the transmission of a data word. Note that for both left and right channels a rising edge is used; therefore in this mode there is no way to determine which data is intended for the left channel and which is intended for the right. The DSP writes data on the rising edge of BCLK and the AD1833 reads it on the falling edge. The DSP raises the frame sync signal on the rising edge of BCLK and then proceeds to transmit data, MSB first, on the next rising edge of BCLK. The data length can be 16, 20, or 24 bits. The frame sync signal can be brought low any time at or after the MSB is transmitted, but must be brought low at least one BCLK period before the start of the next channel transmission.

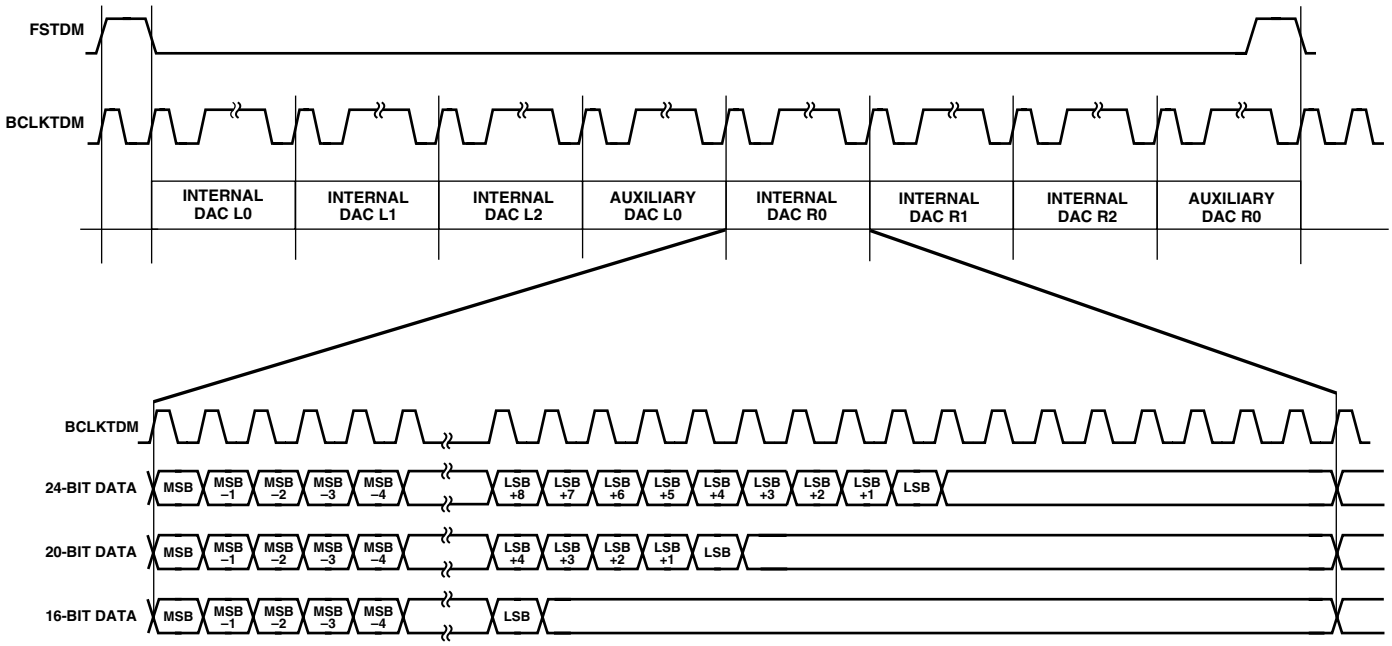


Figure 7. Aux-Mode Timing

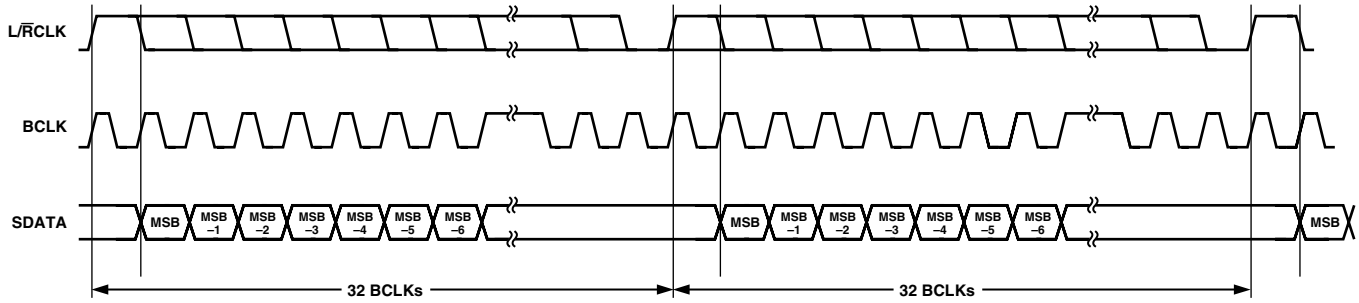


Figure 8. DSP Mode Timing

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Packed Mode 128

In Packed Mode 128, all six data channels are "packed" into one sample interval on one data pin. The BCLK runs at 128 × f_S; therefore there are 128 BCLK periods in each sample interval. Each sample interval is broken into eight time slots, six slots of 20 BCLKs and two of four BCLKs. The data length is restricted in this mode to a maximum of 20 bits. The three left channels are written first, MSB first, and the data is written on the falling edge of BCLK. After the three left channels are written, there is a space of four BCLKs and then the three right channels are written. The L/$\overline{R}$CLK defines the left and right data transmission; it is high for the three left channels and low for the three right channels.

Packed Mode 256

In Packed Mode 256 all six data channels are "packed" into one sample interval on one data pin. The BCLK runs at 256 × f_S; therefore there are 256 BCLK periods in each sample interval. Each sample interval is broken into eight time slots of 32 BCLKs each. The data length can be 16, 20, or 24 bits. The three left channels are written first, MSB first, and the data is written on the falling edge of BCLK with a one BCLK period delay from the start of the slot. After the three left channels are written, there is a space of 32 BCLKs and then the three right channels are written. The L/$\overline{R}$CLK defines the left and right data transmission; it is low for the three left channels and high for the three right channels.

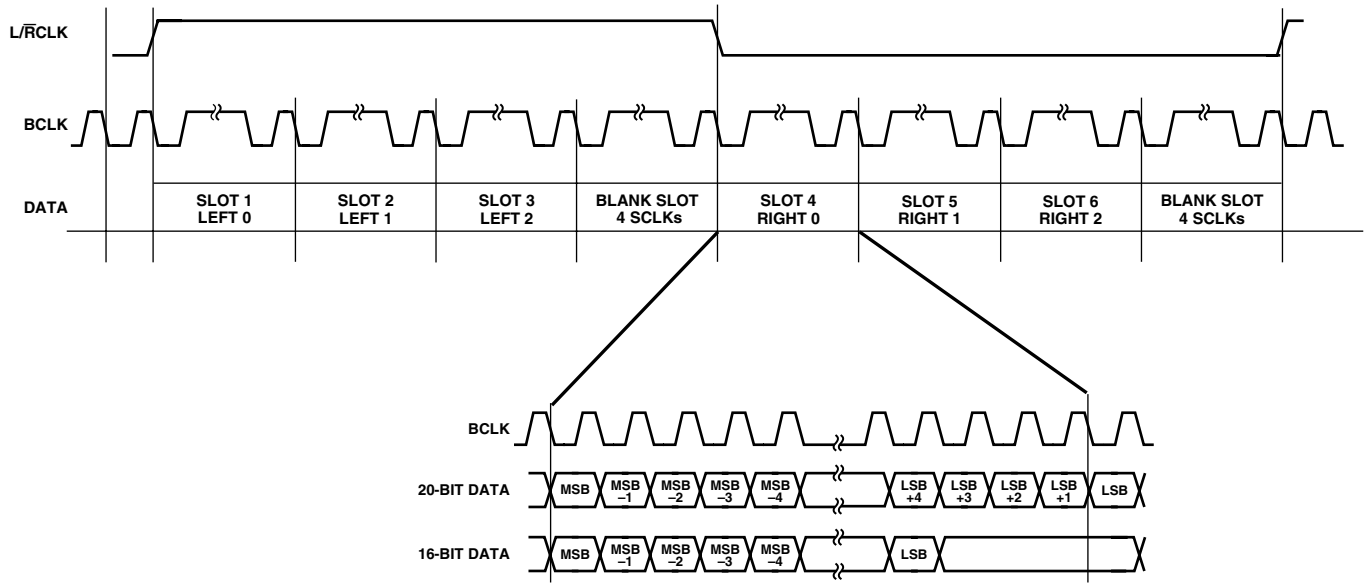


Figure 9. Packed Mode 128

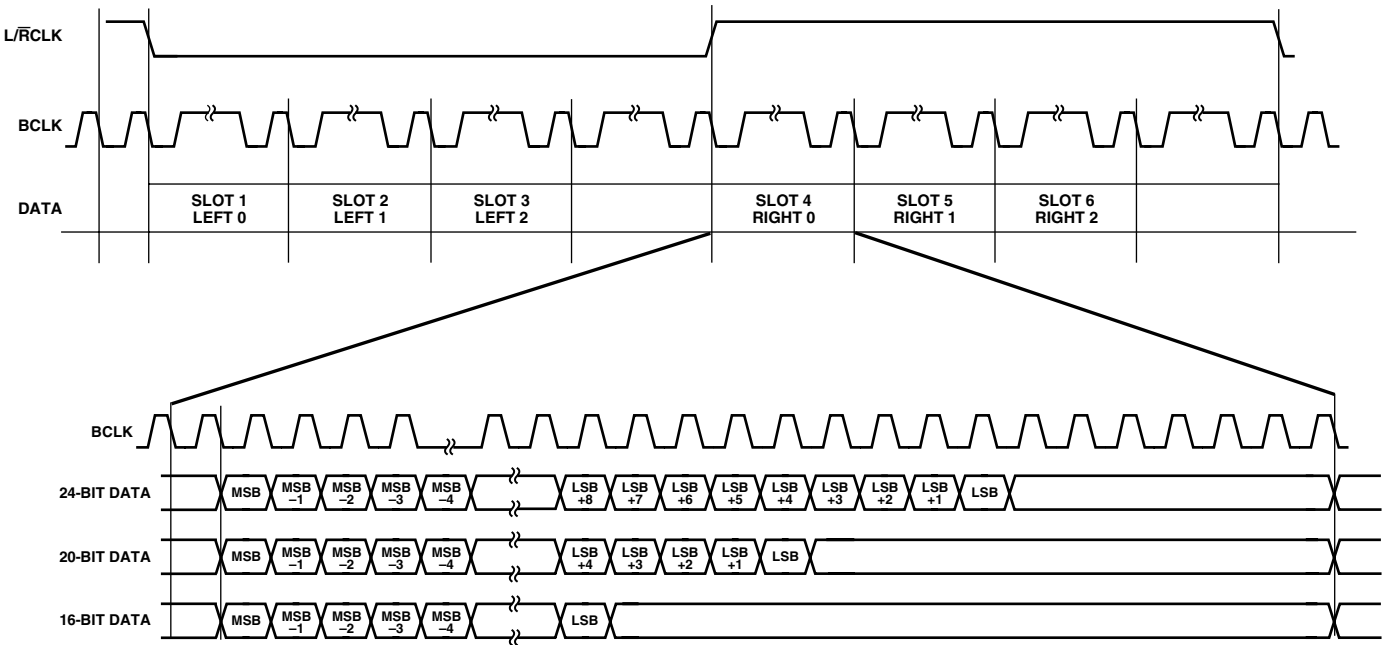


Figure 10. Packed Mode 256

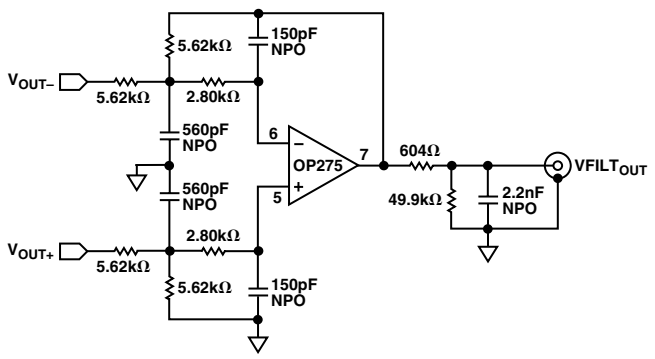


Figure 11. Suggested Output Filter Schematic

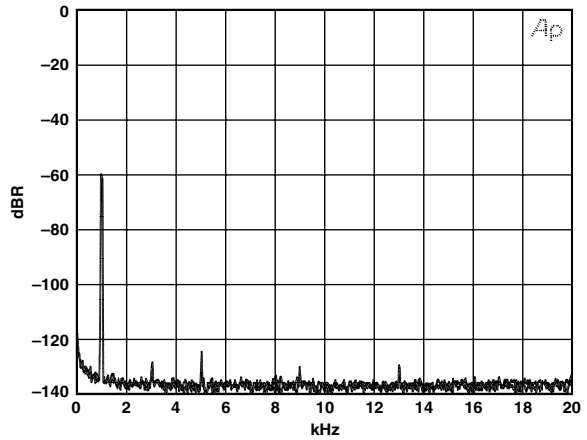


Figure 12. Dynamic Range for 1 kHz @ –60 dBFS, 110 dB, Triangular Dithered Input

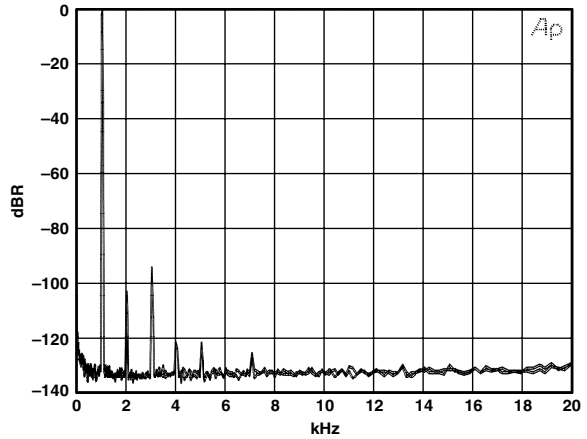


Figure 13. Input 0 dBFS @ 1 kHz, BW 20 Hz to 20 kHz, SR 48 kHz, THD + N –95 dBFS

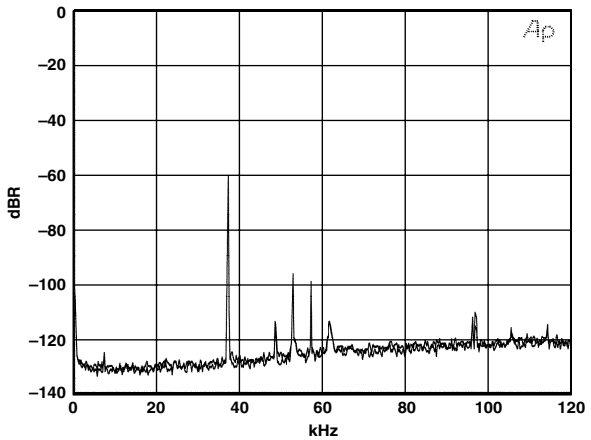


Figure 14. Dynamic Range for 37 kHz @ –60 dBFS, 110 dB, Triangular Dithered Input

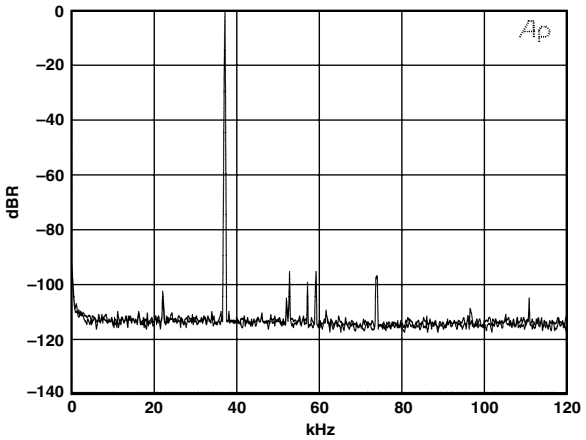


Figure 15. Input 0 dBFS @ 37 kHz, BW 20 Hz to 120 kHz, SR 96 kHz, THD + N –95 dBFS

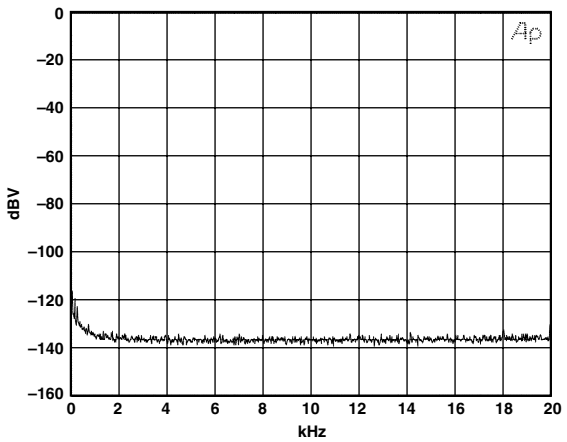


Figure 16. Noise Floor for Zero Input, SR 48 kHz, SNR 110 dBFS A-Weighted

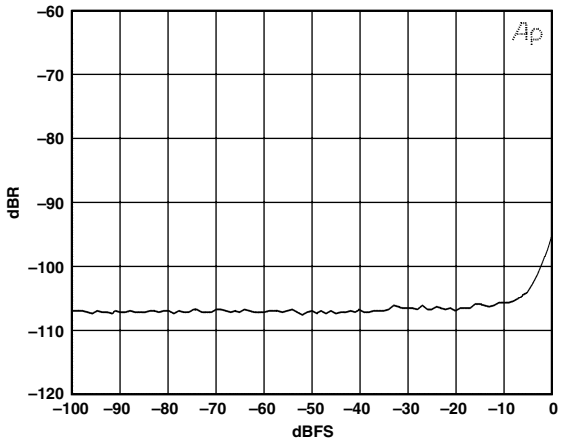


Figure 17. THD + N Ratio vs. Amplitude, Input 1 kHz, SR 48 kHz, 24-Bit

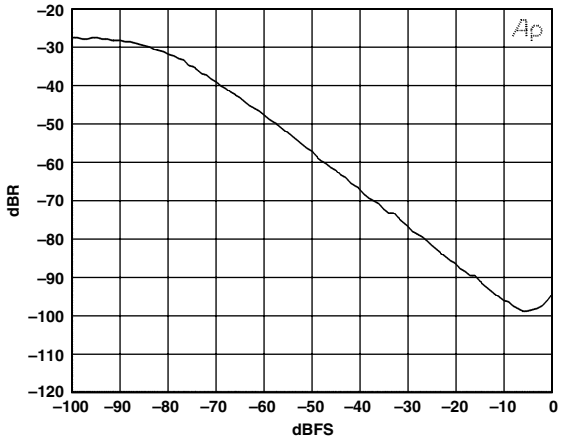


Figure 18. THD + N Ratio vs. Amplitude, @ 1 kHz, SR 48 kHz

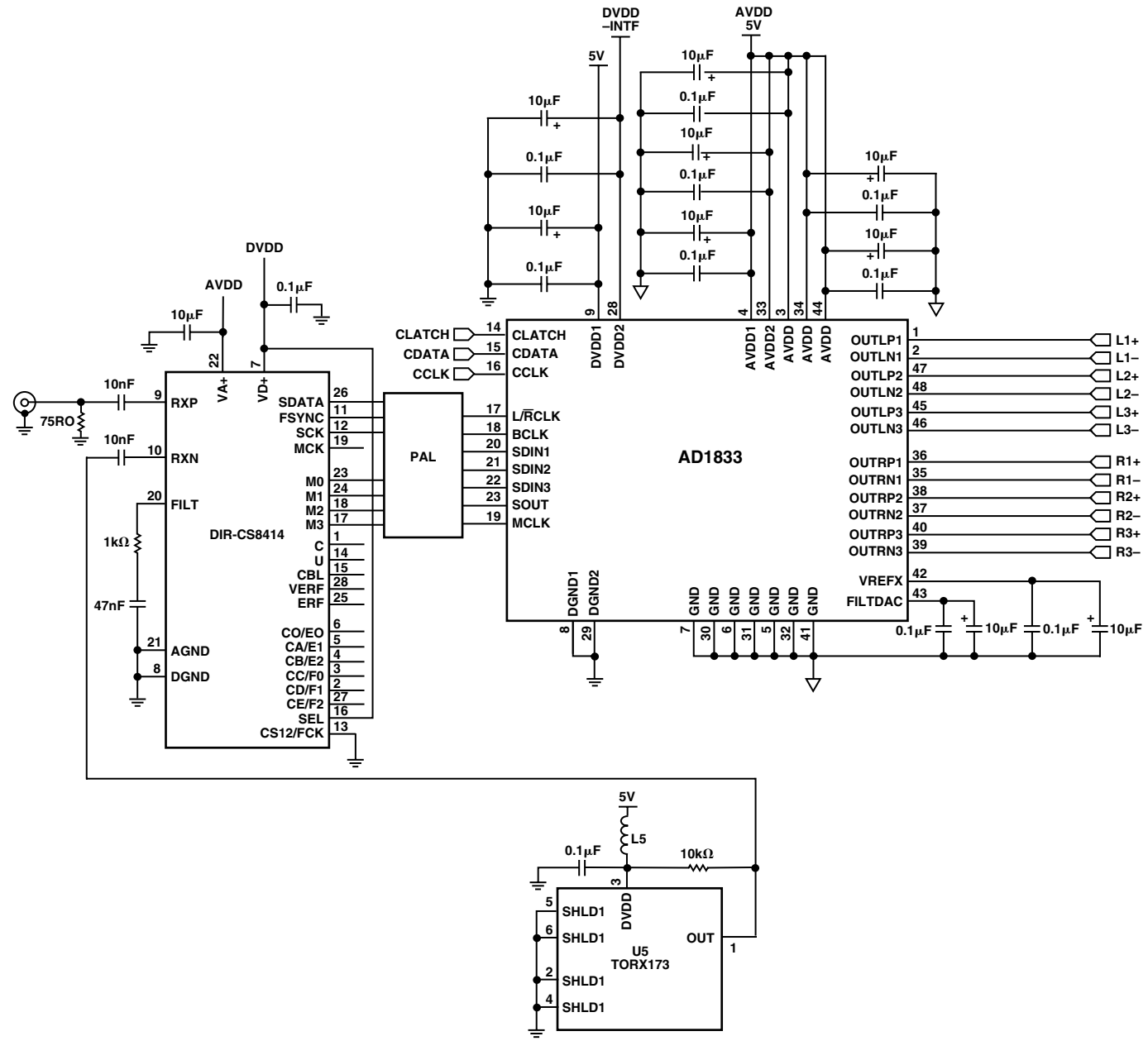
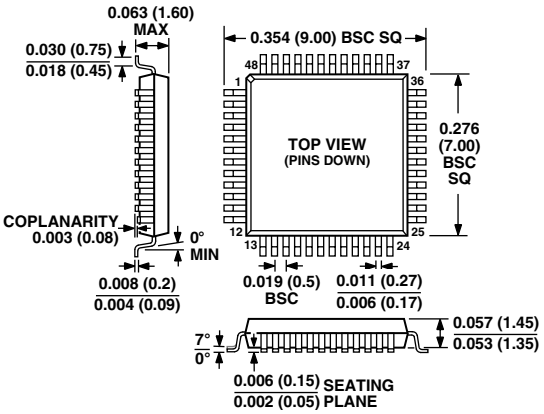


Figure 19. Example Digital Interface

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

48-Lead Thin Plastic Quad Flatpack (ST-48)



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