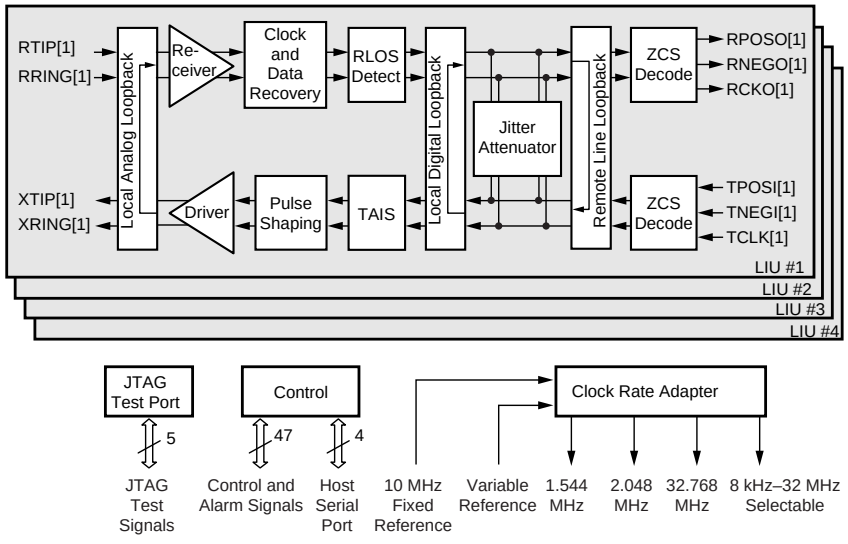
CN8380

Quad T1/E1 Line Interface

The CN8380 is a fully integrated quad line interface unit for both 1.544 Mbps (T1) and 2.048 Mbps (E1) applications. It is designed to complement T1/E1 framers or operate as a stand-alone line interface to synchronous or plesiochronous mappers and multiplexers. The device can be controlled through a host mode serial port or by hardware mode operation, where device control and status are obtained through non-multiplexed dedicated pins. Many of these pins are also dedicated to individual channels for maximum flexibility and for use in redundant systems. Integrated in the CN8380 device is a clock rate adapter (CLAD), which provides various low-jitter programmable system clock outputs. The receive section of the CN8380 is designed to recover encoded signals from lines having up to 12 dB of attenuation. The transmit section consists of a programmable, precision pulse shaper.

Functional Block Diagram



8380_001

Distinguishing Features

- Four T1/E1 short haul line interfaces in a single chip
- On-chip CLAD /system synchronizer
- Digital (crystal-less) jitter attenuators selectable for transmitter/receiver on each line interface
- Meets AT&T pub 62411 jitter specs
- Meets ITU G.703, ETS 300 011 (PSTNX) Connections
- AMI/B8ZS/HDB3 line codes
- Host serial port or hardware only control modes
- On-chip receive clock recovery
- Common transformers for 120/75 Ω E1 and 100 Ω T1
- Low-power 3.3 V power supply
- Transmitter performance monitor
- Compatible with latest ANSI, ITU-T, and ETSI standards
- 128-pin MQFP package
- Remote and local loopbacks

Applications

- SONET/SDH multiplexers
- T3 and E3/E4 (PDH) multiplexers
- ATM multiplexers
- Voice compression and voice processing equipment
- WAN routers and bridges
- Digital loop carrier terminals (DLC)
- HDSL terminal units
- Remote concentrators
- Central office equipment
- PBXs and rural switches
- PCM/voice channel banks
- Digital access and cross-connect systems (DACS)

Ordering Information

Model Number	Package	Operating Temperature
CN8380EPF	128-pin MQFP	–40 °C to +85 °C
CN8398EVM	BT00–D660–001	

Revision History

Revision	Level	Date	Description
A	Advance	April 26, 1999	Created

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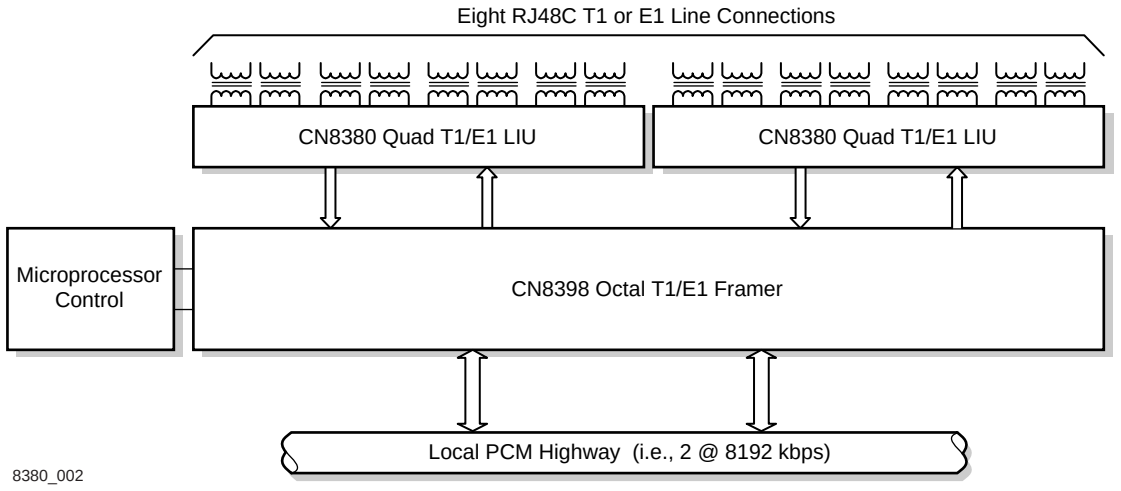
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CN8398EVM Octal T1/E1 Evaluation Module



Contact a Conexant representative for EVM availability and price.

Detailed Feature Summary

Interface Compatibility

- T1.102–1993
- G.703 at 1.544 or 2.048 Mbps
- ITU-T Recommendation I.431

Receive Line Interface

- External Termination
- Equalizer compensation for – 20 dB bridged monitor levels
- + 3 dB to –12 dB receiver sensitivity

Transmit Line Interface

- Pulse shapes for 0–655 ft., in 133 ft. steps (T1 DSX–1)
- External termination for improved return loss
- Line driver enable/disable for protection switching
- Output short circuit protection (for BABT applications)

Jitter Attenuator Elastic Store

- Receive or transmit direction
- 8-, 16-, 32-, 64-, or 128-bit depth
- Automatic and manual centering

Line Codes

- Bipolar alternate mark inversion line coding
- Optional zero code suppression:
  - Independent transmit and receive
  - T1: B8ZS
  - E1: HDB3

Loopbacks

- Remote loopback towards line
  - With or without JAT
  - Retains BPV transparency
- Local loopback towards system
  - Analog line loopback
  - Local digital loopback
- Simultaneous local and remote line loopbacks

Clock Rate Adapter

- Outputs jitter attenuated line rate clock
  - CLK1544 = 1544 k (T1)
  - CLK2048 = 2048 k (E1)
- CLAD output supports 14 output clock frequencies: 8 kHz to 32,768 kHz
- Programmable input timing reference:
  - Receive recovered clock from any channel
  - Internal clock (REFCKI)
  - CLADI
- Subrate CLADI timing reference:
  - Line rate $\div 2^N$, N = 0 to 7
  - References as low as 8 kHz

Host Serial Interface

- Compatible with existing framers
- Compatible with microprocessor serial ports
- Bit rates up to 8 Mbps

In-Service Performance Monitoring

- Transmit alarm detectors:
  - Loss of Transmit Clock (TLOC)
  - Transmit Short Circuit (TSHORT)
- Receive alarm detectors:
  - Loss of Signal (RLOS)
  - Loss of Analog Input (RALOS)
  - Bipolar/Line Code Violations
- Automatic and on-demand transmit alarms:
  - AIS following TLOC
  - Automatic AIS clock switching

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1.0 Pin Descriptions

The CN8380 is packaged in a 128-pin metric quad flat pack (MQFP). A pinout diagram is illustrated in Figure 1-1. Logic diagrams are illustrated in Figure 1-2 and Figure 1-3. Pin labels and numbers, input/output functions, and descriptions are provided in Table 1-1.

The following input pins contain an internal pull-up resistor (> 50 kΩ) and may remain unconnected if unused or if the active high input state is desired:

$\overline{\text{XOE}}$ [1:4]
$\overline{\text{TAIS}}$ [1:4]
$\overline{\text{RAWMD}}$ [1:4]
$\overline{\text{RLOOP}}$ [1:4]
$\overline{\text{LLOOP}}$ [1:4]
HM
UNIPOLAR
JDIR/SCLK
JSEL(2)/SDI
JSEL(1)/$\overline{\text{CS}}$
JSEL(0)
$\overline{\text{RESET}}$
HTERM
CLK_POL
PTS(2:0)
TDI (Unused if JTAG not connected)
TMS (Disables JTAG if not connected)
TCK (Unused if JTAG not connected)
$\overline{\text{TRST}}$ (Unused if JTAG not connected)

Figure 1-1. CN8380 Pinout Diagram

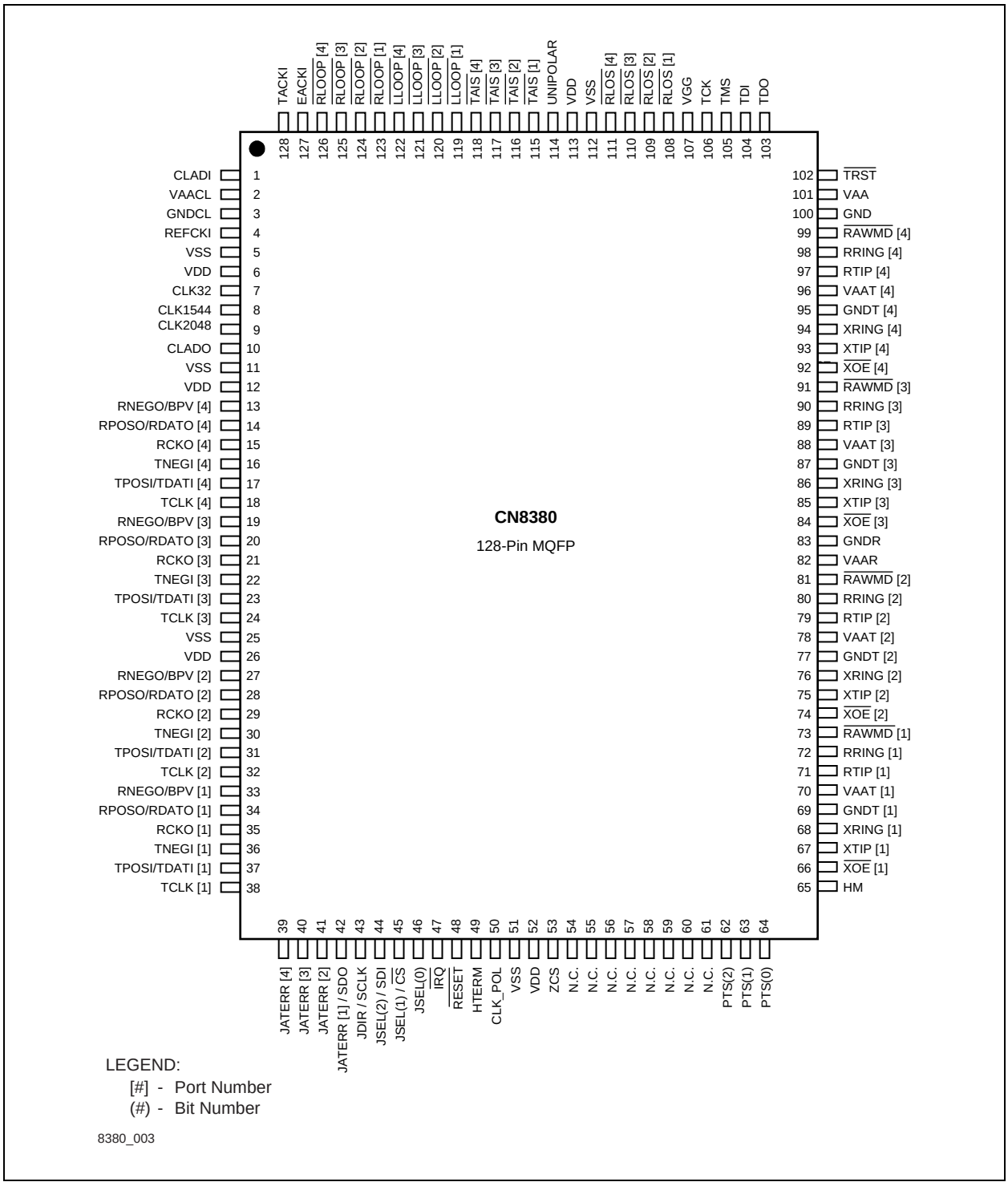


Figure 1-2. CN8380 Logic Diagram (Host Mode)

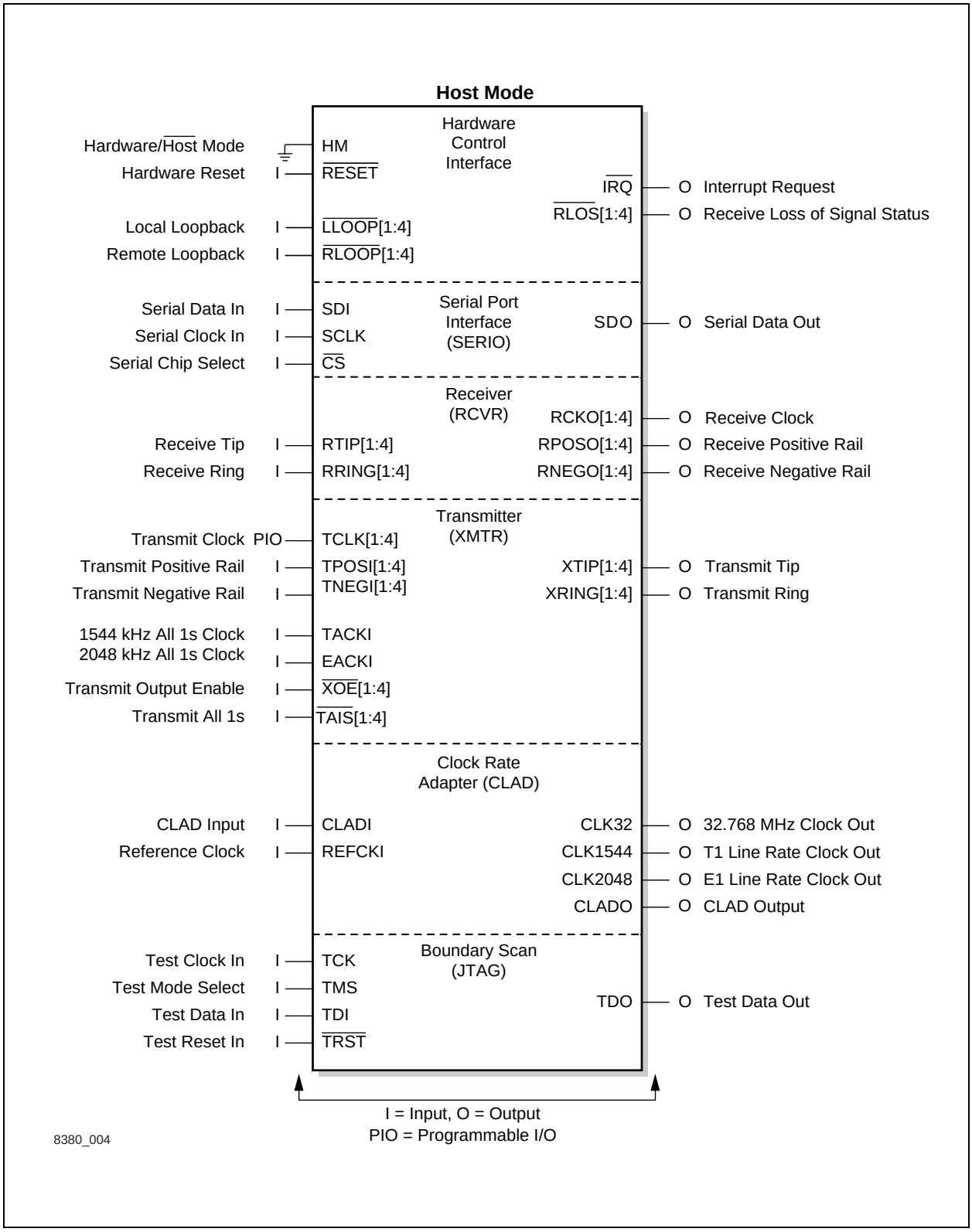


Figure 1-3. CN8380 Logic Diagram (Hardware Mode)

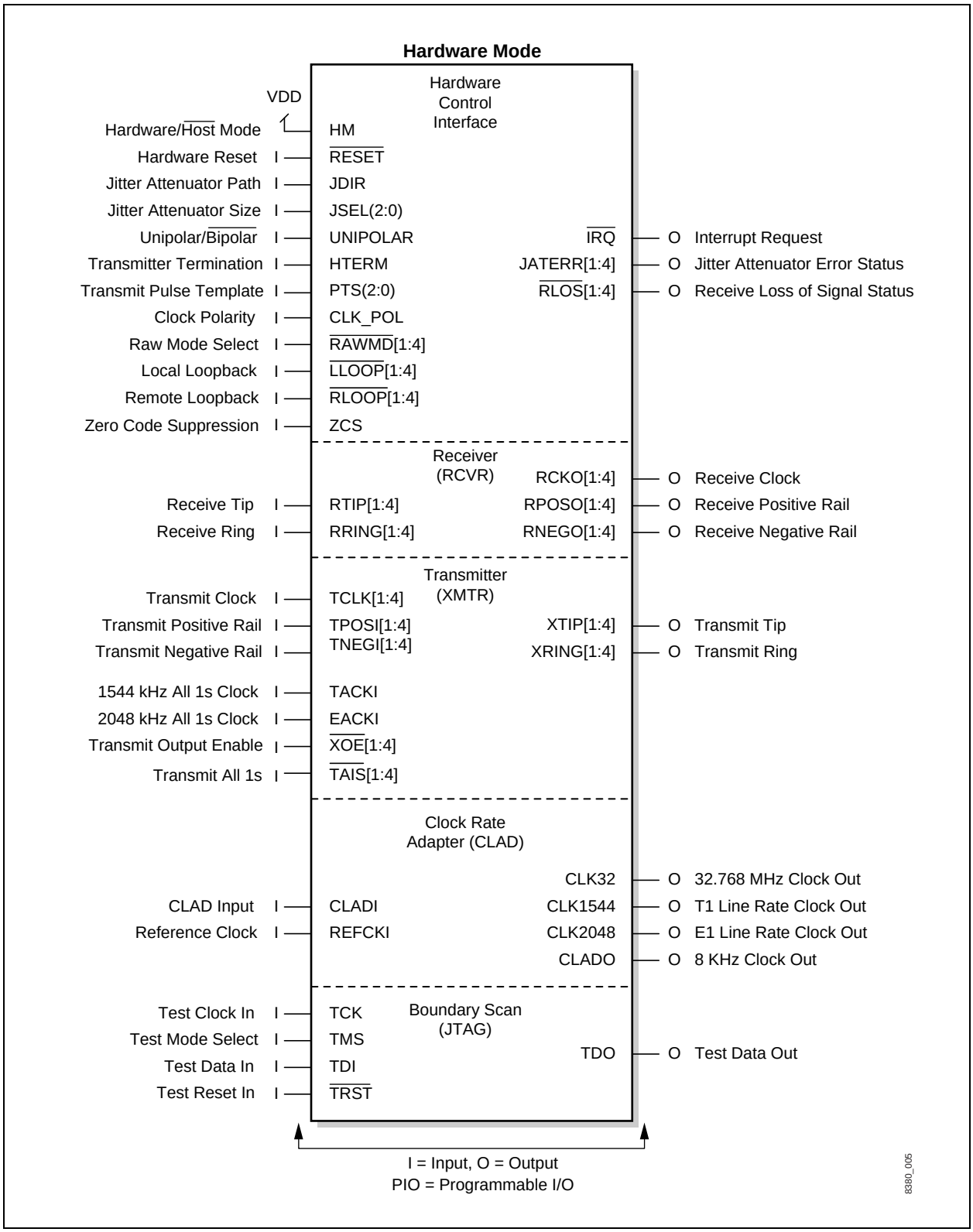


Table 1-1. Hardware Signal Definitions *(1 of 5)*

Pin Label	Signal Name	I/O	Definition
Receiver			
RPOSO[1:4] RDATO[1:4]	RX Positive Rail (Bipolar Mode) RX Data (Unipolar Mode)	O	Line rate data output on the rising or falling edge of RCKO. The clock edge is determined by the CLK_POL pin in Hardware Mode or the CLK_POL register bit [RLIU_CR; addr n1] in Host Mode. In bipolar mode, a high signal indicates receipt of a positive AMI pulse on RTIP/RRING inputs. In unipolar mode, RPOSO is redefined as RDATO and a high signal indicates either a positive or negative AMI pulse on RTIP/RRING inputs. RPOSO/RDATO is three-stated during device reset.
RNEGO[1:4] BPV[1:4]	RX Negative Rail (Bipolar Mode) Bipolar Violation (Unipolar Mode)	O	Line rate data output on rising or falling edge of RCKO. The clock edge is determined by the CLK_POL pin in Hardware Mode or the CLK_POL register bit [RLIU_CR; addr n1] in Host Mode. In bipolar mode, a high signal indicates receipt of a negative AMI pulse on RTIP/RRING inputs. In unipolar mode, RNEGO is redefined as BPV, and a high signal indicates the reception of a BPV which is not part of a ZCS code (B8ZS or HDB3). RNEGO/BPV is three-stated during device reset.
RCKO[1:4]	RX Clock Output	O	Receive clock output. RCKO is the RPLL recovered line rate clock or jitter attenuated clock output, based on the programmed jitter attenuator selection. RCKO is three-stated during device reset.
RTIP[1:4] RRING[1:4]	Receive Tip Receive Ring	I	Differential AMI data inputs for direct connection to receive transformer.
Transmitter			
TPOSI[1:4] TDATI[1:4]	Tx Positive Rail (Bipolar Mode) Tx Data (Unipolar Mode)	I	Positive rail, line rate data source for transmitted XTIP/XRING output pulses. Data is sampled on the falling edge of TCLK. In bipolar mode, a high on TPOSI causes a positive output pulse on XTIP/XRING; and a high on TNEGI causes a negative output pulse. In unipolar mode, TPOSI is redefined as TDATI and accepts single-rail NRZ data. TNEGI is not used in unipolar mode.
TNEGI[1:4]	Tx Negative Rail Input	I	Negative rail, line rate data input on TCLK falling edge. Refer to TPOSI signal definition.
TCLK[1:4]	TX Clock Input	I/O	Transmit line rate clock. TCLK is the transmit clock for TPOSI and TNEGI data inputs and for transmitter timing. Normally, TCLK is an input and samples TPOSI/TNEGI on the falling edge. In Host Mode, TCLK can be configured as an output to supply a line rate transmit clock from the CLAD. The timing reference for the TCLK output (and CLAD) can be selected from six sources.
TACKI EACKI	T1 AIS Clock E1 AIS Clock	I I	Alternate T1 and E1 transmit clock used to transmit AIS (all 1s alarm signal) when the primary transmit clock source, TCLK, fails. TACKI (T1) or EACKI (E1) is either manually or automatically switched to replace TCLK [LIU_CTL; addr n3]. Systems without an AIS clock should connect TACKI and EACKI to ground.
$\overline{\text{XOE}}$[1:4]	Transmit Output Enable	I^P	A low signal enables XTIP and XRING output drivers. Otherwise outputs are high impedance.
$\overline{\text{TAIS}}$[1:4]	Transmit AIS Alarm	I^P	In Hardware Mode, a low signal causes AIS (unframed all 1s) transmission on XTIP/XRING outputs. In Host Mode, these pins can be enabled or disabled [LIU_CTL; addr n3]. If disabled, they are not used and may be left unconnected.

Table 1-1. Hardware Signal Definitions *(2 of 5)*

Pin Label	Signal Name	I/O	Definition
XTIP[1:4] XRING[1:4]	Transmit Tip Transmit Ring	O	Complementary AMI transmitter line outputs for direct connection to transmit transformer. Optionally, both outputs are three-stated when $\overline{XOE}$ is high.
Clock Rate Adapter (CLAD)			
CLADI	CLAD Input	I	CLAD input timing reference used to phase/frequency lock the CLAD outputs to an input clock frequency selected in the range of 8 kHz to 32,768 kHz [CLAD_CR; addr 02]. Systems which do not use CLADI should connect CLADI to ground. In Hardware Mode, the CLAD timing reference automatically switches to internal free-run operation if clock edges are not detected on CLADI pin.
REFCKI	Reference Clock	I	System must apply a 10 MHz ± 50 ppm (E1) or ± 32 ppm (T1) clock signal to act as the frequency reference for the internal numerically controlled oscillator (NCO). REFCKI determines the frequency accuracy and stability of the CLAD output clocks when operating in free-run mode [CLAD_CR; addr 02]. REFCKI is the baseband reference for all CLAD/JAT functions and is used internally to generate clocks of various frequency locked to a selected receive or external clock. ***Note*: REFCKI is always required.**
CLK32	32 MHz Clock Output	O	Fixed rate 32.768 MHz clock output provided by the CLAD. May be used by framers, such as the CN8398 octal T1/E1 framer, to provide system timing reference.
CLK1544	T1 Clock Output	O	Fixed rate 1.544 MHz T1 line rate clock output provided by the CLAD. May be used for TCLK or TACKI clock sources. This clock is locked to the selected CLAD timing reference.
CLK2048	E1 Clock Output	O	Fixed rate 2.048 MHz E1 line rate clock output provided by the CLAD. May be used for TCLK or EACKI clock sources. This clock is locked to the selected CLAD timing reference.
CLADO	CLAD Output	O	In Hardware Mode, CLADO is a fixed rate 8 kHz clock output provided by the CLAD. In Host Mode, CLADO may be configured to operate at one of 14 different clock frequencies [CSEL; addr 03] that include T1 or E1 line rates. CLADO is typically programmed to supply system clocks that are phase-locked to the selected receive or CLAD timing reference [CLAD_CR; addr 02].
Hardware Control Signals			
HM	Hardware Mode	I^P	A high on HM places the device in Hardware Mode, enabling all hardware control pin functions. A low on HM places the device in Host Mode, disabling some hardware-mode-only pin functions and enabling the serial port signals on the dual function pins listed below. The serial port signals allow serial host access to the device registers. Refer to the Host Serial Control Signals section of this table. JSEL(1) / $\overline{CS}$ JSEL(2) / SDI JDIR / SCLK JATERR(1) / SDO
$\overline{RAWMD}$[1:4]	Raw Mode	I^P	Low selects receiver Raw mode. Applicable only in Hardware Mode. In Raw mode, RPOSO and RNEGO represent the data slicer outputs and RCKO is the logical OR of RPOSO and RNEGO.

Table 1-1. Hardware Signal Definitions *(3 of 5)*

Pin Label	Signal Name	I/O	Definition
$\overline{\text{RESET}}$	Hardware Reset	I^P	Active low asynchronous hardware reset. A falling edge forces registers to their default, power-up state. Output pins are forced to the high impedance state while $\overline{\text{RESET}}$ is asserted. $\overline{\text{RESET}}$ is not mandatory at power-up because an internal power-on reset circuit performs an identical function.
UNIPOLAR	Unipolar Mode Select	I^P	Applicable only in Hardware Mode. A high signal on UNIPOLAR configures all RPOSO outputs and TPOSI inputs to operate with unipolar, NRZ-formatted data. In this mode, RNEGO reports non-ZCS BPVs and TNEGI is not used. A low signal on UNIPOLAR configures all channels' RPOSO/RNEGO and TPOSI/TNEGI interfaces to operate with bipolar, dual-rail, NRZ formatted data.
ZCS	Zero Code Suppression Select	I^P	Applicable only in Hardware Mode. A high signal on ZCS enables the transmit ZCS encoder and the receive ZCS decoder if unipolar mode is enabled (UNIPOLAR = 1). In Bipolar Mode (UNIPOLAR = 0), the ZCS encoder and decoder are disabled and ZCS is ignored.
CLK_POL	Rx Clock Polarity Select	I^P	Applicable only in Hardware Mode. High sets RPOSO/RNEGO to be output on the falling edge of RCKO. Low sets RPOSO/RNEGO to be output on the rising edge of RCKO
PTS(2:0)	Transmit Pulse Template Select	I^P	Applicable only in Hardware Mode. The PTS(2:0) control bus selects the transmit pulse template and the line rate (T1 or E1) globally for all channels. Refer to the description of HTERM in this table and to the transmit pulse configurations in Table 2-3.
HTERM	Transmitter Hardware Termination	I^P	Applicable only in Hardware Mode. If an external transmit termination resistor is used to meet return loss specifications; a transformer with a 1:2 turns ratio is used, and HTERM is set high to allow the transmitter to compensate for the increased load. Refer to the Transmitter section of this table and Tables 2-4 through 2-8 for transmitter termination configuration options.
$\overline{\text{IRQ}}$	Interrupt Request	O^D	Active low, open drain output. In Host Mode, $\overline{\text{IRQ}}$ indicates one or more pending interrupt requests ([ISR; addr n6] and [CSTAT; addr 06]). In Hardware Mode, $\overline{\text{IRQ}}$ is the logical NOR of the four internal transmitter driver performance monitor outputs.
JSEL(2:0)	Jitter Attenuator Select	I^P	Applicable only in Hardware Mode. The JSEL and JDIR pins determine the JAT configuration. JSEL(2:0) enables and selects the JAT depth as shown in the table below. SDI/JSEL(2) and $\overline{\text{CS}}$ /JSEL(1) are dual function pins. JSEL(2:0) — JAT Mode 000 — 8 bits 001 — 16 bits 010 — 32 bits 011 — 64 bits 100 — 128 bits 111 — Disable JAT
JDIR	Jitter Attenuator Direction	I^P	Applicable only in Hardware Mode. JDIR determines the path in which the JAT is inserted. If JDIR is low, the JAT (if enabled) is placed in the receive path; if high, the JAT (if enabled) is placed in the transmit path. Refer to the description for JSEL(2:0). SCLK/JDIR is a dual function pin.
JATERR[1:4]	Jitter Attenuator Error	O	Applicable only in Hardware Mode. A high on JATERR indicates an overflow or underflow error in the jitter attenuator elastic store. JATERR(1) / SDO is a dual function pin.

Table 1-1. Hardware Signal Definitions *(4 of 5)*

Pin Label	Signal Name	I/O	Definition
$\overline{\text{RLOS}}$ [1:4]	Receive Loss of Signal	O	$\overline{\text{RLOS}}$ is asserted low when 100 (T1) or 32 (E1) consecutive 0s (no pulses) are received at the line interface or when the received signal level is approximately 18 dB below nominal for at least 1 ms.
$\overline{\text{LLOOP}}$ [1:4] $\overline{\text{RLOOP}}$ [1:4]	Local Loop Remote Loop	I^P I^P	These pins are always enabled in Hardware Mode and may be enabled or disabled in Host Mode [LIU_CTL; addr n3]. A low on LLOOP initiates Local Analog Loopback and a low on RLOOP initiates Remote Line Loopback. Local Digital Loopback is initiated if both signals are asserted together.
Boundary Scan Signals (JTAG)			
TDO	Test Data Output	O	Test data output per IEEE Std. 1149.1-1990. Three-state output used for reading all serial configuration and test data from internal test logic. Updated on the falling edge of TCK.
TDI	Test Data Input	I^P	Test data input per IEEE Std. 1149.1-1990. Used for loading all serial instructions and data into internal test logic. Sampled on the rising edge of TCK. TDI may be left unconnected if not used.
TMS	Test Mode Select	I^P	Active-low test mode select input per IEEE Std 1149.1-1990. Internally pulled-up input signal used to control the test logic state machine. Sampled on the rising edge of TCK. TMS may be left unconnected if not used.
TCK	Test Clock	I^P	Test clock input per IEEE Std. 1149.1-1990. Used for all test interface and internal test-logic operations. If not used, TCK should be pulled low.
$\overline{\text{TRST}}$	Reset	I^P	Active low reset. $\overline{\text{TRST}}$ is pulled up internally and may be left unconnected if not used.
Host Serial Control Signals			
$\overline{\text{CS}}$	Chip Select	I^P	In Host Mode, $\overline{\text{CS}}$ is an active low input used to enable read/write access with the host serial control port. $\overline{\text{CS}}$ /JSEL(1) is a dual function pin.
SDI	Serial Data In	I^P	In Host Mode, SDI is the serial data input for the host serial control port. SDI/JSEL(2) is a dual function pin.
SDO	Serial Data Out	O	In Host Mode, SDO is the serial data output for the host serial control port. SDO/JATERR[1] is a dual function pin.
SCLK	Serial Clock	I^P	In Host Mode, SCLK is the serial clock input for the host serial control port. SCLK/JDIR is a dual function pin.
Power Supply Pins and No-Connect Pins			
VAA GND	Analog Supply Ground	I	+3.3 V $\pm$ 5%. Power supply pair for the analog circuitry.
VAAT[1:4] GNDT[1:4]	Tx Driver Supply Ground	I	+3.3 V $\pm$ 5%. Power supply pairs for the transmitter driver circuitry. These pin pairs should each be bypassed with a tantalum capacitor value of at least 10 µF.
VAAR GNDR	Rx Analog Supply Ground	I	+ 3.3 V $\pm$ 5%. Power supply pair for the analog receiver circuitry.

Table 1-1. Hardware Signal Definitions *(5 of 5)*

Pin Label	Signal Name	I/O	Definition
VAACL GNDCL	CLAD Supply Ground	I	+ 3.3 V ± 5%. Power supply pair for the CLAD PLL circuitry.
VDD VSS	Digital Supply Ground	I	+ 3.3 V + 5%. Power supply pairs for the digital circuitry.
VGG	ESD Rail	I	To insure 5 V tolerance in mixed + 5 V / + 3.3 V systems, this input must be connected to + 5 V. If all logic input signals are 3.3 V levels, then this pin may be connected to the 3.3 V supply.
N.C.	No Connect	—	No-connect pins are reserved for future device compatibility and should be left unconnected.

NOTE(S):

1. I/O Types:
   - I = Standard input
   - I^P = Input with internal pull-up resister
   - O = Standard output
   - O^D = Output with open drain
2. Legend:
   - [#] = Port number
   - (#) = Bit number

2.0 Circuit Description

2.1 Overview

The CN8380 includes four identical T1/E1 transceiver channels and a common CLAD packaged in a 128-pin MQFP carrier. It is designed to interface T1/E1 framers, or to operate as a stand-alone line interface for synchronous or plesiochronous mappers and multiplexers. The CN8380 is ideal for high line density, short-haul applications that require low power (3.3 V supply) operation. The configurable T1/E1 operation and common line interface design allows support for single-board T1 and E1 designs.

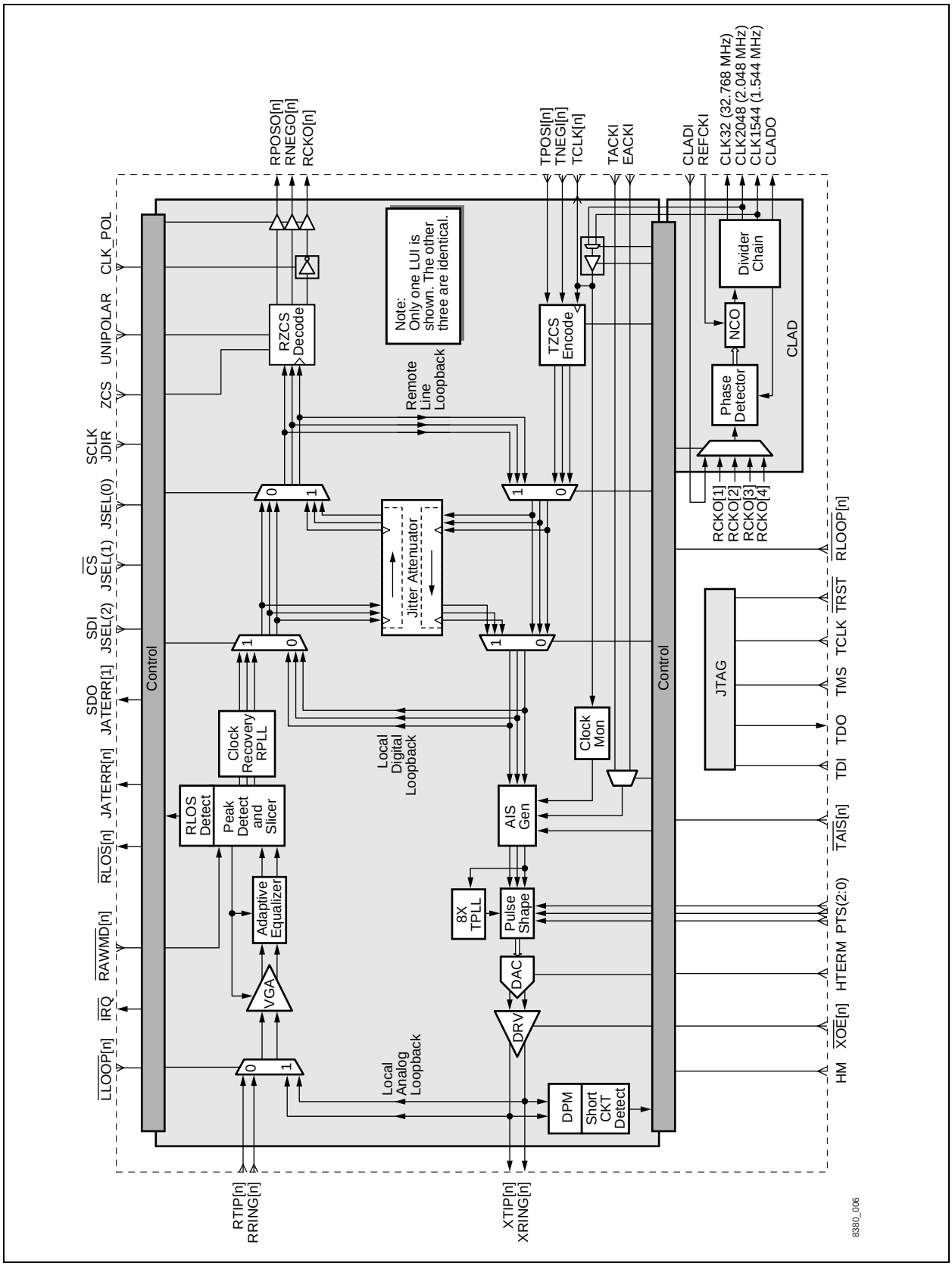
Customer premise applications are supported by an on-chip JAT which conforms to AT&T PUB 62411 and a selectable transmit pulse shape which conforms to FCC Part 68, Pulse Option A. Selectable unipolar or bipolar interface options and internal ZCS encoding and decoding are useful in many multiplexer and mapper applications.

In the most simple configuration, Hardware Mode, the device is controlled using dedicated hardware control pins. In this mode, the four channels are configured globally to identical operating modes (T1, E1, transmit termination, jitter attenuators, and so on). Each channel has device pins dedicated for channel control and status, such as loopback controls, bipolar/unipolar interface modes, and loss of signal indicators. Hardware Mode is selected by pulling the HM pin high.

Host Mode allows control of the device through a 4-line serial port. In this mode, all control and status functions can be accessed using internal registers. Several additional features are also available in Host Mode, such as individual channel operating mode configuration (T1/E1, transmit termination, jitter attenuators, etc.) and programmable CLAD output frequencies. Host Mode is selected by grounding the HM pin.

The CN8380 incorporates printed circuit board testability circuits in compliance with IEEE Std P1149.1a–1993, IEEE Standard Test Access Port and Boundary–Scan Architecture, commonly known as JTAG (Joint Test Action Group). A detailed block diagram is displayed in Figure 2-1.

Figure 2-1. Detailed Block Diagram



2.2 Configuration and Control

2.2.1 Hardware Mode

In Hardware Mode, the device is controlled using dedicated hardware control pins. In this mode, the four channels are configured globally to identical operating modes (T1, E1, transmit termination, jitter attenuators, and so on). Each channel has device pins dedicated for channel control and status, such as loopback controls, bipolar/unipolar interface modes, and loss of signal indicators. Refer to Table 1-1, *Hardware Signal Definitions*, for a description of all hardware pins. Hardware Mode is selected by pulling the HM pin high.

2.2.2 Host Mode

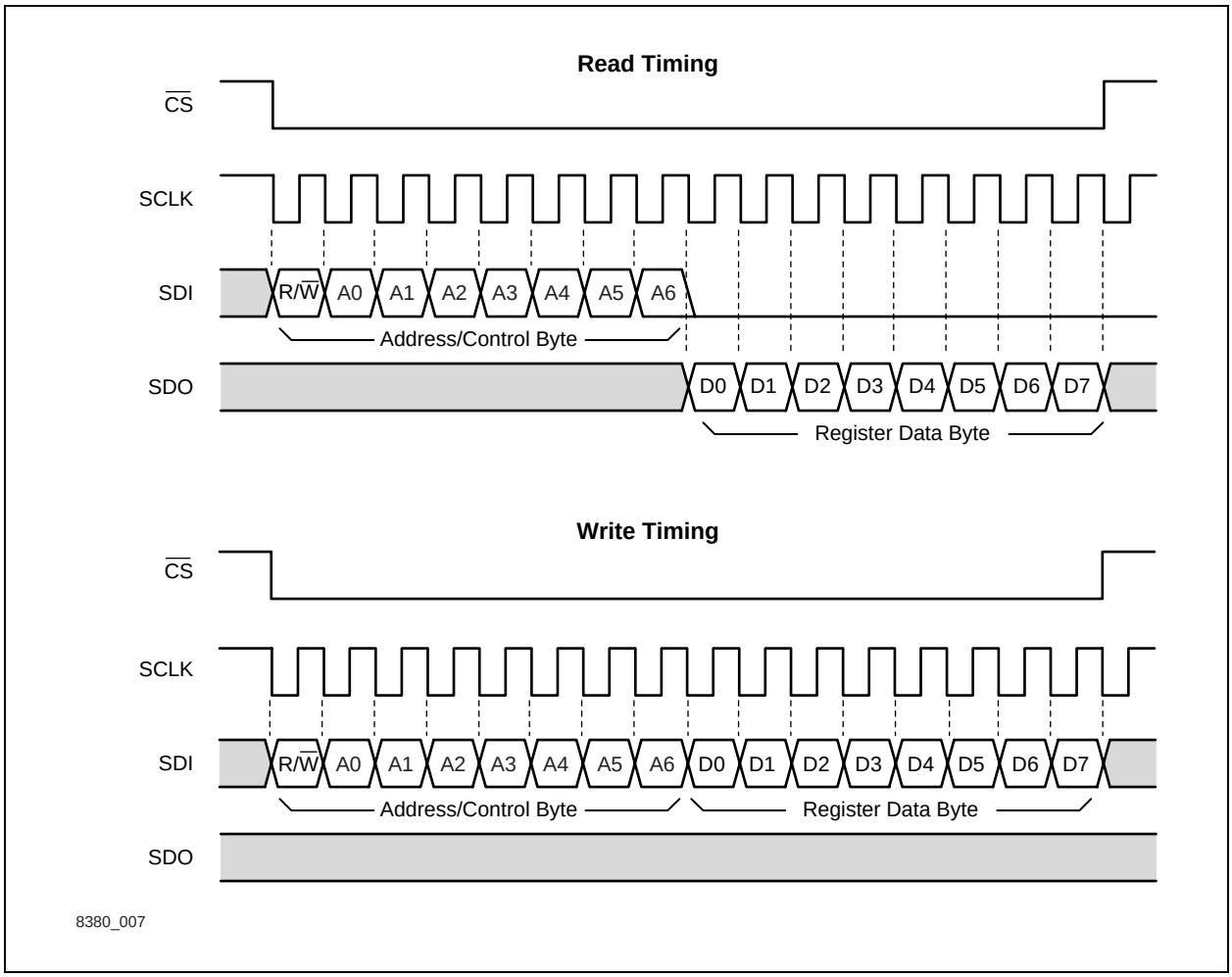
In Host Mode, control of the device is through a four-line serial port. In this mode, all control and status functions can be accessed using internal registers. Refer to Chapter 3.0, *Registers*, for a description of each register. Host Mode is selected by grounding the HM pin.

2.2.3 Host Serial Control Interface

The CN8380 serial interface is a four-wire, slave interface which allows a host processor or framer with a compatible master serial port to communicate with the LIU. This interface allows the host to control and query the CN8380 status by writing and reading internal registers. One 8-bit register in the LIU can be written via the SDI pin or read from the SDO pin at the clock rate determined by SCLK. The serial port is enabled by pulling the chip select pin, $\overline{CS}$, active (low) during the read and write cycles. Refer to Figure 2-2 for host serial port signals.

The serial interface uses a 16-bit process for each write or read operation. During a write or read operation, an 8-bit control word, consisting of a read/write control bit (R/W) and a 7-bit LIU register address (A[6:0]) is transmitted to the LIU using the SDI pin. If the operation is a write operation (R/W = 0), an 8-bit register data (D[7:0]) byte follows the address on the SDI pin. This data is received by the CN8380 and stored in the addressed register. If the operation is a read operation (R/W = 1), the CN8380 outputs the addressed register contents on the SDO pin. The signal input on SDI is sampled on the SCLK falling edge, and data output on SDO changes on the SCLK rising edge.

Figure 2-2. Host Serial Port Signals



2.2.4 Reset

The CN8380 supports three reset methods: power-on reset, hard reset initiated by the $\overline{\text{RESET}}$ pin, and soft reset initiated by the RESET bit in the Global Configuration Register [GCR; addr 01]. In Host Mode, all three reset methods produce the same results as listed below. In Hardware Mode, power-on reset and hard reset produce the same results as shown; and soft reset is not applicable. After RESET is complete, the following is true:

Hardware Mode	Host Mode
Digital receiver outputs (RPOSO[1:4] and RNEGO[1:4], RCKO[1:4]) are enabled.	Digital receiver outputs (RPOSO[1:4] and RNEGO[1:4], RCKO[1:4]) are three-stated.
Transmitter line outputs (XTIP[1:4] and XRING[1:4]) are enabled (controlled by $\overline{\text{XOE}}$).	Transmitter line outputs (XTIP[1:4] and XRING[1:4]) are three-stated.

	Hardware Mode	Host Mode
	CLK1544, CLK2048, and CLADO clock outputs are enabled.	CLK1544, CLK2048, and CLADO clock outputs are three-stated.
	Transmitter clocks, TCLK[1:4], are configured as inputs.	Transmitter clocks, TCLK[1:4], are configured as inputs.
	The $\overline{\text{IRQ}}$ pin is enabled (controlled by DPM).	The $\overline{\text{IRQ}}$ pin is three-stated.
		All interrupt sources are disabled.
		All configuration registers are set to default values as listed in Section 3.1, *Address Map*.

2.2.4.1 Power-on Reset

An internal power-on reset process is initiated during power-up. When VDD has reached approximately 2.6 V, the internal reset process begins and continues for 300 ms maximum if REFCLK is applied. If REFCLK is not present, the CN8380 remains in the reset state.

2.2.4.2 Hard Reset

Hard reset is initiated by bringing the $\overline{\text{RESET}}$ pin active (low). Once initiated, the internal reset process completes in 5 µs maximum. If the $\overline{\text{RESET}}$ pin is held active continuously, the clock and data outputs and the $\overline{\text{IRQ}}$ pin remain three-stated. The following output pins are forced to high impedance while $\overline{\text{RESET}}$ is held active:

RPOSO[1:4]	CLADO
RNEGO[1:4]	TCLK[1:4]
RCKO[1:4]	$\overline{\text{IRQ}}$
XTIP[1:4]	$\overline{\text{RLOS}}$[1:4]
XRING[1:4:]	JATERR[1:4]
CLK1544	SDO
CLK2048	TDO

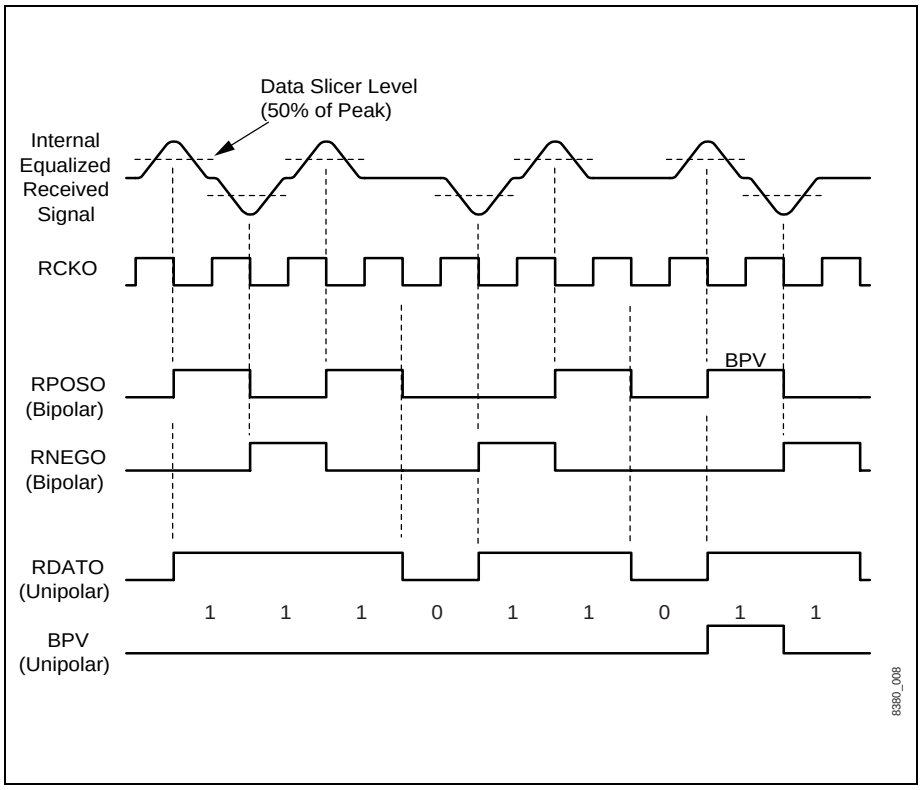
2.2.4.3 Soft Reset

In Host Mode, soft reset is initiated by writing a one to the RESET bit in the Global Configuration register [addr 01]. The RESET bit is self-clearing. Once initiated, the internal reset process completes in 5 µs maximum and the device enters normal operation.

2.3 Receiver

Bipolar AMI pulses are input on the receiver input pins, RTIP[n] and RRING[n]. The receiver recovers clock and data from the AMI signal which has been attenuated and distorted due to the line characteristics. The AMI pulses are converted into bipolar or unipolar, NRZ data and output on RPOSO[n] and RNEGO[n], along with the recovered clock on RCKO[n]. Figure 2-3 illustrates the relationship between the AMI received signal, the recovered clock, and the data outputs. This section discusses each receiver block from the line input to the digital outputs.

Figure 2-3. Receiver Signals



2.3.1 Data Recovery

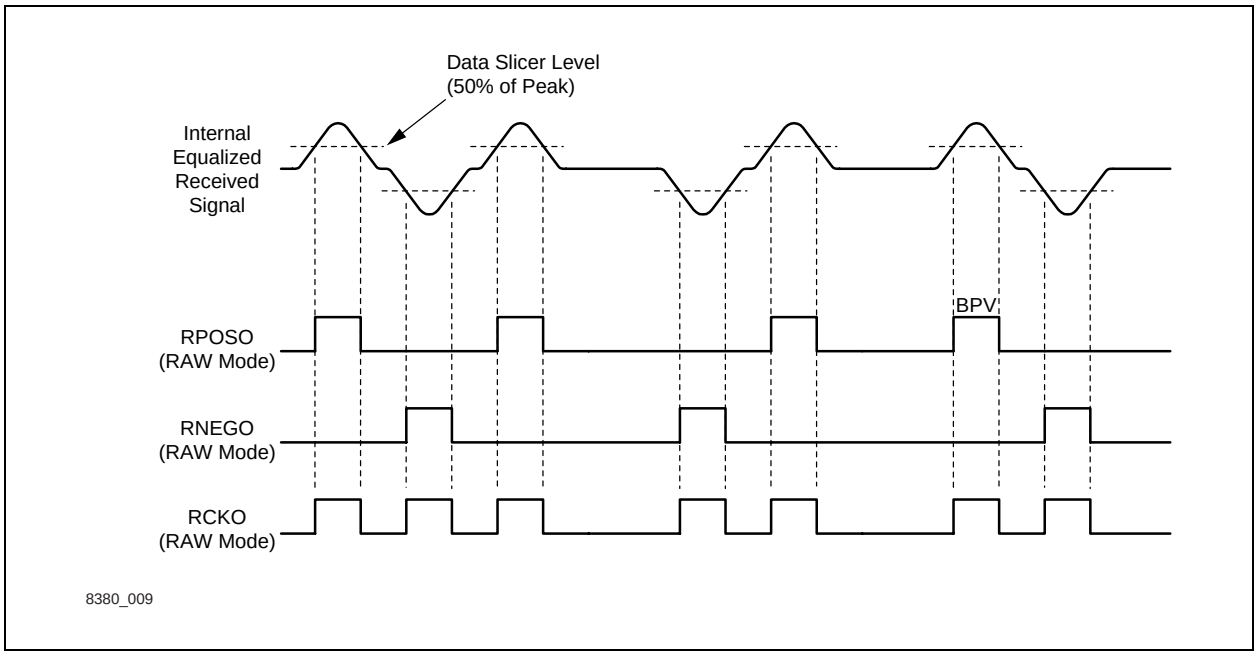
The receiver recovers data by normalizing the input signal with an automatic gain control (AGC) circuit, removing distortion with an equalizer, and extracting the data using a data slicer. The transfer function of the equalizer is adjusted based on the average peak value of the input signal. The AGC maintains the equalizer's average peak output level to a constant value. The data slicer compares the equalizer output to a threshold value equal to 50% of the average peak equalizer output level and produces both positive and negative pulse detect signals. The data slicer outputs are re-timed using the recovered clock and routed to the RZCS decoder (or to the JAT).

2.3.1.1 Raw Receive Mode

Optionally, the data slicer outputs, before re-timing, can be routed directly to the RPOSO and RNEGO digital output pins. This option (raw receive mode) is selected by asserting the $\overline{\text{RAWMD}}$[n] pin in Hardware Mode or by asserting the RAWMD register bit [RLIU_CR; addr n1] in Host Mode. In raw receive mode, RCKO is replaced by the logical OR of the RPOSO and RNEGO output signals.

This mode is useful in applications which provide external clock and data recovery. Figure 2-4 illustrates the raw mode receiver signals.

Figure 2-4. Raw Mode Receiver Signals



2.3.1.2 Sensitivity

The receiver is capable of recovering signals with cable attenuation in the range of +3 to –12 dB in E1 and T1 modes. The receiver is configured by setting register bits appropriately in Host Mode or by setting configuration pins in Hardware Mode. See Table 2-1for line compatible modes.

Table 2-1. Line Compatible Modes

Mode	Receiver Sensitivity	RALOS Threshold	Squelch Threshold	RLOS Detect
T1	+3 dB to –12 dB	–18 dB	–18 dB	100 zeros
T1/E1 20 dB Bridge	–17 dB to –26 dB	NA	NA	100 zeros
E1	+3 dB to –12 dB	–18 dB	–18 dB	32 zeros

2.3.1.3 Bridge Mode

In Host Mode, the receiver allows interfacing to network test (MON) points which are resistively attenuated with resisters in series with transmit and receive Tip and Ring signals. The Bridge Monitor Level is –20 dB. Bridge operation is enabled by setting register bit ATTEN [addr n1] to 1. In this mode, RALOS detection and squelch operation are disabled.

2.3.1.4 Loss Of Signal Detector

The Receive Loss of Signal (RLOS) Detector monitors both consecutive 0s and signal level. Receive Analog Loss Of Signal (RALOS) is declared when RTIP/RRING input signal amplitude is a certain level (RALOS level) below the nominal receive level for at least 1 ms (2 ms maximum). RALOS status is cleared as soon as pulses above the RALOS level are detected.

In Host Mode, the received data can be replaced with all 0s (squelched) if the receive level is also below the SQUELCH level. Squelch is enabled in register RLIU_CR [addr n1]. In Host Mode, RALOS real time status is reported in the ALARM [addr n5] register; and an interrupt status bit is available in the ISR [addr n6] register. Also, RALOS is indicated on the $\overline{\text{RLOS}}$[n] pin, which is the logical NOR of the RLOS[n] status and RALOS[n] status.

RLOS is declared when 100 (T1) or 32 (E1) consecutive bits with no pulses are detected. RLOS status is cleared when pulses are received with at least 12.5% pulse density (during a period of 192 bits starting with the receipt of a pulse) and where no occurrences of 100 or 32 consecutive bits with no pulses are detected. In Host Mode, RLOS real time status is reported in the ALARM register [addr n5]; and an interrupt status bit is available in the ISR register [addr n6]. Also, RLOS is indicated by a 0 level on the $\overline{\text{RLOS}}$[n] pin, which is the logical NOR of the RLOS[n] status and RALOS[n] status.

2.3.2 Clock Recovery

2.3.2.1 Phase Lock Loop

The Receive Phase Lock Loop (RPLL) recovers the line rate clock from the data slicer dual-rail outputs. The RPLL generates a recovered clock that tracks jitter in the data and sustains the data-to-clock phase relationship in the absence of incoming pulses. The RPLL is a digital PLL which adjusts its output phase in 1/16 unit interval (UI) steps. Consequently, the RPLL adds approximately 0.12 UI peak-to-peak jitter to the recovered receive clock.

During loss of signal (RLOS or RALOS), the RPLL maintains an output clock signal and smoothly transitions to a nominal line rate frequency determined by the CLAD input reference (selected by CMUX [GCR; addr 01] or FREE [CLAD_CR; addr 02]). If the CLAD reference is the recovered received clock from a channel which has detected RLOS, the CLAD outputs and the recovered received clock enter a “hold-over” state to maintain the average frequency that was present just before the RLOS was detected.

2.3.2.2 Jitter Tolerance

Figure 2-8, *Receiver Input Jitter Tolerance*, illustrates the receiver’s jitter tolerance for all jitter attenuator (JAT) configurations: JAT disabled and JAT enabled in the receive path with each JAT elastic store size. The jitter tolerance of the clock and data recovery circuit alone (not including the JAT) is illustrated by the curve labeled with “JAT Disabled.” The receiver meets jitter tolerance specifications TR62411, G.823, and G.824. In addition, the receiver meets jitter tolerance tests defined in ETS300 011: ISDN; *Primary Rate User-Network Interface Layer 1 Specification and Test Principles*.

2.3.3 Receive Jitter Attenuator

The data slicer outputs can be routed to the JAT before going to the RZCS decoder. The JAT attenuates clock and data jitter introduced by the line or added by the clock recovery circuit. The JAT can be placed in the receive path or transmit path, but not in both simultaneously. If the JAT is placed in the receive

path, RCKO is replaced with the jitter attenuated clock. The JAT performance is discussed in Section 2.6, *Jitter Attenuator*.

In Host Mode, the JAT is configured for each channel independently and is put in the receive path by setting JEN and JDIR register bits to 1 [JAT_CR; addr n0]. In Hardware Mode, the JAT is configured for all channels globally using the JSEL(2:0) and JDIR pins. Refer to Chapter 1.0, *Pin Descriptions* for details.

2.3.4 RZCS Decoder

The RZCS decoder decodes the dual-rail data from the data slicer or from the JAT. In T1 mode, the RZCS decoder replaces received B8ZS codes with eight 0s. In E1 mode, HDB3 codes are replaced with four 0s. The B8ZS code is 000VB0VB and the HDB3 code is X00V; where B is a normal AMI pulse, V is a bipolar violation, and X is a don't-care.

ZCS decoding (and encoding) can be enabled only if the digital interface mode is unipolar. In Host Mode, RZCS decoding (and TZCS encoding) is enabled for each channel by setting the ZCS [RLIU_CR; addr n1] register bit to 1. In Hardware Mode, ZCS encoding/decoding is controlled globally for all channels by pulling the ZCS pin high. For the Hardware Mode pin definition, see Table 1-1.

2.3.5 Receive Digital Interface

The digital receiver outputs are provided on the RPOSO[n], RNEGO[n], and RCKO[n] pins, where [n] is channel number 1 to 4. The receiver outputs can be configured to operate in two modes: Bipolar NRZ format or unipolar NRZ format. In both modes, RPOSO[n] and RNEGO[n] outputs are clocked by RCKO[n], the recovered line rate clock, or the jitter attenuated clock if the JAT is enabled in the receive path. RCKO[n] polarity is configurable by the CLK_POL pin in Hardware Mode or register bit CLK_POL [RLIU_CR; addr n1] in Host Mode. RPOSO[n], RNEGO[n], and RCKO[n] are three-stated during device reset.

2.3.5.1 Bipolar Mode

In bipolar mode, RPOSO/RNEGO signals output received data in bipolar dual-rail format, where a high level on RPOSO indicates receipt of a positive AMI pulse, and a high level on RNEGO indicates receipt of a negative AMI pulse on RTIP/RING inputs. In bipolar mode, the RZCS decoder is not available. In Hardware Mode, bipolar operation is enabled globally for all channels by pulling the UNIPOLAR pin low. In Host Mode, bipolar operation is enabled per channel by writing a 0 to register bit UNIPOLAR [RLIU_CR; addr n1].

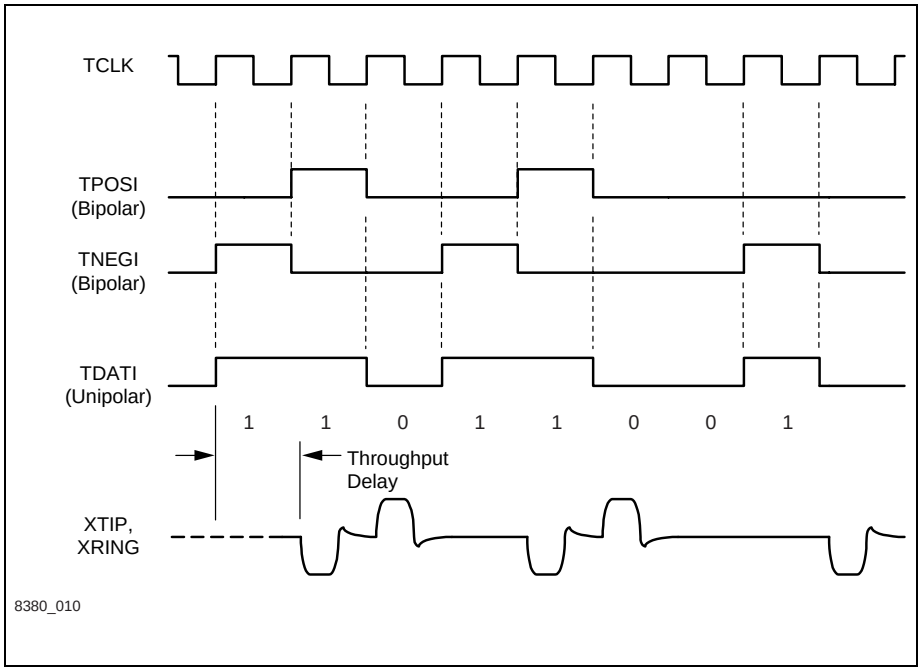
2.3.5.2 Unipolar Mode

In unipolar mode, RPOSO/RNEGO signals are replaced by RDATO/BPV signals. AMI encoded received data is decoded and output on RDATO in NRZ format, and BPV indicates that the currently received bit is a bipolar violation. If the RZCS decoder is enabled, the BPV pin indicates only bipolar violations which are not part of a ZCS code (B8ZS or HDB3). In Hardware Mode, unipolar operation is enabled by pulling the UNIPOLAR pin high. In Host Mode, unipolar operation is enabled by writing a 1 to register bit UNIPOLAR [RLIU_CR; addr n1].

2.4 Transmitter

Bipolar or unipolar, NRZ digital transmit data are input on TPOSI and TNEGI using the transmit clock TCLK. Data are converted into AMI pulses, shaped according to required standards, and transmitted to the line. Figure 2-5 illustrates the relationship between the AMI transmitted signal, the transmit clock, and the data inputs. This section discusses each transmitter block, from the digital inputs to the line output.

Figure 2-5. Transmitter Signals



2.4.1 Transmit Digital Interface

The digital transmitter inputs, TPOSI[n] and TNEGI[n], accept bipolar or unipolar NRZ formatted data for transmission and are sampled by the falling edge of TCLK[n], where [n] is channel number 1 to 4. TCLK[n] is the line rate transmit clock and is normally supplied externally from a line rate source, but can also be sourced internally (only in Host Mode) from the CLAD. If sourced internally, TCLK[n] is configured as an output to provide the line rate clock to external circuitry. TCLK[n] direction is configured globally for all channels by writing to register bit TCLK_I/O [GCR; addr 01].

2.4.1.1 Bipolar Mode

In bipolar mode, TPOSI/TNEGI inputs accept bipolar dual-rail transmit data where a high on TPOSI causes a positive output pulse and a high on TNEGI causes a negative output pulse on XTIP/XRING. In this mode, the TZCS encoder is not available. In Hardware Mode, bipolar operation is enabled globally for all channels by pulling the UNIPOLAR pin low. In Host Mode, bipolar operation is

enabled per channel by writing a 0 to register bit UNIPOLAR [RLIU_CR; addr n1].

2.4.1.2 Unipolar Mode

In unipolar mode, TPOSI is replaced with TDATI and accepts unipolar NRZ-formatted transmit data. TNEGI is not used in this mode. A high on TDATI causes an AMI pulse to be transmitted to the line. In this mode, the TZCS encoder can be enabled to provide B8ZS or HDB3 zero code suppression. In Hardware Mode, unipolar operation is enabled globally for all channels by pulling the UNIPOLAR pin high. In Host Mode, unipolar operation is enabled per channel by writing a 1 to register bit UNIPOLAR [RLIU_CR; addr n1].

2.4.2 TZCS Encoder

If enabled, the TZCS encoder encodes unipolar transmit data on TDATI with B8ZS (T1) or HDB3 (E1) line coding. In T1 mode, eight consecutive 0s are replaced with 000VB0VB; and in E1 mode, four consecutive 0s are replaced with X00V; where B is a normal AMI pulse, V is a bipolar violation, and X is a Don't Care. These are standard T1 and E1 line code options.

ZCS encoding (and decoding) can be enabled only if the digital interface mode is unipolar. In Host Mode, TZCS encoding (and RZCS decoding) is enabled for each channel by setting the ZCS [RLIU_CR; addr n1] register bit to 1. In Hardware Mode, ZCS encoding/decoding is controlled globally for all channels by pulling the ZCS pin high. For the Hardware Mode pin definition, refer to Table 1-1.

2.4.3 Transmit Jitter Attenuator

Transmit data from the TZCS encoder can be routed to the JAT before going to the AIS Generator. The JAT attenuates clock and data jitter from the transmit inputs or from the receiver if Remote Line Loopback (RLL) is active. The JAT can be placed in the receive path or transmit path, but not both simultaneously. If the JAT is placed in the transmit path, the jitter attenuated clock becomes the transmit clock for downstream circuits.

In Host Mode, the JAT is configured for each channel independently and is put in the transmit path by setting the JEN register bit to 1 and the JDIR register bit to 0 [JAT_CR; addr n0]. In Hardware Mode, the JAT is configured for all channels globally using the JSEL(2:0) and JDIR pins. For pin definitions, refer to Chapter 1.0, *Pin Descriptions*; for JAT transfer characteristics, refer to Figure 2-9; and for more information on loopbacks, refer to Section 2.5, *Loopbacks*.

2.4.4 All 1s AIS Generator

The transmit data can be replaced with unframed all 1s for transmitting the alarm indication signal (AIS). This includes replacing data supplied from TPOSI[n]/TNEGI[n] pins and from the receiver during RLL. AIS transmission does not affect transmit data that is looped back to the receiver during Local Digital Loopback (LDL). This allows LDL to be active simultaneously with the transmission of AIS. AIS is used to maintain a valid signal on the line and to inform downstream equipment that the transmit data source has been lost. AIS transmission can be done manually or automatically when loss of transmit clock is detected. A clock monitor circuit allows manual or automatic switching of the transmit clock to an alternate AIS clock.

In Hardware Mode, AIS can be controlled only manually by pulling the $\overline{\text{TAIS}}$[n] hardware pin low. If TCLK[n] is present, then it is used to transmit AIS. If TCLK[n] is not present (for two clock periods), the alternate AIS clock on either TACKI (T1 Mode) or EACKI (E1 Mode) is used. The AIS transmit clock switches back to TCLK[n] when the TCLK[n] signal returns.

In Host Mode, AIS can be transmitted using the $\overline{\text{TAIS}}$[n] hardware pins or the TAIS register bit, or automatically by enabling the AUTO_AIS register bit. AIS clock switching can be enabled by using the AISCLK register bit. Setting AISCLK to 1 forces the use of the alternate AIS clock on either TACKI (T1 Mode) or EACKI (E1 Mode) pins when transmitting AIS. If AUTO_AIS is set to 1, AIS is automatically transmitted when the clock monitor detects loss of clock on TCLK[n]. When using automatic AIS transmission, the user should also enable the AISCLK bit and provide an alternate clock source to insure that AIS will be transmitted. CLAD output clocks CLK2048 and CLK1544 can be connected externally to EACKI and TACKI alternate AIS clock inputs for this purpose. Setting register bit TAIS_PE to 1 disables the TAIS register bit and allows manual transmission of AIS using the $\overline{\text{TAIS}}$[n] hardware pins. Refer to LIU_CTL [addr n3] in Chapter 3.0, *Registers*, and to Table 1-1, *Hardware Signal Definitions*.

If TAIS is activated when Remote Line Loopback is active, AIS is transmitted using the received clock (or JCLK if the JAT is enabled in the receive direction). Table 2-2 lists transmitter operating modes resulting from various configuration settings and input conditions.

Table 2-2. Transmitter Operating Modes

Configuration and Input Status					Transmitter Mode	
RLOOP (W/LLOOP=0)	**TLOC**	**TAIS**	**AUTO_AIS**	**AISCLK**	**Transmit Data**	**Transmit Clock**
0	X	0	0	X	Tx Data	TCLK
0	X	1	X	0	AIS	TCLK
0	X	1	X	1	AIS	TACKI/EACKI
0	0	0	1	X	Tx Data	TCLK
0	1	0	1	0	AIS	TCLK
0	1	0	1	1	AIS	TACKI/EACKI
1	X	0	X	X	Rx Data	RCLK
1	X	1	X	X	AIS	RCLK

NOTE(S): X is don't-care.

2.4.5 Pulse Shaper

All transmit pulse shaping to meet E1 and T1 transmission standards is done internally, eliminating the need for external shaping circuitry. The pulse shape block receives bipolar NRZ transmit data, produces a set of eight 5-bit values which define the pulse shape, and converts the shape values into an analog pulse using a DAC. Table 2-3 lists the transmit pulse template selections and applications.

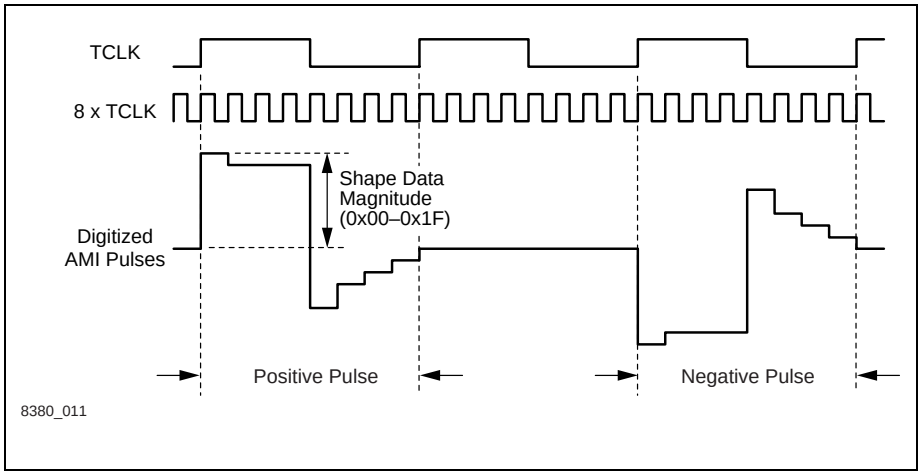
Table 2-3. Transmit Pulse Configurations

Application	Line Rate	Line Length	Hardware Mode Configuration PTS(2:0)	Host Mode Configuration [TLIU_CR; addr n2] PULSE(2:0)
DSX-1 T1.102 CB119 100 Ω Twisted Pair	T1	0–133 ft.	000	000
	T1	133–266 ft.	001	001
	T1	266–399 ft.	010	010
	T1	399–533 ft.	011	011
	T1	533–655 ft.	100	100
ITU–T G.703 75 Ω Coaxial Cable	E1	—	101	101
ITU–T G.703 120 Ω Twisted Pair	E1	—	110	110
FCC Part 68 Opt A I.431 100 Ω Twisted Pair	T1	—	111	111

In Hardware Mode, standard pulse templates are selected globally for all channels using hardware pins PTS(2:0). Refer to the Chapter 1.0, *Pin Descriptions*, and Table 1-1, *Hardware Signal Definitions*.

In Host Mode, standard pulse templates are selected per channel by writing to register bits PULSE(2:0) [TLIU_CR; addr n2]. If desired, custom pulse shapes can be programmed for each channel using the SHAPEn [addr n8 – nF] registers and the PPT [TLIU_CR; addr n2] register bit. The data written into the SHAPEn registers is 5-bit magnitude only. The first four code values of the pulse define the first half of the symbol, and the last four values define the last half of the symbol. The last half symbol polarity is always forced to be opposite from the first half polarity. Figure 2-6 illustrates the shaped transmit signals.

Figure 2-6. Transmit Pulse Shape



2.4.6 Driver

The transmit DAC converts digitally shaped AMI pulses into analog bipolar signals. The line driver provides a high impedance, current drive for the transmit DAC and outputs transmit signals to the XTIP[n] and XRING[n] output pins. The high impedance driver allows line impedance matching using external parallel resistors to meet return loss requirements. In applications which require surge protection, pulse amplitude compensation is provided if protection resistors are needed in series with XTIP[n] and XRING[n]. When a shorted line is detected, transmit monitor and protection circuits reduce the output current level to less than 50 mA peak. The standard transmit transformer for the CN8380 has a turns ratio of 1:2 (chip-side: line-side). To minimize power consumption, an alternate 1:1.36 turns ratio transformer can be used in an unterminated configuration.

2.4.6.1 Transmit Termination Options

Various transmitter termination options are available to meet almost any interface requirement. Figure 2-7 illustrates the location of the transmit termination components. In this figure, Ct is a smoothing capacitor across XTIP and XRING. The recommended value for Ct is 150 pF. If other components are also connected to XTIP/XRING, such as surge protection diodes, Ct's value should be adjusted to maintain a total parallel capacitance of approximately 150 pF.

Rt is a parallel termination resistor selected to provide the required transmitter return loss, typically –18 dB. If an application does not have a return loss requirement, Rt can be omitted in order to reduce total power consumption.

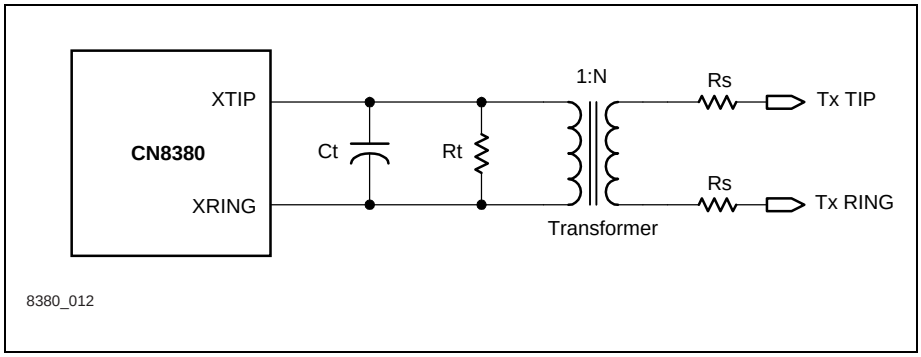
The standard transformer recommended has a turns ratio of 1:2. This turns ratio is required if parallel termination (Rt) or series resistors (Rs) are desired. The alternate transformer has a turns ratio of 1:1.36. This transformer can be used only if all of the following are true:

- Parallel termination (Rt) is not used.
- Series resistors (Rs) are not used.
- T1 DSX-1 transmit pulse is not used.

Refer to Option E in Table 2-7 below. Transmitter power consumption is reduced by approximately 30%, compared to the unterminated, standard transformer configuration.

Resistors (Rs) in series with Tx TIP and Tx RING line connections are sometimes used with surge protection circuits. Without compensation, the addition of these resistors decreases the transmit pulse amplitude. The CN8380 provides an option in Host Mode to boost the output level if resistors are installed. Compensation is optimized for the use of 5.6 Ω Rs values. In Hardware Mode, these resistors are required.

Figure 2-7. Transmit Termination Components



Tables 2-4 through 2-8 provide recommended termination component values and CN8380 configuration information for all termination options supported. The resulting return loss value is also listed. All five options are supported in Host Mode, whereas only options C and D are supported in Hardware Mode.

Before selecting a termination option, refer to Table 2-3, *Transmit Pulse Configurations*, to select an application mode. Then refer to the Transmit Termination tables below to select a termination option.

Option A Option A uses the standard 1:2 transformer, no series protection resistors (Rs), and no parallel termination (Rt) for T1 applications. In E1 applications, Rt is included because it is usually required to provide a minimal level of line impedance matching.

Table 2-4. Transmit Termination Option A

Application	Series Resistors (Rs)	Parallel Termination (Rt, Ω)	Return Loss (dB)
T1—DSX-1	None	None	0
E1—75 Ω	None	126.4	–10
E1—120 Ω	None	204.4	–10
T1— I.431	None	None	0

NOTE(S):
1. Standard Transformer (1:2 turns ratio)
2. Hardware Mode: HTERM=0
3. Host Mode: ALT_TR = 0, TERM = 0, T_BOOST = 0 [TLIU_CR; addr n2]

Option B Option B uses the standard 1:2 transformer and no series protection resistors (Rs). A common parallel termination (Rt) for both T1 and E1 applications is included to provide line impedance matching.

Table 2-5. Transmit Termination Option B

Application	Series Resistors (Rs)	Parallel Termination (Rt, Ω)	Return Loss (dB)
T1—DSX-1	None	23.7	–30
E1—75 Ω	None	23.7	–18
E1—120 Ω	None	23.7	–18
T1— I.431	None	23.7	–30

NOTE(S):
1. Standard Transformer (1:2 turns ratio)
2. Hardware Mode: Not applicable
3. Host Mode: ALT_TR = 0, TERM = 1, T_BOOST = 0 [TLIU_CR; addr n2]

Option C Option C uses the standard 1:2 transformer and no parallel termination (Rt) for T1 applications. In E1 applications, Rt is included because it is usually required to provide a minimal level of line impedance matching. Series protection resistors (Rs) are included. Option C is available only in Host Mode.

Table 2-6. Transmit Termination Option C

Application	Series Resistors (Rs)	Parallel Termination (Rt, Ω)	Return Loss (dB)
T1—DSX-1	2 × 5.6 Ω	None	0
E1—75 Ω	2 × 5.6 Ω	114.8	–10
E1—120 Ω	2 ×5.6 Ω	190.0	–10
T1—I.431	2 × 5.6 Ω	None	0

NOTE(S):
1. Standard Transformer (1:2 turns ratio)
2. Hardware Mode: HTERM = 0
3. Host Mode: ALT_TR = 0, TERM = 0, T_BOOST = 1 [TLIU_CR; addr n2]

Option D Option D uses the standard 1:2 transformer. A common parallel termination (Rt) for both T1 and E1 applications is included to provide line impedance matching. Series protection resistors (Rs) are also included. Option D is available in both Host Mode and Hardware Mode.

Table 2-7. Transmit Termination Option D

Application	Series Resistors (Rs)	Parallel Termination (Rt, Ω)	Return Loss (dB)
T1—DSX-1	2 × 5.6 Ω	21	–30
E1—75 Ω	2 × 5.6 Ω	21	–18
E1—120 Ω	2 × 5.6 Ω	21	–18
T1—I.431	2 × 5.6 Ω	21	–30

NOTE(S):
1. Standard Transformer (1:2 turns ratio)
2. Hardware Mode: HTERM = 1
3. Host Mode: ALT_TR = 0, TERM = 1, T_BOOST = 1 [TLIU_CR; addr n2]

Option E Option E uses the alternate 1:1.36 transformer, no series protection resistors (Rs), and no parallel termination (Rt) for T1 applications. In E1 applications, Rt is included because it is usually required to provide a minimal level of line impedance matching. Option E is available only in Host Mode and cannot be used with DSX-1 applications.

Table 2-8. Transmit Termination Option E

Application	Series Resistors (Rs)	Parallel Termination (Rt, Ω)	Return Loss (dB)
E1—75 Ω	None	68.1	–10
E1—120 Ω	None	107.0	–10
T1—I.431	None	None	0

NOTE(S):
1. Alternate transformer (1:1.36 turns ratio)
2. Hardware Mode: Not Applicable
3. Host Mode: ALT_TR = 1, TERM = 0, T_BOOST = 0 [TLIU_CR; addr n2]

2.4.6.2 Output Disable

The transmitter analog outputs, XTIP[n] and XRING[n], are enabled per channel by pulling the $\overline{\text{XOE}}$[n] pins low and are three-stated by pulling the $\overline{\text{XOE}}$[n] pins high. In Host Mode, the PDN [TLIU_CR; addr n2] register bit also controls the XTIP[n] and XRING[n] outputs. A device RESET sets the PDN bits, thereby disabling XTIP[n] and XRING[n]. User software must clear PDN to enable the transmitter outputs.

In Hardware Mode, the transmitter outputs are disabled while $\overline{\text{RESET}}$ is held active (low). When $\overline{\text{RESET}}$ is deactivated, $\overline{\text{XOE}}$[n] controls the transmitter outputs. If the transmit driver is disabled ($\overline{\text{XOE}}$[n] = 1), the driver performance monitor (DPM) is available for monitoring a transmit signal from an external source. Refer to Section 2.4.7.2, *Driver Performance Monitor*.

2.4.7 Transmitter Output Monitoring

2.4.7.1 Short Circuit Detect

The transmitter output pulse is monitored and a short circuit is detected when the amplitude falls below an internally determined threshold for approximately 64-bit times. The short circuit state deactivates when the amplitude rises above a second threshold for 64-bit times.

When a short is detected, the line driver current is reduced to approximately 50 mA peak, as measured on the line side of the transformer. Typically, this is caused by a transmit cable short circuit or by a transmission line transient current surge. In Host Mode, short circuit activation sets the TSHORT bit in the Alarm Status register [ALARM; addr n5] and in the Interrupt Status Register [ISR; addr n6]. No indication of short circuit is available in Hardware Mode.

2.4.7.2 Driver Performance Monitor

The DPM monitors the line driver output signal for valid signaling activity. The output signal is monitored for pulse level, invalid AMI coding, pulse density, and stuck signals. In Host Mode, a DPM fault condition sets the TLOS bit in the Alarm Status register [ALARM; addr n5] and in the Interrupt Status Register [ISR; addr n6]. In Hardware Mode, the four internal DPM status indicators are combined (logical NOR) and output on the $\overline{IRQ}$ pin.

If the transmit driver is disabled ($\overline{XOE}$ = 1), the DPM is available for monitoring a transmit signal from an external source. In this mode, XTIP[n] and XRING[n] are used as inputs and can be connected to the transmit outputs of another CN8380 channel or device.

2.5 Loopbacks

Three per-channel loopbacks are provided for system diagnostic testing: Local Analog Loopback, Local Digital Loopback, and Remote Line Loopback. Loopbacks can be controlled by either hardware pins or internal register bits. For hardware control, two dedicated pins—$\overline{\text{LLOOP}}$ and $\overline{\text{RLOOP}}$—are provided. If configured in Host Mode, register bits are provided for loopback control. In addition, the $\overline{\text{LLOOP}}$ and $\overline{\text{RLOOP}}$ pins can be enabled by register bits so that loopbacks can be controlled by the hardware pins even in Host Mode. Loopback controls are detailed in Table 2-9. Refer also to register LIU_CTL [addr n3] in Chapter 3.0, *Registers*.

Table 2-9. Loopback Control Pins

$\overline{\text{LLOOP}}$	$\overline{\text{RLOOP}}$	Loopback
1	1	None
1	0	Remote Line Loop
0	1	Local Analog Loop
0	0	Local Digital Loop

2.5.1 Local Analog Loopback

Local Analog Loopback (LAL) causes the transmit data and clock inputs (TPOSI/TNEGI and TCLK) to be looped back to the receiver outputs (RPOSO/RNEGO and RCKO). This loopback connects an internal copy of the analog transmit signal (XTIP and XRING outputs) to the receiver input, so that virtually all of the device circuitry can be tested. While LAL is active, transmit data continues to be transmitted on XTIP and XRING, but RTIP and RRING inputs are ignored. Applying a high on the $\overline{\text{XOE}}$ pin when Local Analog Loopback is active disables the transmitter outputs and causes an RLOS.

2.5.2 Local Digital Loopback

Local Digital Loopback (LDL) causes the transmit data and clock inputs (TPOSI/TNEGI and TCLK) to be looped back to the receiver outputs (RPOSO/RNEGO and RCKO). This loopback includes the JAT (if enabled) but does not include the line transmit and receive circuitry. Consequently, XTIP and XRING transmitter outputs are unaffected, and receiver RTIP and RRING inputs remain connected to the line to monitor for RLOS. Also, the AIS (all 1s) generator is not included in the loopback path so that AIS can be transmitted toward the line while simultaneously providing a local loopback.

2.5.3 Remote Line Loopback

Remote Line Loopback (RLL) causes the received data on RTIP/RRING line inputs to be looped back and re-transmitted on XTIP/XRING line outputs. This loopback includes all receive and transmit circuitry and the JAT, but does not include the ZCS decoder and encoder. If the JAT is not enabled, RLL enables the JAT in the transmit direction for the duration of the loopback. In this case, the JAT elastic store size is 8 bits. The receiver outputs (RPOSO/RNEGO and RCKO) continue to output received data; transmit inputs (TPOSI/TNEGI and TCLK) are ignored.

2.6 Jitter Attenuator

The jitter attenuator (JAT) attenuates jitter in the receive or transmit path, but not both simultaneously. The JAT path configuration and elastic store depth is controlled by the JDIR and JSEL(2:0) pins in Hardware Mode or by the JEN, JDIR, JCENTER, and JSIZE[2:0] bits in the Jitter Attenuator Configuration register [JAT_CR; addr n0] in Host Mode. The JAT can also be completely disabled.

The elastic store is configurable using the JSEL(2:0) pins or the JSIZE[2:0] bits in the JAT_CR register. The elastic store sizes available are 8, 16, 32, 64, and 128 bits. The 32-bit elastic store depth is sufficient to meet jitter tolerance requirements in all cases where the JAT cutoff frequency is 6 Hz or below, and when the selected clock reference is frequency-locked. The larger elastic store depths allow greater accumulated phase offsets. For example, the 128-bit depth can tolerate up to ±64 bits of accumulated phase offset. Because the elastic store is a fixed size, it can overflow and under-run. If either of these conditions occurs, a Jitter Attenuator Elastic Store Limit Error (JATERR) is reported. In Hardware Mode, JATERR[n] pins are provided, and in Host Mode, the JERR bit in the Interrupt Status Register [ISR; addr n6] is set.

The elastic store is a circular buffer with independent read and write pointers. These pointers can be initialized manually using JCENTER in the JAT_CR register. JCENTER resets the write pointer and forces the elastic store read pointer to one half of the programmed JSIZE. Centering is automatic as a result of a JATERR condition, so manually centering is not required.

The dejittered receiver recovered clock is output on the RCKO[n] pin if the JAT is configured in the receive path. The receiver input clock and data jitter tolerance and jitter transfer meet TR 62411-1990. Figures 2-8 and 2-9 illustrate jitter tolerance and JAT transfer characteristics.

Figure 2-8. Receiver Input Jitter Tolerance

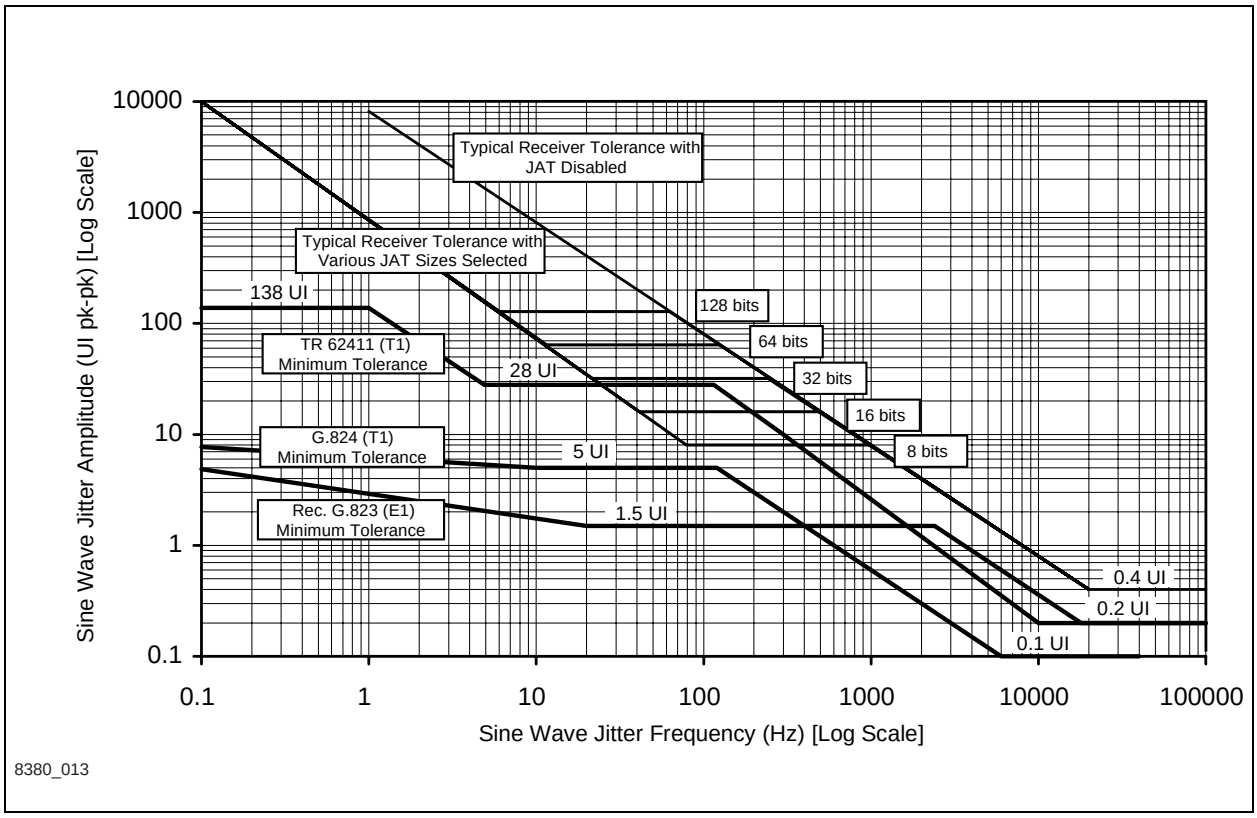
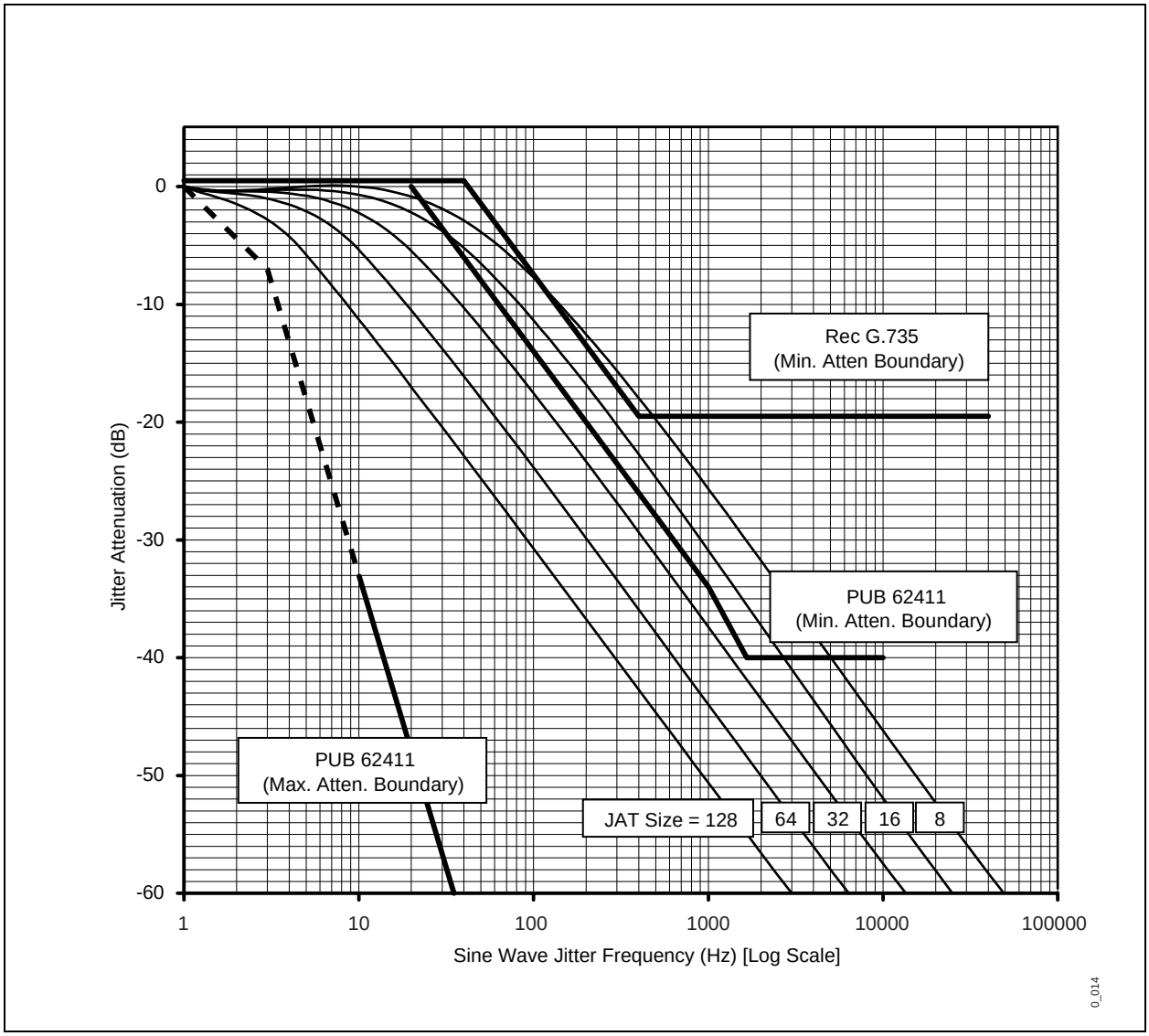


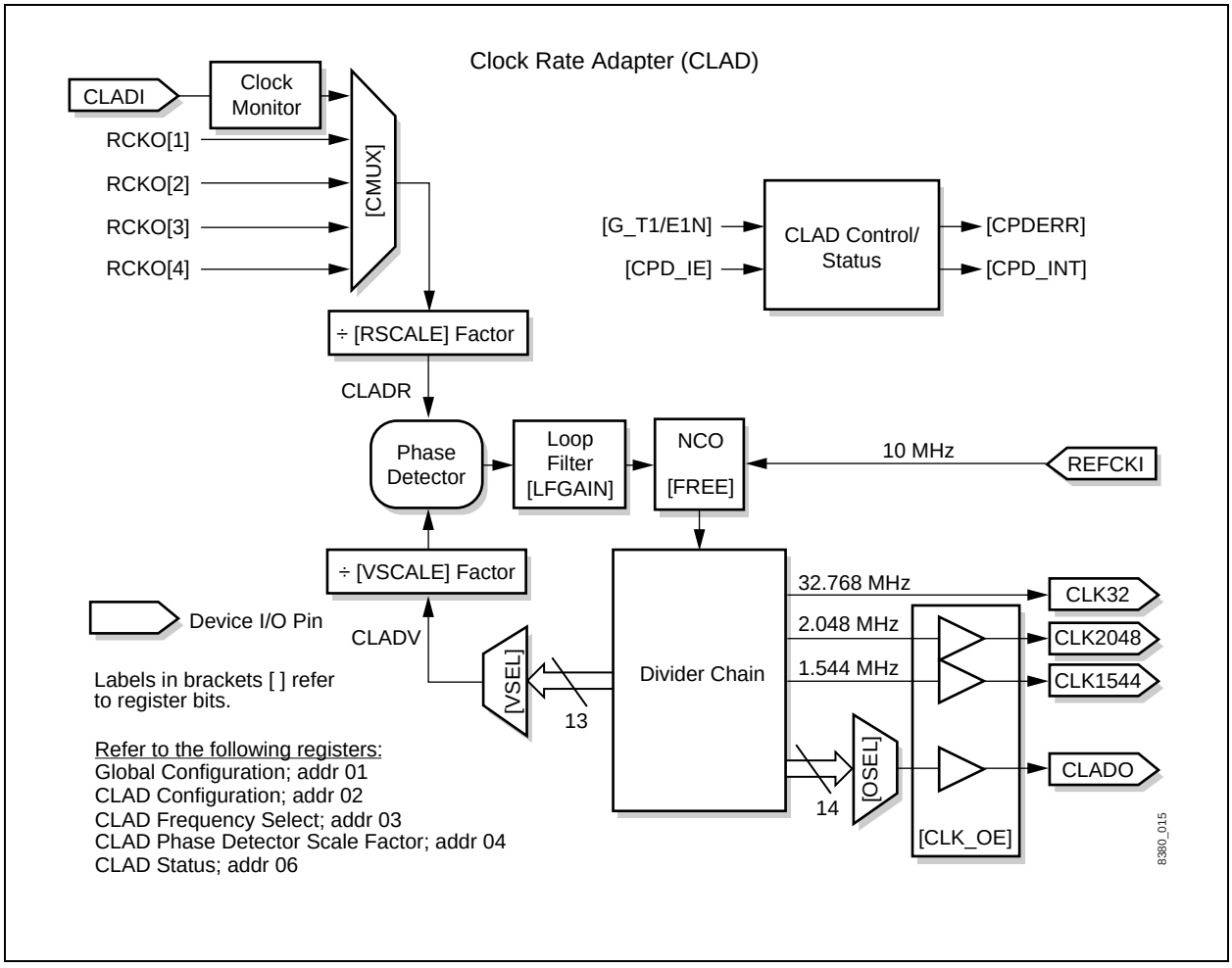
Figure 2-9. Typical JAT Transfer Characteristics with Various JAT Sizes



2.7 Clock Rate Adapter

The CLAD uses an input clock reference at a particular frequency (8 kHz to 16,384 kHz) to synthesize output clocks at a different frequency (8 kHz to 16,384 kHz). The CLAD outputs are frequency-locked to the selected timing reference. The CLAD can operate with input reference frequencies at multiples and submultiples of T1 or E1 line rates. The CLAD block diagram is illustrated in Figure 2-10.

Figure 2-10. CLAD Block Diagram



2.7.1 Inputs

In Hardware Mode, the CLAD input timing reference is normally taken from a line rate (1,544 kHz—T1 or 2,048 kHz—E1) clock on the CLADI pin. The line rate is determined globally for all channels by settings on the PTS(2:0) pins. The CLAD can be set in free-run mode by removing the clock from CLADI (pull high or low). If clock edges are not present on CLADI, an internal clock monitor automatically switches the timing reference to use the 10 MHz, REFCKI reference. When clock edges are sensed on CLADI, the reference is switched back to CLADI.

In Host Mode, the CLAD input timing reference can be selected from six sources. The source can be the received recovered clock (or jitter attenuated clock) output (RCKO[n]) from any of the four channels, the CLADI input pin, or the 10 MHz, REFCKI input (free-run mode). The CLAD reference is configured by writing to the CMUX[2:0] bits in the Global Control Register [GCR; addr 01]. Free-run mode is selected by writing 1 to the FREE bit in the CLAD Configuration Register [CLAD_CR; addr 02].

2.7.2 Outputs

Four CLAD output pins are provided: CLADO, CLK32, CLK1544, and CLK2048. In Hardware Mode, the CLADO output provides only a fixed 8 kHz clock. In Host Mode, the CLADO frequency is programmable. Table 2-10 lists the CLAD outputs and frequencies. For pin definitions, refer to Table 1-1
.

Table 2-10. CLAD Outputs and Frequencies

CLAD Output	Frequency
CLADO	Host Mode—Programmable to various frequencies in the range of 8 kHz to 32,768 kHz. Hardware Mode—Fixed 8 kHz.
CLK32	Fixed 32,768 kHz
CLK1544	Fixed 1,544 kHz
CLK2048	Fixed 2,048 kHz

2.7.3 Configuration Options

CLAD modes are selected using the CLAD Configuration Register [CLAD_CR; addr 02]; the CLAD Frequency Select [CSEL; addr 03]; and the CLAD Phase Detector Scale Factor [CPHASE; addr 04]. The CLAD reference can be any of 41 possible frequencies, as listed in Table 2-11.

Table 2-11. CLAD Reference Frequencies and Configuration Examples *(1 of 2)*

CLAD Reference (kHz)	RSCALE	Phase Compare Frequency (kHz)	VSCALE	CLADV (kHz)	VSEL
8	000	8	111	1024	0001
16	000	16	110	1024	0001
32	000	32	101	1024	0001
64	000	64	100	1024	0001
128	000	128	011	1024	0001
256	000	256	010	1024	0001
512	000	512	001	1024	0001
1024	000	1024	000	1024	0001
2048	000	2048	000	2048	0010
4096	000	4096	000	4096	0011
8192	000	8192	000	8192	0100
16,384	000	16,384	000	16,384	0101
32,768	000	32,768	000	32,768	0110
12.0625	000	12.0625	111	1544	0111
24.125	000	24.125	110	1544	0111
48.25	000	48.25	101	1544	0111
96.5	000	96.5	100	1544	0111
193	000	193	011	1544	0111
386	000	386	010	1544	0111
772	000	772	001	1544	0111
1544	000	1544	000	1544	0111
3088	000	3088	000	3088	1000
6176	000	6176	000	6176	1001
12,352	000	12,352	000	12,352	1010
24,704	000	24,704	000	24,704	1011
12	000	12	111	1536	1101
24	000	24	110	1536	1101
48	000	48	101	1536	1101
96	000	96	100	1536	1101
192	000	192	011	1536	1101

Table 2-11. CLAD Reference Frequencies and Configuration Examples *(2 of 2)*

CLAD Reference (kHz)	RSCALE	Phase Compare Frequency (kHz)	VSCALE	CLADV (kHz)	VSEL
384	000	384	010	1536	1101
768	000	768	001	1536	1101
1536	000	1536	000	1536	1101
20	000	20	111	2560	1100
40	000	40	110	2560	1100
80	000	80	101	2560	1100
160	000	160	100	2560	1100
320	000	320	011	2560	1100
640	000	640	010	2560	1100
1280	000	1280	001	2560	1100
2560	000	2560	000	2560	1100

To configure the CLAD:

1. Choose a CLADO output frequency. Refer to the CLAD Frequency Select register [CSEL; addr 03] for a list of all possible CLADO output frequencies.
2. Configure OSEL to select the CLADO output frequency.
3. Select the desired CLAD timing reference frequency from Table 2-11.
4. Configure RSCALE, VSCALE, VSEL from Table 2-11.

Many RSCALE and VSCALE values other than those shown in Table 2-11 are applicable. For instance, an alternate configuration for an input reference frequency of 2048 kHz is displayed in Table 2-12.

Table 2-12. Sample Alternate Configuration

CLAD Reference (kHz)	RSCALE	Phase Compare Frequency (kHz)	VSCALE	CLADV (kHz)	VSEL
2048	001	1024	011	8192	0100

RSCALE is a programmable frequency divider which scales the CLAD reference clock frequency before it is applied to the CLAD's phase detector. Similarly, VSCALE scales the CLAD's internal feedback clock, CLADV. These two clocks must have the same frequency at the phase detector's inputs for the CLAD's loop to properly lock. So the rule is:

(CLAD reference freq.) ÷ (RSCALE factor) = (CLADV freq.) ÷ (VSCALE factor)

2.8 Test Access Port (JTAG)

The CN8380 incorporates printed circuit board testability circuits in compliance with IEEE Std P1149.1a–1993, IEEE Standard Test Access Port and Boundary–Scan Architecture, commonly known as JTAG (Joint Test Action Group).

The JTAG includes a test access port (TAP) and several data registers. The TAP provides a standard interface through which instructions and test data are communicated. A Boundary Scan Description Language (BSDL) file for the CN8380 is available from the factory upon request.

The test access port consists of the $\overline{\text{TRST}}$, TDI, TCK, TMS, and TDO pins. An internal power on reset circuit or the $\overline{\text{TRST}}$ resets the JTAG port.

2.8.1 Instructions

In addition to the required BYPASS, SAMPLE/PRELOAD, and EXTEST instructions, IDCODE instruction is supported. There are also two private instructions. Table 2-13 lists the JTAG instructions and their codes.

Table 2-13. JTAG Instructions

Instructions	Code
BYPASS	1111
SAMPLE/PRELOAD	0001
EXTEST	0000
IDCODE	0010

2.8.2 Device Identification Register

The JTAG ID register consists of a 4-bit version, a 16-bit part number, and an 11-bit manufacturer number as listed in Table 2-14.

Table 2-14. Device Identification JTAG Register

Version				Part Number															Manufacturer ID											
0	0	0	0	1	0	0	0	0	0	1	1	1	0	0	0	0	0	0	0	0	0	0	1	1	0	1	0	1	1	0	1
0x0				0x8380															0x0D6											
4 Bits				16 Bits															11 Bits											

3.0 Registers

3.1 Address Map

The address map in Table 3-1 lists the three types of registers:

- Global Control and Status Registers
- Per Channel Registers
- Transmitter Shape Registers

Table 3-1. Address Map *(1 of 2)*

Address (Hex)	Acronym	R/W	Description	Default Setting(1) (Hex)
Global Control and Status Registers				
00	DID	R	Device Identification	*(2)*
01	GCR	R/W	Global Configuration	00
02	CLAD_CR	R/W	CLAD Configuration	00
03	CSEL	R/W	CLAD Frequency Select	00
04	CPHASE	R/W	CLAD Phase Detector Scale Factor	00
06	CSTAT	R	CLAD Status	—
Per Channel Registers (n = channel number: 1–4)				
n0	JAT_CR	R/W	Jitter Attenuator Configuration	00
n1	RLIU_CR	R/W	Receiver Configuration	00
n2	TLIU_CR	R/W	Transmitter Configuration	00
n3	LIU_CTL	R/W	Line Interface Unit Control	00
n4	UNUSED	—	—	—
n5	ALARM	R	Alarm Status	—
n6	ISR	R	Interrupt Status Register	00
n7	IER	R/W	Interrupt Enable Register	00
n8	SHAPE0	R/W	Transmit Pulse Shape Configuration	00
n9	SHAPE1	R/W	Transmit Pulse Shape Configuration	00

Table 3-1. Address Map *(2 of 2)*

Address (Hex)	Acronym	R/W	Description	Default Setting(1) (Hex)
nA	SHAPE2	R/W	Transmit Pulse Shape Configuration	00
nB	SHAPE3	R/W	Transmit Pulse Shape Configuration	00
nC	SHAPE4	R/W	Transmit Pulse Shape Configuration	00
nD	SHAPE5	R/W	Transmit Pulse Shape Configuration	00
nE	SHAPE6	R/W	Transmit Pulse Shape Configuration	00
nF	SHAPE7	R/W	Transmit Pulse Shape Configuration	00
Reserved Registers				
05	CTEST	R/W	(Factory use only)	00
07	FREG	R/W	(Factory use only)	00
08	TESTA1	R/W	(Factory use only)	00
09	TESTA2	R/W	(Factory use only)	00
0A	FUSE_CH1	R	(Factory use only)	—
0B	FUSE_CH2	R	(Factory use only)	—
0C	FUSE_CH3	R	(Factory use only)	—
0D	FUSE_CH4	R	(Factory use only)	—
0E	FUSE_RES	R	(Factory use only)	—
0F	TESTD	R/W	(Factory use only)	00
50	TESTA3	R/W	(Factory use only)	00
51	TESTA4	R/W	(Factory use only)	00
52–7F	RESERVED		Reserved	—

Note(s):
(1) Registers shown with a default setting are reset to the indicated value during internal power on reset, software RESET, or hardware reset ($\overline{\text{RESET}}$ pin).
(2) Value depends on the current device revision. Consult factory.

3.2 Global Control and Status Registers

00—Device Identification (DID)

R

7	6	5	4	3	2	1	0
DID[7]	DID[6]	DID[5]	DID[4]	DID[3]	DID[2]	DID[1]	DID[0]

DID[7:4] Device ID

DID[3:0] Device Revision

01—Global Configuration (GCR)

R/W

7	6	5	4	3	2	1	0
RESET	G_T1/E1N	CLK_OE	CPD_IE	TCLK_I/O	CMUX[2]	CMUX[1]	CMUX[0]

RESET Global Reset—When written to 1, initiates an internal global reset process which sets all configuration registers to their default values for all four ports. Also, several output pins are three-stated. After RESET is complete, the following is true:

- Digital receiver outputs (RPOSO[1:4], RNEGO[1:4], RCKO[1:4]) are three-stated.
- Transmitter line outputs (XTIP[1:4], XRING[1:4]) are three-stated.
- CLK1544, CLK2048, and CLADO clock outputs are three-stated.
- Transmitter clocks, TCLK[1:4] are configured as inputs.
- All interrupt sources are disabled.
- All configuration registers are set to default values.

G_T1/E1N Global Clock Mode—This bit selects one of two CLAD operating modes. The CLAD can operate in a mode which insures the minimum output jitter on the CLK1544 output or the CLK 2048 output.

0 = CLK2048 output jitter minimized
1 = CLK1544 output jitter minimized

CLK_OE Clock Output Enable—Determines output state of CLK1544, CLK2048, and CLADO clock outputs.

0 = Clock outputs are three-stated
1 = Clock outputs are enabled

CPD_IE CLAD Phase Detector Error Interrupt Enable—Enables CLAD loss of lock detector, CPD_INT [CSTAT; addr 06], to generate an interrupt request.

0 = Interrupt disabled
1 = Interrupt enabled

TCLK_I/O Transmit Clock Input/Output—Determines whether TCLK[1:4] pins are inputs or outputs.

0 = TCLK[1:4] pins are inputs
1 = TCLK[1:4] pins are outputs

CMUX[2:0] CLAD Multiplexer Select—Selects the CLAD reference clock source input to the CLAD phase detector if FREE = 0 [CLAD_CR; addr 02]. The source can be the receive recovered clock output (RCKO) from any of the four channels or the CLAD input pin.

000 = CLADI pin
001 = RCKO[1] from channel #1
010 = RCKO[2] from channel #2
011 = RCKO[3] from channel #3
100 = RCKO[4] from channel #4

02—CLAD Configuration (CLAD_CR)

R/W

7	6	5	4	3	2	1	0
FREE	RSCALE[2]	RSCALE[1]	RSCALE[0]	LFGAIN[3]	LFGAIN[2]	LFGAIN[1]	LFGAIN[0]

FREE Free-Run CLAD—Disables the CLAD phase detector in the CLAD, which forces the numerically controlled oscillator (NCO) to free-run based on the 10 MHz REFCKI input clock accuracy.

0 = normal (closed loop) CLAD operation
1 = free run (open loop) NCO operation

RSCALE[2:0] CLAD Reference Scale Factor—Divides CLAD reference signal by $2^{[RSCALE]}$ to form CLADR input to the phase detector. Applicable only if FREE is 0. Allows the system to supply CLADI frequency, up to a maximum of 128 times the desired CLADR reference frequency.

RSCALE	Scale Factor	CLADR Reference
000	1	CLADR = CLADI
001	2	CLADR = CLADI/2
010	4	CLADR = CLADI/4
011	8	CLADR = CLADI/8
100	16	CLADR = CLADI/16
101	32	CLADR = CLADI/32
110	64	CLADR = CLADI/64
111	128	CLADR = CLADI/128

LFGAIN[3:0] Loop Filter Gain— Selects the NCO loop filter's proportional phase error gain. Lower gain values reduce phase response time, and higher gain values increase phase response time. Note that loop instability or acquisition failures may result from incorrectly programmed LFGAIN values.

LFGAIN	Proportional Gain
0000	$1/2^0$
|	|
1111	$1/2^{15}$

03—CLAD Frequency Select (CSEL)

R/W

7	6	5	4	3	2	1	0
VSEL[3]	VSEL[2]	VSEL[1]	VSEL[0]	OSEL[3]	OSEL[2]	OSEL[1]	OSEL[0]

VSEL[3:0] CLADV Frequency Select—Applicable only if FREE [CLAD_CR; addr 02] is 0. Picks one of 13 CLAD divider chain frequencies to feed back to the phase detector. The selected CLADV frequency passes to VSCALE for further division before phase detector comparison. Setting VSEL to invalid values is undefined.

VSEL	CLADV Frequency (kHz)	
0000	<Invalid>	
0001	1024	
0010	2048	1 x E1
0011	4096	2 x E1
0100	8192	4 x E1
0101	16,384	8 x E1
0110	32,768	16 x E1
0111	1544	1 x T1
1000	3088	2 x T1
1001	6176	4 x T1
1010	12,352	8 x T1
1011	24,704	16 x T1
1100	2560	
1101	1536	1 x T1 (unframed)
1110	<Invalid>	
1111	<Invalid>	

OSEL[3:0] CLADO Frequency Select—Picks one of 14 CLAD divider chain frequencies to output on the CLADO pin.

OSEL	CLADO Frequency (kHz)	
0000	8	
0001	1024	
0010	2048	1 x E1
0011	4096	2 x E1
0100	8192	4 x E1
0101	16,384	8 x E1
0110	32,768	16 x E1
0111	1544	1 x T1
1000	3088	2 x T1
1001	6176	4 x T1
1010	12,352	8 x T1
1011	24,704	16 x T1
1100	2560	
1101	1536	1 x T1(unframed)
1110	<Invalid>	
1111	<Invalid>	

04—CLAD Phase Detector Scale Factor (CPHASE)

R/W

7	6	5	4	3	2	1	0
—	—	—	—	—	VSCALE[2]	VSCALE[1]	VSCALE[0]

VSCALE[2:0] CLAD Variable Scale Factor—Divides CLADV signal by $2^{[VSCALE]}$ before use in the phase detector. Applicable only if FREE [CLAD_CR; addr 02] is 0. Allows the system to select CLADV frequency that is up to 128 times CLADR.

VSCALE	Scale Factor	Phase Detector Variable Input
000	1	CLADV selected by VSEL [addr 03]
001	2	CLADV/2
010	4	CLADV/4
011	8	CLADV/8
100	16	CLADV/16
101	32	CLADV/32
110	64	CLADV/64
111	128	CLADV/128

05—CLAD Test (CTEST)

R/W

7	6	5	4	3	2	1	0
CTEST[7]	CTEST[6]	CTEST[5]	CTEST[4]	CTEST[3]	CTEST[2]	CTEST[1]	CTEST[0

Factory use only. Must be remain at default value, 00.

06—CLAD Status (CSTAT)

R

7	6	5	4	3	2	1	0
—	—	—	CPDERR	—	—	—	CPD_INT

CPDERR CLAD Phase Detector Error—Real-time indicator of the CLAD phase detector status. CPDERR indicates when the CLADO loses lock with respect to the selected CLADI reference clock.

0 = CLAD Phase Detector is in lock
1 = CLAD Phase Detector is out of lock

CPD_INT CLAD Phase Detector Error Interrupt—Indicates a change in status of CPDERR. CPD_INT is latched high upon a change in status of CPDERR and held until read clear.

07—(FREG)

R/W

7	6	5	4	3	2	1	0
F_OP[1]	F_OP[0]	—	F_ADDR[4]	F_ADDR[3]	F_ADDR[2]	F_ADDR[1]	F_ADDR[0]

Factory use only. Must be remain at default value, 00.

08—(TESTA1)

R/W

7	6	5	4	3	2	1	0
A_TEST[7]	A_TEST[6]	A_TEST[5]	A_TEST[4]	A_TEST[3]	A_TEST[2]	A_TEST[1]	A_TEST[0]

Factory use only. Must be remain at default value, 00.

09—(TESTA2)

R/W

7	6	5	4	3	2	1	0
A_TEST[15]	A_TEST[14]	A_TEST[13]	A_TEST[12]	A_TEST[11]	A_TEST[10]	A_TEST[9]	A_TEST[8]

Factory use only. Must be remain at default value, 00.

0A—(FUSE_CH1)

R/W

7	6	5	4	3	2	1	0
F_TR[5]	—	—	F_TR[4]	F_TR[3]	F_TR[2]	F_TR[1]	F_TR[0]

Factory use only. Must be remain at default value, 00.

0B—(FUSE_CH2)

R/W

7	6	5	4	3	2	1	0
—	—	—	F_TR[10]	F_TR[9]	F_TR[8]	F_TR[7]	F_TR[6]

Factory use only. Must be remain at default value, 00.

0C—(FUSE_CH3)

R/W

7	6	5	4	3	2	1	0
—	—	—	F_TR[15]	F_TR[14]	F_TR[13]	F_TR[12]	F_TR[11]

Factory use only. Must be remain at default value, 00.

0D—(FUSE_CH4)

R/W

7	6	5	4	3	2	1	0
—	—	—	F_TR[20]	F_TR[19]	F_TR[18]	F_TR[17]	F_TR[16]

Factory use only. Must be remain at default value, 00.

0E—(FUSE_RES)

R/W

7	6	5	4	3	2	1	0
PREVIEW	—	F_TR[26]	F_TR[25]	F_TR[24]	F_TR[23]	F_TR[22]	F_TR[21]

Factory use only. Must be remain at default value, 00.

0F—(TESTD)

R/W

7	6	5	4	3	2	1	0
D_CTL[2]	D_CTL[1]	D_CTL[0]	D_CH[1]	D_CH[0]	D_MD[2]	D_MD[1]	D_MD[0]

Factory use only. Must be remain at default value, 00.

3.3 Per Channel Registers

10, 20, 30, 40—Jitter Attenuator Configuration (JAT_CR)

R/W

7	6	5	4	3	2	1	0
T1/$\overline{E1}$	—	JEN	JDIR	JCENTER	JSIZE[2]	JSIZE[1]	JSIZE[0]

T1/$\overline{E1}$ T1/E1 Select—Enables receive and transmit circuits to operate at either the T1 or E1 line rate. All configuration register settings should be re-initialized after changing the T1/$\overline{E1}$ control bit. T1/$\overline{E1}$ selects the nominal line rate (shown below), while the exact receive and transmit line rate frequencies are independently determined by their respective input clock or data references. The actual receive and transmit line frequency can vary within defined tolerances.
0 = 2.048 MHz line rate (E1)
1 = 1.544 MHz line rate (T1)

JEN Jitter Attenuator Enable—JEN enables the JAT in the receive or the transmit path (determined by JDIR bit).
0 = Disable JAT
1 = Enable JAT

JDIR Select JAT Path—Applicable only when the JAT is enabled (see JEN description). JAT elastic store is placed in either the receive or transmit path.
0 = JAT in TX path
1 = JAT in RX direction, jitter attenuated recovered clock output on RCKO

JCENTER Force JAT to Center—Writing a 1 to JCENTER resets the elastic store write pointer and forces the elastic store read pointer to one-half the programmed JSIZE. JCENTER is typically written at power-up. JCENTER can optionally be asserted after recovery from a loss of signal (RLOS or RALOS) or in response to a transmit loss of clock (TLOC), or after recovering from a persistent JAT elastic store error (JERR). The JCENTER bit is self clearing.
0 = normal operation
1 = recenter JAT elastic store

JSIZE[2:0] JAT Elastic Store Size—Selects the maximum depth of the JAT elastic store. The 32-bit depth is sufficient to meet jitter attenuation requirements in all cases where the JAT cutoff frequency is programmed at 6 Hz. However, in cases where an external reference is selected or a narrow loop bandwidth is programmed, the elastic store depth can tolerate up to ±64 UI (128 bits) of accumulated phase offset.

JSIZE	Elastic Store Size
000	8 Bits
001	16 Bits
010	32 Bits
011	64 Bits
1xx	128 Bits

11, 21, 31, 41—Receiver Configuration (RLIU_CR)

R/W

7	6	5	4	3	2	1	0
UNIPOLAR	ZCS	CLK_POL	RAWMD	EQ_DIS	ATTN	—	SQUELCH

UNIPOLAR Unipolar Mode—Selects between unipolar and bipolar modes for digital transmit and receive signals.

In unipolar mode, RPOSO/RNEGO signals are replaced by RDATO/BPV signals. AMI encoded received data is decoded and output on RDATO in unipolar, NRZ format; and BPV indicates that the currently received bit is a bipolar violation. TPOSI is replaced with TDATI and accepts unipolar, NRZ formatted transmit data. TNEGI is not used in this mode. In unipolar mode, ZCS can replace AMI encoding. Refer to the ZCS bit description below.

In bipolar mode, RPOSO/RNEGO signals output received data in bipolar dual-rail format, where a high level on RPOSO indicates receipt of a positive AMI pulse, and a high level on RNEGO indicates receipt of a negative AMI pulse on RTIP/RING inputs. TPOSI/TNEGI inputs accept bipolar dual-rail transmit data, where a high on TPOSI causes a positive output pulse on XTIP/XRING, and a high on TNEGI causes a negative output pulse.

0 = Digital transmit/receive signals are bipolar, dual-rail
1 = Digital transmit/receive signals are unipolar, NRZ

ZCS Zero Code Suppression Enable—Enables HDB3 or B8ZS zero code suppression encoding/decoding on digital transmit and receive signals and is only applicable if unipolar mode is selected. In T1 mode (T1/$\overline{E1}$ = 1) [addr n0], B8ZS encoding/decoding is selected. In E1 mode (T1/$\overline{E1}$ = 0), HDB3 encoding/decoding is selected.

In the transmit direction, the ZCS encoder replaces sequences of eight or four 0s with a recoverable code. In the receive direction, the ZCS decoder replaces received codes with eight 0s in T1 mode, or four 0s in E1 mode. The B8ZS code is 000VB0VB and the HDB3 code is X00V; where B is a normal AMI pulse, V is a bipolar violation, and X is a “don't-care.” These are standard T1 and E1 line code options.

0 = ZCS encode/decode disabled
1 = ZCS encode/decode enabled

CLK_POL Clock Polarity—Selects the digital receive data clocking edge. Normally, RPOSO/RNEGO is output on the rising edge of RCKO. If CLK_POL is set to 1, RPOSO/RNEGO is output on the falling edge of RCKO.

0 = Data out on rising RCKO
1 = Data out on falling RCKO

RAWMD Raw Receive Mode—RPOSO/RNEGO data outputs are replaced by the data slicer output, and RCKO is replaced by the logical OR of RPOSO/RNEGO. A high on RPOSO indicates a positive pulse, and a high on RNEGO indicates a negative pulse on RTIP/RRING line inputs.

0 = Normal receiver output
1 = Slicer data output enabled

EQ_DIS Equalizer Disable—Disables the receiver equalizer. (Test mode only)

0 = Equalizer enabled
1 = Equalizer disabled

ATTN Bridge Attenuation—Compensates for 20 dB resistive signal attenuation caused by placement of bridge resistors in series with the normal receive termination resistance. Also, in this mode a lower threshold for RALOS is selected to compensate for the 20 db attenuation.

0 = Normal receiver input levels
1 = 20 dB compensation enabled

SQUELCH Enable Receive Signal Squelch—The digital receiver outputs, RPOSO/RNEGO, are forced to zero when RALOS is declared. SQUELCH is useful in attached framer applications to allow the framer to detect LOS during an RALOS condition.

0 = Normal

1 = Squelch RPOSO/RNEGO outputs upon RALOS detect

12, 22, 32, 42 —Transmitter Configuration (TLIU_CR)

R/W

7	6	5	4	3	2	1	0
ALT_TR	TERM	PDN	T_BOOST	PPT	PULSE[2]	PULSE[1]	PULSE[0]

ALT_TR Alternate Transformer Select—Adjusts the transmit output level for one of two possible transmitter transformer turns ratios. Normally, a turns ratio of 1:2 for the transmitter is used. An alternate transformer with turns ratio of 1:1.36 can be selected to minimize power dissipation

0 = Normal transformer (1:2)

1 = Alternate transformer (1:1.36)

TERM Transmitter Termination Select—Adjusts the transmit XTIP/XRING output amplitude to compensate for the presence of an optional external termination resistor. The external resistor is placed in parallel across XTIP/XRING on systems that must meet transmitter return loss requirements. Refer to Figure 2-7, *Transmit Termination Components*, for resistor placement. Refer to Tables 2-4 through 2-8 for return loss values.

0 = no external transmit termination resistor used

1 = external transmit termination resistor used

PDN Power Down—Unused channels can be put into a low power mode in order to minimize power dissipation. In low power mode, XTIP/XRING, RPOSO/RNEGO, and RCKO outputs are three-stated. All other receiver functions are not affected.

0 = Channel is disabled, low power mode

1 = Channel is enabled, normal operation

T_BOOST Transmit Level Boost—Adjusts the transmit output level to compensate for series resistance added to the output by surge protection circuitry. Typical resistance values are 5.6 ohms in series with line side XTIP and XRING signals.

0 = No compensation

1 = Compensation enabled

PPT Programmed Pulse Template—Enables custom transmit pulse transmission. The programmed pulse shape stored in the corresponding shape register, SHAPEn [addr n8 – nF], is used for transmission.

0 = Pulse template selected by PULSE(2:0)

1 = Programmed pulse template selected

PULSE[2:0] Transmit Pulse Template Select—Each positive or negative pulse output on XTIP/XRING is shaped to meet the transmit pulse template according to the selected cable length and type. Custom shape programming for alternative cable types or pulse templates can be set using the SHAPE0–SHAPE7 registers [addr n8 – nF].

PULSE	Cable Length	Cable Type	Application
000	0–133 ft.	100 Ω Twisted Pair	T1 DSX
001	133–266 ft.	100 Ω Twisted Pair	T1 DSX
010	266–399 ft.	100 Ω Twisted Pair	T1 DSX
011	399–533 ft.	100 Ω Twisted Pair	T1 DSX
100	533–655 ft.	100 Ω Twisted Pair	T1 DSX
101	ITU–T G.703	75 Ω Coaxial Cable	E1
110	ITU–T G.703	120 Ω Twisted Pair	E1
111	I.431 ISDN	100 Ω Twisted Pair	T1 CSU/NCTE

13, 23, 33, 43—LIU Control (LIU_CTL)

R/W

7	6	5	4	3	2	1	0
AISCLK	AUTO_AIS	TAIS	LLOOP	RLOOP	TAIS_PE	LLOOP_PE	RLOOP_PE

AISCLK Enable Automatic ACKI Switching—If AISCLK is active, the transmitter clock is automatically switched to reference TACKI (T1) or EACKI (E1) instead of TCLK when transmitting AIS (all 1s) data. Set AISCLK only if the system supplies an alternate line rate clock on the TACKI or EACKI pins. Also refer to description of AUTO_AIS/TAIS below.

0 = TACKI/EACKI is not used to transmit AIS
1 = TACKI/EACKI is used to transmit AIS

AUTO_AIS Automatic Transmit Alarm Indication Signal

TAIS Manual Transmit Alarm Indication Signal—When activated manually (TAIS) or automatically (AUTO_AIS), the AIS generator replaces all data output on XTIP/XRING with an unframed all-1s signal (AIS). This includes replacing data supplied from TPOSI/TNEGI and from the receiver during Remote Line Loopback. Automatic mode sends AIS for the duration of transmit loss of clock [TLOC; addr n5]. If AISCLK is enabled, the transmit clock is switched to use TACKI or EACKI to transmit AIS.

AIS transmission does not affect transmit data that is looped back to the receiver during Local Digital Loopback. This allows Local Digital Loopback to be active simultaneously with the transmission of AIS. If TAIS is activated when RLOOP is enabled, AIS is transmitted using the jitter-attenuated received clock. Refer to the descriptions of RLOOP and LLOOP below. Table 3-2 lists transmitter operating modes resulting from various configuration settings and input conditions.

Table 3-2. Transmitter Operating Modes

Configuration and Input Status					Transmitter Mode	
RLOOP	**TLOC**	**TAIS**	**AUTO_AIS**	**AISCLK**	**Transmit Data**	**Transmit Clock**
0	X	0	0	X	Tx Data	TCLK
0	X	1	X	0	AIS	TCLK
0	X	1	X	1	AIS	TACKI/EACKI
0	0	0	1	X	Tx Data	TCLK
0	1	0	1	0	AIS	TCLK
0	1	0	1	1	AIS	TACKI/EACKI
1	X	0	X	X	Rx Data	RCLK
1	X	1	X	X	AIS	RCLK

Note: X is don't-care.

LLOOP Local Analog Loopback—Bipolar data from XTIP/XRING is internally connected to RTIP/RRING inputs. Externally applied data on RTIP/RRING inputs is ignored. XTIP/XRING output data is unaffected. Asserting both LLOOP and RLOOP activates Local Digital Loopback. Refer to the RLOOP description below.

RLOOP Remote Line Loopback—Dual-rail bipolar data from the receiver (or receive JAT) is internally connected to the transmitter (or transmit JAT). The recovered clock from the RPLL (or JCLK) is also looped to provide the transmit clock. Loopback data retains BPV transparency. Received data is allowed to pass to the RZCS decoder, and digital outputs are unaffected.

Asserting both LLOOP and RLOOP activates LDL. Dual-rail bipolar data from the TZCS encoder (or transmit jitter attenuator) is internally connected to the RZCS decoder (or receive jitter attenuator) inputs. The transmit clock, TCLK, is also looped to provide the receive clock, RCKO. Externally applied data on RTIP/RRING inputs are blocked; however, RLOS and RALOS detect circuitry continues to operate and report receive signal status. XTIP/XRING output data is unaffected.

LLOOP	RLOOP	Loopback
0	0	No loopback
0	1	Remote Line Loopback
1	0	Local Analog Loopback
1	1	Local Digital Loopback

TAIS_PE TAIS Pin Enable—Allows the use of the $\overline{\text{TAIS}}$ hardware pin instead of the TAIS register bit to manually transmit AIS.

0 = Use TAIS register bit
1 = Use $\overline{\text{TAIS}}$ pin

LLOOP_PE LLOOP Pin Enable—Allows the use of the $\overline{\text{LLOOP}}$ hardware pin instead of the LLOOP register bit to control loopbacks.
0 = Use LLOOP register bit
1 = Use $\overline{\text{LLOOP}}$ pin

RLOOP_PE RLOOP Pin Enable—Allows the use of the $\overline{\text{RLOOP}}$ hardware pin instead of the RLOOP register bit to control loopbacks.
0 = Use RLOOP register bit
1 = Use $\overline{\text{RLOOP}}$ pin

15, 25, 35, 45—Alarm Status (ALARM)

R

7	6	5	4	3	2	1	0
RALOS	RLOS	TLOC	TLOS	TSHORT	JERR	BPV	—

RALOS Receive Analog Loss of Signal Detect—Indicates receiver analog loss of signal.

RLOS Receive Loss of Signal Detect—Indicates receiver loss of signal.

TLOC Transmit Loss of Clock Detect—Indicates loss of transmit clock, TCLK.

TLOS Transmit Loss of Signal Detect—Indicates a transmitter signal fault detected by the DPM.

TSHORT Transmit Short Circuit Detect—Indicates transmitter output overload.

JERR Jitter Attenuator Error Detect—Indicates jitter attenuator FIFO overflow or underrun.

BPV Bipolar Violation Detect—Indicates a bipolar violation error. If ZCS encoding/decoding is enabled, BPV is asserted only for bipolar violations which are not part of the ZCS code.

16, 26, 36, 46—Interrupt Status Register (ISR)

An Interrupt Status register (ISR) bit is latched active (high) whenever its corresponding interrupt source [ALARM; addr n5] reports an interrupt event. All latched ISR bits are cleared when ISR is read. If the corresponding interrupt enable [IER; addr n7] is active (high), each interrupt event forces the $\overline{\text{IRQ}}$ output pin active (low).

ISR reports an interrupt event when an alarm status [ALARM; addr n5] changes from inactive to active (rising edge) or from active to inactive (falling edge). The associated real-time alarm status must be read to determine the current alarm state.

R

7	6	5	4	3	2	1	0
RALOS	RLOS	TLOC	TLOS	TSHORT	JERR	BPV	—

RALOS Receive Analog Loss of Signal—Indicates receiver analog loss of signal status change.

RLOS Receive Loss of Signal—Indicates receiver loss of signal status change.

TLOC Transmit Loss of Clock—Indicates transmitter loss of clock status change.

TLOS Transmit Loss of Signal—Indicates transmitter output signal fault status change.

TSHORT Transmit Short Circuit—Indicates transmitter loss of analog signal status change.

JERR Jitter Attenuator Error— Indicates JAT FIFO empty/full status change.

BPV Bipolar Violation— Indicates a non-zero code bipolar violation status change.

17, 27, 37, 47—Interrupt Enable Register (IER)

R/W

7	6	5	4	3	2	1	0
RALOS	RLOS	TLOC	TLOS	TSHORT	JERR	BPV	—

RALOS Enables Receive Analog Loss Of Signal

RLOS Enables Receive Loss Of Signal

TLOC Enables Transmit Loss Of Clock

TLOS Enables Transmit Loss Of Signal

TSHORT Enables Transmit Short Circuit

JERR Enables Jitter Attenuator Error

BPV Enables Bipolar Violation

3.4 Transmitter Shape Registers

The following SHAPE registers allow custom programming of the transmit signal pulse shapes. Each set of eight registers determines the shape for its corresponding channel. A channel [n] is configured to use custom shapes by first programming the eight SHAPE[n] registers, then setting register bit PPT [addr n1]. For more information on transmitter functionality, refer to Section 2.4, *Transmitter*.

18 - 1F—Transmit PULSE Shape CONFIGURATION (SHAPE1)

R/W

7	6	5	4	3	2	1	0
—	—	—	SHAPE[4]	SHAPE[3]	SHAPE[2]	SHAPE[1]	SHAPE[0]

28 - 2F—Transmit PULSE Shape CONFIGURATION (SHAPE2)

R/W

7	6	5	4	3	2	1	0
—	—	—	SHAPE[4]	SHAPE[3]	SHAPE[2]	SHAPE[1]	SHAPE[0]

38 - 3F—Transmit PULSE Shape CONFIGURATION (SHAPE3)

R/W

7	6	5	4	3	2	1	0
—	—	—	SHAPE[4]	SHAPE[3]	SHAPE[2]	SHAPE[1]	SHAPE[0]

48 - 4F—Transmit PULSE Shape CONFIGURATION (SHAPE4)

R/W

7	6	5	4	3	2	1	0
—	—	—	SHAPE[4]	SHAPE[3]	SHAPE[2]	SHAPE[1]	SHAPE[0]

50—(TESTA3)

R/W

7	6	5	4	3	2	1	0
A_TEST[23]	A_TEST[22]	A_TEST[21]	A_TEST[20]	A_TEST[19]	A_TEST[18]	A_TEST[17]	A_TEST[16]

Factory use only. Must be remain at default value, 00.

51—(TESTA4)

R/W

7	6	5	4	3	2	1	0
A_TEST[31]	A_TEST[30]	A_TEST[29]	A_TEST[28]	A_TEST[17]	A_TEST[16]	A_TEST[15]	A_TEST[14]

Factory use only. Must be remain at default value, 00.

4.0 Electrical/Mechanical Specifications

This chapter contains the following sections:

- Absolute Maximum Ratings
- Recommended Operating Conditions
- DC Characteristics
- Performance Characteristics
- AC Characteristics
- Packaging

4.1 Absolute Maximum Ratings

Table 4-1. Absolute Maximum Ratings

Symbol	Parameter	Minimum	Maximum	Units
V_{DD}	Power Supply (measured to GND)	–0.5	5.0	V
ΔV_{DD}	Voltage Differential (between any 2 V_{DD} pins)		0.5	V
V_i	Constant Voltage on any Signal Pin	–1.0	V_{DD} + 0.5	V
ESD	Transient Voltage on any Signal Pin HBM rating CDM rating MMM rating		 ±2 ± 700 ±200	 kV V V
I_i	Constant Current on any Signal Pin	–10	+10	mA
LATCHUP	Transient Current on any Signal Pin Digital Pins Analog Pins (TIP, RING)	 –400 –400	 +400 +400	 mA mA
T_s	Storage Temperature	–65	150	°C
T_j	Junction Temperature: (θ_{jA} x V_{DD} x I_{DD}) + T_{amb}	–40	125	°C
T_{vsol}	Vapor Phase Soldering Temperature (1 minute)		220	°C
θ_{JA}	Thermal Resistance (128 MQFP), Still Air		36	°C /W
CAUTION	Stresses above those listed here may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions beyond those indicated in the other sections of this document is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.			

4.2 Recommended Operating Conditions

Table 4-2. Recommended Operating Conditions

Symbol	Parameter	Minimum	Maximum	Units
V_{DD}, V_{AA}, V_{AAT}, V_{AAR}, V_{AACC}	Supply voltage	3.14	3.47	V
V_{GG} *(1)*	ESD Rail	3.14	5.25	V
T_{amb}	Ambient operating temperature	–40	+85	°C
V_{ih} *(1)*	Input high voltage	2.0	V_{GG} + 0.5	V
V_{il}	Input low voltage	–0.5	0.8	V

NOTE(S):
(1) V_{GG} is normally connected to $V_{DD.}$ V_{GG} is connected to + 5 V supply if input signals are 5 V logic.

4.3 DC Characteristics

Table 4-3. DC Characteristics

Symbol	Parameter	Minimum	Typical	Maximum	Units
I_{DD}	Supply current (all channels in low power mode, PDN [TLIU_CR; addr n2])	60	—	—	mA
	Supply current (50% 1s, all channels enabled, includes transmit load current)	—	200	—	mA
	Supply current (all 1s, all channels enabled, includes transmit load current)	—	—	650	mA
P_D	Device power dissipation (all channels in low power mode, PDN [TLIU_CR; addr n2])	0.2	—	—	W
	Device power dissipation (50% 1s, all channels enabled)	—	0.5	—	W
	Device power dissipation (all 1s, all channels enabled)	—	—	1.25	W
V_{oh}	Output high voltage (I_{oh} = – 400 µA)	2.5	—	—	V
V_{ol}	Output low voltage (I_{oh} = – 400 µA)	—	—	1.0	V
V_{ih}	Input high voltage	2.0	—	V_{GG} + 0.5	V
V_{il}	Input low voltage	–0.5	—	0.8	V
I_{pr}	Resistive pull-up current	40	100	500	µA
I_I	Input leakage current	–10	1	10	µA
I_{oz}	Three-state leakage current	–10	1	10	µA
C_{in}	Input capacitance (f = 1 MHz)	—	2	5	pF
C_{out}	Output capacitance	—	2	5	pF
C_{ld}	Capacitive loading (test condition)	—	70	85	pF
I_{osc}	Short circuit output current (except XTIP/XRING)	37	50	160	mA

4.4 Performance Characteristics

Table 4-4. Performance Characteristics

Parameter	Minimum	Typical	Maximum	Units
Receiver				
T1 receiver sensitivity (attenuation @ 772 kHz)	+3	—	–12	dB
E1 receiver sensitivity (attenuation @ 1024 kHz)	+3	—	–12	dB
RTIP[n]. RRING[n] inputs: Input impedance (unterminated) Peak-to-peak voltage (differential) Return loss		 10 6 TBD	 12 10	 kΩ V dB
Receive clock recovery (PLL) Consecutive zeros tolerance before loss of lock T1 frequency lock range E1 frequency lock range	 23 –0.1 –0.4	 75 — —	 100 +0.3 +0.4	 bits kHz kHz
Receive noise immunity (SNR) Near-end crosstalk (2^{15} PRBS) 60 Hz longitudinal Gaussian white noise	 — — —	 15 18 TBD	 18 20 TBD	 dB dB dB
RCKO intrinsic jitter with JAT disabled	—	—	0.125	UI P-P
RCKO intrinsic jitter with JAT enabled	—	—	0.05	UI P-P
Transmitter				
Transmitter XTIP[n], XRING[n] outputs: Output impedance ($\overline{XOE}$ = 1, high impedance) Output impedance ($\overline{XOE}$ = 0, unterminated) Short circuit current into 1 Ω load T1 pulse amplitude, 100 Ω UTP[(1)] E1 pulse amplitude, 75 Ω coax[(1)] E1 pulse amplitude, 120 Ω UTP[(1)] Positive/negative pulse imbalance Return loss	 10 — — 2.7 2.14 2.7 –10 —	 100 1 2 3.0 2.37 3.0 — TBD	 — — 50 3.3 2.6 3.3 +10 —	 kΩ kΩ mA V V V % dB
Transmitter signal power level (3 kHz band): Power @ 772 kHz Power @ 1544 kHz (relative to power @ 772 kHz)	 12 –25	 15 –36	 +19 —	 dBm dB
Transmitter output intrinsic jitter with JAT disabled	—	—	0.125	UI
Transmitter output intrinsic jitter with JAT enabled	—	—	0.05	UI

NOTE(S):
(1) These values are measured on the line side of the transformer with an appropriate value load resister in place of a cable.

4.5 AC Characteristics

This section provides details about the following timing features:

- $\overline{\text{XOE}}$
- $\overline{\text{RESET}}$
- CLAD
- Receiver signals
- Transmitter signals
- Host serial port
- JTAG interface

Table 4-5. $\overline{\text{XOE}}$ Timing Parameters

Symbol	Parameter	Minimum	Maximum	Units
1	$\overline{\text{XOE}}$[n] high to XTIP[n]/XRING[n] three-state		20	ns
2	$\overline{\text{XOE}}$[n] low to XTIP[n]/XRING[n] active		20	ns
NOTE(S): See Figure 4-1.				

Figure 4-1. $\overline{\text{XOE}}$ Timing Diagram

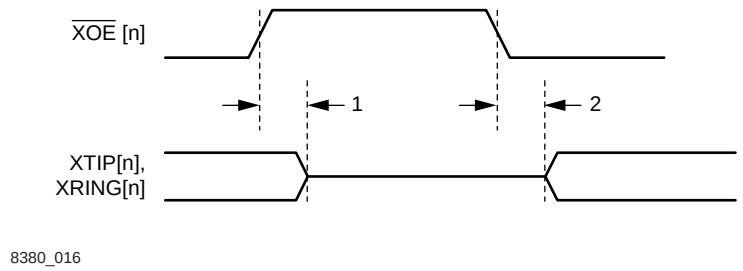


Table 4-6. $\overline{\text{RESET}}$ Timing Parameters

Symbol	Parameter	Minimum	Maximum	Units
1	$\overline{\text{RESET}}$ pulse width	500		ns
2	$\overline{\text{RESET}}$ low to output signals three-state		20	ns
3	$\overline{\text{RESET}}$[n] high to output signals active		20	ns

NOTE(S):
1. Output signals: RCKO[n], RPOSO[n], RNEGO[n], XTIP[n], XRING[n], CLK1544, CLK2048, CLADO, $\overline{\text{RLOS}}$[n], JATERR[n], TDO, SDO, $\overline{\text{IRQ}}$
2. See Figure 4-2.

Figure 4-2. $\overline{\text{RESET}}$ Timing Diagram

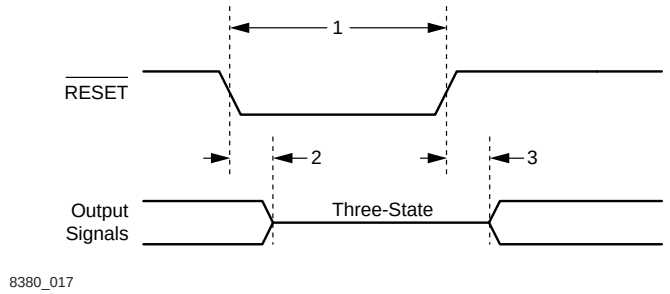


Table 4-7. CLAD Timing Parameters

Symbol	Parameter	Minimum	Maximum	Units
1	REFCKI frequency	9.999	10.001	MHz
—	CLADI frequency	8	16,384	kHz
2	Duty cycle REFCKI, CLADI	40	60	%
3	Rise/fall time (10% to 90%) REFCKI, CLADI	—	20	ns
1	CLADO frequency	8	16,384	MHz
1	CLK32 frequency	32.768 (Locked to CLAD reference)		MHz
1	CLK1544 frequency	1.544 (Locked to CLAD reference)		MHz
1	CLK2048 frequency	2.048 (Locked to CLAD reference)		MHz
2	Duty cycle CLADO, CLK32, CLK1544, CLK2048	45	55	%
3	Rise/fall time CLADO, CLK32, CLK1544, CLK2048	—	20	ns

NOTE(S): See Figure 4-3.

Figure 4-3. CLAD Timing Diagram

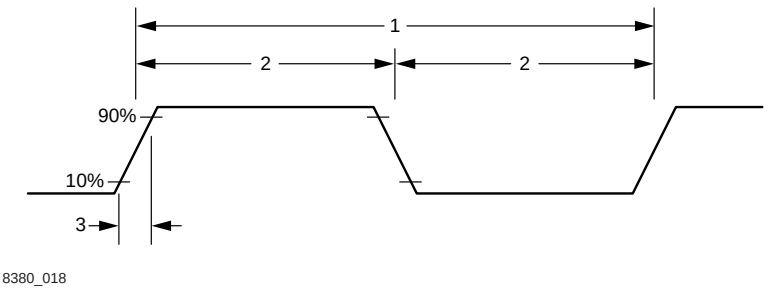


Table 4-8. Receiver Signals Timing Parameters

Symbol	Parameter	Minimum	Maximum	Units
1	RCKO[n] frequency	1,544 or 2,048 (Locked to line rate)		kHz
2/1	RCKO[n] duty cycle	45	55	%
—	Rise/fall time (10% to 90%) RCKO[n], RPOSO[n], RNEGO[n], RDATO[n], BPV[n]	—	20	ns
3	RCKO[n] (rising or falling edge) to data valid	—	20	ns
NOTE(S): See Figure 4-4.				

Figure 4-4. Receiver Signals Timing Diagram

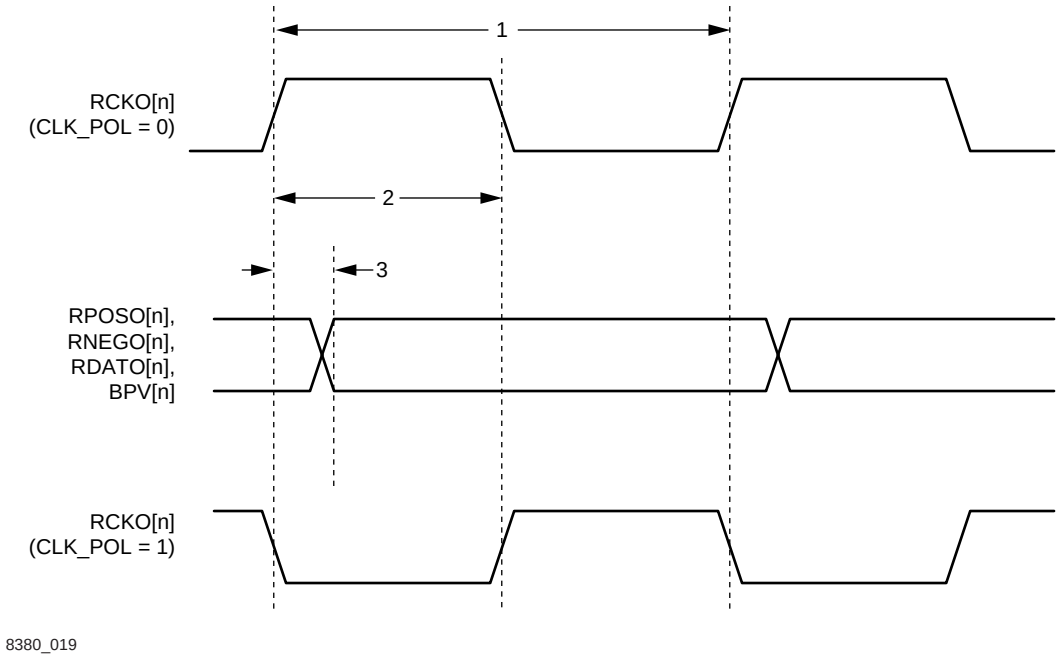


Table 4-9. Transmitter Signals Timing Parameters

Symbol	Parameter	Minimum	Maximum	Units
1	TCLK[n] frequency (input or output)	1.5	2.1	MHz
2/1	TCLK[n] duty cycle (input)	20	80	%
2/1	TCLK[n] duty cycle (output)	45	55	%
—	Rise/fall time (10% to 90%) TCLK[n], TPOSI[n], TNEGI[n], TDATI[n]	—	20	ns
3	Data Input to TCLK[n] falling edge setup time	5	—	ns
4	TCLK[n] falling edge to data input hold time	5	—	ns

NOTE(S): See Figure 4-5.

Figure 4-5. Transmitter Signals Timing Diagram

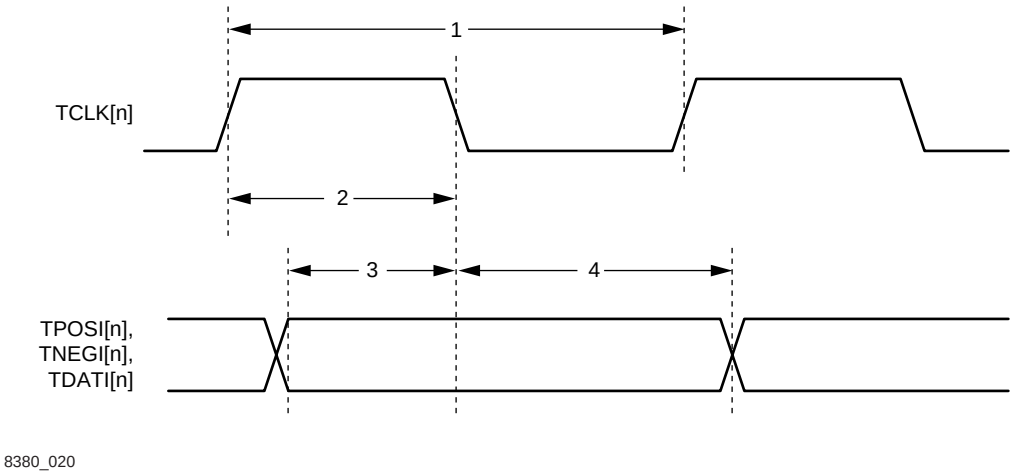


Table 4-10. Host Serial Port Timing Parameters

Symbol	Parameter	Minimum	Maximum	Units
1	$\overline{CS}$ Setup Before SCLK Rising Edge	10	—	ns
2, 3	SCLK Frequency	—	8	MHz
2	SCLK High Pulse Width	50	—	ns
3	SCLK Low Pulse Width	50	—	ns
4	SDI to SCLK Rising Edge Setup Time	10	—	ns
5	SCLK Rising Edge to SDI Hold Time	5	—	ns
6	SCLK Rising Edge to $\overline{CS}$ Hold Time	5	—	ns
7	$\overline{CS}$ Inactive Cycle Time	100	—	ns
8	$\overline{CS}$ Inactive to SDO Three-State	100	—	ns
9	SCLK Falling Edge to SDO Valid Time		50	ns
—	Rise/Fall Time (10% to 90%) SCLK, SDI, SDO	—	20	ns

NOTE(S): See Figures 4-6 through 4-8.

Figure 4-6. Host Serial Port Timing Diagram

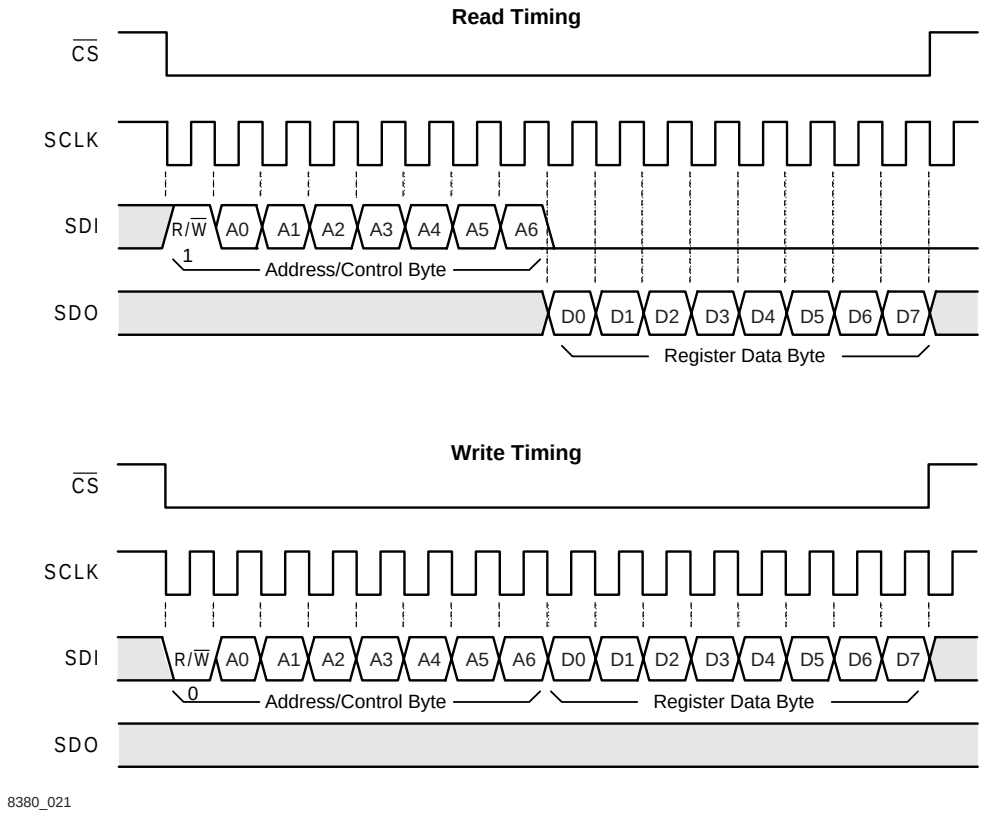


Figure 4-7. Host Serial Port Write Timing

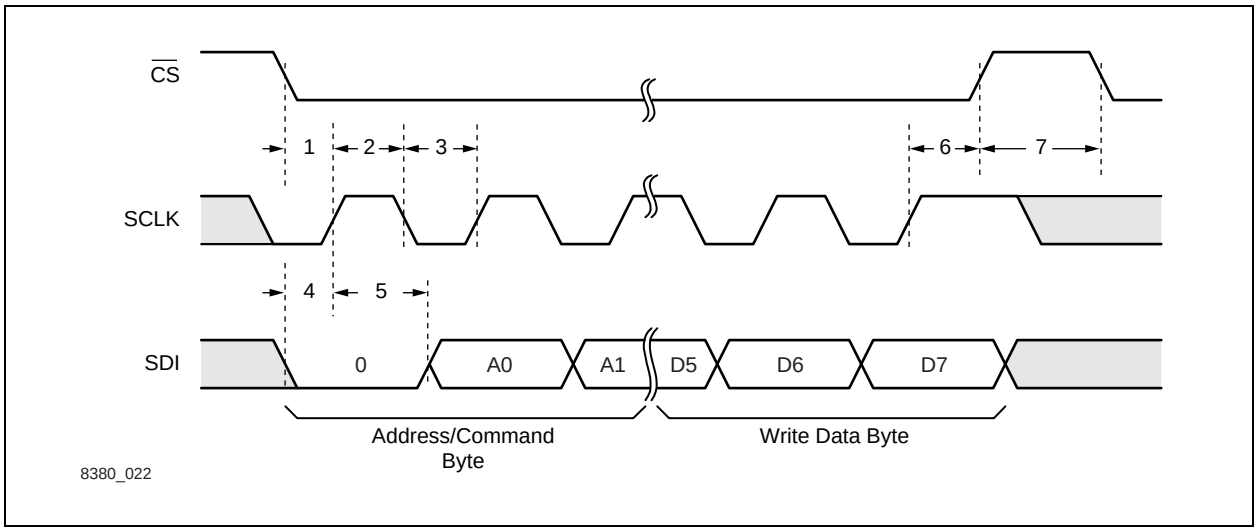


Figure 4-8. Host Serial Port Read Timing

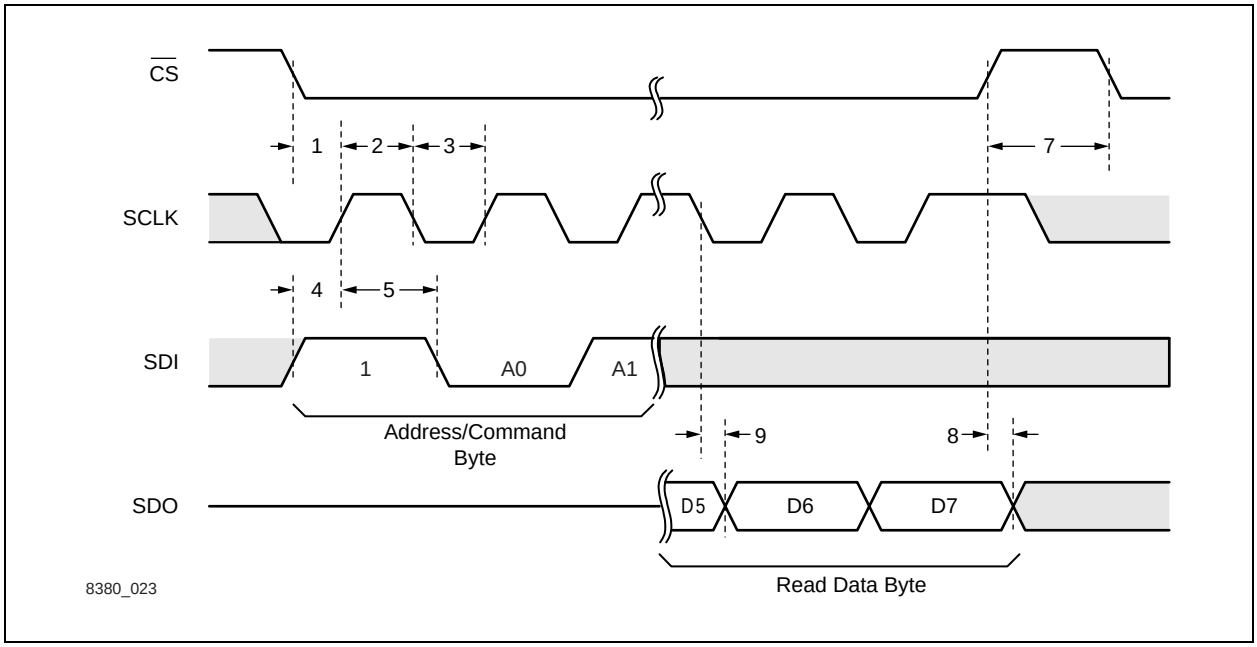
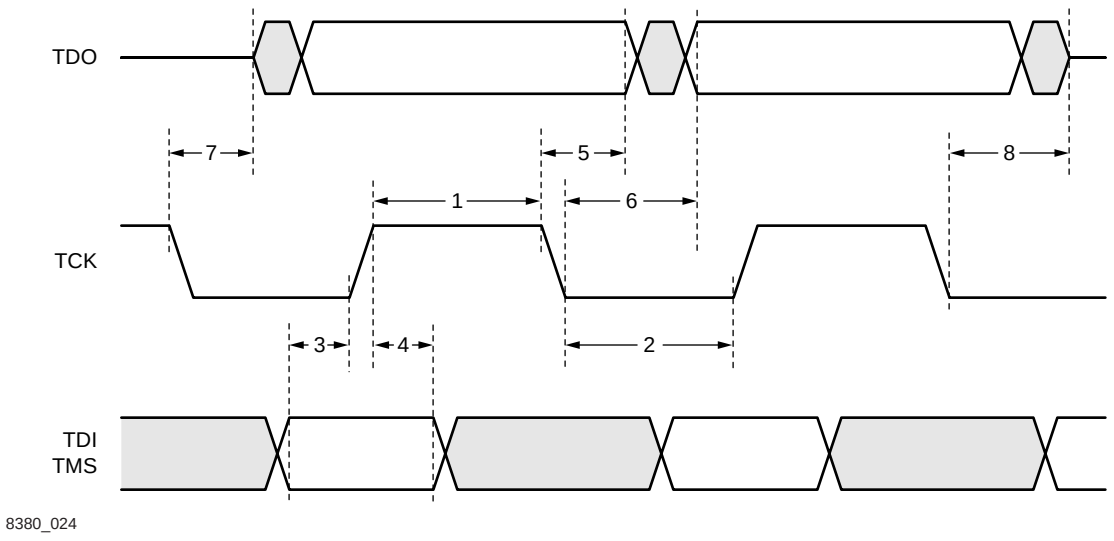


Table 4-11. JTAG Interface Timing Parameters

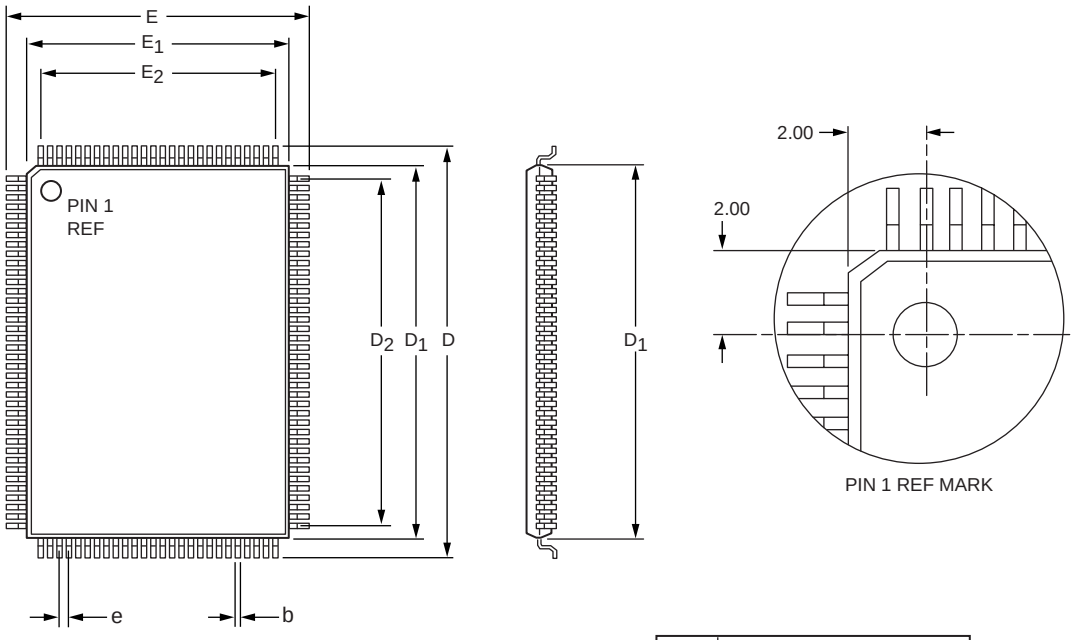
Symbol	Parameter	Minimum	Maximum	Units
1	TCK pulse width high	80	—	ns
2	TCK pulse width low	80	—	ns
3	TMS, TDI setup to TCK rising edge	20	—	ns
4	TMS, TDI hold after TCK high	20	—	ns
5	TDO hold after TCK falling edge	0	—	ns
6	TDO delay after TCK low	—	50	ns
7	TDO enable (Low Z) after TCK falling edge	2	—	ns
8	TDO disable (High Z) after TCK low	—	25	ns
NOTE(S): See Figure 4-9.				

Figure 4-9. JTAG Interface Timing Diagram



4.6 Packaging

Figure 4-10. 128-Pin MQFP Mechanical Drawing



SYMBOL	ALL DIMENSIONS IN MILLIMETERS		
	MIN.	NOM.	MAX
A		3.04	3.40
A_1	0.25	0.33	
A_2	2.57	2.71	2.87
D		23.20 REF.	
D_1		20.0 REF.	
D_2		18.5 REF	
E		17.20 RE.	
E_1		14.0 REF	
E_2		12.5 REF	
L	0.73	0.88	1.03
L_1		1.6 REF	
e		0.50 BSC	
b	0.13	----	0.28
c	0.13	----	0.23
Ref. 128-PIN MQFP (GP00-D448)			

Appendix A: Applicable Standards

Table A-1. Applicable Standards *(1 of 2)*

Standard	Title
ANSI	
T1.101-1987	Digital Hierarchy—Timing Synchronization
T1.102-1993	Digital Hierarchy—Electrical Interfaces
T1.403-1995	Network to Customer Installation—DS1 Metallic Interface
T1.408-1990	ISDN Primary Rate—Customer Installation Metallic Interfaces
AT&T	
TR 41449-1986	ISDN Primary Rate Interface Specification
TR 43801(A)-1985	Digital Channel Bank—Requirements and Objectives
TR 62411-1990	Accunet T1.5 Service Description and Interface Specification
CB 119	Compatibility Bulletin
Bellcore	
TR-TSY-000008 Issue 2, 1987	Digital Interface Between the SLC 96 Digital Loop Carrier System and a Local Digital Switch
TR-TSY-000009 Issue 1, 1986	Asynchronous Digital Multiplexer Requirements and Objectives
TR-NPL-000054 Issue 1, 1989	High-Capacity Digital Service (HCDS) Interface Generic Requirements
TR-NWT-000057 Issue 2, 1993	Functional Criteria for Digital Loop Carrier Systems
TR-TSY-000170 Issue 2, 1993	Digital Cross-Connect System (DCS) Requirements and Objectives
TR-TSY-000191 Issue 1, 1986	Alarm Indication Signal (AIS) Requirements and Objectives
TR-TSY-000303 Issue 2, 1992	Integrated Digital Loop Carrier (IDLC) System Generic Requirements
TR-NPL-000320 Issue 1, 1988	Fundamental Generic Requirements for Metallic Digital Signal Cross-connect Systems
TA-TSY-000435 Issue 1, 1987	DS1 Automatic Facility Protection Switching (AFPS) Rqts. and Objectives
TR-NWT-000499 Issue 5, 1993	Transport Systems Generic Requirements
SR-NWT-002343 Issue 1, 1993	ISDN Primary Rate Interface Guidelines for Customer Premises Equipment
ETSI	
ETS 300 011 (4/92)	ISDN Primary Rate User-Network Interface Specification and Test Principles
ETS 300 233	Access Digital Section for ISDN Primary Rate

Table A-1. Applicable Standards *(2 of 2)*

Standard	Title
ITU-T	
Recommendation G.703 (1991)	Physical/Electrical Characteristics of Hierarchical Digital Interfaces
Recommendation G.704 (1991)	Synchronous Frame Structures used at Primary Hierarchical Levels
Recommendation G.706 (1991)	Frame Alignment and CRC Procedures Relating to G.704 Frame Structures
Recommendation G.732	Characteristics of Primary PCM Multiplex Equipment at 2048 kbps
Recommendation G.733	Characteristics of Primary PCM Multiplex Equipment at 1544 kbps
Recommendation G.734	Characteristics of Synchronous Digital Multiplex Equipment at 1544 kbps
Recommendation G.735	Characteristics of Primary PCM Multiplex Equipment at 2048 kbps; offering Synchronous Digital Access at 384 kbps and/or 64 kbps
Recommendation G.736	Characteristics of Synchronous Digital Multiplex Equipment at 2048 kbps
Recommendation G.737	Characteristics of External Access Equipment at 2048 kbps; offering Synchronous Digital Access at 384 kbps and/or 64 kbps
Recommendation G.738	Characteristics of Primary PCM Multiplex Equipment at 2048 kbps; offering Synchronous Digital Access at 320 kbps and/or 64 kbps
Draft Recommendation G.775	Loss of Signal (LOS) and Alarm Indication Signal (AIS) Defect Detection
Recommendation G.821	Error Performance Monitoring on International Connections
Recommendation G.823 (3/93)	Control of Jitter and Wander in Digital Networks based on 2048 kbps
Recommendation G.824 (3/93)	Control of Jitter and Wander in Digital Networks based on 1544 kbps
Recommendation I.431	Primary Rate User-Network Interface—Layer 1 Specification
Recommendation K.10	Unbalance about Earth of Telecommunication Installations
Recommendation K.20	Resistibility of Switching Equipment to Overvoltages and Overcurrents
Recommendation M.3604	Application of Maintenance Principles to ISDN Primary Rate Access
IEEE Std 1149.1a-1993	IEEE Standard Test Access Port and Boundary Scan Architecture (JTAG)
FCC Part 68.302 (d)	Environment Simulation Metallic Voltage Surge
FCC Part 68.308	Signal Power Limitations

Appendix B: External Component Specifications

Table B-1 lists the transformer specifications. Table B-2 lists the REFCKI crystal oscillator specifications. Figure B-1 illustrates the minimum hardware configuration.

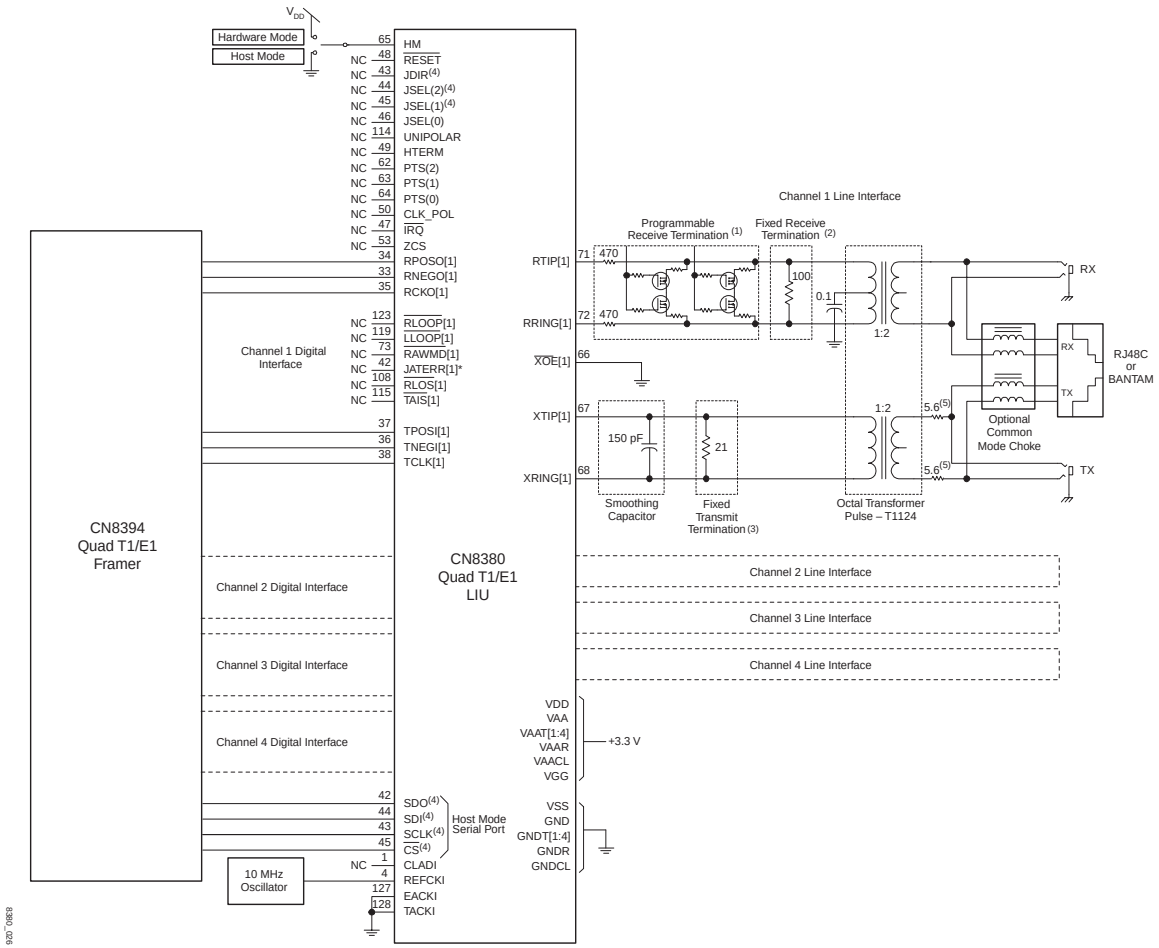
Table B-1. Transformer Specifications

Parameter	RX Value	TX Value
Turns Ratio	2:1 CT	1:2
Pulse Engineering Part Number: Temp. 0 °C to 70 °C Octal SMT	Pulse (1) T1124	
Serial Resistance	1 Ω maximum	
Primary Inductance	OCL 1.2 mH @ 25 °C	
Isolation Voltage	1500 V_{rms}	
Leakage Inductance	0.8 µH	
Note(s): (1) Contact Pulse Engineering for other part numbers: Phone (619) 674-8100 Web: http://www.pulseeng.com		

Table B-2. REFCKI (10 MHz) Crystal Oscillator Specifications

Parameter	Value
Nominal Frequency	10 MHz
Frequency Accuracy (E1)	±50 ppm
Frequency Accuracy (T1)	±32 ppm
Output Level (1)	3.3 V Logic, CMOS or TTL
Aging	2 ppm/year, 10 ppm maximum
Note(s): (1) If the V_{GG} pin is connected to +5 V supply, 5 V logic output may be used. Refer to the V_{GG} pin description in Chapter 1.0, *Pin Descriptions* .	

Figure B-1. Minimum Hardware Configuration



Note(s):

(1) Optional programmable receive termination: 75/100/120 Ω

(2) Required fixed receive termination. The parallel combination of the fixed termination and programmable termination must match the line impedance.

(3) Optional fixed transmit termination. The value shown provides acceptable transmit return loss for T1 and E1 applications. (See Table 2-7, *Transmit Termination Option D*.)

(4) Pins shown twice for Hardware Mode and Host Mode.

(5) In Hardware Mode, 5.6 Ω line feed resistors are required. In Host Mode, they are optional.

Appendix C: Acronym List

Acronym	Definition
AGC	automatic gain control
AIS	alarm indication signal
AMI	alternate mark inversion
ANSI	American National Standards Institute
B8ZS	binary with 8-zero substitution
BABT	British Approvals Board for Telecommunications
BPV	bipolar violation
BSDL	boundary scan description language
CCIR	International Radio Communications Committee
CIF	common interchange format
CLAD	clock rate adapter
CMOS	complementary metal-oxide semiconductor
CRC	cyclic redundancy check
CSU	channel service unit
DAC	digital-to-analog converter
DMA	direct memory access
DPM	driver performance monitor
DSX	digital signal cross connect
ETSI	European Telecommunications Standards Institute
FCC	Federal Communications Commission
FIFO	first-in first-out buffer
GPIO	general purpose input/output
HDB3	high-density bipolar of order 3
HDSL	high bit-rate digital subscriber line
I^2C	inter-integrated circuit
ISDN	Integrated Services Digital Network
ITU–T	International Telegraph and Telephone Consultative Committee
JAT	jitter attenuator
JTAG	Joint Test Action Group
LAL	local analog loopback

LDL	local digital loopback
LIU	line interface unit
LOS	loss of signal
MSB	most significant bit
NCO	numerically controlled oscillator
NCTE	network channel-terminating equipment
NRZ	non-return to zero
PCI	peripheral component interconnect
PCM	pulse code modulation
PLL	phase locked loop
MQFP	metric quad flat pack
PRBS	pseudo-random bit sequence
PRI	primary rate interface
RALOS	receive loss of analog input
RLL	remote line loopback
RLOS	receive loss of signal
RPLL	receive phase lock loop
RZCS	receive zero code suppression
SDH	Synchronous Digital Hierarchy
SONET	Synchronous Optical Network
TAP	test access port
TLOC	transmit loss of clock
TLOS	transmit loss of signal
TZCS	transmit zero code suppression
UI	unit interval
UTP	unshielded twisted pair
ZCS	zero code suppression



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Упорный труд, качественный результат дают нам право быть уверенными в себе и надежными для наших клиентов.

Наша компания это:

- Гарантия качества поставляемой продукции
- Широкий ассортимент
- Минимальные сроки поставок
- Техническая поддержка
- Подбор комплектации
- Индивидуальный подход
- Гибкое ценообразование

Наша организация особенно сильна в поставках модулей, микросхем, пассивных компонентов, ксайленсах (XC), EPF, EPM и силовой электроники.

Большой выбор предлагаемой продукции, различные виды оплаты и доставки, позволят Вам сэкономить время и получить максимум выгоды от сотрудничества с нами!

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Перечень производителей, продукцию которых мы поставляем на российский рынок



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С удовольствием будем прорабатывать для Вас поставки всех необходимых компонентов по текущим запросам для скорейшего выявления групп элементов, по которым сотрудничество именно с нашей компанией будет для Вас максимально выгодным!

С уважением,

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