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Evaluating the AD9551 Multiservice Clock Generator

FEATURES

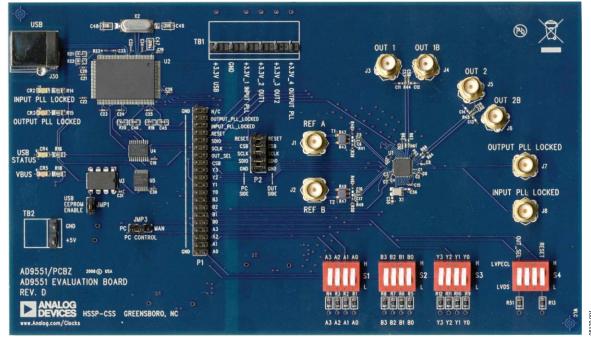
Simple power connection using USB connection and on-board LDO voltage regulators LDOs are easily bypassed for power measurements **AC-coupled differential LVPECL SMA connectors** SMA connectors for 2 reference inputs 2 PLL lock detect outputs Microsoft Windows®-based evaluation software with simple graphical user interface **On-board PLL loop filter** Easy access to digital I/O and diagnostic signals via I/O header **Status LEDs for diagnostic signals USB** computer interface Dip switch configurable for manual operation Software calculator provides flexibility, allowing programming almost any rational input/output frequency ratio

GENERAL DESCRIPTION

This user guide describes the hardware and software of the AD9551 evaluation board and includes detailed schematics and PCB layout artwork. The AD9551 Revision D evaluation board is a compact, easy to use platform for evaluating all features of the AD9551 multiservice clock generator.

The AD9551 accepts one or two reference input signals to synthesize one or two output signals. The AD9551 uses a fractional-N PLL that precisely translates the reference frequency to the desired output frequency. The input receivers and output drivers provide both single-ended and differential operation. Reference conditioning and switchover circuitry internally synchronizes the two references so that if one reference fails, there is virtually no phase perturbation at the output.

The AD9551 uses an external crystal and an internal DCXO to provide for holdover operation. If both references fail, the device maintains a steady output signal. This may mislead you to believe that the PLL is locked and the board is configured properly. A simple test is to move the input REF A or REF B clock a few kilohertz and verify that the changes in output frequency track the input.



DIGITAL PICTURE OF THE EVALUATION BOARD

Figure 1. AD9551 Evaluation Board, Revision D

Evaluation Board User Guide

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REVISION HISTORY

4/09—Revision 0: Initial Version

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EVALUATION BOARD HARDWARE

The following instructions are for setting up the physical connections to the AD9551 evaluation board.

SETTING UP THE POWER AND PC CONNECTIONS

Set up the power and PC connections as follows:

1. Install the AD9551 evaluation software before connecting the evaluation board to your PC for the first time (see the Installing the Software section). Administrative privileges are required for installation.

The AD9551 has the option of either being pin or register programmable. If the pin programmable option is desired, then no software is needed to control the part. However, it is recommended to install the software because if it is not installed, the computer will recognize the evaluation board as new hardware and attempt to install drivers.

2. Connect the USB cables to the evaluation board and the computer.

The red LED labeled VBUS (CR2) on the AD9551 evaluation board should illuminate, and the USBSTAT LED should start blinking. If the USBSTAT LED is not blinking, ensure that the USB port on the PC is operational and that the USB cable is not damaged.

3. If the **Found New Hardware Wizard** automatically appears when the evaluation board is connected, select **Install the software automatically** and then click **Next**.

The **Found New Hardware Wizard** may appear twice, and a system restart may be required.

Refer to the Evaluation Board Software section for details on running the AD9551 evaluation board software.

SETTING UP THE SIGNAL CONNECTIONS

After setting up the power and PC connections, use the following procedure to set up the signal connections:

1. Connect a signal generator to REF A SMA Connector J1.

By default, the reference inputs on this evaluation board are ac-coupled and terminated 50 Ω to ground. An amplitude setting of 6 dBm is sufficient.

- 2. To connect a signal to REF B, connect the signal to SMA Connector J2.
- 3. Connect an oscilloscope, spectrum analyzer, or other lab equipment to any of the J3 to J6 SMA connectors on the upper right side of the board. The output connectors are single ended. A 50 Ω termination should be placed on all unused outputs.

BYPASSING THE USB POWER SUPPLY

The evaluation board can be configured to supply power to the AD9551 from an external power supply. Bypass the USB power supply as follows:

- 1. Remove the F2 ferrite bead (located on the backside of the board).
- 2. Connect a bench power supply to Pin 3.3V_1 of TB1 on the evaluation board. In addition, resistors on the evaluation board can be removed to further separate power supply connections to the AD9551. This is useful for measuring the AD9551 power consumption. Refer to the evaluation board schematics provided on the CD in the evaluation board kit (also available at www.analog.com) for further details.

EVALUATION BOARD SOFTWARE

The instructions included in this section are for setting up the AD9551 evaluation board software.

INSTALLING THE SOFTWARE

Do not connect the evaluation board until the software installation is complete. To install the software,

- 1. Insert the AD9551 evaluation software CD-ROM into a PC CD disc drive.
- 2. Click **My Computer**, and then double-click the **AD9551EV CD** icon.

A window opens showing the contents of the CD divided into four sections: data sheet, layout, schematic, and software. The **readme.txt** file contains a description of the CD-ROM contents, as well as any last minute instructions or information.

- Double-click the Software folder, and then double-click AD9551Eval_Setup1.1.0.exe. Follow the installation instructions. The default location for the evaluation software is C:\Program Files\Analog Devices\AD9551 Eval Software\.
- 4. If there are any updates to the evaluation software on a supplemental CD or in the **\Software\Updates** folder, be sure to copy the new .EXE file, as well as any setup files, to the default location.

USING THE SOFTWARE

After the evaluation software has been installed, you can run the software as follows:

- 1. Power up and connect the evaluation board to the PC.
- 2. Double-click **AD9551 Eval Software** to run the AD9551 evaluation software.

A hardware installation window appears. Depending on whether the evaluation board was found by the software, the text in this window is either light blue, indicating that the evaluation board was found, or red, indicating that the evaluation board was not found.

3. If the evaluation board was found, click in the window when the **Evaluation Software Ready** message appears.

The main window of the evaluation board software appears. Proceed to the Guide to Programming the AD9551 section for more details about using the software.

- 4. If the evaluation board was not found, a dialog box appears that allows you to select an evaluation board to use while the software runs in standalone mode. Standalone mode is useful for viewing and generating register setup files.
- 5. If you connect the evaluation board while the evaluation board software is running, the window shown in Figure 2 usually appears to prompt you to load the evaluation board with the evaluation board software settings or to read the current evaluation board settings into the software.

SYNC Evaluation Software				
Communication with the evaluation board has been restored!				
The current state of the AD9520 is unknown! Click the SYNC button to synchronize the evaluation board and software.				
Options				
$\ensuremath{\mathfrak{C}}$ Load the evaluation board with the current software settings.				
C Read the current evaluation board settings into the software.				
SYNC Cancel				

Figure 2. SYNC Evaluation Software Window

6. If the evaluation board was not automatically detected when it was connected, choose **Select Evaluation Board** from the **I/O** menu, and then select EZSSP-0, EZSSP-1, or EZSSP-2 (see Figure 3).

Select the Evaluation Board to use:		
Device	Firmware Rev.	HostID
Ezssp-O	1.4	Using
[]		1

Figure 3. Select USB Device Window

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GUIDE TO PROGRAMMING THE AD9551

The AD9551 can be programmed via an SPI port or by setting the logic levels on the frequency select pins of the device. To program the device using the serial port, the evaluation board software must be installed.

For pin programming, there are two options: manually use the dip switches or use the evaluation board software to override the settings of the dip switches and change the logic levels of the frequency select pins. Using the dip switches on the evaluation board to establish the logic levels on the pins allows the AD9551 to power on with preset conditions. Alternatively, you can use the software to override the settings of the dip switches on the evaluation board and change the logic levels on the frequency select pins.

USING AN SPI PORT

After the evaluation software is installed and the evaluation board is connected to a PC and loaded with the software, the following procedure can be used to configure and lock the PLLs.

In this example, the input frequency is 622.08 MHz on REF A, and the output frequency is 622.08 MHz.

- 1. Ensure that Jumper JMP3 is positioned for PC control.
- 2. Verify that all five jumpers are in place on Connector P2.
- 3. Set the S1, S2, and S3 switches high. Set the S4 switch setting to high, except for RESET, which must be set to low (RESET is an active high pin).

These steps assume that the input signal is present, that the evaluation board has not been modified, and that the PLL loop filter is suitable for the application. However, this guide covers only simple PLL operation (that is, to start and run the PLL). For a detailed explanation of more advanced AD9551 features, see the AD9551 data sheet. In addition, see the Software Operation section.

USING DIP SWITCHES (MANUAL CONTROL)

The following procedure explains how the AD9551 can be programmed manually by using the dip switches on the evaluation board to set the logic levels of the frequency select pins.

In this example, the input frequency is 622.08 MHz on REF A, and the output frequency is 622.08 MHz.

- 1. Ensure Jumper JMP3 is positioned for manual control.
- 2. Verify that all five jumpers are removed on Connector P2.
- 3. Set the S1, S2, and S3 dip switch positions to low. (Note that S2 controls REF B. If REF B is not used, there is no need to change the S2 settings.).
- 4. Connect a signal generator to REF A SMA Connector J1. By default, the reference inputs on this evaluation board are ac-coupled and terminated 50 Ω to ground.

- 5. Set the amplitude and frequency. An amplitude setting of 6 dBm is sufficient. Set the frequency to 622.08 MHz.
- 6. To connect a signal to REF B, connect the signal to SMA Connector J2.
- 7. Connect an oscilloscope, spectrum analyzer, or other lab equipment to any of the J3 to J6 SMA connectors on the upper right side of the board.
- 8. Power the evaluation board by plugging it into the USB port.
- 9. A frequency of 622.08 MHz should be observed on the OUT1 SMA connector.

If another input and/or output frequency is desired, remove the USB port. Then change the dip switch settings, and reapply the USB port connection.

After each dip switch setting, the AD9551 must be powered down by removing the USB cable to reprogram the AD9551. See the AD9551 data sheet for an explanation of pin programming.

USING SOFTWARE TO OVERRIDE DIP SWITCHES (SOFTWARE CONTROL)

The evaluation board software can be used to override the settings of the dip switches and apply a logic level to the AD9551 frequency selection pins.

After the evaluation software is installed and the evaluation board is connected to a PC and loaded with the software, the following steps can be used to configure and lock the PLLs.

In this example, the input frequency is 622.08 MHz on REF A, and the output frequency is 622.08 MHz.

- 1. Ensure that Jumper JMP3 is positioned for PC control.
- 2. Verify that all five jumpers are in place on Connector P2.
- 3. Set the S1, S2, and S3 dip switch positions to high.
- Select 622.08 MHz for the input frequency in the REF A (MHz) box in the main window of the evaluation software (see Figure 4 and the Reference Input Boxes section for more information).
- Select 622.08 MHz for the output frequency in the Output Loop Config: box in the main window of the evaluation software (see Figure 4).
- 6. A frequency of 622.08 MHz should be observed on the OUT SMA connector.

These steps assume that the input signal is present, that the evaluation board has not been modified, and that the PLL loop filter is suitable for the application. However, these steps are appropriate only for simple PLL operation (that is, to set up and run the PLL). See the AD9551 data sheet for more information about the various AD9551 features.

SOFTWARE OPERATION

The main window of the AD9551 evaluation board software is comprised of subsections that correspond to the major functional blocks of the AD9551 (see Figure 4). These subsections, most of which have their own window, are outlined in this section. From the main window, the window for each functional block can be accessed by clicking the appropriate box in the main window. When a subsection window closes after clicking **OK**, you may notice that the **LOAD** button on the main window starts blinking. This indicates that there are settings that have not been loaded to the AD9551 evaluation board. Click **LOAD** to load these settings to the evaluation board.

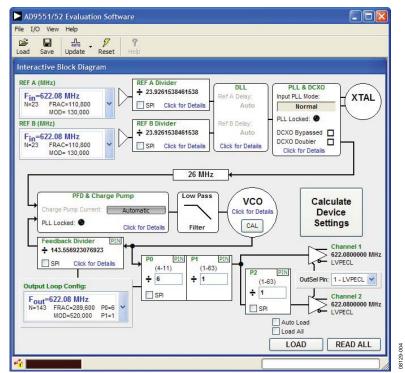


Figure 4. AD9551 Evaluation Software Main Window

MENU BAR OF MAIN WINDOW

File Menu

The **File** menu allows you to load a previously saved AD9551 setup file or to save a new AD9551 setup file. A setup file (.STP) is a text file that contains the AD9551 register setup file, plus any evaluation board settings.

To load a previously saved setup file, select **Load Setup** from the **File** menu. Note that you must still perform a VCO calibration. Alternatively, to save a new setup file, select **Save Setup** from the **File** menu.

To exit the evaluation software, select **Exit** from the **File** menu. However, note that no checking is done to ensure that the existing setup is saved.

I/O Menu

The AD9551 evaluation system allows one PC to control multiple evaluation boards. The **Select USB Device** window, accessed by choosing **Select Evaluation Board** from the **I/O** menu, allows you to select which evaluation board the software controls (see Figure 5). Click **Refresh List** to detect a recently connected evaluation board.

Sel	ect the Evaluation Board	to use:
Device	Firmware Rev.	HostID
Ezssp-0	1.4	Using

Figure 5. Select USB Device Window

Selecting **Configure Serial Port** from the **I/O** menu allows you to control how the USB controller interacts with the AD9551 serial port (see Figure 6) by configuring Register 0x00 (shown as 00H in Figure 8).

🖃 Serial Port C 🔳 🗖 🔀	
Data Format:	
MSB First	
LSB First	
Reset Serial Port	
LOAD READ	000 00100

Figure 6. Serial Port Configuration Window

View Menu

The **Debug** window, accessed by selecting **Debug Window** from the **View** menu, allows you to write and read registers directly and to force the various configuration pins high or low (see Figure 7).

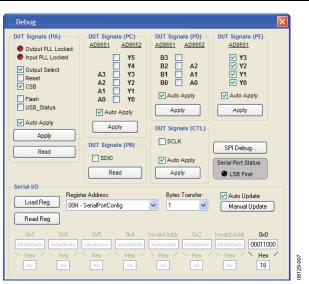


Figure 7. Debug Window

The **Register Map Debug** window, accessed by selecting **Register Debug Window** from the **View** menu, allows you to write and read registers (see Figure 8).

🖻 Register Map Debu	3			×
Register	Data	Load All	ReadAll)
00H SerialPortConfig	00011000	Load	Read	^
02H VersionRegister	00000000	Load	Read	-
04H ReadBackControl	00000000	Load	Read	
05H IOupdate	00000000	Load	Read	
06H reserve1	00000000	Load	Read	
07H reserve2	00000000	Load	Read	
0AH PFD-ChargePump	10000000	Load	Read	
0BH PFD-ChargePump	00110000	Load	Read	
0CH PFD-ChargePump	00000000	Load	Read	
0DH PFD-ChargePump	00000000	Load	Read	
0EH VCOsettings	01110100	Load	Read	
0FH VCOsettings	10000000	Load	Read	
10H VCOsettings	10000000	Load	Read	
11H OPPLLControl	00000000	Load	Read	
12H OPPLLControl	10000000	Load	Read	
13H OPPLLControl	00000000	Load	Read	
14H OPPLLControl	00000000	Load	Read	
15H OPPLLControl	00100000	Load	Read	
16H OPPLLControl	00000000	Load	Read	~
<			>	

Figure 8. Register Map Debug Window

Help Menu

Selecting **Help** from the **Help** menu opens the **About AD9551** window, which contains information such as revision number, region information, and contact information.

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BUTTON BAR OF MAIN WINDOW

The buttons described in this section provide easy access to common features.

Load and Save

Clicking **Load** and **Save** allows you to load and save an AD9551 setup file. A setup file (.STP) is a text file that contains the AD9551 register setup file, plus any evaluation board settings.

Update

Clicking **Update** toggles the I/O update bit (Register 0x05, Bit 0) of the AD9551.

Reset

Clicking **Reset** resets the evaluation board and restores the AD9551 to its default power-up state. In addition, clicking **Reset** enables the VCO calibration function by writing the enable VCO calibration bit.

USING SOFTWARE TO CONTROL THE FUNCTIONAL BLOCKS OF AD9551

The AD9551 evaluation software contains subsections that correspond to the major functional blocks of the AD9551. These subsections, most of which have their own window, are described in this section.

You can access each window by clicking **Click for Details** in the appropriate subsection box of the main window.

Most subsection boxes in the main window have a checkbox labeled **SPI**. If this box is selected, the software allows serial port writes when conditions are changed in the corresponding subsection window.

When a subsection window closes after clicking **OK**, you may notice that the **LOAD** button on the main window starts blinking. This indicates that there are settings that have not been loaded to the AD9551 evaluation board. Click **LOAD** to load these settings to the evaluation board.

Reference Input Boxes

The reference input boxes, which are labeled **REF A** (**MHz**) and **REF B** (**MHz**) in the main window, allow you to select an input frequency for REF A and REF B (see Figure 9 for an example for REF A). These boxes can be used to change the logic levels of the input frequency select pins.

REF A Divider + 23.9261538461538 REF A (MHz) PLL & DCX Fin=622.08 MHz XTAL SPI Click for Details Normal FRAC=110,800 MOD= 130,000 PLL Locked: 0 REF B Divider + 23.9261538461538 Fin=622.08 MHz h=23 FRAG=110, H000-130 DCXO Bypassed DCXO Doubler SPI Click for Detail Fin=625 MHz N=24 FRAC=-120,000 MOD= 130,000 26 MHz Fin=627.33 MHz N=24 FRAC=-114,594 MOD= 154,050 Low Pas vco Calculate Fin=641.52 MHz N=24 FRAC=45,200 MOD= 130,000 Device Settings CAL Click for De Filter Fin=644.53125 MHz N=24 FRAC=96,400 MOD= 166,400 D0 PIN P1 Fin=657.421875 MHz N=25 FRAC=-44,625 MOD= 104,000 LVPECL (4-11) (1-63) ÷ 5 (1-63) Fin=660.18 MHz N=25 FRAC=-42,891 MOD= 198,016 SPI S Fin=666.51 MHz N=25 FRAC=41,820 MOD= 154,700 Auto Load R129-009 LOAD READ ALL Fin=669.33 MHz

Figure 9. REF A List Box (in Main Window)

Reference Dividers

Clicking **Click for Details** in the **REF A Divider** and **REF B Divider** boxes of the main window accesses the **RefA Input Divider** window and the **RefB Input Divider** window (see Figure 10 for an example of the **RefA Input Divider** window).

These windows are used to set the desired reference divider for the integer or Σ - Δ modulator mode. The counters can be set individually.

RefA Input Divider	
Divider	
SDM Value:	16.25
Integer Value:	(0 to 63) 16
Fractional Value:	(-524288 to 524287) 262144 (0 to 524287)
Modulus Value:	(0 to 524287) -524288
	ОК

Figure 10. RefA Input Divider Window

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DLL Window

Clicking **Click for Details** in the **DLL** box of the main window accesses the **DLL** window (see Figure 11). This window can be used to manually override the automatic time alignment between the REF A and REF B clock input signals to the PLL1 phase detector.

DLL	
Reference A Delay	Reference B Delay
Manual Control	Manual Control
(0 to 76.650ns) Ref A Delay: 38.400 ns	(0 to 76.650ns) Ref B Delay: 38.400 ns
	ОК

Figure 11. DLL Window

Input PLL + DCXO Window

Clicking **Click for Details** in the **PLL & DCXO** box in the main window accesses the **Input PLL + DCXO** window (see Figure 12).

Input PLL + DCXO	
Input PLL	
Input PLL Mode:	Loop Filter Sample Rate Ctrl:
Normal 🗸	Use 8x Clock Divider 🛛 🗸
Crystal Frequency:	Select 2x Frequency Divider:
52.000 MHz 🖌	Bypass 2x Frequency Divider 💟
DCXO Tuning Capacitor	DCXO Varactor Control
Tuning Cap Control Value:	Varactor Value: 0
	ОК

Figure 12. Input PLL + DCXO Window

PFD and Charge Pump Window

Clicking **Click for Details** in the **PFD & Charge Pump** box of the main window accesses the **PFD and Charge Pump** window (see Figure 13).

acklash Period	Charge Pump
Ianual Control	Manual Control
Low High Max	(3.5 μA to 900μA) Charge Pump Current: 448.0 μA
PFD Control Lock Detector: Active	Enable Charge Pump State Control Charge Pump State Control Normal
Active Edge: Positive 🗸	Enable Charge Pump Offset Charge Pump Offset Type: Pump Offset Up
e Mid Supply VCO Control Voltage	Offset Current Magnitude: 1/2
е мю Suppry voo Control Voltage	Offset Current Magnitude: 1/2

Figure 13. PFD and Charge Pump Window

VCO Control Window

Clicking **Click for Details** in the **VCO** box of the main window accesses the **VCO Control** window (see Figure 14).

VCO Control			
General			
Boost VCO Supply by 100mV			
VCO Threshold Level			
Manual Control	Manual Control		
VCO Threshold Level: 6	Band Setting (0 to 127): 64		
Bias Control	VCO Calibrate		
Level Control (0 to 63): 32	Manual Control		
	Manual VCO Calibrate		
	ОК		

Figure 14. VCO Control Window

Feedback Window

Clicking **Click for Details** in the **Feedback Divider** box of the main window accesses the **Feedback** window, which allows you to change the feedback divider settings (see Figure 15).

Feedback		
Feedback Divider		
Integer Mode Disable SDM		OP Reset
SDM Value:	0.25	
	(0 to 255)	
Integer Value:	0	
Fractional Value:	(0 to 1048575) 131072	
Modulus Value:	(0 to 1048575)	
		ОК

Figure 15. Feedback Window

P0, P1, and P2 (Output Dividers) Boxes

Selecting the **SPI** check box in any of the divider settings boxes (that is, the P0, P1, or P2 box) in the main window enables a drop-down selection of predetermined divider settings (see Figure 16).

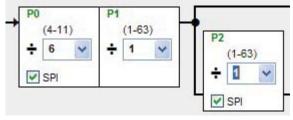


Figure 16. P0, P1, and P2 Boxes (in Main Window)

Output Loop Config: Box

The **Output Loop Config:** box can be used to change the output frequency of the AD9551. This control changes the logic levels of the output frequency selection pins of the AD9551.



Figure 17. Output Loop Config: Box (in Main Window)

OutSel Pin: Box

The **OutSel Pin:** drop-down box (see Figure 18) in the main window controls the logic level on the OUTSEL pin of the AD9551. However, this value can be overwritten by using the SPI control register.

OutSel Pin:	1 - LVPECL	*

Figure 18. OutSel Pin Box (in Main Window)

USING SOFTWARE TO CALCULATE THE DEVICE SETTINGS

The following procedure explains how the evaluation board software can be used to automatically calculate and set the settings to program the AD9551.

In this example, the input frequency is 122.88 MHz on REF A, and the output frequency is 122.88 MHz.

- 1. Ensure that Jumper JMP3 is positioned for PC control.
- 2. Verify that all five jumpers are in place on Connector P2.
- 3. Set the positions of the S1, S2, and S3 dip switches to high.
- 4. Click **Calculate Device Settings** in the main window of the evaluation board software.



Figure 19. Calculate Device Settings Button (in Main Window)

5. The **Enable Control?** window, shown in Figure 20, appears.

Enable	Control?
?	The following sections of the AD9551 are configured using external pins. These sections will not be configured by this tool.
	Input PLL Loop Reference A Divider Reference B Divider
	Output PLL Loop Feed Back Divider P0 and P1 Dividers P2 Divider
	Would you like to allow the calculator to configure these sections?
	Yes No

Figure 20. AD9551 Serial Port Programming Warning

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6. Click Yes to enable serial port register programming.

7. The **Calculator** window, shown in Figure 21, appears.

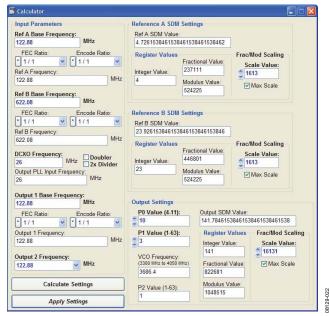


Figure 21. Calculator Window

- 8. Type 122.88 into the **Ref A Base Frequency:** box and 122.88 into the **Output 1 Base Frequency:** box.
- 9. Click **Calculate Settings**, and then click **Apply Settings**. You should now be able to measure 122.88 MHz at the OUT1 SMA connector.

ROUTING 26 MHz TO TEST PORT

The following procedure explains how to route the 26 MHz crystal oscillator to the AD9551 test port. The test port is SMA J7 and is labeled output PLL locked.

In this example, the input frequency is 122.88 MHz on REF A, and the output frequency is 122.88 MHz.

- 1. Ensure that Jumper JMP3 is positioned for PC control.
- 2. Verify that all five jumpers are in place on Connector P2.
- 3. Set the positions of the S1, S2, and S3 dip switches to high.
- 4. Click **Calculate Device Settings** in the main window of the evaluation board software.



Figure 22. Calculate Device Settings Button (in Main Window)

5. The **Enable Control?** window, shown in Figure 23, appears.

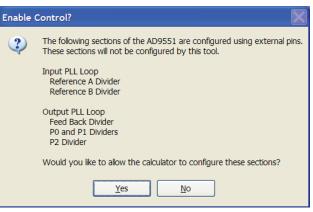


Figure 23. AD9551 Serial Port Programming Warning

- 6. Click Yes to enable serial port register programming.
- 7. The Calculator window, shown in Figure 24, appears.

Input Parameters Ref A Base Frequency:	Reference A SDM Settings Ref A SDM Value:			
122.88 MHz	4.7261538461538461538461538461538462			
PEC Ratio: Encode Ratio: 1 / 1 IIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIII	Register Values Integer Value 4	Fractional Value 237111 Modulus Value	Frac/Mod Scaling Scale Value: 1613	
Ref B Base Frequency: 622.08 MHz		524225	Mar Scale	
FEC Ratio: Encode Ratio:	Reference B SDM Ref B SDM Value: 23 926153846153			
Correspondency: MHz DCXO Frequency: Doubler 26 MHz Doubler Doubler Output PLL Input Frequency: MHz	23 320 153646 153646 153646 153646 153646 Register Values Fractional Value Integer Value: 446801 23 Modulus Value 524225 524225		Frac/Mod Scaling Scale Value: 1613 WMax Scale	
Output 1 Base Frequency: 122.88 MHz	Output Settings			
FEC Ratio: Encode Ratio:	P0 Value (4-11):	Output SDN 141.784615	I Value: 38461538461538461538	
Output 1 Frequency: 122 88 MHz Output 2 Frequency:	P1 Value (1.63): 3 VCO Frequency:	Register V Integer Val		
122.88 MHz	(3300 MHz to 4050 t 3686.4	Hz) Fractional 822681	Value: 🕑 Max Scale	
Calculate Settings	P2 Value (1-63):	Modulus V 1048515	alue:	
Apply Settings				

Figure 24. Calculator Window

- 8. Type 122.88 into the **Ref A Base Frequency:** box and 122.88 into the **Output 1 Base Frequency:** box.
- 9. Click **Calculate Settings**, and then click **Apply Settings**. You should now be able to measure 122.88 MHz at the OUT1 SMA connector.
- 10. From the **View** menu in the main window, select **Register Debug Window**. The window shown in Figure 25 appears.

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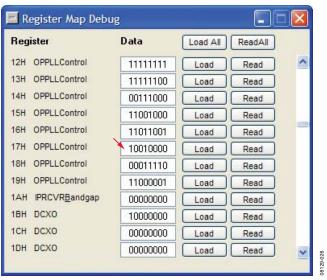


Figure 25. Register Debug Window

- 11. Bit 3 of Register 0x17 must be set to 1 to enable the PLL locked pin as a test port. By default, the 26 MHz crystal frequency is present at the output.
- 12. The ac signal has a dc offset of approximately 1.6 V. Be aware that some test equipment has a limit of 0 V dc; therefore, a dc block must be used in such cases.

SETTING THE 19.44 MHz MODE

The following instructions can be used to configure the AD9551 to operate in the 19.44 MHz mode. Refer to the AD9551 data sheet for more details about this mode of operation.

The following case is an example for the AD9551 in 19.44 MHz mode:

- 1. Replace the crystal on the evaluation board.
- 2. Replace the loop filter capacitor on the evaluation board.
- Click Click for Details in the PLL & DCXO box in the main window of the evaluation board software to access the Input PLL + DCXO window (see Figure 26).
- 4. Select **19.44MHz Mode** in the **Input PLL Mode:** box, and then click **OK**.
- 5. Click **Click for Details** in the **PFD & Charge Pump** box in the main window of the evaluation board software to access the **PFD and Charge Pump** window (see Figure 27).

Evaluation Board User Guide

Input PLL Mode:	Loop Filter Sample Rate Ctrl:	1.000
19.44MHz Mode 🛛 👻	Use 8x Clock Divider	~
Crystal Frequency:	Select 2x Frequency Divider	
52.000 MHz 🛛 🗸	Use 2x Frequency Divider	Y
	able Doubler DCXO Varactor Control	
Bypass DCXO Ena CXO Tuning Capacitor Enable Manual Control Tuning Cap Control Value:		rol

Figure 26. Input PLL + DCXO Window

Anti-backlash Period	Charge Pump	
Manual Control	Manual Control	
	(3.5 µA to 900µA)	
)	Charge Pump Current: 24.5 µA	
Min Low High Max	1	
PFD Control	Enable Charge Pump State Control	
ock Detector: Active		
	Charge Pump State Control: Normal	
eedback Active Edge: Positive		
Ref In Active Edge: Positive	Enable Charge Pump Offset	
	Charge Pump Offset Type: Pump Offset Up	
Use Mid Supply VCO Control Voltage	Offset Current Magnitude: 1/2	
	1/2	

Figure 27. PFD and Charge Pump Window

- Change the charge pump current to the appropriate current level specified in the AD9551 data sheet (approximately 25 μA), and then click OK.
- 7. If the **LOAD** button in the main window starts blinking, this indicates that there are settings that have not been loaded to the AD9551 evaluation board. Click **LOAD** to load these settings to the evaluation board.

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

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