CY25568

Spread Spectrum Clock Generator

FEATURES

- 4 to 32 MHz Input Frequency Range
- 4 to 128 MHz Output Frequency Range
- Accepts Clock, Crystal and Resonator Inputs
- 1x, 2x and 4x Frequency Multiplication
- Non-modulated Reference Frequency Output
- Center and Down Spread Modulation
- Low Power Dissipation
  - 3.3V = 52 mW-typ @ 6MHz
  - 3.3V = 60 mW-typ @ 12MHz
  - 3.3V = 72 mW-typ @ 24MHz
- Power Down Mode
- Low Cycle-to Cycle Jitter
  - 8MHz = 195 ps-typ
  - 16MHz = 175 ps-typ
  - 32MHz = 100 ps-typ
- Available in 16-pin (150 mil.) SOIC package

APPLICATIONS

- Printers and MFPs
- LCD Panels and Monitors
- Digital Copiers
- PDAs
- Automotive
- CD-ROM, VCD and DVD
- Networking, LAN/WAN
- Scanners
- Modems
- Embedded Digital Systems

BENEFITS

- Peak EMI reduction by 8 to 16dB
- Fast Time to Market
- Cost Reduction

GENERAL DESCRIPTION

The Cypress CY25568 is a Spread Spectrum Clock Generator (SSCG) IC used for the purpose of reducing Electro Magnetic Interference (EMI) found in today's high-speed digital electronic systems.

The CY25568 uses a Cypress proprietary Phase-Locked Loop (PLL) and Spread Spectrum Clock (SSC) technology to synthesize and modulate the frequency of the digital clock. By frequency modulating the clock, the measured EMI at the fundamental and harmonic frequencies is greatly reduced.
This reduction in radiated energy can significantly reduce the cost of complying with regulatory agency requirements and improve time to market without degrading system performance.

The CY25568 input frequency range is 4 to 32 MHz and accepts clock, crystal and ceramic resonator inputs. The output clocks can be programmed to produce 1x, 2x and 4x multiplication of the input frequency with Spread Spectrum. A separate non-modulated reference clock is also provided.

The use of 2x or 4x frequency multiplication eliminates the need for higher order crystals and allows the user to generate up to 128 MHz Spread Spectrum Clock (SSC) by using only first order crystals. This will reduce the cost while improving the system clock accuracy, performance and complexity

Center Spread or Down Spread frequency modulation can be selected by the user based on 4 discrete values of Spread % for each Spread Mode with the option of a Non-Spread mode for system test and verification purposes.

The CY25568 is available in a 16 pin SOIC (150-mil.) package with a commercial operating temperature range of 0 to 70°C. Contact Cypress for availability of -25 to +85°C Industrial Temperature Range Operation. Refer to CY25811/12/14 products for 8-pin SOIC package versions of the CY25568.

BLOCK DIAGRAM

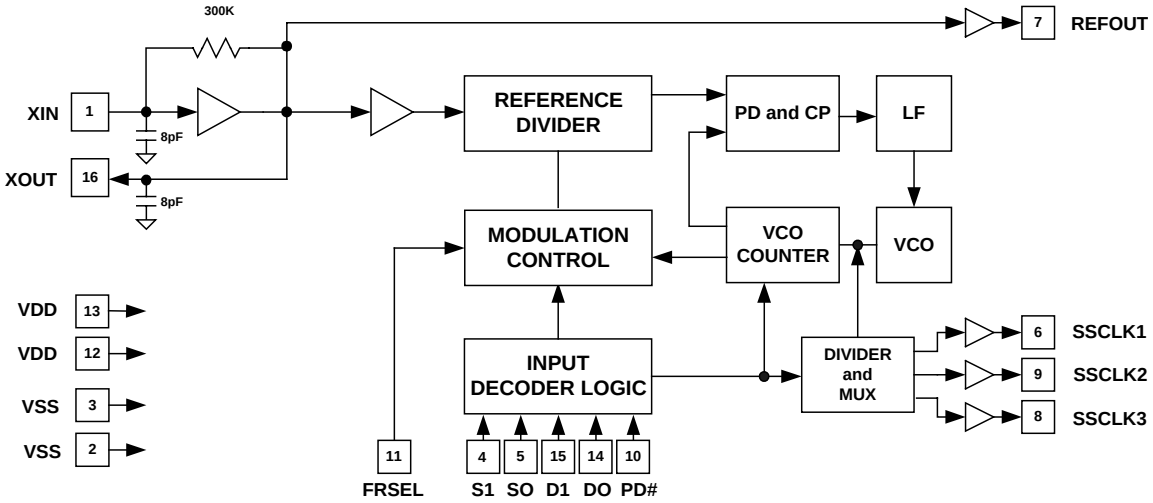


Figure 1. Block Diagram

ORDERING INFORMATION

Part No.	Package	Operating Temperature Range
CY25568SC	16 Pin SOIC	0 to 70°C

Table 1. Ordering Information

PIN CONFIGURATION

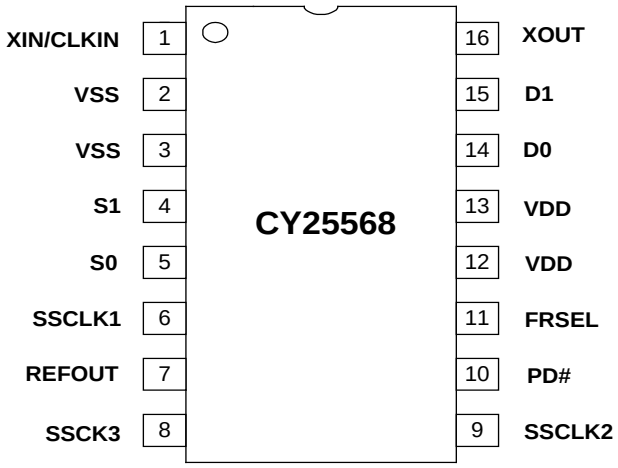


Figure 2. 16 Pin SOIC Pin Assignment

PIN DESCRIPTION

Pin	Function	Description
1	Xin/CLK	Clock, crystal or ceramic resonator input pin.
2	VSS	Power Supply Ground.
3	VSS	Power Supply Ground.
4	S1	Digital Spread % control pin. 3-Level input (H-M-L). Default=M.
5	S0	Digital Spread % control pin. 3-Level input (H-M-L). Default=M.
6	SSCLK1	Output Clock. Refer to Table-6 for frequency programmability.
7	REFOUT	Reference Clock Output. The same frequency as Xin/CLK input.
8	SSCLK3	Output Clock. Refer to Table-6 for frequency programmability.
9	SSCLK2	Output Clock. Refer to Table-6 for frequency programmability.
10	PD#	Power Down Control. Internally Pulled to VDD, Default=High.
11	FRSEL	Input Frequency Range Selection digital control input. 3-Level input (H-M-L). Default=M.
12	VDD	Positive Power Supply.
13	VDD	Positive Power Supply.
14	D0	3-Level (H-M-L) Digital output clock scaling control. Refer to Table-6. Default=M.
15	D1	3-Level (H-M-L) Digital output clock scaling control. Refer to Table-6. Default=M.
16	XOUT	Crystal or ceramic resonator output pin.

Table 2. Pin Description

ABSOLUTE MAXIMUM RATINGS[1]:

Supply Voltage (VDD): +5.5V
Input Voltage Relative to VDD: VDD+0.3V
Input Voltage Relative to VSS: VSS-0.3V

Operating Temperature: 0 to 70°C
Storage Temperature: -65 to +150°C

Note: Operation at any Absolute Maximum Rating is not implied.

DC ELECTRICAL CHARACTERISTICS:

Test Conditions: VDD=3.3V, T=25°, unless otherwise noted.

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
VDD	Power Supply Range	2.90	3.3	3.60	V	
VINH	Input High Voltage	0.85VDD	VDD	VDD	V	S0,S1,D0,D1 and FRSEL Inputs
VINM	Input Middle Voltage	0.40VDD	0.50VDD	0.60VDD	V	S0,S1,D0,D1 and FRSEL Inputs
VINL	Input Low Voltage	0.0	0.0	0.15VDD	V	S0,S1,D0,D1 and FRSEL Inputs
VINH1	Input High Voltage	2.0	-	-	V	PD# Input Only
VINL1	Input Low Voltage	-	-	0.8	V	PD# Input Only
VOH1	Output High Voltage	2.4	-	-	V	IOH = 4 ma, all Output Clocks
VOH2	Output High Voltage	2.0	-	-	V	IOH = 6 ma, all Output Clocks
VOL1	Output Low Voltage	-	-	0.4	V	IOL = 4 ma, all Output Clocks
VOL2	Output Low Voltage	-	-	1.2	V	IOL = 10 ma, all Output Clocks
Cin1	Input Capacitance	6.0	7.5	9.0	pF	Xin (Pin 1) and Xout (Pin 16)
Cin2	Input Capacitance	3.5	4.5	6.0	pF	All Digital Inputs
IDD1	Power Supply Current	-	13.0	16.0	mA	Fin=4MHz, no load (refer to Figure 4C)
IDD2	Power Supply Current	-	28.0	32.0	mA	Fin=32MHz, no load (refer to Figure 4C)
IDD3	Power Supply Current	-	300	400	µA	PD#=GND

Table 3

TIMING ELECTRICAL CHARACTERISTICS:

Test Conditions: VDD=3.3V, T=25°C, CL=15pF. Rise/Fall time @ 0.4 and 2.4V, duty cycle at 1.5 V

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
ICLKFR	Input Frequency Range	4		32	MHz	Clock, Crystal or Ceramic Resonator Input
trise1	Clock Rise Time	2.4	3.2	4.0	ns	SSCLK1,2, and 3, all cases when 1x or 2x scaling selected, when 4x if FRSEL=1 or 0
tfall1	Clock Fall Time	2.4	3.2	4.0	ns	SSCLK1,2, and 3, all cases when 1x or 2x scaling selected, when 4x if FRSEL=1 or 0
trise2	Clock Rise Time	1.2	1.6	2.0	ns	SSCLK2, and 3, only when 4x scaling is selected and FRSEL=M
tfall2	Clock Fall Time	1.2	1.6	2.0	ns	SSCLK2, and 3, only when 4x scaling is selected and FRSEL=M
trise3	Clock Rise Time	2.4	3.2	4.0	ns	REFOUT only
tfall3	Clock Fall Time	2.4	3.2	4.0	ns	REFOUT only
CDCin	Input Clock Duty Cycle	20	50	80	%	XIN/CLK (Pin 1)

[1] **Single Power Supply:** The voltage on any input or I/O pin cannot exceed the power pin during power-up.

CDCout	Output Clock Duty Cycle	45	50	55	%	SSCLK1,2 and 3
CCJ1	Cycle-to-Cycle Jitter	-	195	260	ps	Fin=8 MHz (refer to Figure 4A)
CCJ2	Cycle-to-Cycle Jitter	-	170	225	ps	Fin=16 MHz (refer to Figure 4A)
CCJ3	Cycle-to-Cycle Jitter	-	100	150	ps	Fin=32 MHz (refer to Figure 4A)

Table 4

INPUT FREQUENCY RANGE AND SELECTION

The CY25568 input frequency range is 4 to 32 MHz. This range is divided into 3 segments and controlled by 3-Level FRSEL pin as given in Table 5.

FRSEL	INPUT FREQUENCY RANGE
0	4.0 to 8.0 MHz
1	8.0 to 16.0 MHz
M	16.0 to 32.0 MHz

Table 5 – Input Frequency Selection

OUTPUT CLOCKS

The CY25568 provides 4 separate output clocks, REFOUT, SSCLK1, SSCLK2 and SSCLK3, for use in a wide variety of applications. Each clock output is described below in detail.

REFOUT

REFOUT is a 3.3-volt CMOS level non-modulated copy of the clock at XIN/CLKIN.

SSCLK1, 2 and 3

SSCLK1, SSCLK2 and SSCLK3 are Spread Spectrum clock outputs used for the purpose of reducing EMI in digital systems. Each clock can drive separate nets with a capacitive load of up to 20 pF.

The frequency function of these clock outputs are selected by using 3-Level D0 and D1 digital inputs and are given in Table 6.

D0	D1	REFOUT	SSCLK1	SSCLK2	SSCLK3
0	0	REF	REF	1x	1x
0	M	REF	1x	2x	2x
0	1	REF	REF	2x	2x
M	0	REF	REF	1x	2x
M	M	REF	REF	REF	REF
M	1	REF	REF	2x	4x
1	0	REF	REF	4x	4x
1	M	REF	1x	2x	4x
1	1	REF	1x	2x	4x

REF is the same non-modulated frequency as the input clock.
1x, 2x, or 4x are modulated and multiplied (in the case of 2x and 4x) frequency of the input clock.

Table 6 – Output Clocks Function Selection

SPREAD % SELECTION

The CY25568 provides Center-Spread, Down-Spread and No-Spread functions. These functions and the amount of Spread % are selected by using 3-Level S0 and S1 digital inputs and are given in Table 7.

XIN (MHz)	FRSEL	S1=0 S0=0	S1=0 S0=M	S1=0 S0=1	S1=M S0=0	S1=1 S0=1	S1=1 S0=0	S1=M S0=1	S1=1 S0=M	S1=M S0=M
		CENTER (%)	CENTER (%)	CENTER (%)	CENTER (%)	DOWN (%)	DOWN (%)	DOWN (%)	DOWN (%)	NO SPREAD
4-5	**0**	+/-1.4	+/-1.2	+/-0.6	+/-0.5	-3.0	-2.2	-1.9	-0.7	0
5-6	**0**	+/-1.3	+/-1.1	+/-0.5	+/-0.4	-2.7	-1.9	-1.7	-0.6	0
6-7	**0**	+/-1.2	+/-0.9	+/-0.5	+/-0.4	-2.5	-1.8	-1.5	-0.6	0
7-8	**0**	+/-1.1	+/-0.9	+/-0.4	+/-0.3	-2.3	-1.7	-1.4	-0.5	0
8-10	**1**	+/-1.4	+/-1.2	+/-0.6	+/-0.5	-3.0	-2.2	-1.9	-0.7	0
10-12	**1**	+/-1.3	+/-1.1	+/-0.5	+/-0.4	-2.7	-1.9	-1.7	-0.6	0
12-14	**1**	+/-1.2	+/-0.9	+/-0.5	+/-0.4	-2.5	-1.8	-1.5	-0.6	0
14-16	**1**	+/-1.1	+/-0.9	+/-0.4	+/-0.3	-2.3	-1.7	-1.4	-0.5	0
16-20	**M**	+/-1.4	+/-1.2	+/-0.6	+/-0.5	-3.0	-2.2	-1.9	-0.7	0
20-24	**M**	+/-1.3	+/-1.1	+/-0.5	+/-0.4	-2.7	-1.9	-1.7	-0.6	0
24-28	**M**	+/-1.2	+/-0.9	+/-0.5	+/-0.4	-2.5	-1.8	-1.5	-0.6	0
28-32	**M**	+/-1.1	+/-0.9	+/-0.4	+/-0.3	-2.3	-1.7	-1.4	-0.5	0

Table 7 – Spread % Selection

3-LEVEL DIGITAL INPUTS

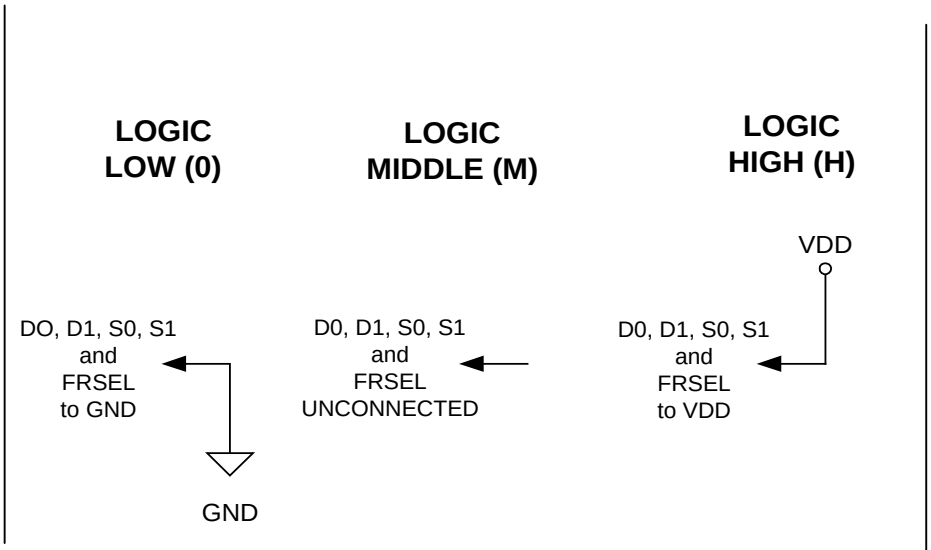


Figure 3. 3-Level Logic

S0, S1, D0, D1 and FRSEL digital inputs of the CY25568 are designed to sense 3 different logic levels designated as High “1”, Low “0” and Middle “M”. With this 3-Level digital input logic, the CY25568 is able to detect 9 different logic states in the case of (S0, S1) and (D0, D1) logic pairs and 3 different logic states in the case of FRSEL.

S0, S1, D0, D1 and FRSEL pins include an on chip 20K (10K /10K) resistor divider. No external application resistors are needed to implement the 3-Level logic levels as shown below:

Logic State “0” = 3-Level logic pin connected to GND.
Logic State “M” = 3-Level logic pin left floating (no connection).
Logic State “1” = 3-Level logic pin connected to VDD.

Figure 3 illustrates how to implement 3-Level Logic.

POWER DOWN (PD#)

CY25568 includes a Power Down (PD#, Pin 10) function. This input uses standard 2-Level CMOS logic and is internally pulled up to VDD (HIGH). Connect this pin to GND if power is to be turned off.

MODULATION RATE

Spread Spectrum Clock Generators utilize frequency modulation (FM) to distribute energy over a specific band of frequencies. The maximum frequency of the clock (fmax) and minimum frequency of the clock (fmin) determine this band of frequencies. The time required to transition from fmin to fmax and back to fmin is the period of the Modulation Rate, Tmod. The Modulation Rate of SSCG clocks are generally referred to in terms of frequency or fmod = 1/Tmod.

The input clock frequency, fin, and the internal divider determine the Modulation Rate.

In the case of CY25568, the (Spread Spectrum) Modulation Rate is given by the following formula: fmod = fin/DR

Where; fmod is the Modulation Rate, fin is the Input Frequency and DR is the Divider Ratio as given in Table 8. Notice that Input Frequency Range is set by FRSEL.

FRSEL	INPUT FREQUENCY RANGE (MHz)	DIVIDER RATIO (DR)
0	4 to 8	128
1	8 to 16	256
M	16 to 32	512

Table 8

CHARACTERISTIC CURVES

The following curves demonstrate the characteristic behavior of the CY25568 when tested over a number of environmental and application specific parameters. These are typical performance curves and are not meant to replace any parameter specified in tables 3 and 4.

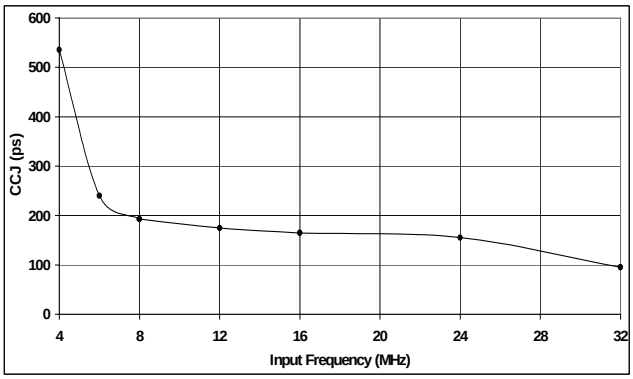


Figure 4A. Jitter vs. Input Frequency (No Load)

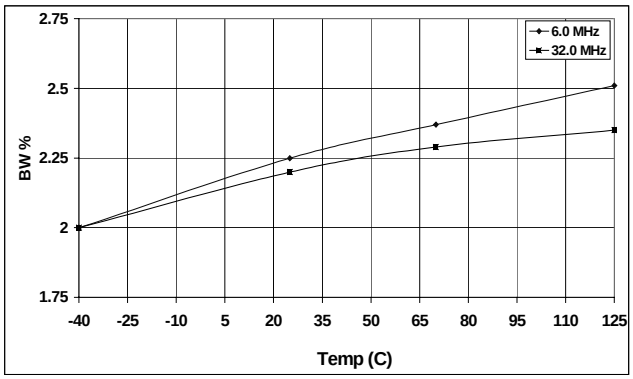


Figure 4B Bandwidth % vs. Temperature

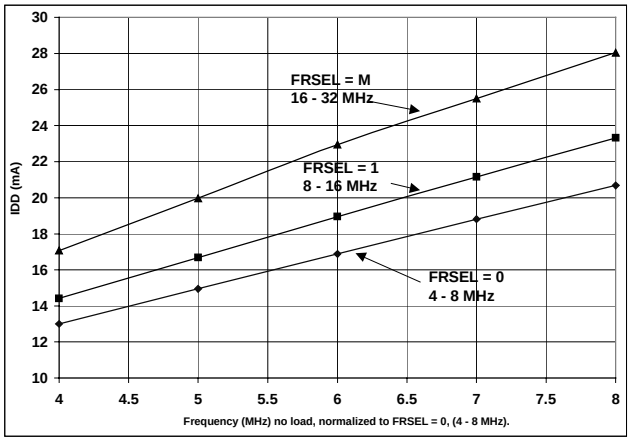


Figure 4C. IDD vs. Frequency (FRSEL = 0, 1, M)

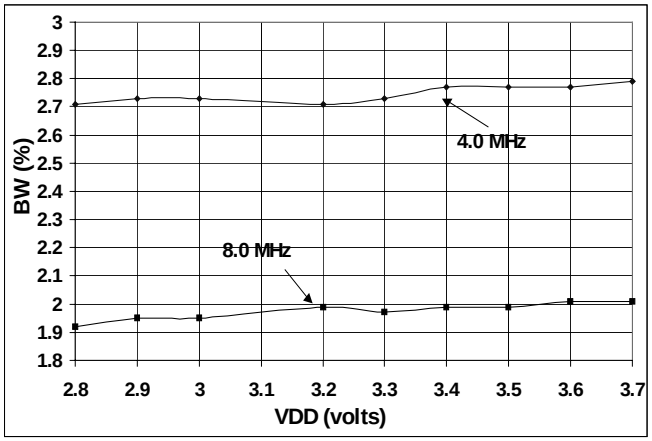
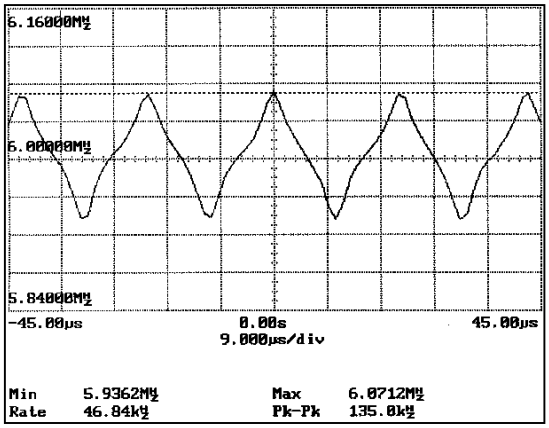


Figure 4D. Bandwidth % vs. VDD

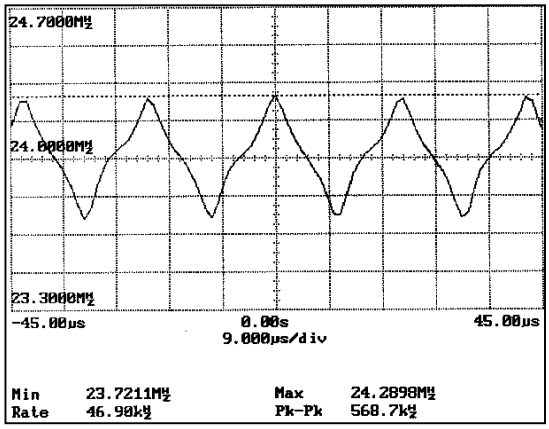
SSCG PROFILES

The CY25568 uses a non-linear frequency profile as shown in Figure 5. The use of Cypress proprietary "optimized" frequency profile maintains flat energy distribution over the fundamental and higher order harmonics. This results in additional EMI reduction in electronic systems.



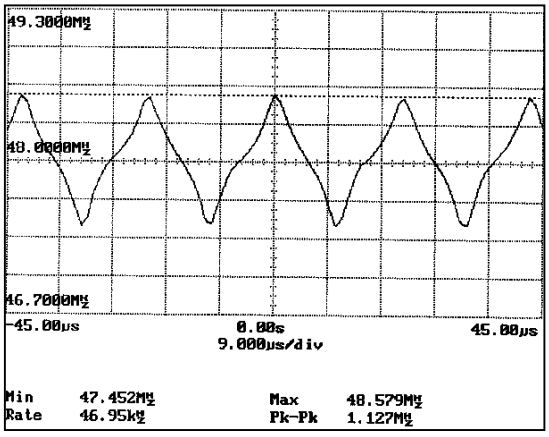
Xin = 6.0 MHz
S1, S0 = 0
FRSEL = 0

SSCLK1 = 6.0 MHz
D1, D0 = 1



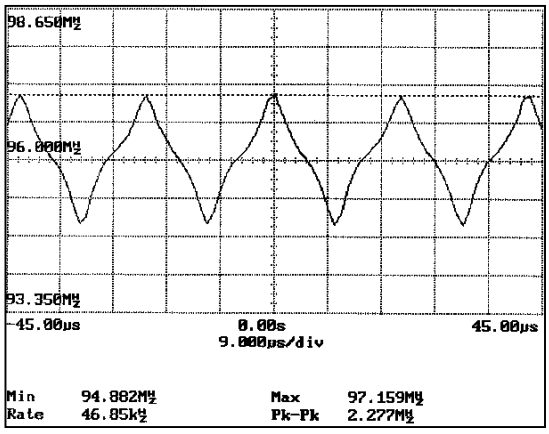
Xin = 24.0 MHz
S1, S0 = 0
FRSEL = M

SSCLK1 = 24.0 MHz
D1, D0 = 1



Xin = 12.0 MHz
S1, S0 = 0
FRSEL = 1

SSCLK1 = 48.0 MHz
D1, D0 = 1



Xin = 24.0 MHz
S1, S0 = 0
FRSEL = M

SSCLK1 = 96.0 MHz
D1, D0 = 1

Figure 5. Spread Spectrum Profiles (Frequency versus Time)

APPLICATION SCHEMATIC

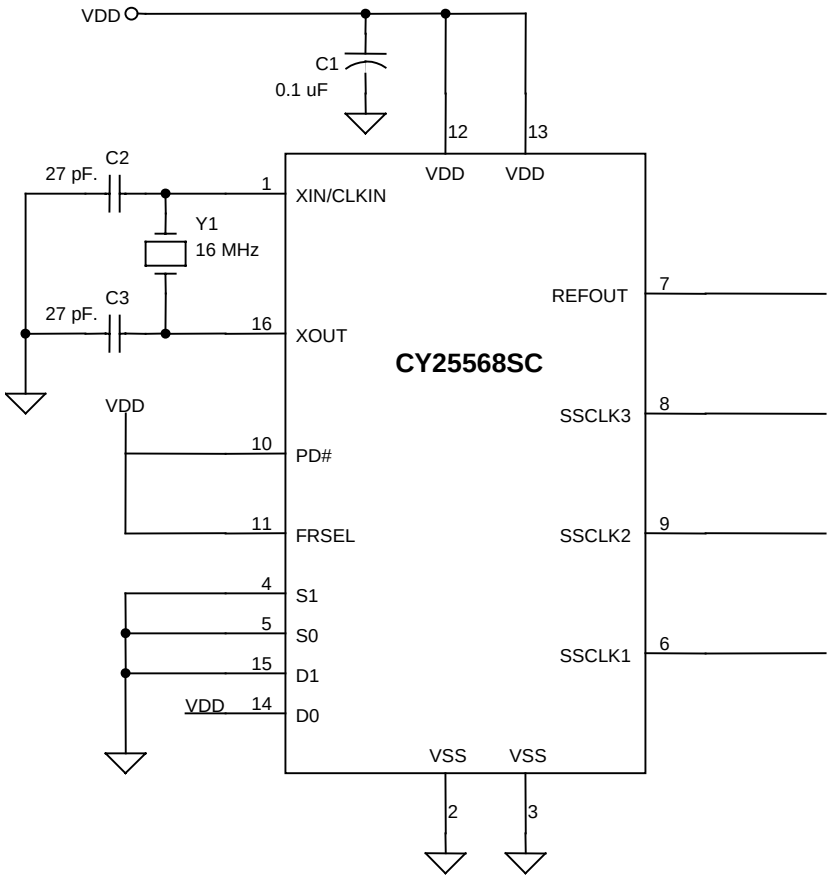


Figure 6. Application Schematic

16 PIN SOIC PACKAGE DRAWING AND OUTLINE

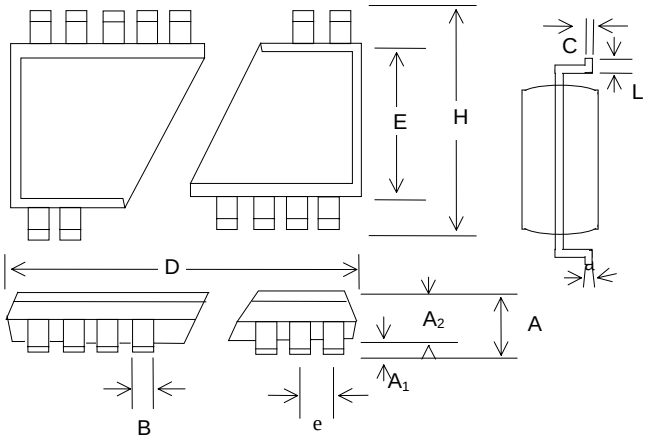


Figure 7. SOIC16 Drawing

16 Pin SOIC Outline Dimensions (150 mil)

	INCHES			MILLIMETERS		
SYMBOL	MIN	NOM	MAX	MIN	NOM	MAX
A	0.053	-	0.069	1.35	-	1.75
A_1	0.004	-	0.010	0.10	-	0.25
A2	0.047	-	0.059	1.20	-	1.50
B	0.013	-	0.020	0.33	-	0.51
C	0.007	-	0.010	0.19	-	0.25
D	0.366	-	0.394	9.80	-	10.00
E	0.150	-	0.157	3.80	-	4.00
e	0.050 BSC			1.27 BSC		
H	0.228	-	0.244	5.80	-	6.20
L	0.016	-	0.050	0.40	-	1.27
a	0º	-	8º	0º	-	8º

Table 9. SOIC16 Outline

Notice

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Document Title: CY25568 Spread Spectrum Clock Generator **Document Number:** 38-07111				
Rev.	**ECN No.**	**Issue Date**	**Orig. of Change**	**Description of Change**
**	107515	06/14/01	NDP	Convert from IMI to Cypress
*A	108182	07/03/01	NDP	Delete “Junction Temp” in Absolute maximum Ratings (page 4)
*B	122682	12/21/02	RBI	Added power up requirements to Absolute Maximum Ratings information.

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