MAX9526

Low-Power, High-Performance NTSC/PAL Video Decoder

General Description

The MAX9526 is a low-power video decoder that converts NTSC or PAL composite video signals to 8-bit or 10-bit YCbCr component video compliant with the ITU-R BT.656 standard. The device powers up in fully operational mode and automatically configures itself to decode the detected input standard. The MAX9526 typically consumes 200mW of power in normal operation and typically less than 100µW in shutdown mode.

An internal 10-bit, 54MHz analog-to-digital converter (ADC) samples the input with four times oversampling. The MAX9526 features a DC restoration circuit with offset correction and automatic gain control to accurately optimize the full-scale range of the ADC.

An integrated analog anti-aliasing filter eliminates the need for external filtering. The MAX9526 includes a 2:1 input multiplexer with automatic signal selection based on activity at the inputs.

An internal line-locked phase-locked loop (PLL) generates the sample clock and the line-locked clock (LLC) output to provide an ITU-compliant output. Alternatively, the PLL can be configured to provide a sample clock and output clock at 2x and 1x the frequency of the crystal oscillator, respectively.

The MAX9526 provides a multiline adaptive comb filter to reduce cross-chrominance and cross-luminance artifacts.

A single 1.8V supply is used for both the digital and analog supplies. The digital outputs operate from a separate +1.7V to +3.45V supply to allow direct connection to a wide range of digital processors. The MAX9526 operates over the -40°C to +125°C automotive temperature range and is available in both a 28-pin QSOP and a 32-pin TQFN (5mm x 6mm).

Applications

Automotive Entertainment Systems

Collision Avoidance Systems

Security Surveillance/CCTV Systems

Televisions

Features

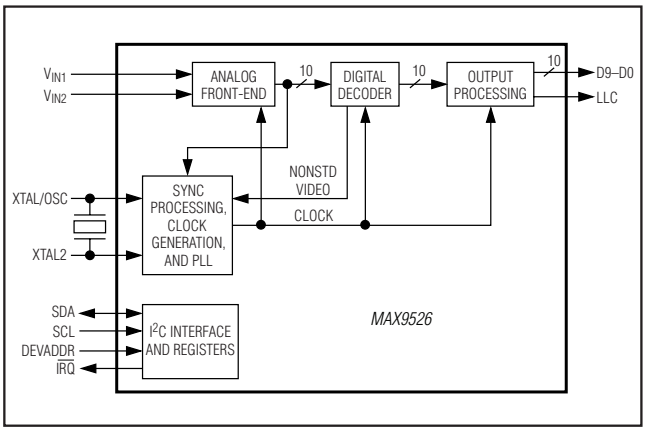
- **Supports All NTSC and PAL Standards**
  NTSC M, NTSC J, NTSC 4.43,
  PAL B/G/H/I/D, PAL M, PAL N, PAL 60
- **Easy to Configure and Operate with Only 16 User-Programmable Registers**
- **Automatic Configuration and Standard Select**
- **10-Bit 4x Oversampling (54Msps) ADC with True 10-Bit Digital Processing**
- **Flexible Output Formatting**
  10-Bit Parallel ITU-R BT.656 Output with Embedded TRS
  8-Bit Parallel ITU-R BT.656 Output with Separate HS and VS
- **+1.8V Digital and Analog Supply Voltage**
- **+1.7V to +3.45V Digital I/O Supply Voltage**
- **Full Automotive Temperature Range (-40°C to +125°C)**
- **Low-Power Modes**
  Shutdown (< 100µW typ)
  Sleep Mode with Continuous Activity Detection (< 5mW typ)
- **2-to-1 Video Input Mux with AGC**

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX9526AEI+	-40°C to +125°C	28 QSOP
MAX9526AEI/V+	-40°C to +125°C	28 QSOP
MAX9526ATJ+	-40°C to +125°C	32 TQFN-EP*
MAX9526ATJ/V+	-40°C to +125°C	32 TQFN-EP*

+Denotes lead(Pb)-free/RoHS-compliant package.
/V denotes an automotive qualified part.
**EP = Exposed pad.*

Functional Diagram



For pricing, delivery, and ordering information, please contact Maxim Direct at 1-888-629-4642, or visit Maxim's website at www.maximintegrated.com.

19-4535; Rev 3; 2/11

ABSOLUTE MAXIMUM RATINGS

AVDD to AGND .....-0.3V to +2V
DVDD to DGND .....-0.3V to +2V
DVDDIO to DGND .....-0.3V to +3.6V
AGND to DGND.....-0.1V to +0.1V
D9–D0, LLC to DGND .....-0.3V to (DVDDIO + 0.3V)
V_{IN1}, V_{IN2}, V_{REF} to AGND .....-0.3V to (AVDD + 0.3V)
XTAL/OSC, XTAL2 to AGND .....-0.3V to +2V
$\overline{IRQ}$, SDA, SCL, DEVADR to DGND .....-0.3V to +3.6V
Continuous Current In/Out All Pins .....±50mA
Continuous Power Dissipation (T_A = +70°C)
28-Pin QSOP Single-Layer Board
(derate 10.8mW/°C above +70°C).....860mW
28-Pin QSOP Multilayer Board
(derate 12.6mW°C above +70°C).....1009mW
32-Pin TQFN Multilayer Board
(derate 20.8mW/°C above +70°C).....1663mW
Operating Temperature Range .....-40°C to +125°C
Junction Temperature.....+150°C
Storage Temperature Range .....-65°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C
Soldering Temperature (reflow) .....+260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{AVDD} = V_{DVDD} = +1.8V, V_{DVDDIO} = +3.3V, V_{AGND} = V_{DGND} = 0V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SUPPLIES						
Analog Supply Voltage Range	AVDD		1.7	1.8	1.9	V
Digital Supply Voltage Range	DVDD		1.7	1.8	1.9	V
Digital I/O Supply Voltage Range	DVDDIO		1.7	3.3	3.45	V
Analog Supply Current (Note 2)	I_{AVDD}	Normal operation		42	55	mA
		Sleep mode		2.2	3	
		Shutdown		0.5	100	µA
Digital Supply Current (Note 2)	I_{DVDD}	Normal operation		70	110	mA
		Sleep mode		5	1000	µA
		Shutdown		5	1000	
Digital I/O Supply Current (Note 2)	I_{DVDDIO}	Normal operation, V_{DVDDIO} = 1.8V		3.5		mA
		Normal operation, V_{DVDDIO} = 3.3V		6.4		
		Sleep mode, V_{DVDDIO} = 3.3V		0.8	10	µA
		Shutdown, V_{DVDDIO} = 3.3V		0.8	10	
VIDEO INPUTS, V_{REF}, AND CLAMP						
Input Voltage Range		Guaranteed by full-scale conversion range	0.27	0.5	0.83	V_{P-P}
Input Resistance	R_{IN}			2		MΩ
Input Capacitance	C_{IN}			8		pF
Video Input Reference Voltage (V_{REF})	V_{REF}			850		mV
Sync-Tip Clamp Level	V_{CLMP2}	Activity detect clamp		550		mV
Input Clamping Current		Activity detect clamp, V_{VIN} = V_{CLMP2} + 150mV		2.0		µA

ELECTRICAL CHARACTERISTICS (continued)

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PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Sync Slice Comparator Level		Activity detect slicer, referenced to V_{CLMP}			50		mV
DC Restore Current DAC Full-Scale Range (Source and Sink) (Note 3)		Slow			3		µA
		Medium			6		
		Medium-fast (default)			12		
		Fast			24		
DC Restore Sync-Tip Level at V_{IN1}/V_{IN2}		AGCGAIN = 0x0, ADAGC = 1			0.51		V
		AGCGAIN = 0xF, ADAGC = 1			0.72		
ANALOG INPUT FILTER AND ADC (Note 4)							
Cutoff Frequency (3dB)	f_{3dB}				13		MHz
Passband Flatness		f < 5MHz, V_{VIN} = 0.65V_{P-P}, reference level measured at 1MHz			0.25		dB
Stopband Cutoff	f_{SB}				53		MHz
Stopband Attenuation		f > f_{SB}, V_{VIN} = 0.65V_{P-P}, reference level measured at 1MHz			36		dB
Full-Scale Conversion Range		AGC disabled, gain programmed using I²C (ADAGC = 1), referenced to V_{IN1}/V_{IN2}	AGCGAIN = 0x0	670		830	mV_{P-P}
			AGCGAIN = 0xF	270		330	
AGC Gain Stepsize					0.167		V/V
Differential Nonlinearity	DNL	AGCGAIN = 0x0, ADAGC = 1			±0.5		LSB
Integral Nonlinearity	INL	AGCGAIN = 0x0, ADAGC = 1			±1		LSB
Signal-to-Noise Ratio	SNR	Includes filter + ADC + digital anti-aliasing filter, input is -1dBFS; ADAGC = 1, AGCGAIN[3:0] = 0x0, defined as ratio of RMS signal to RMS noise in dB			58.8		dB
Power-Supply Rejection	PSR	ADAGC = 1 AGCGAIN[3:0] = 0x0 input level = 1MHz sine wave at -2dBFS	1.7V < V_{AVDD} < 1.9V, 1.7V < V_{DVDD} < 1.9V			-40	dBFS
			V_{AVDD} = 1.8V + 100mV_{P-P} at 500kHz		-67		
			V_{AVDD} = 1.8V + 100mV_{P-P} at 3.58MHz		-58		
			V_{AVDD} = 1.8V + 100mV_{P-P} at 4.43MHz		-57		
Differential Phase	DP	5-step modulated staircase, f = 3.58MHz or 4.43MHz			1.0		degrees

ELECTRICAL CHARACTERISTICS (continued)

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PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Differential Gain	DG	5-step modulated staircase, f = 3.58MHz or 4.43MHz		1		%
2T Pulse Response		2T = 200ns or 250ns		0.4		%
2T Bar Response		Bar time is 18µs, the beginning 2.5% and ending 2.5% of the bar time are ignored, 2T = 200ns or 250ns		0.2		%
2T Pulse to Bar Rating		Bar time is 18µs, the beginning 2.5% and ending 2.5% of the bar time are ignored, 2T = 200ns or 250ns		0.2		%
Group Delay Distortion		100kHz < f < 5MHz		±1		ns
DECODED LUMINANCE AND CHROMINANCE CHANNELS (Note 5)						
Chroma Bandwidth	BW_C			1		MHz
Luma Bandwidth	BW_L			5.5		MHz
Luma Nonlinearity		5-step staircase		1		%
Luma Line Time Distortion (H-Tilt)	LD	Measured at the output regarding active video		0.5		%
Luma Field Time Distortion (V-Tilt)	FD	Measured at the output regarding active video		0.1		%
DIGITAL COMPOSITE DECODER						
Lock Time				3		frames
Horizontal Line Time Static Variation			-5		+5	%
Maximum Horizontal Line Time Jitter (Async Mode)				5		µs
Maximum Horizontal Line Time Jitter (LLC mode)				160		ns
Line-Locked Clock Frequency	f_{LLC}	Varies with input line rate		27		MHz
Minimum Peak Signal to RMS Noise		Proper composite decoder operation		23		dB
PLL						
Async Mode Jitter		Ideal input clock		20		ps_{RMS}
Line-Locked PLL Loop Bandwidth Set by Register 0x0E[2:0]		000		180		Hz
		001		250		
		010		375		
		011 (default)		500		
		100		750		
		101		1000		
		110		1500		
		111		2000		

ELECTRICAL CHARACTERISTICS (continued)

(V_{AVDD} = V_{DVDD} = +1.8V, V_{DVDDIO} = +3.3V, V_{AGND} = V_{DGND} = 0V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
CRYSTAL OSCILLATOR						
Frequency		Fundamental mode only		27.000		MHz
XTAL/OSC, XTAL2 Input Capacitance	C_{XTAL}, C_{XTAL2}			4		pF
Maximum Load Capacitor	C_{L1}, C_{L2}			45		pF
Frequency Accuracy				±50		ppm
XTAL/OSC Logic-Low Threshold	V_{IL}	XTAL oscillator disabled, clock input mode (XTAL_DIS = 1)			0.3 x V_{DVDD}	V
XTAL/OSC Logic-High Threshold	V_{IH}	XTAL oscillator disabled, clock input mode (XTAL_DIS = 1)	0.7 x V_{DVDD}			V
XTAL/OSC Input Leakage Current	I_{IH}, I_{IL}	XTAL oscillator disabled, clock input mode (XTAL_DIS = 1)	-10	±0.01	+10	µA
Maximum Input Clock Jitter				500		ps_{P-P}
I^2C SERIAL INTERFACE (Note 6)						
Serial-Clock Frequency	f_{SCL}		0		400	kHz
Bus Free Time Between STOP and START Conditions	t_{BUF}		1.3			µs
Hold Time (REPEATED) START Condition	$t_{HD, STA}$		0.6			µs
SCL Pulse-Width Low	t_{LOW}		1.3			µs
SCL Pulse-Width High	t_{HIGH}		0.6			µs
Setup Time for a REPEATED START Condition	$t_{SU, STA}$		0.6			µs
Data Hold Time	$t_{HD, DAT}$		0		900	ns
Data Setup Time	$t_{SU, DAT}$		100			ns
SDA and SCL Receiving Rise Time (Note 7)	t_R		20 + 0.1C_B		300	ns
SDA and SCL Receiving Fall Time (Note 7)	t_F		20 + 0.1C_B		300	ns
SDA Transmitting Fall Time (Note 7)	t_F	V_{DVDDIO} = 3.3V	20 + 0.1C_B		250	ns
		V_{DVDDIO} = 1.8V		150		
Setup Time for STOP Condition	$t_{SU, STO}$		0.6			µs
Bus Capacitance	C_B				400	pF
Pulse Width of Suppressed Spike	t_{SP}		0		50	ns
HIGH-SPEED LOGIC OUTPUTS (D9–D0, LLC)						
Output Low Voltage	V_{OL}	I_{OL} = 5mA, V_{DVDDIO} = 3.3V			0.4	V
		I_{OL} = 2mA, V_{DVDDIO} = 1.7V			0.4	

ELECTRICAL CHARACTERISTICS (continued)

(V_{AVDD} = V_{DVDD} = +1.8V, V_{DVDDIO} = +3.3V, V_{AGND} = V_{DGND} = 0V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

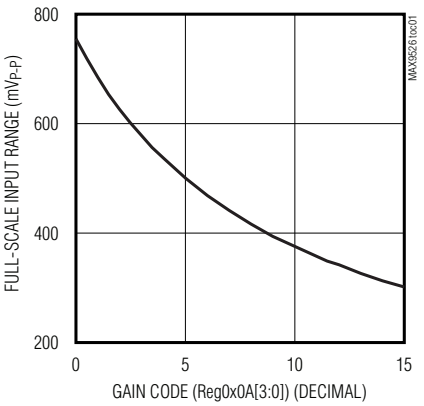
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output High Voltage	V_{OH}	I_{OH} = 5mA, V_{DVDDIO} = 3.3V	V_{DVDDIO} x 0.8V			V
		I_{OH} = 2mA, V_{DVDDIO} = 1.7V	V_{DVDDIO} - 0.4V			
Data to LLC Rising Edge Hold Time	t_{HD}		13.5	18.5	23.5	ns
Data to LLC Rising Edge Setup Time	t_{SU}		13.5	18.5	23.5	ns
Rise and Fall Time	t_R, t_F	C_L = 10pF, V_{DVDDIO} = 1.8V		3		ns
		C_L = 25pF, V_{DVDDIO} = 3.3V		3		
Output Leakage	I_{OH}, I_{OL}	Outputs in high-impedance mode	-10	±0.01	+10	µA
OPEN-DRAIN OUTPUTS (SDA and $\overline{IRQ}$)						
Output Low Voltage	V_{OL}	I_{OL} = 3mA, 1.7V < V_{DVDDIO} < 2V			0.2 x V_{DVDDIO}	V
		I_{OL} = 3mA, 2V < V_{DVDDIO} < 3.3V			0.4	
Output High Current	I_{OH}	V_{OUT} = 3.3V		±0.01	10	µA
LOGIC INPUTS (SDA, SCL, DEVADR)						
Logic-Low Threshold	V_{IL}				0.3 x V_{DVDDIO}	V
Logic-High Threshold	V_{IH}		0.7 x V_{DVDDIO}			V
Input Leakage Current	I_{IH}, I_{IL}		-10	±0.01	+10	µA
SDA/SCL Off Leakage Current	I_{IH}	V_{AVDD} = V_{DVDD} = V_{DVDDIO} = 0V	-10	±0.01	+10	µA

Note 1: All devices are 100% production tested at T_A = +25°C. Specifications over temperature limits are guaranteed by design.
Note 2: NTSC 75% color bar signal applied to video input. C_L = 10pF on D9–D0 and LLC. External XTAL.
Note 3: Internal test only. Digital core controls sync level adjustment current to adjust offset in analog signal path. Adjust level is based on value of sync level as converted by ADC. Digital core switches sourcing or sinking current into V_{IN1} or V_{IN2} nodes. Speed of correction (value of current) is controlled through I^2C.
Note 4: Filter and ADC performance measured using ADC outputs prior to composite digital demodulation (decoding).
Note 5: Decoded luminance and chrominance specifications measured using entire signal path from video input to digital component outputs.
Note 6: V_{DVDDIO} = 1.8V and 3.3V.
Note 7: C_B is in pF.

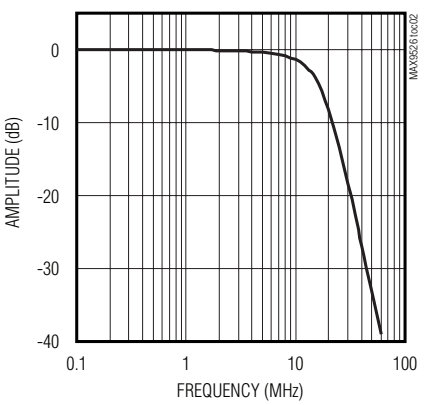
Typical Operating Characteristics

(V_{AVDD} = V_{DVDD} = +1.8V, V_{DVDDIO} = 3.3V, V_{AGND} = V_{DGND} = 0V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

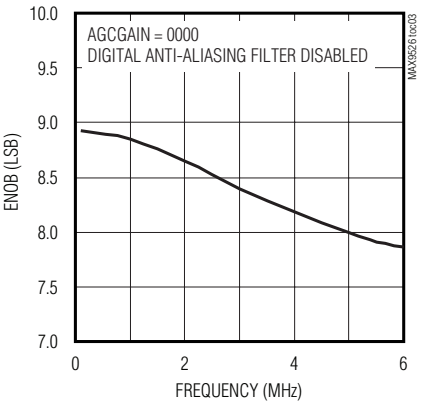
FULL-SCALE CONVERSION RANGE



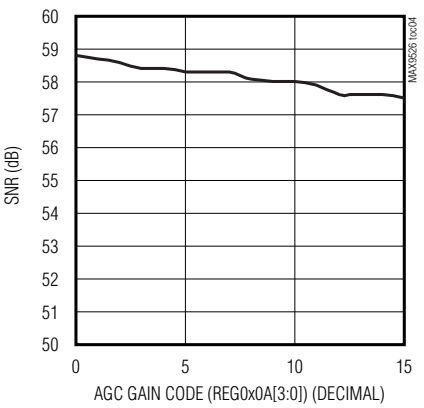
ANALOG INPUT FILTER RESPONSE



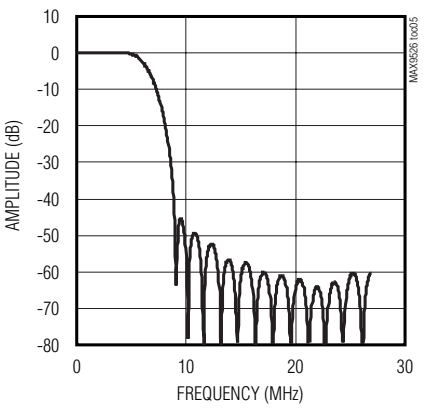
ADC EFFECTIVE NUMBER OF BITS vs. INPUT FREQUENCY



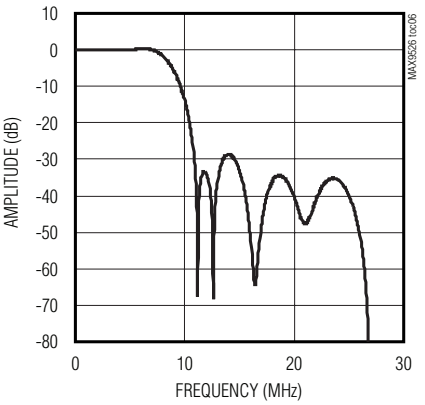
ADC SNR vs. GAIN CODE



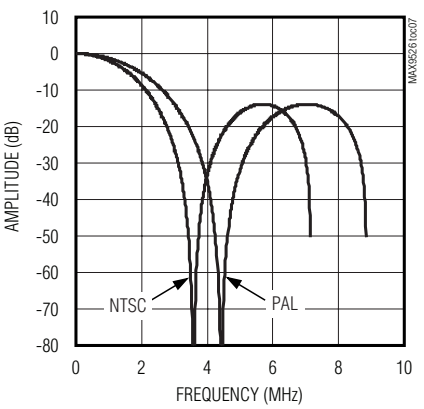
DIGITAL COMPOSITE ANTI-ALIASING FILTER



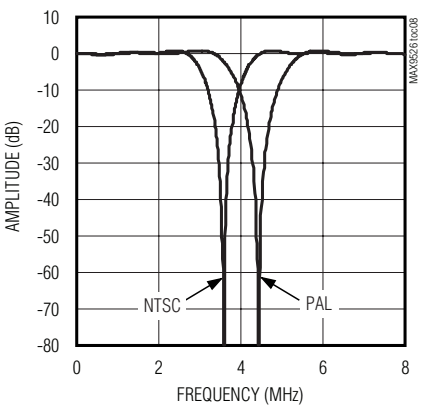
DIGITAL Y FILTER



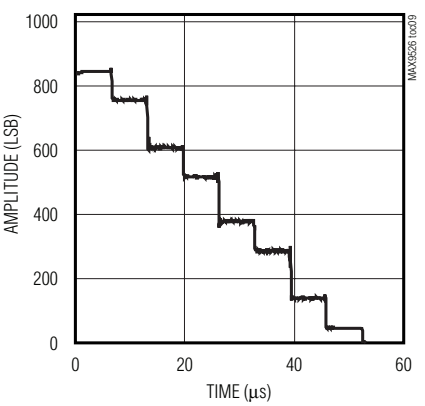
DIGITAL Cb/Cr FILTER



DIGITAL NOTCH FILTER



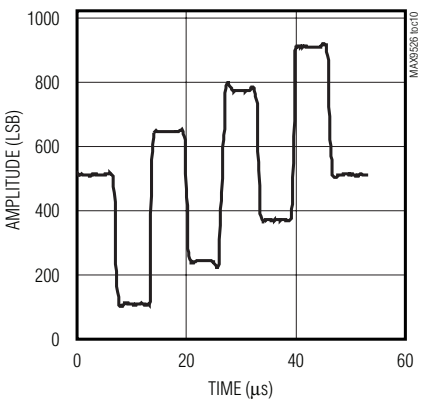
DECODED VIDEO OUTPUT 100% COLOR BARS (Y WAVEFORM)



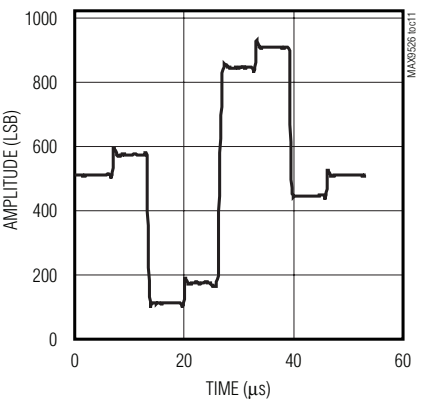
Typical Operating Characteristics (continued)

(V_{AVDD} = V_{DVDD} = +1.8V, V_{DVDDIO} = 3.3V, V_{AGND} = V_{DGND} = 0V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

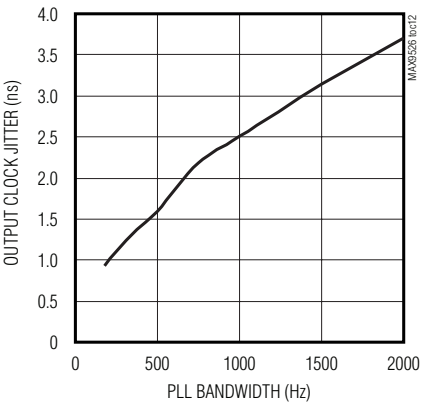
DECODED VIDEO OUTPUT 100% COLOR BARS (Cb WAVEFORM)



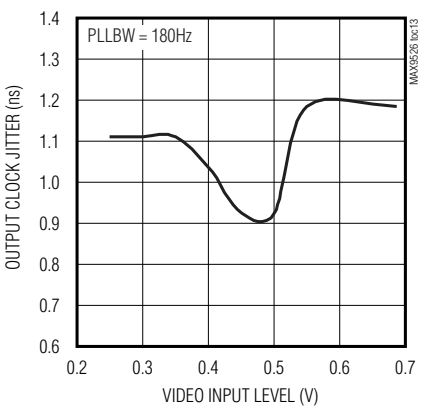
DECODED VIDEO OUTPUT 100% COLOR BARS (Cr WAVEFORM)



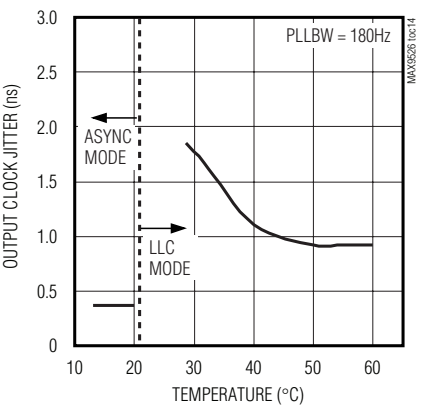
OUTPUT CLOCK JITTER vs. PLL BANDWIDTH



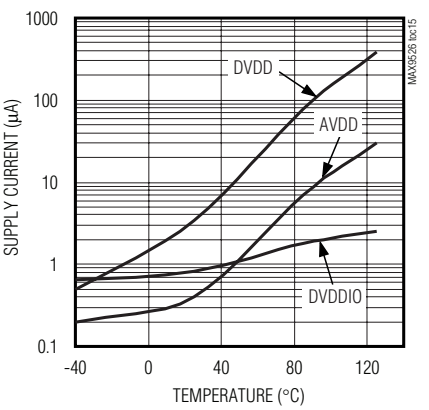
OUTPUT CLOCK JITTER vs. VIDEO INPUT LEVEL



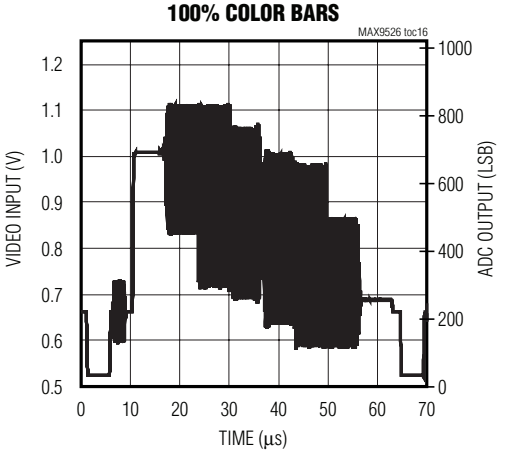
OUTPUT CLOCK JITTER vs. VIDEO INPUT SNR



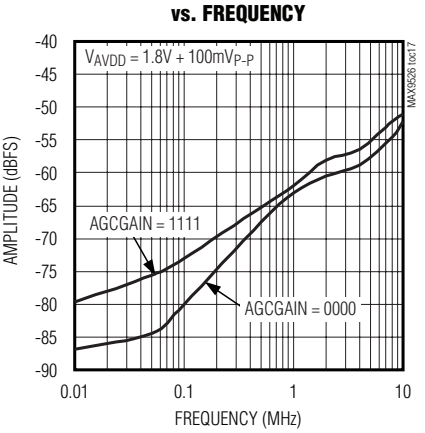
SHUTDOWN SUPPLY CURRENT vs. TEMPERATURE



VIDEO INPUT AND ADC OUTPUT 100% COLOR BARS



POWER-SUPPLY REJECTION vs. FREQUENCY



Pin Description

PIN		NAME	FUNCTION
QSOP	TQFN-EP		
1	30	V_{IN1}	Single-Ended Composite Video Input 1. AC-couple the input video signal with a 0.1µF capacitor.
2	31	V_{REF}	Video Reference Bypass. Bypass V_{REF} to AGND with a 0.1µF capacitor as close as possible to the device.
3	32	V_{IN2}	Single-Ended Composite Video Input 2. AC-couple the input video signal with a 0.1µF capacitor.
4	1	AGND	Analog Ground
5	2	AVDD	Analog Power-Supply Input. Connect to a +1.8V supply. Bypass AVDD to AGND with a 0.1µF capacitor.
6	3	XTAL2	External Crystal. Connect XTAL2 to one terminal of the crystal oscillator. Ground XTAL2 when applying an external clock to XTAL/OSC.
7	4	XTAL/OSC	External Crystal/Oscillator. Connect XTAL/OSC to one terminal of a crystal or an external clock source. Connect XTAL2 to the other terminal of the crystal oscillator.
8	5	I.C.	Internal connection. Connect to DGND.
9	6	DEVADR	I^2C Device Address Select Input. Connect to DVDD, DGND, or SDA to select 1 of 3 available I^2C slave addresses (see Table 5).
10, 22	7, 21	DVDD	Digital Power-Supply Input. Connect to a +1.8V supply. Bypass DVDD to DGND with a 0.1µF capacitor in parallel with a 10µF capacitor.
11, 23	8, 22	DGND	Digital Ground. Connect both DGND terminals together.
12	10	SDA	I^2C-Compatible Serial-Data Input/Output. Connect a 10kΩ pullup resistor from SDA to DVDDIO for full output swing.
13	11	SCL	I^2C-Compatible Serial-Clock Input. Connect a 10kΩ pullup resistor from SCL to DVDDIO for full output swing.
14	12	$\overline{IRQ}$	Hardware Interrupt Open-Drain Output. If not masked, $\overline{IRQ}$ is pulled low when the bits in the status register change state. Repeated faults have no effect on $\overline{IRQ}$ until $\overline{IRQ}$ is cleared by reading the corresponding status register. Connect a 10kΩ pullup resistor from $\overline{IRQ}$ to DVDDIO for full output swing.
15–20, 25–28	13–16, 18, 19, 24, 26, 27, 28	D0–D9	Digital Video Outputs Bit 0–Bit 9, 10-Bit Component Digital Video Outputs. The output format is 10-bit ITU-R BT.656, 4:2:2 with embedded sync. D1 and D0 can be configured as horizontal and vertical sync outputs using the Clock and Output register 0x0D. D0 is LSB.
21	20	LLC	Line-Locked 27MHz Clock Output. With line-locked mode, the LLC clock varies in response to horizontal line rate of the incoming video. In async mode, the LLC clock is synchronous to the crystal (see Table 1).
24	23	DVDDIO	Digital I/O Power-Supply Input. Accepts a +1.7V to +3.45V voltage input. Bypass to DGND with a 0.1µF capacitor.
—	9, 17, 25, 29	N.C.	No Connection. Not internally connected.
—	—	EP	Exposed Pad (TQFN Only). EP is internally connected to GND. Connect EP to GND.

Detailed Description

The MAX9526 is a simple, low-power video decoder that converts all modes of NTSC and PAL composite video signals to 10-bit YCbCr component video compatible with the ITU-R BT.656 standard. The device powers up in fully operational mode and automatically configures itself to standard NTSC or standard PAL.

An internal 10-bit, 54MHz ADC samples at four times the sampling rate specified in ITU-R BT.601. The analog front-end of the MAX9526 features a DC restoration circuit, automatic gain control, and automatic offset correction. These blocks are controlled with digital processing to accurately optimize the full-scale range of the ADC. An integrated analog anti-aliasing filter eliminates the need for off-chip filtering. The device includes a 2:1 input multiplexer that can be configured to automatically select the input based on activity.

The system clock is generated with an external 27MHz crystal and an internal oscillator. Optionally, a 27MHz or 54MHz external clock can be connected to the XTAL/OSC input. An internal line-locked digital PLL is used to generate the 54MHz ADC sample clock that is synchronous to the incoming video signal with up to ±5% variation in horizontal line length. The digital output data and LLC clock are line locked to the video input and provide a standard ITU output. The PLL can also be configured to asynchronously sample the input using the crystal oscillator or external clock.

The MAX9526 provides a 5-line adaptive comb filter to separate the luminance (Y) and chrominance (C) video components and reduce cross-chrominance and cross-luminance artifacts. The MAX9526 operates with any type of standard composite video signal source including DVD players, video cameras, navigation systems, and VCRs.

The device powers up in fully operational video decoder mode. An I²C register interface monitors status and enables programming of many decoder functions including brightness, contrast, saturation, and hue. The 10-bit output can be reconfigured to provide 8-bit data with separate horizontal and vertical syncs.

Analog Front-End (AFE)

The MAX9526 AFE implements DC restoration, automatic gain control (AGC), analog anti-aliasing filter (LPF), activity detection, channel selection, and analog-to-digital conversion. A block diagram of the AFE is shown in Figure 1.

Activity Detect and Automatic Channel Selection

The MAX9526 continuously monitors activity at both video inputs, V_{IN1} and V_{IN2}. Activity on the selected channel is detected using the ADC output. On the unselected channel an analog sync-tip clamp and sync slicer are used to detect sync amplitudes greater than 50mV. In sleep mode, the analog sync-tip clamps and sync slicers are used to detect activity on both inputs, while the rest of the AFE is in a shutdown state.

The output of the activity detect circuit is reported through the Status register 0x00. The user must manually select which video input to process by setting INSEL in register 0x09 appropriately.

The MAX9526 can optionally be configured to automatically select the video input that indicates the presence of activity by setting AUTOSEL = 1 in register 0x09. When activity is present on both V_{IN1} and V_{IN2} at power-up or when there is no activity on either input channel, V_{IN1} is selected. When there is activity on V_{IN2} and there is no activity on V_{IN1}, then V_{IN2} is selected. When V_{IN2} is automatically selected with the presence of activity, the input only switches to V_{IN1} when activity goes away on V_{IN2}.

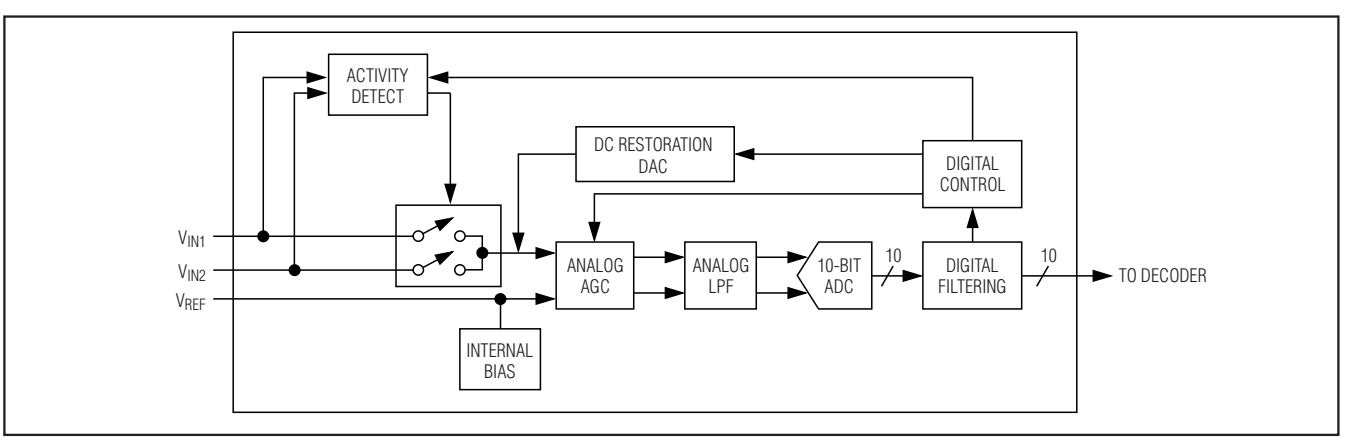


Figure 1. Analog Front-End

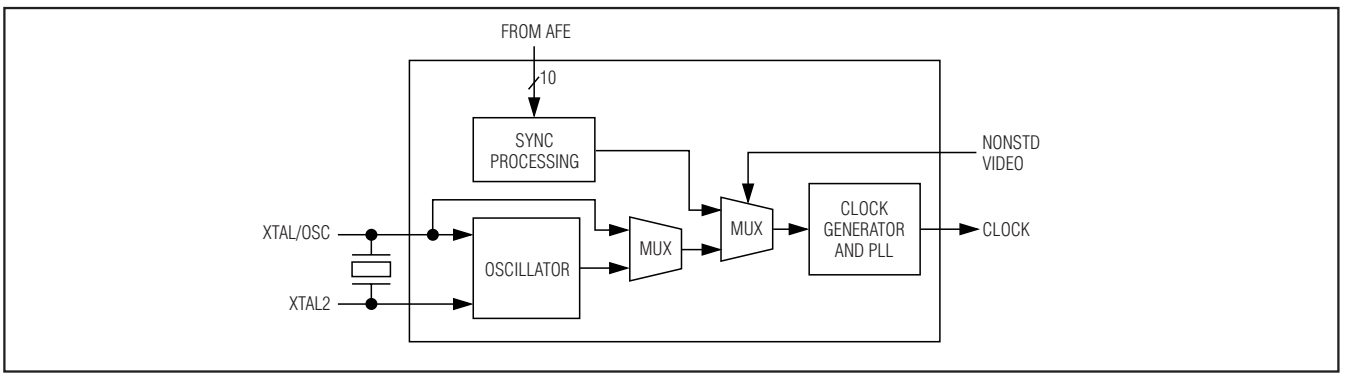


Figure 2. Sync Processing, Clock Generation, and PLL

V_{REF} Generation

A differential signal path is used to process the analog video signal to minimize the effect of noise coupling. A DC reference (V_{REF}) of 850mV is internally generated and decoupled externally with a 0.1µF capacitor. Identical signal paths and video buffers are used for both the selected video input and the video reference voltage. The signals are converted to a fully differential signal by the analog AGC circuit.

DC Restoration DAC

The video inputs, V_{IN1} and V_{IN2}, are AC-coupled to the MAX9526 with 0.1µF capacitors. The DC restoration circuit sets the sync level at the output of the ADC by sinking or sourcing current at the selected video input. A digital control at the ADC output is used to monitor the average sync level. An error signal is generated in the digital control block that is used by a current DAC to source or sink current to the AC-coupled input to restore the DC level. The DC restoration circuit also corrects the offset in the analog signal chain and sets the sync level at the ADC output to code 32 (decimal).

Analog Automatic Gain Control (Analog AGC)

The MAX9526 includes an analog variable-gain amplifier with a digitally controlled gain for automatic gain control (AGC). The AGC uses the sync amplitude at the output of the ADC to control the gain. For signals without copy protection, the AGC adjusts the gain until the sync amplitude is 208 (decimal) codes at the ADC output. For inputs with copy protection, the AGC automatically compensates for the reduced sync amplitude on active lines.

The analog AGC loop can be disabled and the gain is set manually to 1 of 16 values using the Gain Control register 0x0A. The range of analog gain is 3.5dB to 12dB.

Analog Lowpass Filter (LPF)

The MAX9526 includes a high-performance anti-aliasing analog lowpass filter with a 3dB bandwidth of 13MHz (typ) and better than 0.25dB (typ) passband flatness to 5MHz. This eliminates the need for external filtering on the video inputs. The filter typically provides 36dB attenuation at 53MHz (1MHz below ADC sample rate).

54Msps Video ADC

A 10-bit, 54Msps ADC converts the filtered analog composite video signal for digital signal processing (composite video demodulation).

Digital Filtering

Digital filtering at the ADC output removes any out-of-band interference and improves the signal-to-noise ratio before decoding. The signal path includes a digital anti-aliasing lowpass filter that has 1dB of passband flatness to 5.5MHz and a minimum of 45dB of stopband attenuation for frequencies greater than 9MHz.

Sync Processing, Clock Generation, and PLL

The sync processing, clock generation, and PLL extract the timing information from incoming video and generate the clock for the rest of the chip. Figure 2 shows the block diagram for this block.

Crystal Oscillator/Clock Input

The MAX9526 includes a low-jitter crystal oscillator circuit optimized for use with an external 27MHz crystal. The device also accepts an external CMOS logic-level clock at either 27MHz or 54MHz. To use an external clock (27MHz or 54MHz) instead of a crystal, set XTAL_DIS = 1 in register 0x0D. To use a 54MHz external clock instead of a 27MHz clock, SEL_54MHz must also be set to 1 in register 0x0D.

Sync Processing

The sync processing block extracts the sync information and automatically detects 525 line or 625 line inputs.

Clock Generator and PLL

The PLL operates in either line-locked clock (LLC) mode or async mode. Selection of the mode is controlled automatically by the MAX9526 or can optionally be overwritten with the LLC_MODE bits in PLL Control register 0x0E.

In LLC mode, a hybrid analog/digital PLL generates a low-jitter line-locked clock. The 54MHz sample clock is synchronous to the input video. The LLC clock output is also synchronous to the input video. The ITU output has the correct number of samples per line and lines per field. The PLL is designed to lock to signals with up to 160ns peak jitter. When the jitter exceeds the 160ns peak, the PLL coasts until the jitter improves. If the jitter continuously exceeds the 160ns peak, the PLL relocks and the HLOCK status bit in register 0x00 is set to 0.

In LLC mode, the bandwidth of the PLL can be optionally programmed to one of eight values between 180Hz and 2000Hz using the PLLBW bits in PLL Control register 0x0E. The default value for the PLL bandwidth is 500Hz.

In async mode, the sample clock frequency is generated by multiplying the crystal frequency by a factor of two and the video signal is sampled asynchronously with the 2x crystal clock. To eliminate artifacts, the MAX9526 uses an adaptive poly-phase filter to correct timing and phase errors introduced by the asynchronous sampling. The LLC output is generated by dividing the 54MHz sampling clock by two.

The ITU output in async mode has the correct number of lines per frame and the correct number of pixels per line except on the first line of each field. The timing correction block uses this line to compensate for timing errors between the incoming video signal and the crystal. As a result, the first line of each field is longer or shorter for several pixels depending on the magnitude of the frequency difference between the incoming video signal and the local crystal. For example, a 100ppm frequency difference between the incoming video signal and the crystal results in approximately 23 extra or fewer pixels on the first line of each field. Line length errors on line one are of no consequence for most applications since it is in the vertical blanking interval and does not contain active video or any other type of data.

The types of inputs that cause the PLL to automatically switch to async mode are video inputs with a nonstandard carrier frequency. For standard video, the carrier frequency is always a precise multiple of the horizontal frequency. A typical nonstandard input is video cassette recorders in which the carrier is not a precise multiple of the horizontal frequency. The nonstandard detect (NONSTD) status from the decoder is used to automatically switch the PLL to async mode when nonstandard carrier frequencies are detected. The NONSTD status is monitored in the Status register 0x00.

Clocking Modes

In addition to automatic configuration, the MAX9526 can also be manually configured to provide maximum flexibility in setting the clock inputs and outputs of the chip. Table 1 summarizes the clocking modes that are supported.

Digital Composite Decoding

Figure 3 shows a block diagram of the digital composite decoder. This block converts the digitized composite video signal to digital component video.

Sync Level Correction and Sync Extraction

The sync extraction function extracts the raw sync signals from the video and the extracted sync information is sent to the sync processor. The sync level from the AFE is code 32 (decimal) on a 10-bit scale and the blanking level is approximately 208 (decimal) codes above the sync level. The sync slicer default threshold is set to approximately the middle of the sync pulse at decimal code 128. The sync slice level can optionally be manually adjusted using the slice bits in register 0x0F.

The sync level correction block features an optional digital clamp that can be enabled in register 0x09. Enabling the digital clamp sets the sync level to code 0 (decimal) and gives higher frequency tracking of the input signals. When the digital clamp is enabled, the sync slice level in register 0x0F should be adjusted accordingly to provide equivalent noise rejection.

Sync Processor and Analog Copy Protection Detection

The sync processor extracts the horizontal sync and vertical sync signals. Field pulses and burst gate pulses are generated based on VSYNC and HSYNC, respectively. The sync processing block provides sync timing to measure the sync level and amplitude for the black level control and composite AGC. The sync processor also detects incoming video signal standards (525 line NTSC and 625 line PAL). Video standard information is available in Status register 0x01. The detected video standard is used to automatically configure the decoder. The MAX9526 detects NTSC-M (standard NTSC) and PAL B/G/H/I/D (standard PAL)

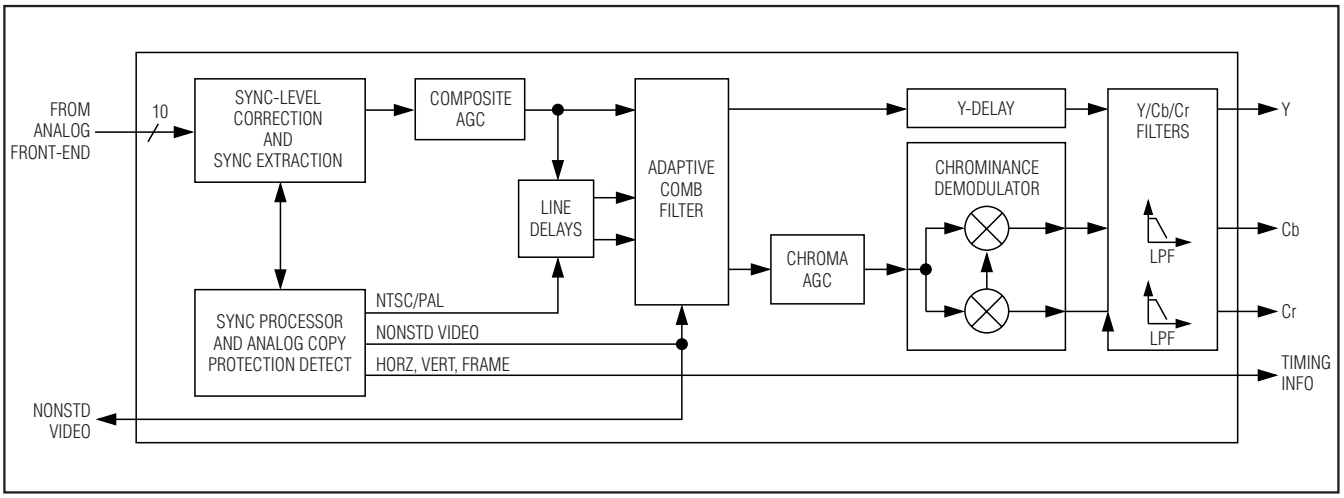


Figure 3. Digital Composite Decoding Functional Diagram

standards automatically. See the *Standard Select, Shutdown, and Control Register* section for manual programming.

The sync processor block also detects analog copy protection. Extracted copy protection information is available in Status register 0x01.

Composite Automatic Gain Control (AGC)

In addition to the analog AGC that optimizes the ADC full-scale range, a digital AGC is used to more accurately set the video amplitude. The Composite AGC uses the amplitude of the sync signal to set the gain.

Adaptive Comb Filter

The MAX9526 uses a 5-line adaptive comb filter to separate luminance and chrominance components from a single composite channel. The adaptation algorithm does not require configuration. The adaptive comb filter adjusts based on the relationship and content of video data between neighboring lines. The filter automatically adapts the comb filter structure between a 5-line filter and a notch filter.

Chrominance Signal Demodulator

After luminance (Y) and chrominance (C) components are separated, the Y component passes through a delay line to compensate for the C component delay through the demodulator. The chrominance signal path contains an AGC before the signal demodulator. The chrominance AGC uses the color burst amplitude to set the gain. The chrominance is demodulated using a subcarrier signal locked to the burst. The demodulated chrominance signals, Cb and Cr, are lowpass filtered to eliminate unwanted products of demodulation.

Output Formatting

Figure 4 shows the output formatting section of the MAX9526.

Image Enhancement and Color Correction

The MAX9526 provides contrast, brightness, hue, and saturation manual control in registers 0x05 to 0x08.

Time Base Correction

The MAX9526 provides time base correction (TBC) to allow the decoder to properly process unstable and nonstandard video from sources such as a VCR. The time base correction minimizes the effect of sampling jitter to ensure that there are a correct number of pixels per active line.

Test Pattern Insertion

The MAX9526 automatically outputs a black screen when there is no video at the inputs. The test pattern can also be configured to provide a blue screen, 75% color bars, or 100% color bars through register 0x0C.

Timing Reference Signal Insertion and ITU-R BT.656 Encoding

The MAX9526 multiplexes the Y, Cr, and Cb signals with an embedded timing reference signal conforming to the ITU-R BT.656 standard.

SAV and EAV sequences are inserted into the data stream to indicate the active video time in ITU-R BT.656 format. The output timing insertion is illustrated in Figure 5. The SAV and EAV sequences are shown in Table 2.

Output Timing

The output setup and hold diagram is shown in Figure 6.

Table 1. MAX9526 Clock Mode Summary

SEL _54MHz REGISTER 0x0D B4	XTAL_DIS REGISTER 0x0D B3	PLLBYP REGISTER 0x0E B3	LLC_MODE REGISTER 0x0E B5-4	CLOCK MODE DESCRIPTION
0	0	0	00	Input clock = 27MHz crystal. Sample clock = line locked or async (autodetected). This is the default power-up mode for the MAX9526.
0	0	0	10	Input clock = 27MHz crystal. Sample clock = line locked (forced on).
0	0	0	11	Input clock = 27MHz crystal. Sample clock = 2x input clock.
0	X	1	XX	Invalid modes. The PLL can only be bypassed if the input clock is 54MHz.
0	1	0	00	Input clock = 27MHz external clock. Sample clock = line locked or async (autodetected).
0	1	0	10	Input clock = 27MHz external clock. Sample clock = line locked (forced on).
0	1	0	11	Input clock = 27MHz external clock. Sample clock = 2x input clock.
1	0	X	XX	Invalid mode. 54MHz crystal not supported.
1	1	0	00	Input clock = 54MHz external clock. Sample clock = line locked or async (autodetected).
1	1	0	10	Input clock = 54MHz external clock. Sample clock = line locked (forced on).
1	1	0	11	Input clock = 54MHz external clock. Sample clock = input clock divided by 2, then multiplied by 2x through the PLL. This mode uses the PLL to filter high-frequency jitter on the input source.
1	1	1	X0	Invalid mode. The PLL can only be bypassed when the output is not a line-locked clock.
1	1	1	11	Input clock = 54MHz external clock. Sample clock = input clock. Use this mode when a low-jitter, 54MHz input clock is used.

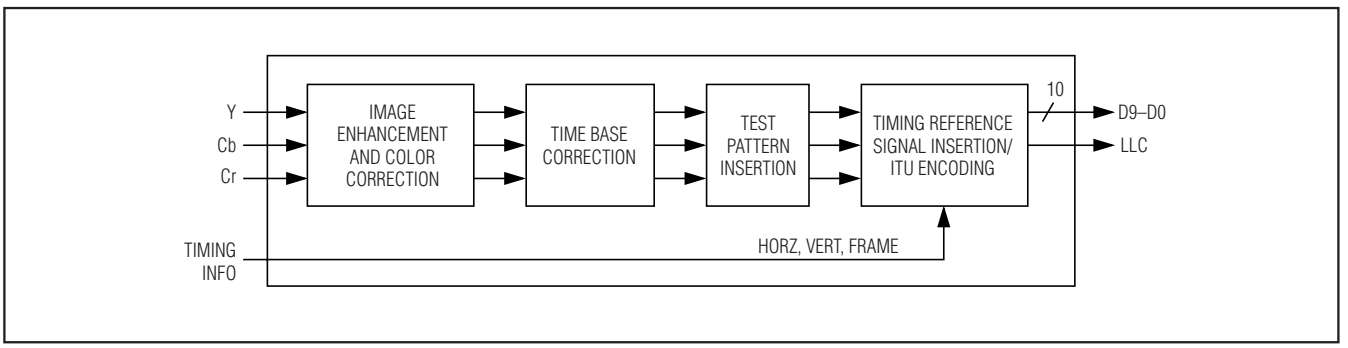


Figure 4. Digital Output Processing

Table 2. ITU-R BT.656 SAV and EAV Code Sequence

CONDITION			FVH			VALUE SAV/EAV CODE SEQUENCE			
FIELD	**V TIME**	**H TIME**	**F**	**V**	**H**	**FIRST**	**SECOND**	**THIRD**	**TRS**
Even	Blank	EAV	1	1	1	0xFF	0x00	0x00	0xF1
Even	Blank	SAV	1	1	0	0xFF	0x00	0x00	0xEC
Even	Active	EAV	1	0	1	0xFF	0x00	0x00	0xDA
Even	Active	SAV	1	0	0	0xFF	0x00	0x00	0xC7
Odd	Blank	EAV	0	1	1	0xFF	0x00	0x00	0xB6
Odd	Blank	SAV	0	1	0	0xFF	0x00	0x00	0xAB
Odd	Active	EAV	0	0	1	0xFF	0x00	0x00	0x9D
Odd	Active	SAV	0	0	0	0xFF	0x00	0x00	0x80

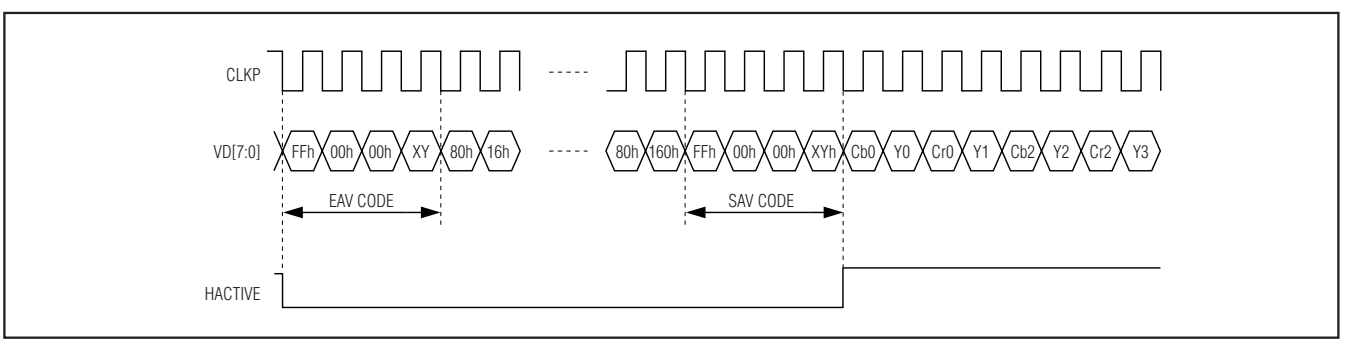


Figure 5. Timing Diagram of ITU-R BT.656 Format

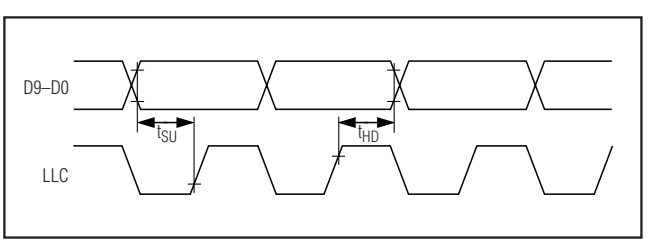


Figure 6. Output Setup and Hold

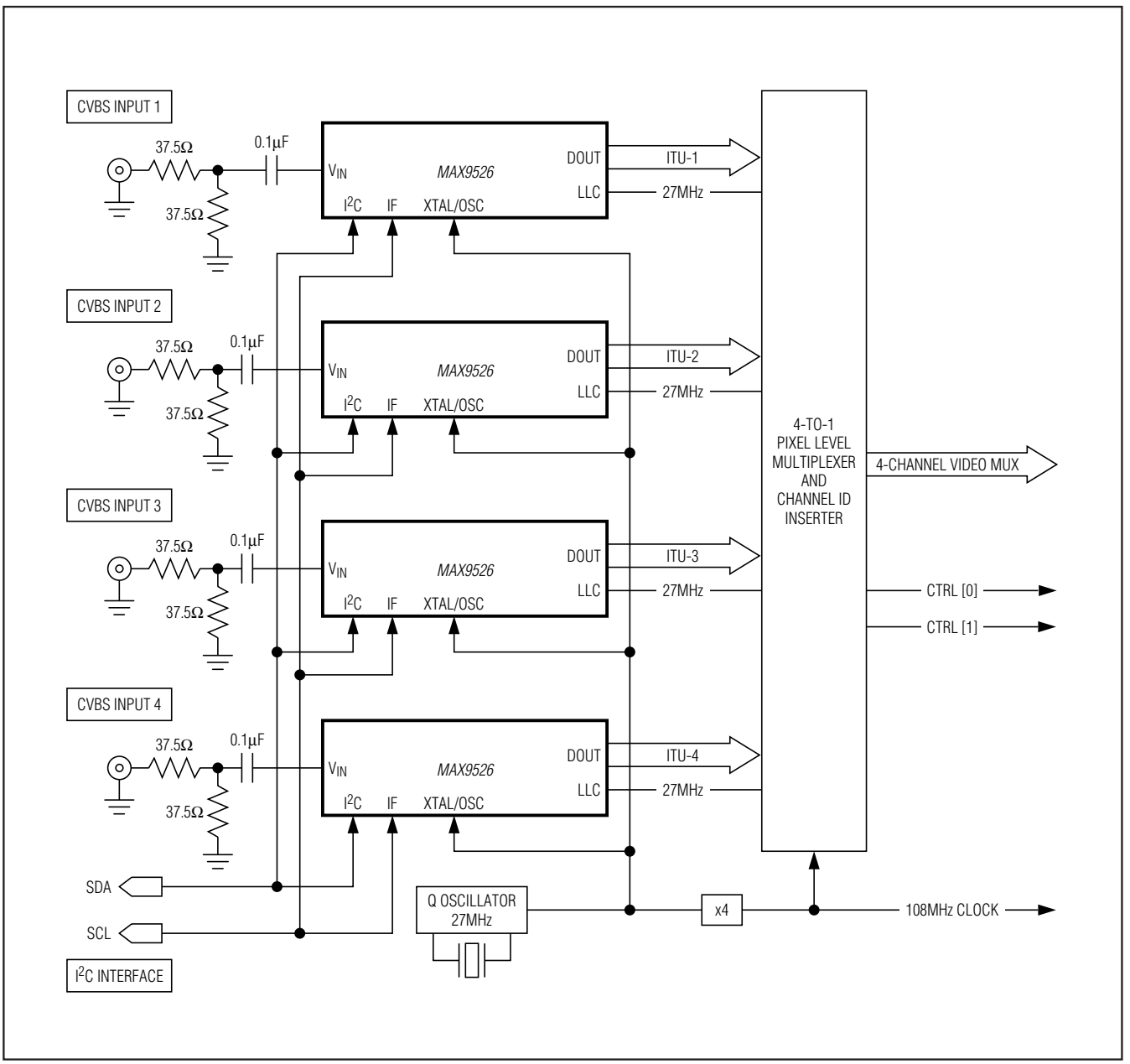


Figure 7. Multiple Video Input Processing

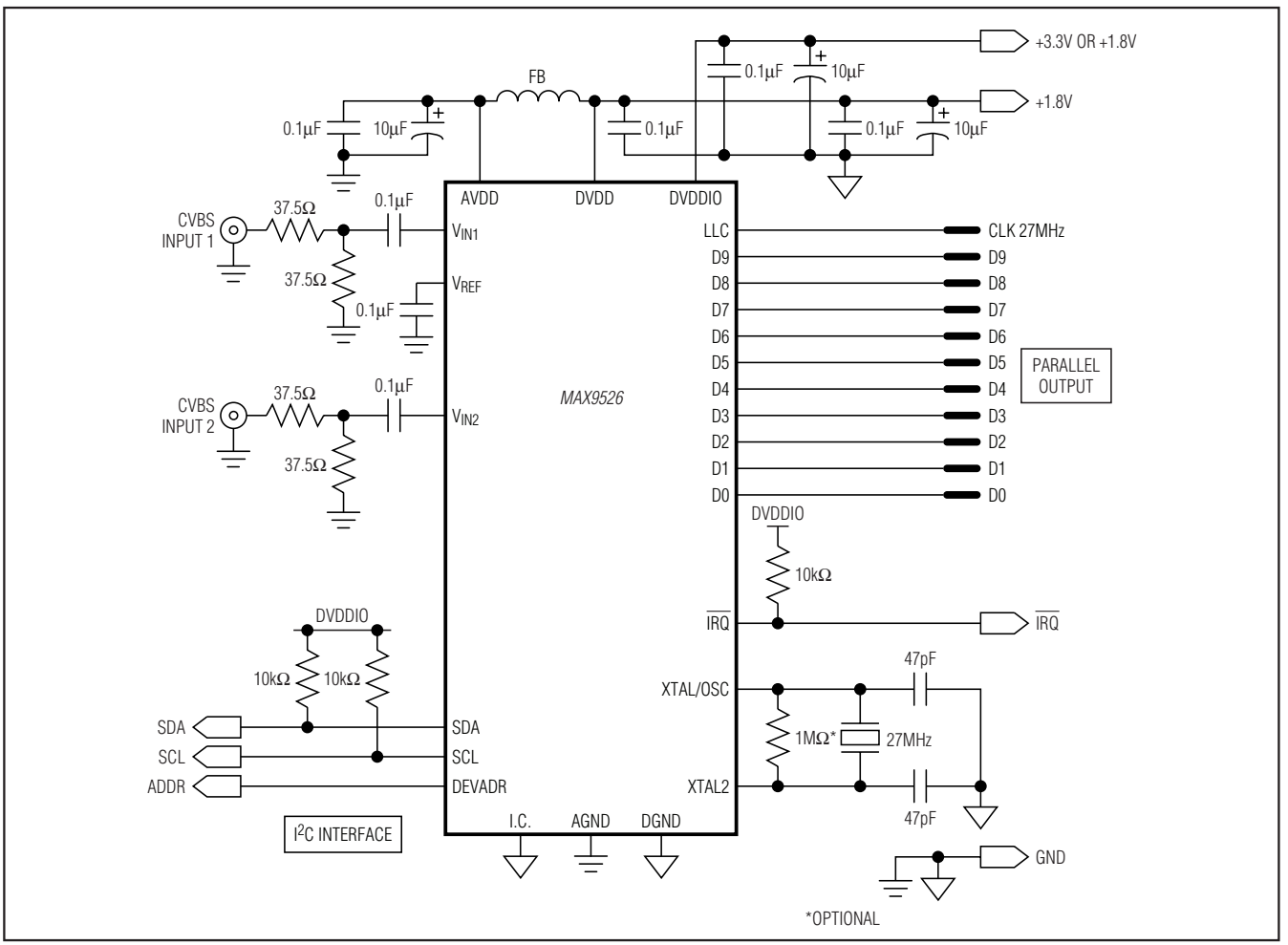


Figure 8. MAX9526 Typical Application Circuit with Additional Supply Isolation

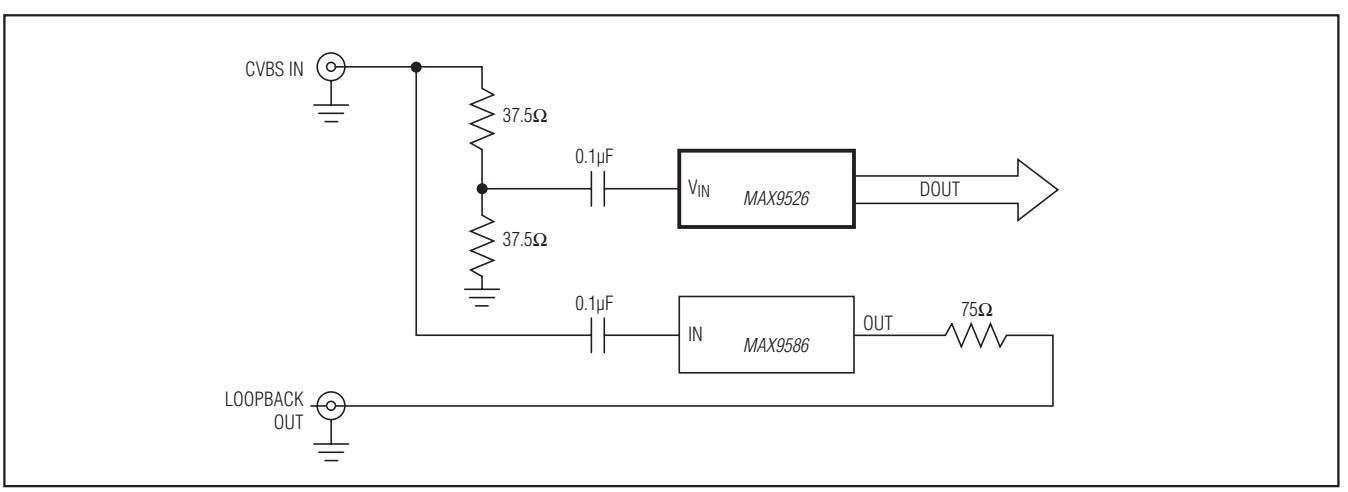


Figure 9. Loopback Operation Application Diagram

Table 3. Recommended Crystal Parameters

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Frequency	Fundamental mode only		27.000		MHz
Maximum Crystal ESR	Room temperature		30		Ω
Accuracy	Line-locked mode		±50		ppm
	Async mode with multiple decoders		±50		

Applications Information

Multiple Decoder Operation

Multiple asynchronous video input signals can be decoded synchronously using multiple MAX9526s in asynchronous (async) sampling mode. Figure 7 shows an example of decoding four video input signals.

The MAX9526 is configured for async sampling mode by writing the following registers:

Register 0x0D, B3 (XTAL_DIS) = 1 (disables the crystal oscillator)

Register 0x0E, B5-4 (LLC_MODE) = 11 (forces sampling to async mode)

When the MAX9526 is in async sampling mode, the data outputs, D9–D0, of all decoders are synchronous with the input clock (XTAL/OSC). The video content in the data outputs is not frame aligned because the video sources into each MAX9526 is asynchronous. A small FPGA can be implemented to multiplex all four channels into a single 8- or 10-bit bus. This FPGA can also format the outputs to be compatible for input into a compression processor, which is commonly used in digital video recorders (DVRs).

The crystal oscillator (external or internal) must have better than ±50ppm accuracy for acceptable decoding in this mode. An accuracy of ±10ppm is recommended for optimal performance.

Recommended Crystal Parameters

Recommended crystal parameters are shown in Table 3.

Power-Supply Decoupling

For systems where additional power-supply isolation is required, the circuit shown in Figure 8 can be used. Additional supply decoupling is added and analog power (AVDD) isolation is increased with the use of a ferrite bead (FB). The analog ground connection (AGND) should be connected to a separate ground plane that has a small bridge to the main ground plane of the system. The video input termination (V_{IN1}/V_{IN2}), video reference (V_{REF}) decoupling, and AVDD supply decoupling should also be connected to the AGND ground plane.

SMBus is a trademark of Intel Corp.

I²C Serial Interface

The MAX9526 features an I²C/SMBus™-compatible, 2-wire serial interface consisting of a serial-data line (SDA) and a serial-clock line (SCL). SDA and SCL facilitate communication between the MAX9526 and the master at clock rates up to 400kHz. Figure 10 shows the 2-wire interface timing diagram. The master generates SCL and initiates data transfer on the bus. The master device writes data to the MAX9526 by transmitting the proper slave address followed by the register address and then the data word. Each transmit sequence is framed by a START (S) or REPEATED START (Sr) condition and a STOP (P) condition. Each word transmitted to the MAX9526 is 8 bits long and is followed by an acknowledge clock pulse. A master reading data from the MAX9526 transmits the proper slave address followed by a series of nine SCL pulses. The MAX9526 transmits data on SDA in sync with the master-generated SCL pulses. The master acknowledges receipt of each byte of data. Each read sequence is framed by a START or REPEATED START condition, a not acknowledge, and a STOP condition. SDA operates as both an input and an open-drain output. A pullup resistor, typically greater than 500Ω, is required on SDA. SCL operates only as an input. A pullup resistor, typically greater than 500Ω, is required on SCL if there are multiple masters on the bus, or if the single master has an open-drain SCL output. Series resistors in line with SDA and SCL are optional. Series resistors protect the digital inputs of the MAX9526 from high-voltage spikes on the bus lines, as well as minimize crosstalk and undershoot of the bus signals.

Bit Transfer

One data bit is transferred during each SCL cycle. The data on SDA must remain stable during the high period of the SCL pulse. Changes in SDA while SCL is high are control signals (see the *START and STOP Conditions* section).

START and STOP Conditions

SDA and SCL idle high when the bus is not in use. A master initiates communication by issuing a START condition. A START condition is a high-to-low transition on SDA with SCL high. A STOP condition is a low-to-high

transition on SDA while SCL is high (Figure 11). A START condition from the master signals the beginning of a transmission to the MAX9526. The master terminates transmission, and frees the bus, by issuing a STOP condition. The bus remains active if a REPEATED START condition is generated instead of a STOP condition.

Early STOP Conditions

The MAX9526 recognizes a STOP condition at any point during data transmission except if the STOP condition occurs in the same high pulse as a START condition. For proper operation, do not send a STOP condition during the same SCL high pulse as the START condition.

Slave Address

The slave address is defined as the seven most significant bits (MSBs) followed by the read/write bit. For DEVADR connected to DGND, setting the read/write bit to 1 (slave address = 0x43) configures the MAX9526 for read mode. Setting the read/write bit to 0 (slave address = 0x42) configures the MAX9526 for write mode. The address is the first byte of information sent to the MAX9526 after the START condition. The MAX9526 slave address is configurable with DEVADR. Table 5 shows the addresses of the MAX9526.

Acknowledge

The acknowledge bit (ACK) is a clocked 9th bit that the MAX9526 uses to handshake receipt each byte of data when in write mode (see Figure 12). The MAX9526 pulls down SDA during the entire master-generated 9th clock pulse if the previous byte is successfully received. Monitoring ACK allows for detection of unsuccessful data transfers. An unsuccessful data transfer occurs if a receiving device is busy or if a system fault has occurred. In the event of an unsuccessful data transfer, the bus master retries communication. The master pulls down SDA during the 9th clock cycle to acknowledge receipt of data when the MAX9526 is in read mode. An acknowledge is sent by the master after each read byte to allow data transfer to continue. A not acknowledge is sent when the master reads the final byte of data from the MAX9526, followed by a STOP condition.

Write Data Format

A write to the MAX9526 includes transmission of a START condition, the slave address with the R/$\overline{W}$ bit set to 0, one byte of data to configure the internal register address pointer, one or more bytes of data, and a STOP condition. Figure 13 illustrates the proper frame format for writing one byte of data to the MAX9526. Figure 14 illustrates the frame format for writing n bytes of data to the MAX9526.

The slave address with the R/$\overline{W}$ bit set to 0 indicates that the master intends to write data to the MAX9526. The MAX9526 acknowledges receipt of the address byte during the master-generated 9th SCL pulse.

The second byte transmitted from the master configures the MAX9526's internal register address pointer. The pointer tells the MAX9526 where to write the next byte of data. An acknowledge pulse is sent by the MAX9526 upon receipt of the address pointer data.

The third byte sent to the MAX9526 contains the data that is written to the chosen register. An acknowledge pulse from the MAX9526 signals receipt of the data byte. The address pointer autoincrements to the next register address after each received data byte. This autoincrement feature allows a master to write to sequential registers within one continuous frame. Figure 14 illustrates how to write to multiple registers with one frame. The master signals the end of transmission by issuing a STOP condition.

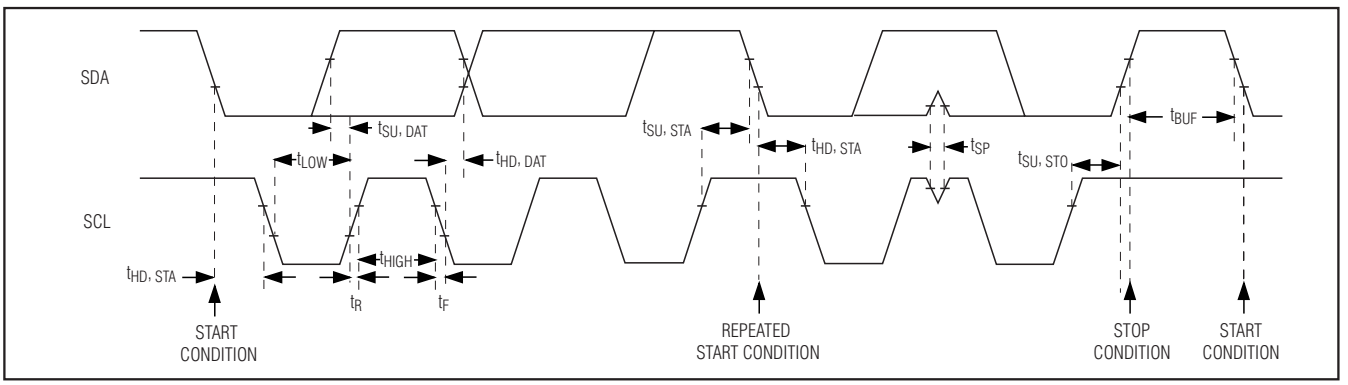


Figure 10. I²C Serial Interface Timing Diagram

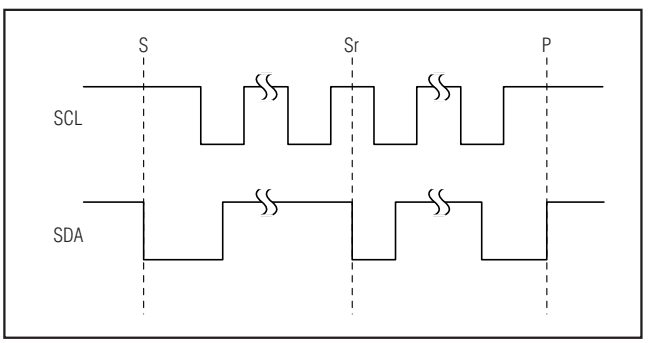


Figure 11. START, STOP, and REPEATED START Conditions

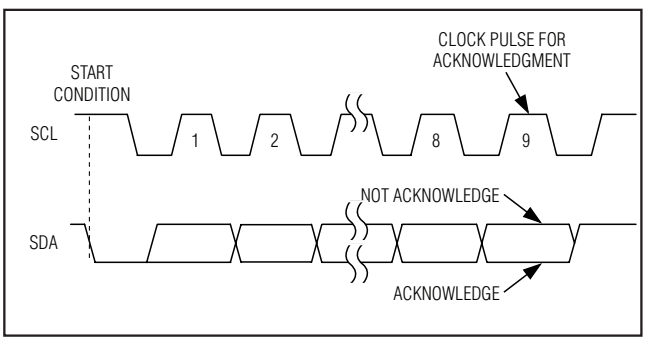


Figure 12. Acknowledge

Read Data Format

Send the slave address with the R/$\overline{W}$ bit set to 1 to initiate a read operation. The MAX9526 acknowledges receipt of its slave address by pulling SDA low during the 9th SCL clock pulse. A START command followed by a read command resets the address pointer to register 0x00.

The first byte transmitted from the MAX9526 is the contents of register 0x00. Transmitted data is valid on the rising edge of SCL. The address pointer autoincrements after each read data byte. This autoincrement feature allows all registers to be read sequentially within one continuous frame. A STOP condition can be issued after any number of read data bytes. If a STOP condition is issued followed by another read operation, the first data byte to be read is from register 0x00.

The address pointer can be preset to a specific register before a read command is issued. The master presets the address pointer by first sending the MAX9526's slave address with the R/$\overline{W}$ bit set to 0 followed by the register address. A REPEATED START condition is then sent followed by the slave address with the R/$\overline{W}$ bit set to 1. The MAX9526 then transmits the contents of the specified register. The address pointer autoincrements after transmitting the first byte.

The master acknowledges receipt of each read byte during the acknowledge clock pulse. The master must acknowledge all correctly received bytes except the last byte. The final byte must be followed by a not acknowledge from the master and then a STOP condition. Figure 15 illustrates the frame format for reading one byte from the MAX9526. Figure 16 illustrates the frame format for reading multiple bytes from the MAX9526.

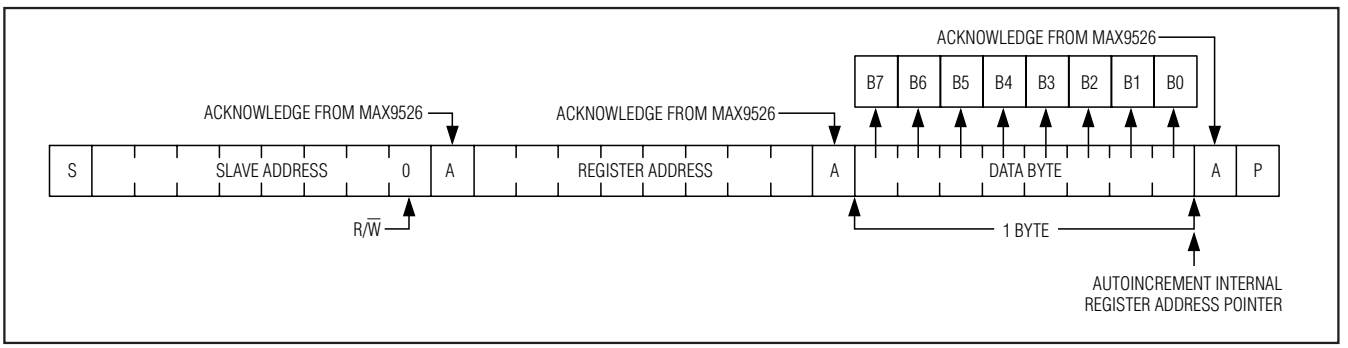


Figure 13. Writing a Byte of Data to the MAX9526

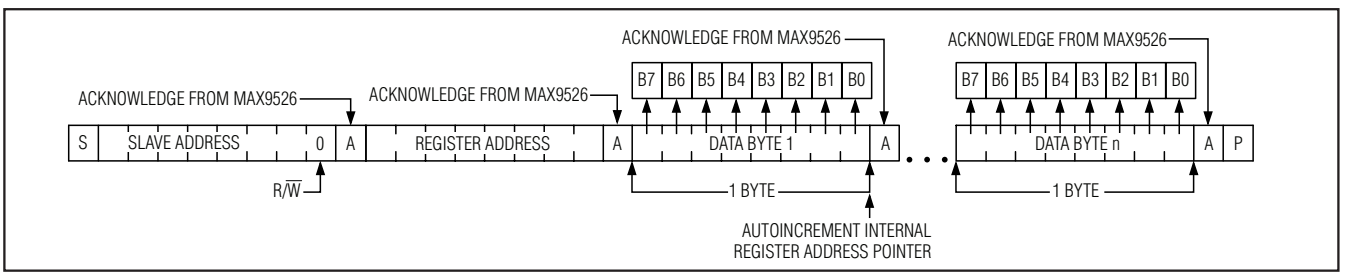


Figure 14. Writing n Bytes of Data to the MAX9526

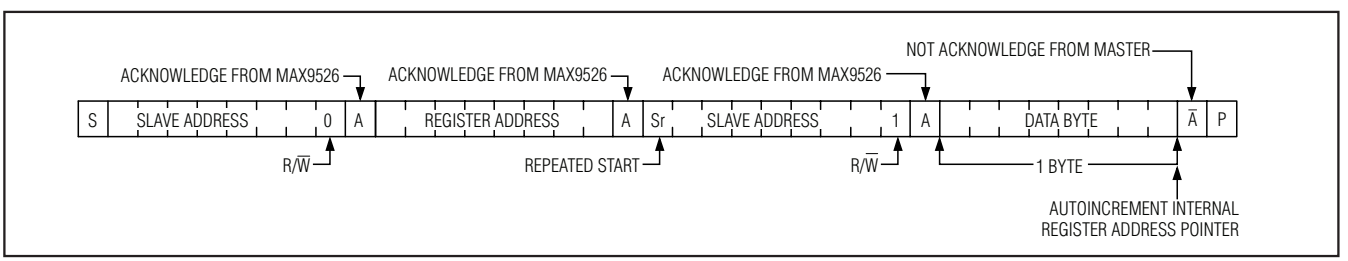


Figure 15. Reading One Indexed Byte of Data from the MAX9526

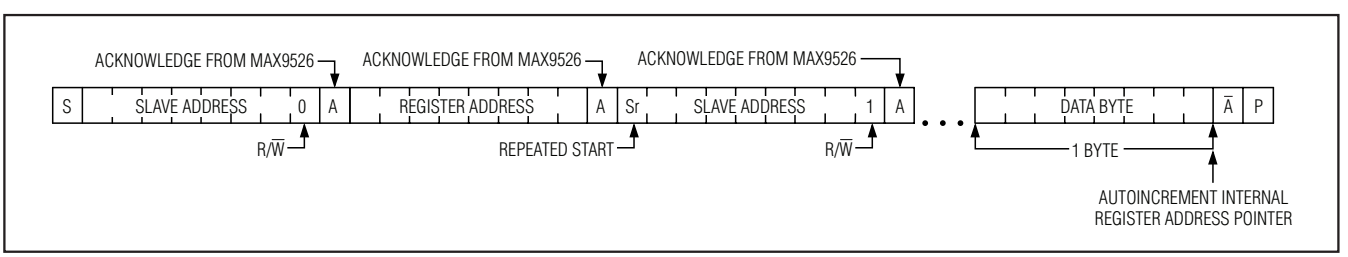


Figure 16. Reading n Bytes of Indexed Data from the MAX9526

Programming the MAX9526

I²C Register Map

Table 4 shows an I²C register map. All static bits should not be programmed to any values other than the default value listed in Table 4.

Table 4. Register Map Overview

REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	REG ADDR	POWER-ON STATE
Status 0	VID1	VID2	0	CTHR	ADCOVR	HLOCK	NONSTD	LSTLCK	0x00	n/a
Status 1	0	L525	0	0	0	0	0	ACP	0x01	n/a
IRQ MASK 0	IVID1	IVID2	0	ICTHR	IADCOVR	IHLOCK	INONSTD	ILSTLCK	0x02	0x00
IRQ MASK 1	0	IL525	0	0	0	0	0	IACP	0x03	0x00
Standard Select, Shutdown, and Control	STDSEL			AUTOD	SHDN	RESET	SLEEP	RESET_S	0x04	0x10
Contrast	CONT								0x05	0x80
Brightness	BRIGHT								0x06	0x00
Hue	HUE								0x07	0x80
Saturation	SATU								0x08	0x88
Video Input Select and Clamp	AUTOSEL	INSEL	DCRESTORE_RANGE		0	0	D_CLMP_DIS	0	0x09	0x02
Gain Control	CRAGC	CMPAGC	0	ADAGC	ADCGAIN				0x0A	0x00
Color Kill	BW	CRKDIS	1	0	CTHRSH				0x0B	0x23
Output Test Signal	RAWADC	0	TGEnab	TGTIM	TGSRC	0	CBAR		0x0C	0x00
Clock and Output	0	CLIP	LLC_INV	SEL_54 MHZ	XTAL_DIS	HSVS	DATAZ	LLCZ	0x0D	0x00
PLL Control	0	0	LLC_MODE		PLLBYP	PLLBW			0x0E	0x03
Miscellaneous	0	0	DISAAFLT	1	SSLICE				0x0F	0x18

Table 5. I²C Slave Address

ADDRESS CONNECTION (DEVADR)	WRITE ADDRESS	READ ADDRESS
DVDD	0x40	0x41
DGND	0x42	0x43
SDA	0x44	0x45

I²C Bit Descriptions

Status Register 0

REG	B7	B6	B5	B4	B3	B2	B1	B0
0x00	VID1	VID2	0	CTHR	ADCOVR	HLOCK	NONSTD	LSTLCK

Video Input 1 Active (VID1)

1 = Active video detected at V_{IN1}.

0 = No active video detected on V_{IN1}.

Video Input 2 Active (VID2)

1 = Active video detected at V_{IN2}.

0 = No active video detected on V_{IN2}.

Below Color Kill Threshold (CTHR)

1 = Color carrier has fallen below color kill threshold since last register 0 read.

0 = Color carrier has not fallen below color kill threshold since last register 0 read.

CTHR reports when the chroma carrier is below color kill threshold. See register 0x0B for color kill threshold and color kill enable settings.

ADC Out-of-Range (ADCOVR)

1 = ADC has gone outside the full-scale range since last register 0 read.

0 = ADC has not gone outside the full-scale range since last register 0 read.

ADCOVR triggers when the ADC input is above or below the ADC input range. This bit is cleared after reading status register 0. ADCOVR is not triggered on lines during the vertical blanking interval, on lines at the start or end of the field that may have pulses from copy protection, or on lines that may have ancillary data.

Horizontal Lock (HLOCK)

1 = Line-locked PLL is locked to horizontal line rate and has not lost lock since last status register 0 read.

0 = Line-locked PLL has lost lock since last status register 0 read.

Nonstandard Video (NONSTD)

1 = Nonstandard video detected.

0 = Standard video format detected.

For standard video, the carrier frequency is always a precise multiple of the horizontal frequency. An example of nonstandard inputs are video cassette recorders in which the carrier is not a precise multiple of the horizontal frequency.

Demodulator Lost Lock (LSTLCK)

1 = Demodulator has lost lock since last status register 0 read.

0 = Demodulator has maintained lock since last status register 0 read.

Status Register 1

REG	B7	B6	B5	B4	B3	B2	B1	B0
0x01	0	L525	0	0	0	0	0	ACP

525 Line Mode (L525)

1 = 525 line video detected.

0 = 625 line video detected.

This output is only valid when the decoder is locked and operating normally.

Analog Copy Protection (ACP)

1 = Analog copy protection detected.

0 = No analog copy protection detected.

Interrupt Mask Register 0

REG	B7	B6	B5	B4	B3	B2	B1	B0
0x02	IVID1	IVID2	0	ICTHR	IADCOVR	IHLOCK	INONSTD	ILSTLCK

Active Video 1 Interrupt (IVID1)

1 = Change in VID1 bit status triggers a hardware interrupt.

0 = No interrupt on VID1 changes (default).

See register 0x00, B7.

Active Video 2 Interrupt (IVID2)

1 = Change in VID2 bit status triggers a hardware interrupt.

0 = No interrupt on VID2 changes (default).

See register 0x00, B6.

Color Kill Threshold Interrupt (ICTHR)

1 = Transition in CTHR bit from 0 to 1 triggers a hardware interrupt.

0 = No interrupt on CTHR changes (default).

See register 0x00, B4.

ADC Out-of-Range Interrupt Enable (IADCOVR)

1 = Change in ADCOVR bit from 0 to 1 triggers a hardware interrupt.

0 = No interrupt on ADCOVR changes (default).

See register 0x00, B3.

Horizontal Lock Interrupt Enable (IHLOCK)

1 = Change in HLOCK bit from 1 to 0 triggers a hardware interrupt.

0 = No interrupt on HLOCK changes (default).

See register 0x00, B2.

Nonstandard Video Interrupt Enable (INONSTD)

1 = Change in NONSTD bit from 0 to 1 triggers a hardware interrupt.

0 = No interrupt on NONSTD changes (default).

See register 0x00, B1.

Demodulator Lock Interrupt Enable (ILSTLCK)

1 = Change in LSTLCK bit from 0 to 1 triggers a hardware interrupt.

0 = No interrupt on LSTLCK changes (default).

See register 0x00, B0.

Interrupt Mask Register 1

REG	B7	B6	B5	B4	B3	B2	B1	B0
0x03	0	IL525	0	0	0	0	0	IACP

525 Line Video Interrupt Enable (IL525)

1 = Change in L525 bit status triggers a hardware interrupt.

0 = No interrupt on L525 changes (default).

This interrupt is masked by the HLOCK and LSTLCK status. Changes in the L525 status triggers a hardware interrupt only when HLOCK = 1 and LSTLCK = 0. See register 0x01, B6.

Analog Copy Protection Interrupt Enable (IACP)

1 = Any change in ACP status bit (register 0x01, B0) triggers a hardware interrupt.

0 = No interrupt on analog copy protection changes (default).

See register 0x01, B0.

Standard Select, Shutdown, and Control Register

REG	B7	B6	B5	B4	B3	B2	B1	B0
0x04	STDSEL			AUTOD	SHDN	RESET	SLEEP	RESET_S

Video Standard Select (STDSEL) Bit B7 (TYPE)

1 = NTSC J, PAL 60, NTSC 4.43.

0 = NTSC M (standard NTSC), PAL M, PAL B/G/H/I/D (standard PAL), PAL Combination N (default).

Bit B6 (525 Line)

1 = 525 line video.

0 = 625 line video (or NTSC 4.43) (default).

Bit B6 sets the video line rate when AUTOD = 0. When AUTOD = 1 (default), B6 is ignored.

Bit B5 (Unconventional Video)

1 = PAL Combination N, PAL M, NTSC 4.43, PAL 60.

0 = PAL B/G/H/I/D (standard PAL), NTSC M (standard NSTC), or NTSC J (default).

The 3 bits in the STDSEL register can be used to program the expected input video format. Bit B6 (525 vs. 625 line video) can be automatically set by using the autodetect function (see AUTOD bit description, register 0x04, B4).

B[7:5]

000: PAL B/G/H/I/D (standard PAL)

001: PAL Combination N

010: NTSC M (standard NTSC)

011: PAL M

100: N/A

101: NTSC 4.43

110: NTSC J

111: PAL60

Standard Autodetect (AUTOD)

1 = Automatically detects 525 vs. 625 line video (default).

0 = Manually programs 525 vs. 625 line video.

Autodetect function can only be used to distinguish between standard PAL and standard NTSC. The autodetect function requires register 0x04, B7 = B5 = 0.

Low-Power Shutdown (SHDN)

1 = Low-power shutdown mode.

0 = Normal operation (default).

In shutdown, all logic outputs are low (unless programmed to high impedance using register 0x0D, B1). I^2C register contents are retained during shutdown.

System Reset (RESET)

1 = All registers and system state returned to power-on default conditions.

0 = Normal operation (default).

Because all registers' contents are set to power-on default state, this bit clears itself after being written.

Sleep Mode (SLEEP)

1 = Low-power sleep mode.

0 = Normal operation (default).

In sleep mode, all logic outputs are low (unless programmed to high impedance using register 0x0D, B1). I^2C register contents are retained. Video activity detect is still active. Activity status is available in register 0x00.

Soft Reset (RESET_S)

This bit resets everything on the device except the register values. This bit is self-clearing.

1 = Soft reset.

0 = Normal operation (default).

Contrast Control Register

REG	B7	B6	B5	B4	B3	B2	B1	B0
0x05	CONT							

Contrast (CONT)

0x00 = Luma gain is 0.

0x80 = Luma gain is 1 (default).

0xFF = Luma gain is 255/128, or approximately 2.

When ACP is detected (register 0x01, B0), 15 (decimal) is subtracted from CONT.

Brightness Control Register

REG	B7	B6	B5	B4	B3	B2	B1	B0
0x06	BRIGHT							

Brightness (BRIGHT)

0x00 = Luma offset is 0 IRE (default).

0x7F = Luma offset is +75.66 IRE.

0x80 = Luma offset is -76.22 IRE.

Hue Control Register

REG	B7	B6	B5	B4	B3	B2	B1	B0
0x07	HUE							

Hue (HUE)

0x80 = Chroma phase is 0 degrees with respect to color burst (default).

0xFF = Chroma phase is approximately +45 degrees with respect to color burst.

0x00 = Chroma phase is -45 degrees with respect to color burst.

Saturation Control Register

REG	B7	B6	B5	B4	B3	B2	B1	B0
0x08	SATU							

Saturation (SATU)

0x00 = Chroma gain is 0.

0x80 = Chroma gain is 1.

0x88 = Default.

0xFF = Chroma gain is 255/128, or approximately 2.

When ACP is detected (register 0x01, B0), 8 (decimal) is added to SATU.

Video Input Select and Clamp Control Register

REG	B7	B6	B5	B4	B3	B2	B1	B0
0x09	AUTOSEL	INSEL	DCRESTORE_RANGE		0	0	D_CLMP_DIS	0

Video Auto-Select (AUTOSEL)

1 = Automatically selects video input with activity detect.

When activity is present on both or neither V_{IN1} and V_{IN2} after a reset (POR, register reset, sleep mode, shutdown), V_{IN1} is selected. If there is activity on V_{IN2} and no activity on V_{IN1}, then V_{IN2} is selected. When V_{IN2} is automatically selected with the presence of activity, the input switches to V_{IN1} only when activity goes away on V_{IN2}.

0 = Video input is selected manually (default).

See INSEL (register 0x09, B6) for manual input selection.

Manual Video Input Select (INSEL)

1 = Select V_{IN2}.

0 = Select V_{IN1} (default).

Video autoselect bit (AUTOSEL) must be 0 for this register to take effect.

Analog DC Restoration Current Range (DCRESTORE_RANGE)

This bit sets the full-scale range of the DC restoration DAC. Increasing the full-scale current range increases the bandwidth and range of the DC restoration loop.

10 = Slow (±3µA into video input coupling capacitor)

11 = Medium (±6µA into video input coupling capacitor)

00 = Medium-fast (±12µA into video input coupling capacitor) (default)

01 = Fast (±24µA into video input coupling capacitor)

Digital Clamp Disable (D_CLMP_DIS)

This bit disables the digital clamp.

1 = Disables digital sync-tip clamp (default).

0 = Enables digital sync-tip clamp.

Enabling the digital clamp sets the sync level to code 0 (decimal) and gives higher frequency tracking of input signals. If the digital clamp is enabled, the sync slice level in register 0x0F should be adjusted accordingly to provide equivalent noise rejection. Typically, SSLICE[3:0] should be reduced by 2 LSBs when D_CLMP_DIS is set to 1.

Gain-Control Register

REG	B7	B6	B5	B4	B3	B2	B1	B0
0x0A	CRAGC	CMPAGC	0	ADAGC	AGCGAIN			

Chrominance AGC Disable (CRAGC)

1 = Chroma gain is frozen.

0 = Automatic chroma gain is based on color burst level (default).

To freeze the chroma gain at the default value of 17 (hex), set CRAGC = 1 and apply a soft reset.

Composite AGC Disable (CMPAGC)

1 = Digital composite gain frozen at default value (80 (hex)).

0 = Automatic digital composite gain based on sync level (default).

Disable Analog Automatic Gain Control (ADAGC)

1 = Analog automatic gain control is disabled.

0 = Analog automatic gain control is enabled (default).

The analog automatic gain-control (AGC) loop adjusts the AGC gain to optimally use the available ADC full-scale range.

Analog AGC Gain (AGCGAIN)

This bit controls the gain of the analog AGC preceding the ADC. This bit only functions when ADAGC = 1. The gain steps are linear in magnitude. Table 6 shows the AGC's effect on the input full-scale conversion range.

Table 6. Analog AGC Code and Gain Values

AGC GAIN CODE	TYPICAL FULL-SCALE CONVERSION RANGE (mV)	AGC GAIN CODE	TYPICAL FULL-SCALE CONVERSION RANGE (mV)
0000 (default)	752	1000	417
0001	683	1001	394
0010	626	1010	375
0011	578	1011	357
0100	535	1100	341
0101	500	1101	326
0110	469	1110	313
0111	441	1111	300

Color Kill Register

REG	B7	B6	B5	B4	B3	B2	B1	B0
0x0B	BW	CRKDIS	1	0	CTHRSH			

Black and White (BW)

1 = Chrominance demodulator is disabled and component video output is black and white only.

0 = Chrominance demodulator is enabled (default).

Color Kill Disable (CRKDIS)

1 = Color kill is disabled.

0 = Automatic color kill is enabled (default).

Black and white (BW) control bit takes precedence over CRKDIS.

Color Kill Threshold (CTHRSH)

The color kill threshold is relative to the peak-to-peak amplitude of the color burst of the composite video signal at the video inputs (V_{IN1}/V_{IN2}). The threshold values assume the sync amplitude is the standard level.

CTHRSH	BURST AMPLITUDE (mV)	CTHRSH	BURST AMPLITUDE (mV)
0000	Off	1000	35
0001	Off	1001	39
0010	19	1010	40
0011 (default)	25	1011	41
0100	27	1100	43
0101	29	1101	45
0110	30	1110	48
0111	31	1111	51

Color Test Signal Register

REG	B7	B6	B5	B4	B3	B2	B1	B0
0x0C	RAWADC	0	TGEnab	TGTIM	TGSRC	0	CBAR	

ADC-Only Mode (RAWADC)

1 = D9–D0 are the ADC outputs directly without being processed by video demodulator.

0 = D9–D0 are 10-bit YCbCr component video (default).

With RAWADC = 1, the D9–D0 output data rate is 54Msps and the LLC clock output is 54MHz. Figure 17 shows the typical setup and hold timings of the output signals with RAWADC = 1.

LLC can optionally be inverted by setting LLC_INV = 1 in register 0x0D, B5.

With RAWADC = 1 the ADC outputs are filtered with the digital lowpass filter before being routed to D9–D0. The ADC outputs can be directly connected to D9–D0 without filtering by setting RAWADC = 1 and DISAAFLT = 1 in register 0x0F, B5.

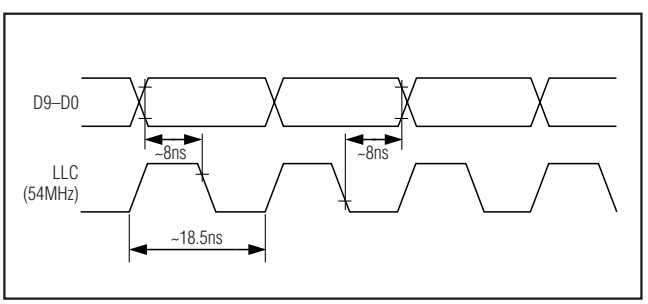


Figure 17. Typical Setup and Hold Timings in RAWADC Mode

Table 7. Output Test Signal Setup

DESCRIPTION	STDSEL REGISTER 0x04 B7-5	AUTOD REGISTER 0x04 B4	TGENAB REGISTER 0x0C B5	TGTIM REGISTER 0x0C B4	TGSRC REGISTER 0x0C B3	OUTPUT OF DECODER	
						NO VIDEO INPUT	VALID VIDEO INPUT
Default mode, test pattern has last timing standard used at output	0X0	1	0	X	X	Test pattern	Decoded input
Force test pattern with last timing standard used at output	0X0	1	1	X	1	Test pattern	Test pattern
Force test pattern with 50Hz timing	XXX	X	1	0	0	50Hz test pattern	50Hz test pattern
Force test pattern with 60Hz timing	XXX	X	1	1	0	60Hz test pattern	60Hz test pattern
Force 50Hz timing for decoding and test pattern	X0X	0	0	X	X	50Hz test pattern	Decoded input with 50Hz timing
Force 60Hz timing for decoding and test pattern	X1X	0	0	X	X	60Hz test pattern	Decoded input with 60Hz timing

Test Pattern Generation

In default mode, the MAX9526 outputs a test pattern when video is removed. The timing standard for the test pattern is the last timing standard that is at the output of the decoder. If the MAX9526 is reset and has no video inputs, the default output timing standard is 525 lines (60Hz). See register 0x04 for manually configuring the video standard decoding. Table 7 gives some common examples of setting up video standards and test pattern generation.

Test Pattern Enable (TGEnab)

1 = Force a test pattern at video output.

0 = Output a test pattern if no video is present at the video inputs (default).

Test Signal Output Timing Standard (TGTIM)

1 = 525 line, 60Hz frame rate.

0 = 625 line, 50Hz frame rate (default).

This bit is ignored if TGSRC = 1.

Test Signal Timing Source (TGSRC)

1 = Test generator uses timing from incoming video signal (if signal is valid).

0 = Test generator uses internally generated timing (default).

Color Bar Select (CBAR)

00 = Black screen (default)

01 = Blue screen

10 = 75% color bars

11 = 100% color bars

Clock and Output Control Register

REG	B7	B6	B5	B4	B3	B2	B1	B0
0x0D	0	CLIP	LLC_INV	SEL_54MHZ	XTAL_DIS	HSVS	DATAZ	LLCZ

ITU-R BT.656 Standard Clipping Level (CLIP)

1 = Clip ITU output to Y range is between 64–940 and CbCr range is between 64–960.

0 = Clip ITU output to Y range and CbCr range is between 5–1019 (default).

Inverted Line-Locked Clock (LLC_INV)

This signal inverts the polarity of the line-locked clock that is output from the MAX9526. This can be used to solve board level timing problems for other devices.

1 = Invert LLC clock.

0 = Do not invert LLC clock (default).

Input Clock Frequency Select (SEL_54MHz)

1 = 54MHz clock at XTAL/OSC input.

0 = 27MHz clock at XTAL/OSC input (default).

This bit is only applicable when the crystal oscillator is disabled (XTAL_DIS = 1).

Crystal Oscillator Disable (XTAL_DIS)

1 = XTAL/OSC is either a 27MHz or a 54MHz CMOS clock input.

0 = Enables the 27MHz crystal oscillator (default).

Horizontal/Vertical Sync Output (HSVS)

1 = D1 and D0 output horizontal and vertical sync pulses, respectively.

0 = D1 and D0 are LSBs of digital component video output (default).

The rising edge of horizontal sync (HS) coincides with the end of active video (rises after 3FFh 000h of EAV code). The falling edge coincides with the start of active video (SAV) code (falls after completing 3FFh 000h of SAV code). Figure 18 shows the horizontal and vertical sync timing.

The vertical sync pulse (VS) line transitions are detailed in Table 8. Note that the VS line transitions on pin D0 are shifted by 1 to 2 lines relative to the V flag transitions embedded in the ITU data stream. The V flag transitions embedded in the ITU data stream follow the ITU-R BT.656-4 standard.

Data Output Disable (DATAZ)

1 = Logic data outputs (D9–D0) are disabled and placed in high-impedance state.

0 = Logic data outputs (D9–D0) are enabled (default).

The DATAZ bit forces data outputs high impedance regardless of whether the device is in shutdown.

Clock Output Disable (LLCZ)

1 = Logic clock output (LLC) is disabled and placed in a high-impedance state.

0 = Logic clock output (LLC) is enabled (default).

The LLCZ bit forces LLC high impedance regardless of whether the device is in shutdown.

Table 8. VS (Pin D0) Line Transitions

VERTICAL SYNC PULSES (VS on Pin D0)		625	525
Field 1	Start (VS = 1)	Line 623	Line 2
	Finish (VS = 0)	Line 21	Line 21
Field 2	Start (VS = 1)	Line 309	Line 265
	Finish (VS = 0)	Line 335	Line 284

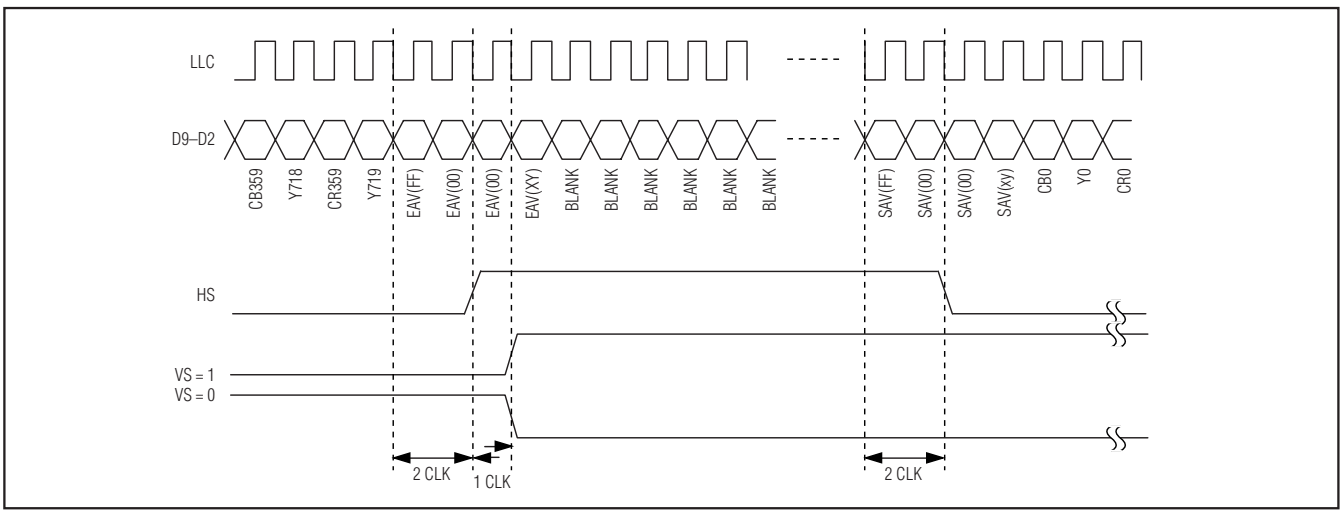


Figure 18. Horizontal and Vertical Sync Timing

PLL Control Register

REG	B7	B6	B5	B4	B3	B2	B1	B0
0x0E	0	0	LLC_MODE		PLLBYP	PLLBW		

Line-Locked Clock Mode (LLC_MODE)

0X = Async mode or line-locked mode is set automatically (default).

10 = PLL is forced to line-locked mode.

11 = PLL is forced to async mode.

PLL Bypass Mode (PLLBYP)

When PLLBYP = 1, the ADC and the decoder use the input crystal or clock (XTAL/OSC, XTAL2) directly.

1 = Bypass the PLL.

0 = PLL is enabled (default).

Line-Locked PLL Tracking Speed (PLLBW)

PLLBW controls a digital loop filter that sets the bandwidth of the line-locked PLL.

000 = 180Hz

001 = 250Hz

010 = 375Hz

011 = 500Hz (default)

100 = 750Hz

101 = 1kHz

110 = 1.5kHz

111 = 2kHz

Miscellaneous Register

REG	B7	B6	B5	B4	B3	B2	B1	B0
0x0F	0	0	DISAAFLT	1	SSLICE			

Disable Digital Anti-Aliasing Filter (DISAAFLT)

Disable the digital anti-aliasing filter following the ADC.

1 = Disables filter.

0 = Enables filter (default).

Sync Slicing Level (SSLICE)

Sets the sync slicing level.

1111 = Slice at 240 (decimal), near the blanking level.

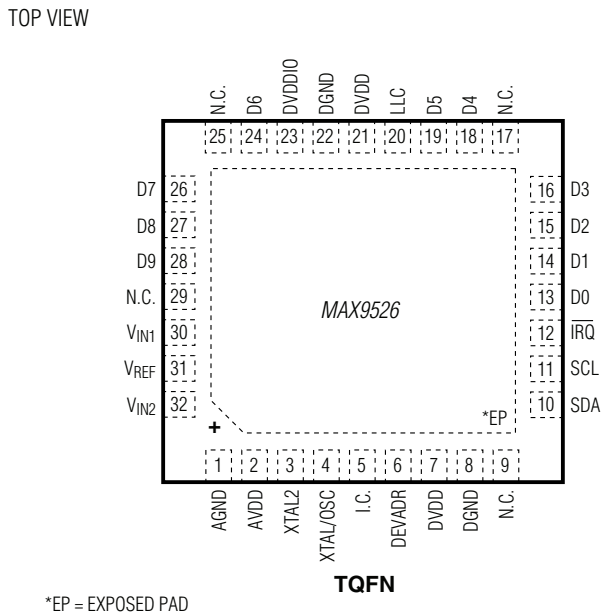
1000 = Slice at 128 (decimal), near the center of the sync (default).

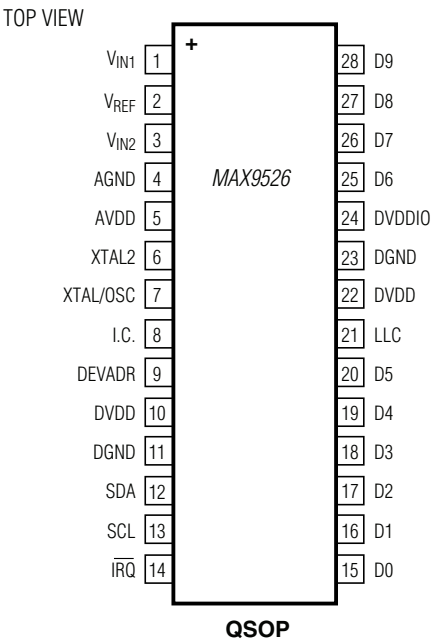
0100 = Slice at 64 (decimal), about 25% of the sync.

0000 = Slice at 0 (decimal), near the bottom of the sync.

All values between 0000 and 1111 are valid.

Pin Configurations

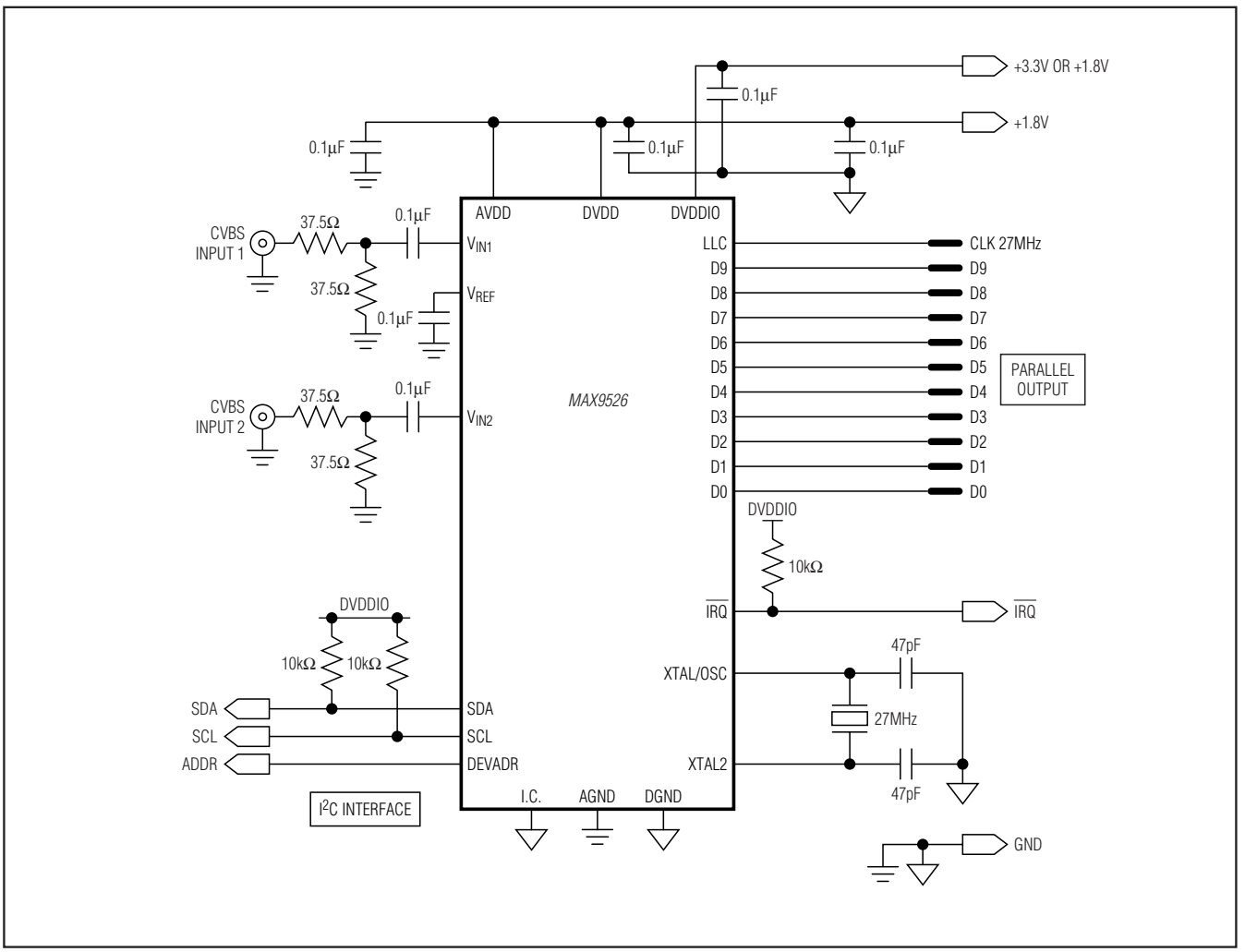




Chip Information

PROCESS: CMOS

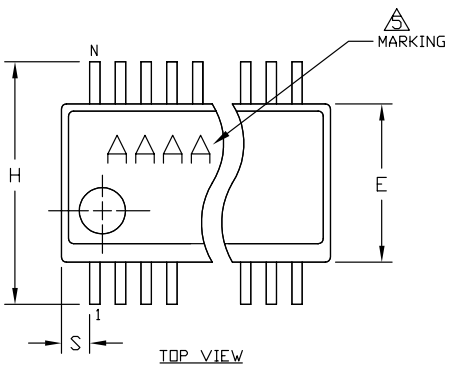
Typical Operating Circuit

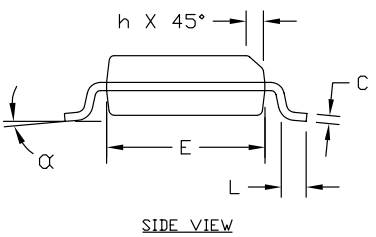


Package Information

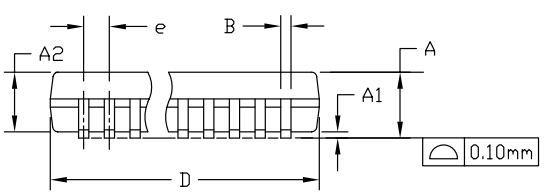
For the latest package outline information and land patterns (footprints), go to **www.maxim-ic.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
28 QSOP	E28-1	21-0055	90-0173
32 TQFN-EP	T3256-1	21-0183	90-0134





	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	.053	.069	1.35	1.75
A1	.004	.010	.102	.254
A2	.049	.065	1.245	1.651
B	.008	.012	0.20	0.30
C	.0075	.0098	0.191	0.249
D	SEE VARIATIONS			
E	.150	.157	3.81	3.99
e	.025 BSC		0.635 BSC	
H	.230	.244	5.84	6.20
h	.010	.016	0.25	0.41
L	.016	.035	0.41	0.89
N	SEE VARIATIONS			
α	0°	8°	0°	8°



VARIATIONS:

	INCHES		MILLIMETERS			
	MIN.	MAX.	MIN.	MAX.	N	PKG CODES
D	.189	.196	4.80	4.98	16	E16-1, E16M-1, E16-4, E16-5, E16-8F
S	.0020	.0070	0.05	0.18		
D	.337	.344	8.56	8.74	20	E20-1, E20-2, E20-3
S	.0500	.0550	1.270	1.397		
D	.337	.344	8.56	8.74	24	E24-1, E24-2, E24-3
S	.0250	.0300	0.635	0.762		
D	.386	.393	9.80	9.98	28	E28-1, E28M-1, E28-2
S	.0250	.0300	0.635	0.762		

NOTES:
1. D & E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED .006" PER SIDE.
3. CONTROLLING DIMENSIONS: INCHES.
4. MEETS JEDEC MO137.
5. MARKING SHOWN IS FOR PKG. ORIENTATION ONLY.
6. ALL DIMENSIONS APPLY TO BOTH LEADED (-) AND PbFREE (+) PKG. CODES.

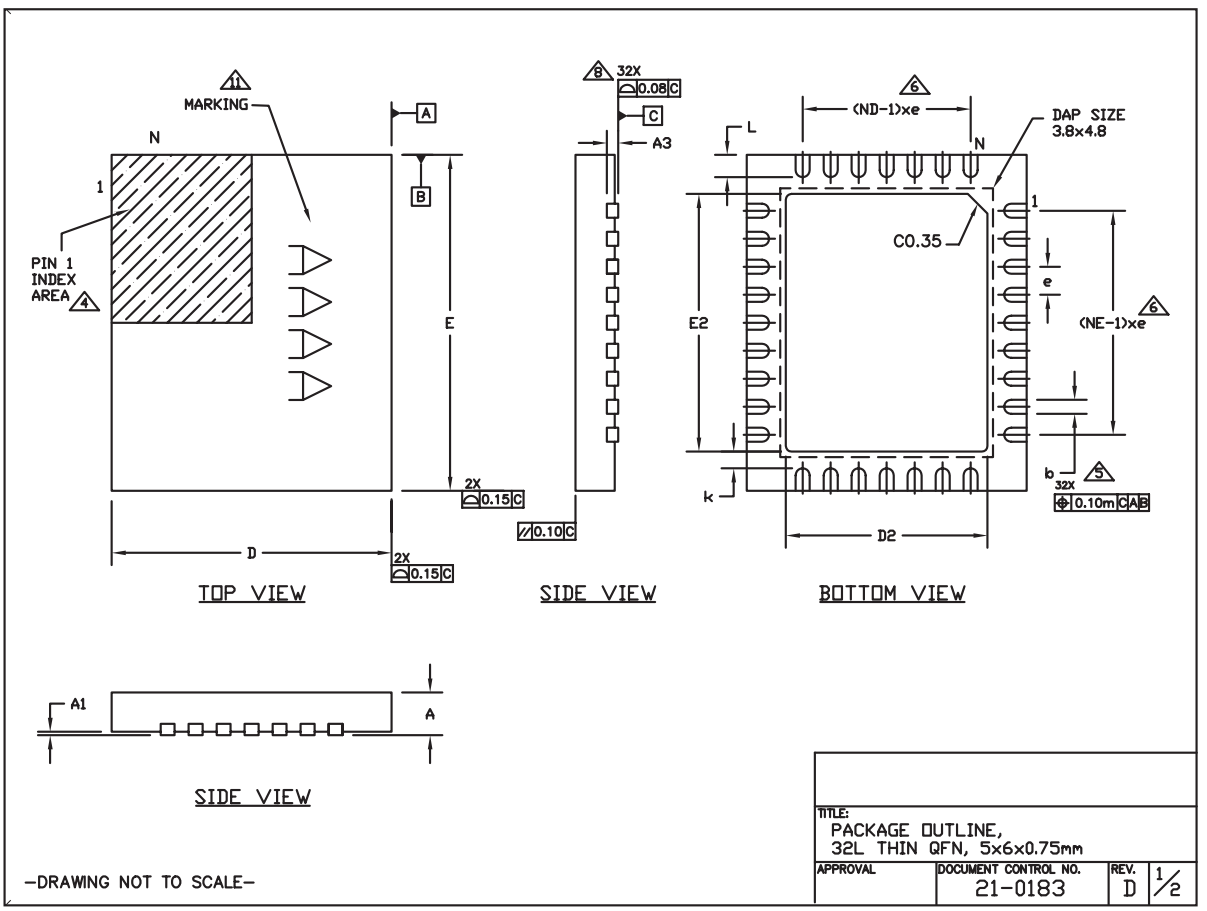
—DRAWING NOT TO SCALE—

TITLE: PACKAGE OUTLINE QSOP .150", .025" LEAD PITCH

APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0055	J	1/1

Package Information (continued)

For the latest package outline information and land patterns (footprints), go to **www.maxim-ic.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.



Package Information (continued)

For the latest package outline information and land patterns (footprints), go to **www.maxim-ic.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

REF.	MIN.	NOM.	MAX.	NOTE
A	0.70	0.75	0.80	
A1	0	-	0.05	
A3	0.20 REF			
b	0.20	0.25	0.30	
D	4.90	5.00	5.10	
E	5.90	6.00	6.10	
e	0.50 BSC			
k	0.25	-	-	
L	0.35	0.40	0.45	ALL PINS
N	32			
ND	7			
NE	9			

EXPOSED PAD VARIATIONS						
PKG. CODE	D2			E2		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
T3256-1	3.50	3.60	3.70	4.50	4.60	4.70
T3256MN-1	3.50	3.60	3.70	4.50	4.60	4.70

NOTES:
1. DIMENSIONING & TOLERANCING CONFORM TO ASME Y14.5M-1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES ARE IN DEGREES.
3. N IS THE TOTAL NUMBER OF TERMINALS.
4. THE TERMINAL #1 IDENTIFIER AND TERMINAL NUMBERING CONVENTION SHALL CONFORM TO JESD 95-1 SPP-012. DETAILS OF TERMINAL #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE TERMINAL #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE.
5. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.25mm AND 0.30mm FROM TERMINAL TIP.
6. ND AND NE REFER TO THE NUMBER OF TERMINALS ON EACH D AND E SIDE RESPECTIVELY.
7. DEPOPULATION IS POSSIBLE IN A SYMMETRICAL FASHION.
8. COPLANARITY APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.
9. REFER TO JEDEC MO-220 (WHJD) EXCEPT D2 & E2 DIMENSIONS.
10. WARPAGE SHALL NOT EXCEED 0.10mm.
11. MARKING IS FOR PACKAGE ORIENTATION REFERENCE ONLY.
12. ALL DIMENSIONS APPLY TO BOTH LEADED (-) AND PbFREE (+) PKG. CODES.

-DRAWING NOT TO SCALE-

TITLE: PACKAGE OUTLINE, 32L THIN QFN, 5x6x0.75mm

APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0183	D	2/2

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	5/09	Initial release	—
1	7/09	Corrected TQFN package diagram	36, 37
2	2/10	Added automotive parts	1
3	2/11	Added Loopback Operation Application Diagram and renumbered subsequent figures	18–21, 30, 32, 33

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