74AHC1G66; 74AHCT1G66

Single-pole single-throw analog switch

Rev. 04 — 18 December 2008 Product data sheet

1. General description

74AHC1G66 and 74AHCT1G66 are high-speed Si-gate CMOS devices. They are single-pole single-throw analog switches. The switch has two input/output pins (Y and Z) and an active HIGH enable input pin (E). When pin E is LOW, the analog switch is turned off.

2. Features

- Very low ON resistance:
  - 26 Ω (typ.) at V_{CC} = 3.0 V
  - 16 Ω (typ.) at V_{CC} = 4.5 V
  - 14 Ω (typ.) at V_{CC} = 5.5 V
- High noise immunity
- Low power dissipation
- Balanced propagation delays
- Multiple package options
- ESD protection:
  - HMB JESD22-A114E exceeds 2000 V
  - MM JESD22-A115-A exceeds 200 V
  - CDM JESD22-C101C exceeds 1000 V
- Specified from –40 °C to +85 °C and –40 °C to +125 °C

3. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74AHC1G66GW	–40 °C to +125 °C	TSSOP5	plastic thin shrink small outline package; 5 leads; body width 1.25 mm	SOT353-1
74AHCT1G66GW				
74AHC1G66GV	–40 °C to +125 °C	SC-74A	plastic surface-mounted package; 5 leads	SOT753
74AHCT1G66GV				

founded by Philips

4. Marking

Table 2. Marking codes

Type number	Marking
74AHC1G66GW	AL
74AHCT1G66GW	CL
74AHC1G66GV	A66
74AHCT1G66GV	C66

5. Functional diagram

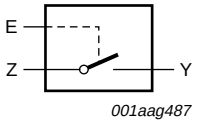

Fig 1. Logic symbol

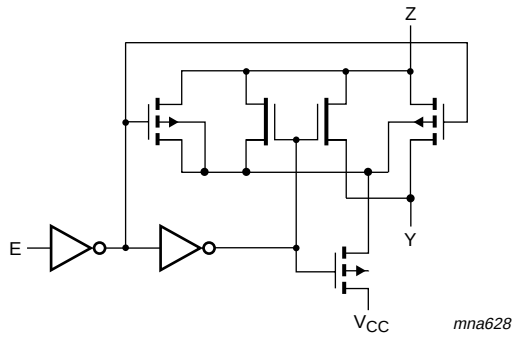

Fig 2. Logic diagram

6. Pinning information

6.1 Pinning

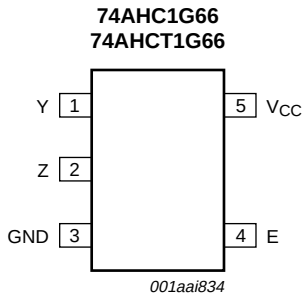

Fig 3. Pin configuration SOT353-1 and SOT753

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6.2 Pin description

Table 3. Pin description

Symbol	Pin	Description
Y	1	independent input or output
Z	2	independent input or output
GND	3	ground (0 V)
E	4	enable input (active HIGH)
V_{CC}	5	supply voltage

7. Functional description

Table 4. Function table[1]

Input E	Switch
L	OFF
H	ON

[1] H = HIGH voltage level; L = LOW voltage level.

8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{CC}	supply voltage			–0.5	+7.0	V
I_{IK}	input clamping current	$V_I < -0.5$ V	[1]	–20	-	mA
I_{SK}	switch clamping current	$V_I < -0.5$ V or $V_I > V_{CC} + 0.5$ V	[1]	-	±20	mA
I_{SW}	switch current	-0.5 V $< V_O < V_{CC} + 0.5$ V		-	±25	mA
I_{CC}	supply current			-	75	mA
I_{GND}	ground current			–75	-	mA
T_{stg}	storage temperature			–65	+150	°C
P_{tot}	total power dissipation	T_{amb} = –40 °C to +125 °C	[2]	-	250	mW

[1] The input and output voltage ratings may be exceeded if the input and output voltage ratings are observed.

[2] For TSSOP5 and SC-74A packages: above 87.5 °C the value of P_{tot} derates linearly with 4.0 mW/K.

9. Recommended operating conditions

Table 6. Recommended operating conditions

Voltages are referenced to GND (ground = 0 V).[1]

Symbol	Parameter	Conditions	74AHC1G66			74AHCT1G66			Unit
			Min	Typ	Max	Min	Typ	Max	
V_{CC}	supply voltage		2.0	5.0	5.5	4.5	5.0	5.5	V
V_I	input voltage		0	-	5.5	0	-	5.5	V
V_{SW}	switch voltage		0	-	V_{CC}	0	-	V_{CC}	V

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Table 6. Recommended operating conditions *...continued*

Voltages are referenced to GND (ground = 0 V).[1]

Symbol	Parameter	Conditions		74AHC1G66			74AHCT1G66			Unit
				Min	Typ	Max	Min	Typ	Max	
T_{amb}	ambient temperature			–40	+25	+125	–40	+25	+125	°C
Δt/ΔV	input transition rise and fall rate	V_{CC} = 3.3 ± 0.3 V	[2]	-	-	100	-	-	-	ns/V
		V_{CC} = 5.0 ± 0.5 V	[2]	-	-	20	-	-	20	ns/V

[1] To avoid drawing V_{CC} current out of pin Z, when switch current flows in pin Y, the voltage drop across the bidirectional switch must not exceed 0.4 V. If the switch current flows into pin Z, no V_{CC} current will flow out of terminal Y. In this case there is no limit for the voltage drop across the switch, but the voltage at pins Y and Z may not exceed V_{CC} or GND.

[2] Applies to control signal levels.

10. Static characteristics

Table 7. Static characteristics

Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	25 °C			–40 °C to +85 °C		–40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
74AHC1G66										
V_{IH}	HIGH-level input voltage	V_{CC} = 2.0 V	1.5	-	-	1.5	-	1.5	-	V
		V_{CC} = 3.0 V	2.1	-	-	2.1	-	2.1	-	V
		V_{CC} = 5.5 V	3.85	-	-	3.85	-	3.85	-	V
V_{IL}	LOW-level input voltage	V_{CC} = 2.0 V	-	-	0.5	-	0.5	-	0.5	V
		V_{CC} = 3.0 V	-	-	0.9	-	0.9	-	0.9	V
		V_{CC} = 5.5 V	-	-	1.65	-	1.65	-	1.65	V
I_I	input leakage current	V_I = 5.5 V or GND; V_{CC} = 5.5 V	-	-	0.1	-	1.0	-	2.0	μA
$I_{S(OFF)}$	OFF-state leakage current	Y or Z; V_{CC} = 5.5 V; see Figure 4	-	-	0.1	-	1.0	-	4.0	μA
$I_{S(ON)}$	ON-state leakage current	Y or Z; V_{CC} = 5.5 V; see Figure 5	-	-	0.1	-	1.0	-	4.0	μA
I_{CC}	supply current	E, Y or Z = V_{CC} or GND; V_{CC} = 5.5 V	-	-	1.0	-	10	-	40	μA
C_I	input capacitance	E input	-	2.0	10	-	10	-	10	pF
$C_{S(ON)}$	ON-state capacitance	Y or Z input or output	-	4.0	10	-	10	-	10	pF
74AHCT1G66										
V_{IH}	HIGH-level input voltage	V_{CC} = 4.5 V to 5.5 V	2.0	-	-	2.0	-	2.0	-	V
V_{IL}	LOW-level input voltage	V_{CC} = 4.5 V to 5.5 V	-	-	0.8	-	0.8	-	0.8	V
I_I	input leakage current	V_I = 5.5 V or GND; V_{CC} = 5.5 V	-	-	0.1	-	1.0	-	2.0	μA

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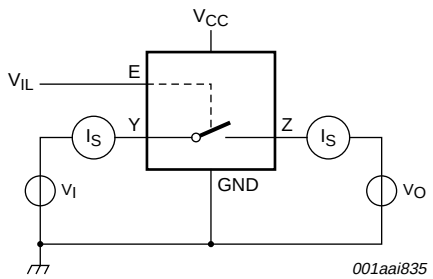
Table 7. Static characteristics *...continued*

Voltages are referenced to GND (ground = 0 V).

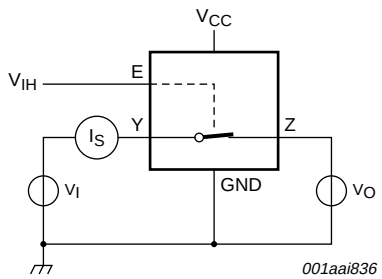
Symbol	Parameter	Conditions	25 °C			–40 °C to +85 °C		–40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
$I_{S(OFF)}$	OFF-state leakage current	Y or Z; V_{CC} = 5.5 V; see Figure 4	-	-	0.1	-	1.0	-	4.0	µA
$I_{S(ON)}$	ON-state leakage current	Y or Z; V_{CC} = 5.5 V; see Figure 5	-	-	0.1	-	1.0	-	4.0	µA
I_{CC}	supply current	E, Y or Z = V_{CC} or GND; V_{CC} = 5.5 V	-	-	1.0	-	10	-	40	µA
ΔI_{CC}	additional supply current	per input pin; V_I = 3.4 V; other inputs at V_{CC} or GND; I_O = 0 A; V_{CC} = 5.5 V	-	-	1.35	-	1.5	-	1.5	mA
C_I	input capacitance	E input	-	2.0	10	-	10	-	10	pF
$C_{S(ON)}$	ON-state capacitance	Y or Z input or output	-	4.0	10	-	10	-	10	pF

10.1 Test circuits



V_I = V_{CC} or GND and V_O = GND or V_{CC}.

Fig 4. Test circuit for measuring OFF-state leakage current



V_I = V_{CC} or GND and V_O = open circuit.

Fig 5. Test circuit for measuring ON-state leakage current

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10.2 ON resistance

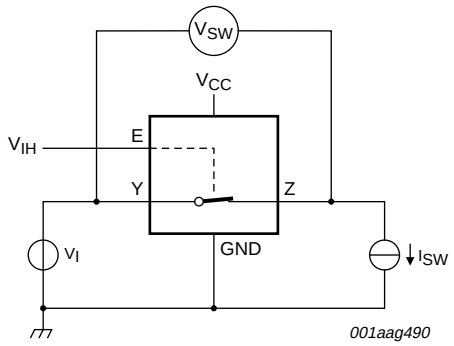
Table 8. ON resistance

At recommended operating conditions; voltages are referenced to GND (ground 0 V); for graph see Figure 7 [1].

Symbol	Parameter	Conditions	25 °C		−40 °C to +85 °C	−40 °C to +125 °C	Unit
			Typ	max	Max	Max	
74AHC1G66 and 74AHCT1G66							
$R_{ON(peak)}$	ON resistance (peak)	$V_I = V_{CC}$ to GND; see Figure 6					
		I_{SW} = 1.0 mA; V_{CC} = 2.0 V	148[1]	-	-	-	Ω
		I_{SW} = 10 mA; V_{CC} = 3.0 V to 3.6 V	28	50	70	110	Ω
		I_{SW} = 10 mA; V_{CC} = 4.5 V to 5.5 V	15	30	40	60	Ω
$R_{ON(rail)}$	ON resistance (rail)	V_I = GND; see Figure 6					
		I_{SW} = 1.0 mA; V_{CC} = 2.0 V	30	-	-	-	Ω
		I_{SW} = 10 mA; V_{CC} = 3.0 V to 3.6 V	20	50	65	90	Ω
		I_{SW} = 10 mA; V_{CC} = 4.5 V to 5.5 V	15	22	26	40	Ω
		$V_I = V_{CC}$; see Figure 6					
		I_{SW} = 1.0 mA; V_{CC} = 2.0 V	28	-	-	-	Ω
		I_{SW} = 10 mA; V_{CC} = 3.0 V to 3.6 V	18	50	65	90	Ω
		I_{SW} = 10 mA; V_{CC} = 4.5 V to 5.5 V	13	22	26	40	Ω

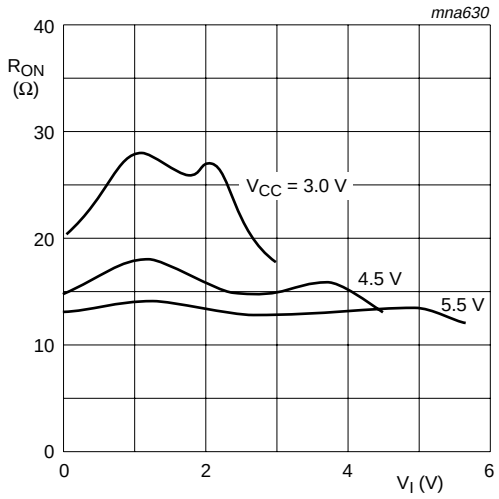
[1] At supply voltages approaching 2 V, the analog switch ON resistance becomes extremely non-linear. Therefore it is recommended that these devices be used to transmit digital signals only, when using this supply voltage.

10.3 ON resistance test circuit and graphs



$R_{ON} = V_{SW} / I_{SW}$.

Fig 6. Test circuit for measuring ON resistance



T_{amb} = 25 °C.

Fig 7. Typical ON resistance as a function of input voltage

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11. Dynamic characteristics

Table 9. Dynamic characteristics

Voltages are referenced to GND (ground = 0 V); C_L = 50 pF; unless otherwise specified; *For test circuit see Figure 10.*

Symbol	Parameter	Conditions		25 °C		–40 °C to +85 °C	–40 °C to +125 °C	Unit
				Typ[1]	max	Max	Max	
74AHC1G66								
t_{pd}	propagation delay	Y to Z or Z to Y; see Figure 8	[2]					
		V_{CC} = 2.0 V		2.2	5.0	6.0	7.0	ns
		V_{CC} = 3.0 V to 3.6 V		1.0	2.0	3.0	4.0	ns
		V_{CC} = 4.5 V to 5.5 V		0.6	1.0	2.0	3.0	ns
t_{en}	enable time	E to Y or Z; see Figure 9	[2]					
		V_{CC} = 2.0 V; C_L = 15 pF		7.0	25.0	33.0	40.0	ns
		V_{CC} = 2.0 V		11.0	35.0	46.0	57.0	ns
		V_{CC} = 3.0 V to 3.6 V; C_L = 15 pF		4.0	11.0	14.0	18.0	ns
		V_{CC} = 3.0 V to 3.6 V		5.8	15.0	20.0	25.0	ns
		V_{CC} = 4.5 V to 5.5 V; C_L = 15 pF		3.0	8.0	10.0	13.0	ns
		V_{CC} = 4.5 V to 5.5 V		4.0	11.0	13.0	17.0	ns
t_{dis}	disable time	E to Y or Z; see Figure 9	[2]					
		V_{CC} = 2.0 V; C_L = 15 pF		9.0	25.0	33.0	40.0	ns
		V_{CC} = 2.0 V		13.0	35.0	46.0	57.0	ns
		V_{CC} = 3.0 V to 3.6 V; C_L = 15 pF		6.0	11.0	14.0	18.0	ns
		V_{CC} = 3.0 V to 3.6 V		8.4	15.0	20.0	25.0	ns
		V_{CC} = 4.5 V to 5.5 V; C_L = 15 pF		5.0	8.0	10.0	13.0	ns
		V_{CC} = 4.5 V to 5.5 V		6.1	11.0	13.0	17.0	ns
C_{PD}	power dissipation capacitance	V_I = GND to V_{CC}	[3]	13	-	-	-	pF
74AHCT1G66								
t_{pd}	propagation delay	Y to Z or Z to Y; see Figure 8	[2]					
		V_{CC} = 4.5 V to 5.5 V		0.7	1.0	2.0	3.0	ns
t_{en}	enable time	E to Y or Z; see Figure 9	[2]					
		V_{CC} = 4.5 V to 5.5 V; C_L = 15 pF		3.0	7.0	10.0	13.0	ns
		V_{CC} = 4.5 V to 5.5 V		4.7	10.0	13.0	17.0	ns
t_{dis}	disable time	E to Y or Z; see Figure 9	[2]					
		V_{CC} = 4.5 V to 5.5 V; C_L = 15 pF		5.0	8.0	10.0	13.0	ns
		V_{CC} = 4.5 V to 5.5 V		6.5	11.0	13.0	17.0	ns

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Table 9. Dynamic characteristics *...continued*

Voltages are referenced to GND (ground = 0 V); C_L = 50 pF; unless otherwise specified; *For test circuit see Figure 10.*

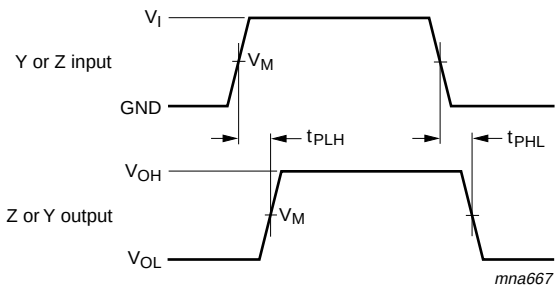
Symbol	Parameter	Conditions		25 °C		–40 °C to +85 °C	–40 °C to +125 °C	Unit
				Typ[1]	max	Max	Max	
C_{PD}	power dissipation capacitance	V_I = GND to V_{CC}	[3]	15	-	-	-	pF

[1] All typical values are measured at V_{CC} = 2.0 V, V_{CC} = 3.3 V, V_{CC} = 5.0 V and T_{amb} = 25 °C.

[2] t_{pd} is the same as t_{PLH} and t_{PHL}.
t_{en} is the same as t_{PZL} and t_{PZH}.
t_{dis} is the same as t_{PLZ} and t_{PHZ}.

[3] C_{PD} is used to determine the dynamic power dissipation P_D (μW).
$P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma ((C_L \times C_{SW}) \times V_{CC}^2 \times f_o)$ where:
f_i = input frequency in MHz;
f_o = output frequency in MHz;
C_L = output load capacitance in pF;
C_{SW} = maximum switch capacitance in pF (see Table 7);
V_{CC} = supply voltage in Volt;
$\Sigma ((C_L \times C_{SW}) \times V_{CC}^2 \times f_o)$ = sum of outputs.

11.1 Waveforms and test circuit



Measurement points are given in Table 10.

Logic levels: V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Fig 8. Input (Y or Z) to output (Z or Y) propagation delays

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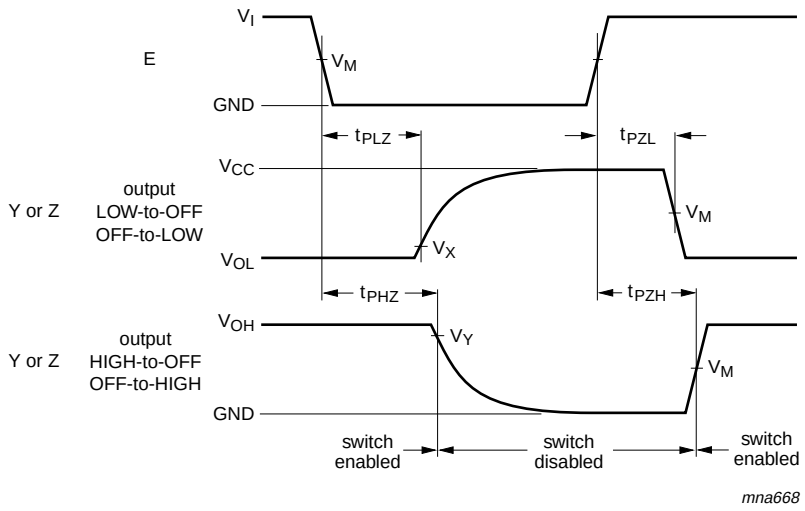

Measurement points are given in Table 10.

Logic levels: V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Fig 9. Enable and disable times

Table 10. Measurement points

Type	Input	Output		
	V_M	V_M	V_X	V_Y
74AHC1G66	$0.5V_{CC}$	$0.5V_{CC}$	V_{OL} + 0.3 V	V_{OH} – 0.3 V
74AHCT1G66	1.5 V	1.5 V	V_{OL} + 0.3 V	V_{OH} – 0.3 V

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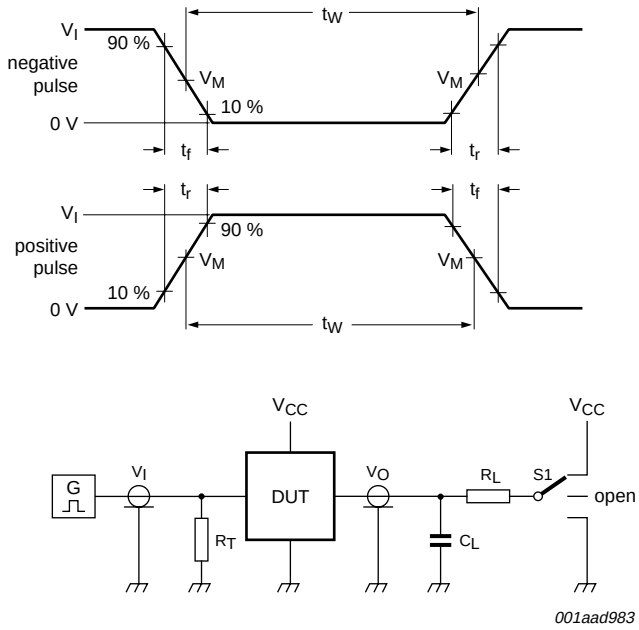

Test data is given in Table 11.

Definitions for test circuit:

R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator.

C_L = Load capacitance including jig and probe capacitance.

R_L = Load resistance.

S1 = Test selection switch.

Fig 10. Test circuit for measuring switching times

Table 11. Test data

Type	Input		Load		S1 position		
	V_I	t_r, t_f	C_L	R_L	t_{PHL}, t_{PLH}	t_{PZH}, t_{PHZ}	t_{PZL}, t_{PLZ}
74AHC1G66	GND to V_{CC}	3 ns	15 pF, 50 pF	1 kΩ	open	GND	V_{CC}
74AHCT1G66	GND to 3 V	3 ns	15 pF, 50 pF	1 kΩ	open	GND	V_{CC}

11.2 Additional dynamic characteristics

Table 12. Additional dynamic characteristics for 74AHC1G66 and 74AHCT1G66

GND = 0 V; $t_r = t_f$ = 3.0 ns; C_L = 50 pF; unless otherwise specified. All typical values are measured at T_{amb} = 25 °C.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
THD	total harmonic distortion	f_i = 1 kHz; R_L = 10 kΩ; see Figure 11				
		V_{CC} = 3.0 V to 3.6 V	-	0.025	-	%
		V_{CC} = 4.5 V to 5.5 V	-	0.015	-	%
		f_i = 10 kHz; R_L = 10 kΩ; see Figure 11				
		V_{CC} = 3.0 V to 3.6 V; V_I = 2.5 V	-	0.025	-	%
		V_{CC} = 4.5 V to 5.5 V; V_I = 4.0 V	-	0.015	-	%

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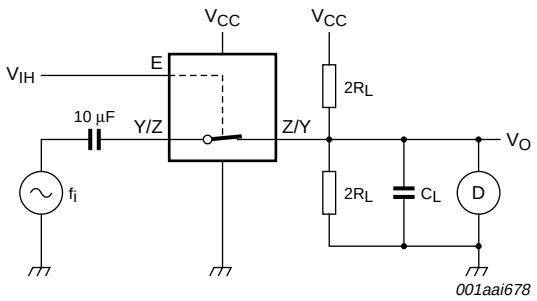
Table 12. Additional dynamic characteristics for 74AHC1G66 and 74AHCT1G66 *...continued*

GND = 0 V; $t_r = t_f = 3.0$ ns; $C_L = 50$ pF; unless otherwise specified. All typical values are measured at $T_{amb} = 25\,°C$.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$f_{(-3dB)}$	–3 dB frequency response	$R_L = 50\,\Omega$; $C_L = 10$ pF; see Figure 12 and 13					
		$V_{CC} = 3.0$ V to 3.6 V		-	230	-	MHz
		$V_{CC} = 4.5$ V to 5.5 V		-	280	-	MHz
α_{iso}	isolation (OFF-state)	$R_L = 600\,\Omega$; $f_i = 1$ MHz; see Figure 14	[1]				
		$V_{CC} = 3.0$ V to 3.6 V; $V_I = 2.5$ V		-	–50	-	dB
		$V_{CC} = 4.5$ V to 5.5 V; $V_I = 4.0$ V		-	–50	-	dB

[1] Adjust input voltage V_I to 0 dBm level (0 dBm =1 mW into 50 Ω).

11.3 Test circuits and graphs

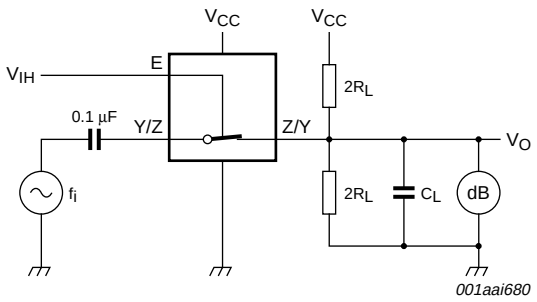


Test conditions:

$V_{CC} = 3.0$ V to 3.6 V; $V_I = 2.5$ V (p-p).

$V_{CC} = 4.5$ V to 5.5 V; $V_I = 4.0$ V (p-p).

Fig 11. Test circuit for measuring total harmonic distortion



With $f_i = 1$ MHz adjust the switch input voltage for a 0 dBm level at the switch output, (0 dBm = 1 mW into 50 Ω). Then increase the input f_i frequency until the dB meter reads –3 dB.

Fig 12. Test circuit for measuring the –3 dB frequency response

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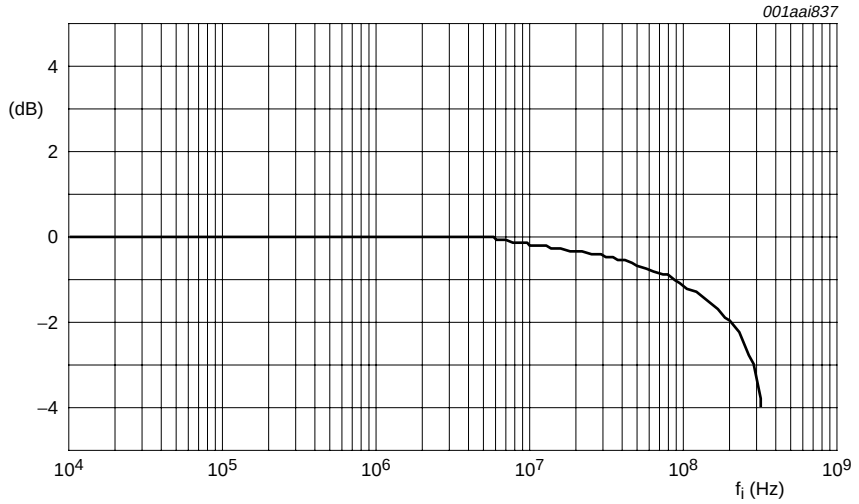
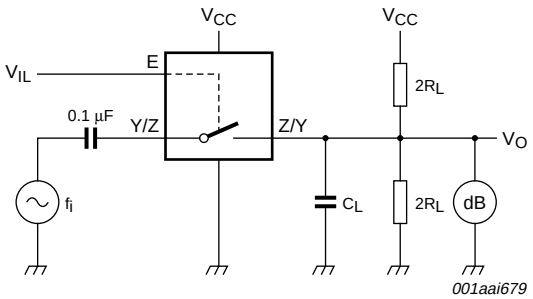


Test conditions: V_{CC} = 4.5 V; GND = 0 V; R_L = 50 Ω; R_{SOURCE} = 1 kΩ.

Fig 13. Typical –3 dB frequency response



Adjust the switch input voltage for a 0 dBm level (0 dBm = 1 mW into 600 Ω).

Fig 14. Test circuit for measuring isolation (OFF-state)

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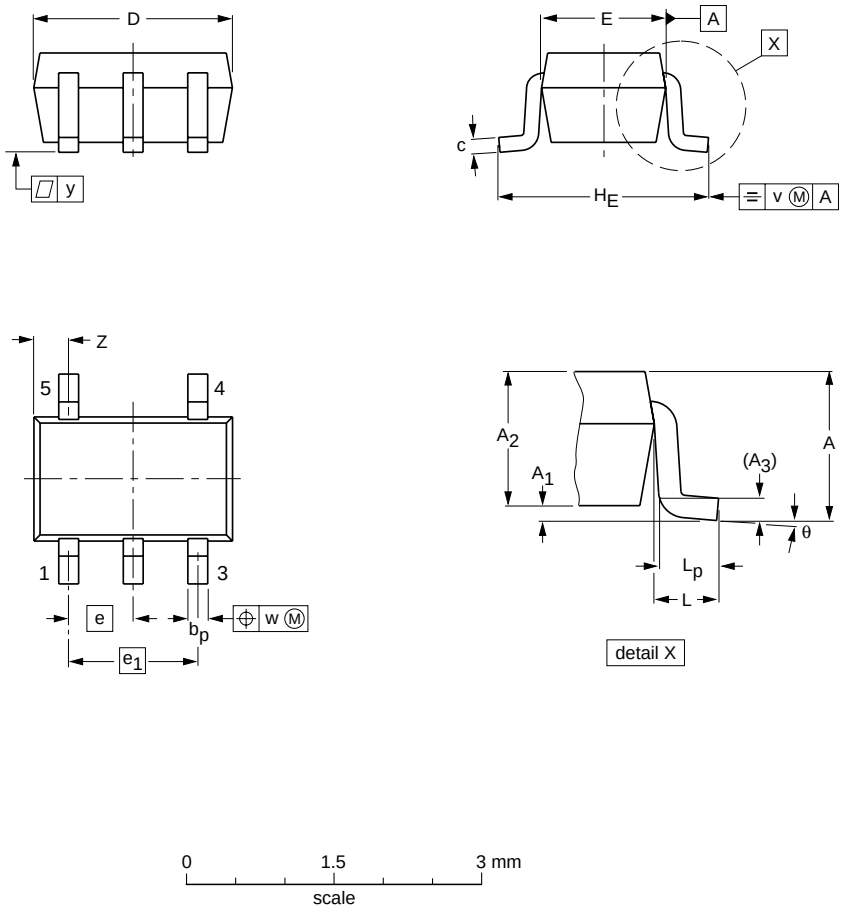
12. Package outline

TSSOP5: plastic thin shrink small outline package; 5 leads; body width 1.25 mm **SOT353-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D(1)	E(1)	e	e_1	H_E	L	L_p	v	w	y	Z(1)	θ
mm	1.1	0.1 0	1.0 0.8	0.15	0.30 0.15	0.25 0.08	2.25 1.85	1.35 1.15	0.65	1.3	2.25 2.0	0.425	0.46 0.21	0.3	0.1	0.1	0.60 0.15	7° 0°

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT353-1		MO-203	SC-88A			~~00-09-01~~ 03-02-19

Fig 15. Package outline SOT353-1 (TSSOP5)

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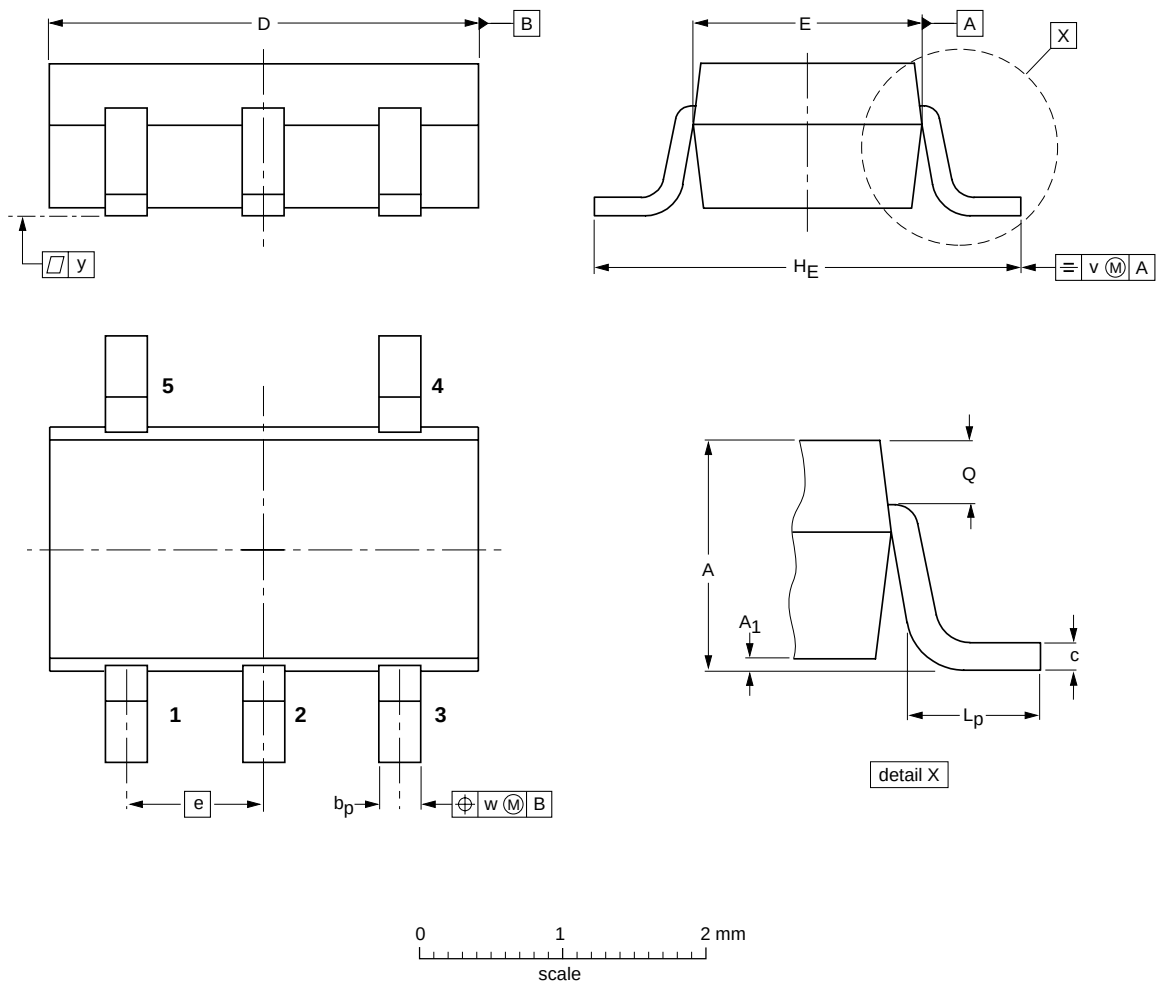
Plastic surface-mounted package; 5 leads **SOT753**



DIMENSIONS (mm are the original dimensions)

UNIT	A	A_1	b_p	c	D	E	e	H_E	L_p	Q	v	w	y
mm	1.1 0.9	0.100 0.013	0.40 0.25	0.26 0.10	3.1 2.7	1.7 1.3	0.95	3.0 2.5	0.6 0.2	0.33 0.23	0.2	0.2	0.1

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT753			SC-74A			~~02-04-16~~ 06-03-16

Fig 16. Package outline SOT753 (SC-74A)

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13. Abbreviations

Table 13. Abbreviations

Acronym	Description
CDM	Charged Device Model
CMOS	Complementary Metal-Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model

14. Revision history

Table 14. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74AHC_AHCT1G66_4	20081218	Product data sheet	-	74AHC_AHCT1G66_3
Modifications:	• The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors. • Legal texts have been adapted to the new company name where appropriate. • Package SOT353 changed to SOT353-1 in Table 1 and Figure 15. • Quick Reference Data and Soldering sections removed. • Section 2 “Features” updated.			
74AHC_AHCT1G66_3	20020606	Product specification	-	74AHC_AHCT1G66_2
74AHC_AHCT1G66_2	20020215	Product specification	-	74AHC_AHCT1G66_1
74AHC_AHCT1G66_1	20010129	Product specification	-	-

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15.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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