

# DATA SHEET

## **UAA3515A** 900 MHz analog cordless telephone IC

Product specification  
File under Integrated Circuits, IC17

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**900 MHz analog cordless telephone IC****UAA3515A**

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**1 FEATURES****1.1 Single frequency conversion FM receiver**

- Integrated Low Noise Amplifier (LNA)
- Image reject mixer
- FM detector (10.7 MHz) with:
  - IF limiter
  - wide band PLL demodulator
  - output amplifier
  - Received Signal Strength Indicator (RSSI) output
- Carrier Detector (CD) with programmable threshold
- Programmable data amplifier (slicer) phase.

**1.2 Receiver baseband**

- Programmable receiver gain
- Expander
- Earpiece amplifier with volume control feature
- Data amplifier.

**1.3 Synthesizer**

- Crystal reference oscillator with integrated tuning capacitor
- Reference frequency divider
- Narrow band receiver PLL including VCO with integrated variable capacitance diodes
- Narrow band transmitter PLL including VCO with integrated variable capacitance diodes
- Integrated VCO circuits designed to function with external inductors etched directly as part of the printed-circuit board (cost-saving feature)
- Programmable clock divider with output buffer to drive the microcontroller.

**1.4 Transmitter**

- Internal buffered Power Amplifier (PA) with programmable gain
- Data transmission summing amplifier.

**1.5 Transmitter baseband**

- Programmable transmitter gain
- Microphone amplifier
- Compressor with Automatic Level Control (ALC) and hard limiter.

**1.6 Microcontroller interface**

- Three-wire serial interface.

**1.7 Power supplies**

- Voltage regulator for internal PLL supplies
- Selectable voltage doubler
- Programmable Low-Battery Detection (LBD) (time-multiplexed with RSSI carrier detector).

**2 APPLICATIONS**

- Analog cordless telephone sets (900 MHz).

**3 GENERAL DESCRIPTION**

The UAA3515A is a BiCMOS integrated circuit that performs all functions from antenna to microcontroller in reception and transmission for both base station and handset of a 900 MHz cordless telephone set. In addition, the implemented programming reduces significantly the amount of external components, board space and external adjustments required.

**4 ORDERING INFORMATION**

| TYPE NUMBER | PACKAGE |   |          |
|-------------|---------|---|----------|
|             | NAME    | DESCRIPTION   | VERSION  |
| UAA3515AHL  | LQFP64  | plastic, low profile quad flat package; 64 leads; body 10 × 10 × 1.4 mm | SOT314-2 |

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5 BLOCK DIAGRAM

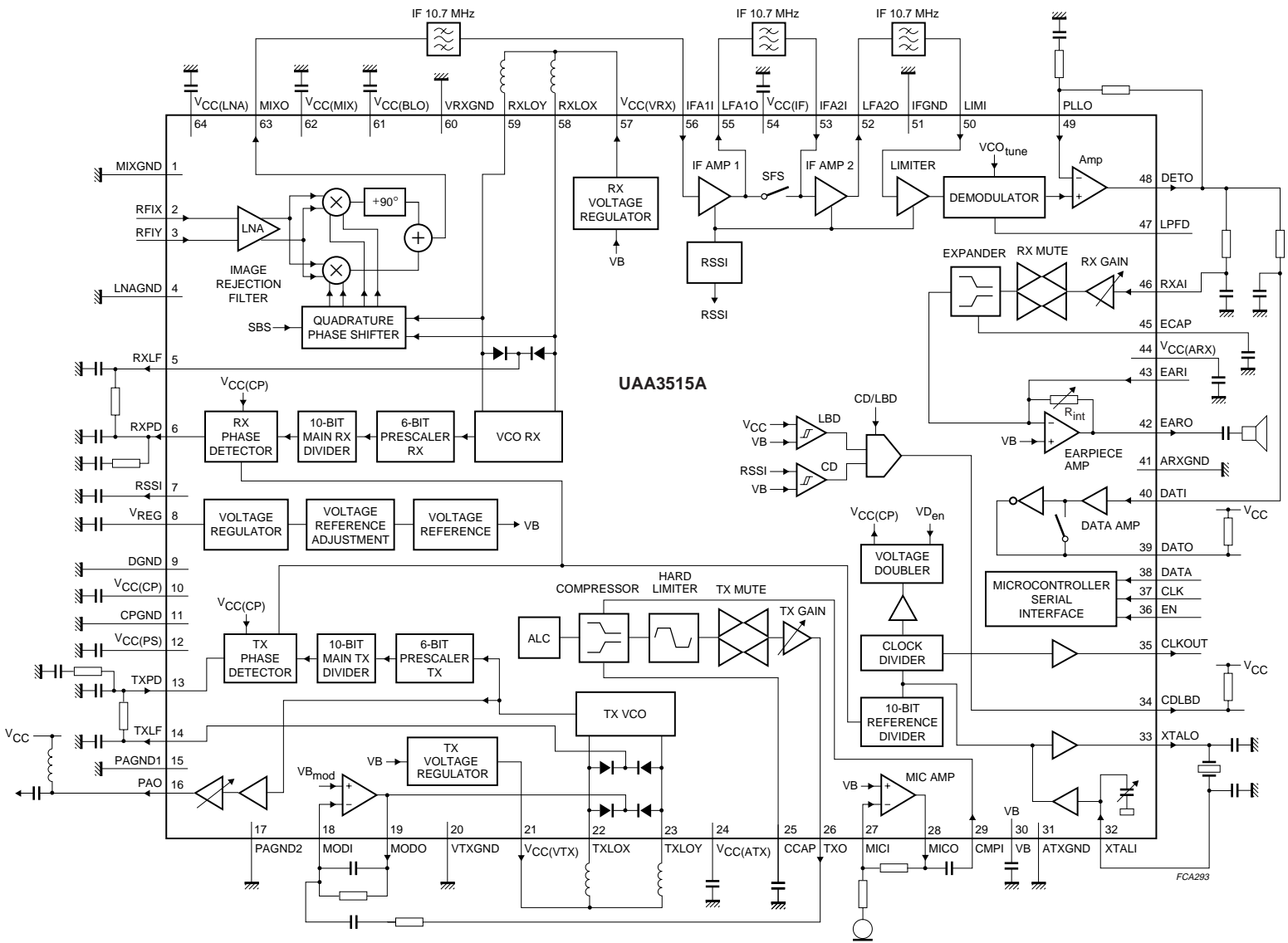


Fig.1 Block diagram.

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## 6 PINNING

| SYMBOL               | PIN | DESCRIPTION  |
|----------------------|-----|--|
| MIXGND               | 1   | mixer ground   |
| RFIX                 | 2   | LNA voltage (X) input  |
| RFIY                 | 3   | LNA voltage (Y) input  |
| LNAGND               | 4   | LNA ground   |
| RXLF                 | 5   | RX PLL filter output   |
| RXPD                 | 6   | RX phase detector voltage output   |
| RSSI                 | 7   | RSSI output  |
| V <sub>REG</sub>     | 8   | pin for internal voltage regulator   |
| DGND                 | 9   | digital ground   |
| V <sub>CC(CP)</sub>  | 10  | internal voltage doubler supply voltage (or positive supply voltage input) for charge pumps        |
| CPGND                | 11  | charge pump ground   |
| V <sub>CC(PS)</sub>  | 12  | prescaler positive supply voltage input  |
| TXPD                 | 13  | TX phase detector voltage input  |
| TXLF                 | 14  | TX PLL filter output   |
| PAGND1               | 15  | power amplifier ground 1   |
| PAO                  | 16  | power amplifier output   |
| PAGND2               | 17  | power amplifier ground 2   |
| MODI                 | 18  | summing amplifier input  |
| MODO                 | 19  | summing amplifier output   |
| VTXGND               | 20  | transmitter VCO ground   |
| V <sub>CC(VTX)</sub> | 21  | transmitter VCO positive supply voltage input  |
| TXLOX                | 22  | transmitter VCO voltage (X) to external inductor   |
| TXLOY                | 23  | transmitter VCO voltage (Y) to external inductor   |
| V <sub>CC(ATX)</sub> | 24  | transmitter audio positive supply voltage input  |
| CCAP                 | 25  | external capacitor for compressor  |
| TXO                  | 26  | audio transmitter output   |
| MICI                 | 27  | microphone amplifier input   |
| MICO                 | 28  | microphone amplifier output  |
| CMPI                 | 29  | compressor input   |
| VB                   | 30  | reference voltage  |
| ATXGND               | 31  | transmitter audio ground   |
| XTALI                | 32  | crystal input  |
| XTALO                | 33  | crystal output   |
| CDLBD                | 34  | CD or LBD open collector output (out-of-lock synthesizer receiver and/or transmitter in test mode) |
| CLKOUT               | 35  | clock output (CMOS levels)   |
| EN                   | 36  | enable input for serial interface  |
| CLK                  | 37  | clock input for serial interface   |
| DATA                 | 38  | data input for serial interface  |

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| SYMBOL               | PIN | DESCRIPTION                                      |
|----------------------|-----|--|
| DATO                 | 39  | data amplifier open collector output             |
| DATI                 | 40  | data amplifier input                             |
| ARXGND               | 41  | audio receiver ground                            |
| EARO                 | 42  | earpiece amplifier output                        |
| EARI                 | 43  | earpiece amplifier input                         |
| V <sub>CC(ARX)</sub> | 44  | audio receiver positive supply voltage input     |
| ECAP                 | 45  | external capacitor for expander                  |
| RXAI                 | 46  | audio receiver input                             |
| LPFD                 | 47  | demodulator loop filter output                   |
| DETO                 | 48  | demodulator amplifier output                     |
| PLLO                 | 49  | demodulator amplifier negative input             |
| LIMI                 | 50  | limiter input                                    |
| IFGND                | 51  | IF negative supply voltage                       |
| IFA2O                | 52  | IF second amplifier output                       |
| IFA2I                | 53  | IF second amplifier input                        |
| V <sub>CC(IF)</sub>  | 54  | IF positive supply voltage input                 |
| IFA1O                | 55  | IF first amplifier output                        |
| IFA1I                | 56  | IF first amplifier input                         |
| V <sub>CC(VRX)</sub> | 57  | receiver VCO positive supply voltage input       |
| RXLOX                | 58  | receiver VCO voltage (X) to external inductor    |
| RXLOY                | 59  | receiver VCO voltage (Y) to external inductor    |
| VRXGND               | 60  | receiver VCO ground                              |
| V <sub>CC(BLO)</sub> | 61  | receiver LO buffer positive supply voltage input |
| V <sub>CC(MIX)</sub> | 62  | mixers positive supply voltage input             |
| MIXO                 | 63  | mixer output                                     |
| V <sub>CC(LNA)</sub> | 64  | LNA positive supply voltage input                |

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Fig.2 Pin configuration.

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**7 FUNCTIONAL DESCRIPTION****7.1 Power supply and power management****7.1.1 POWER SUPPLY**

The UAA3515A is used in a cordless telephone handset and in a base unit. The handset unit is battery powered and operates on three NiCd cells. The minimum supply voltage ( $V_{CC}$ ) is 2.9 V.

**7.1.2 POWER SAVING**

When the UAA3515A is used in a handset, it is important to minimize current consumption. The main operating modes are:

- Active mode (talk): all blocks are powered
- RX mode: all circuits in the receiver part are powered

- Inactive mode: with the exception of the microcontroller interface, all circuits are powered-down. The crystal reference oscillator, the output clock buffer, the voltage regulator and the voltage doubler can be disabled separately. To reduce microcontroller current consumption, the crystal frequency to the clock output can be divided by 128. A low current consumption mode for the crystal oscillator can be programmed.

Latch memory is maintained in all modes. Blocks that are powered are shown in Table 1 per operating mode.

The crystal oscillator, the clock output buffer, the voltage reference adjustment, the power amplifier, the voltage doubler, the earpiece, the hard limiter and the ALC can be activated separately. Blocks that can be activated in each mode are shown in Table 2.

**Table 1** Power operating modes

| CIRCUIT BLOCK                | ACTIVE MODE | RX MODE   | INACTIVE MODE |
|------------------------------|-------------|-----------|---------------|
| Voltage reference adjustment | power ON    | power ON  | power OFF     |
| RF receiver                  | power ON    | power ON  | power OFF     |
| RX PLL                       | power ON    | power ON  | power OFF     |
| RX and TX audio paths        | power ON    | power OFF | power OFF     |
| RF TX (and PA, when enabled) | power ON    | power OFF | power OFF     |

**Table 2** Powered circuit blocks

| CIRCUIT BLOCK                                    | ACTIVE MODE | RX MODE   | INACTIVE MODE |
|--|-------------|-----------|---------------|
| Crystal oscillator; note 1                       | power ON    | power ON  | power ON      |
| Clock output buffer                              | power ON    | power ON  | power ON      |
| Voltage reference enable; note 2                 | power ON    | power ON  | power ON      |
| Power amplifier (PA2 = 1)                        | power ON    | power OFF | power OFF     |
| Voltage doubler enable; note 3                   | power ON    | power ON  | power ON      |
| Hard limiter and ALC not disabled                | power ON    | power OFF | power OFF     |
| Earpiece amplifier (earpiece enable = 1); note 4 | power ON    | power ON  | power OFF     |

**Notes**

1. In RX and active mode, the crystal oscillator is activated automatically. An external frequency can be forced at the crystal pins XTALI and XTALO.
2. In RX and active mode, the voltage reference is enabled automatically (whether bit  $V_{REG}$  enable is logic 0 or 1).
3. If the voltage doubler is enabled, the crystal oscillator is activated automatically.
4. In inactive mode the amplifier is disabled automatically.



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## 7.1.3 CURRENT CONSUMPTION

The control bit values for selection of each mode and typical current consumption for the modes are shown in Table 3.

When clock out is activated there is an extra power demand proportional to the programmed output level (see Table 4 for examples). When bit Xtal high = 0 (oscillator is in low current consumption mode), the crystal in use must have losses less than 20  $\Omega$  to ensure oscillator start-up.

**Table 3** Typical current consumption

$V_{CC} = 3.3$  V;  $T_{amb} = 25$  °C;  $f_{(i)xtal} = 10.24$  MHz.

| POWER OPERATING MODE | CONDITIONS   | TYPICAL CURRENT CONSUMPTION |
|----------------------|--|-----------------------------|
| Active mode          |  | 76 mA                       |
| RX mode              |  | 58 mA                       |
| Inactive mode        | xtal active = 0; $V_{REG}$ enable = 0; note 1                | <10 $\mu$ A                 |
|                      | xtal active = 1; $V_{REG}$ enable = 0; Xtal high = 0; note 1 | 230 $\mu$ A                 |
|                      | xtal active = 1; $V_{REG}$ enable = 0; Xtal high = 1; note 1 | 330 $\mu$ A                 |
|                      | xtal active = 1; $V_{REG}$ enable = 1; Xtal high = 1; note 1 | 550 $\mu$ A                 |
|                      | xtal active = 1; $V_{REG}$ enable = 1; Xtal high = 0; note 2 | 690 $\mu$ A                 |

**Notes**

1. Voltage doubler and clock output buffer disabled.
2. Voltage doubler enabled, clock output buffer disabled.

**Table 4** Examples of additional current consumption

$V_{CC} = 3.3$  V;  $T_{amb} = 25$  °C;  $f_{(i)xtal} = 10.24$  MHz;  $C_{L(CLKOUT)} = 14$  pF.

| DIVIDER RATIO       | CURRENT CONSUMPTION ADDITIONAL TO TYPICAL VALUE |                |
|---------------------|---|----------------|
|                     | CLKO level = 0                                  | CLKO level = 1 |
| 1, 2, 2.5, 4 or 128 | 770 $\mu$ A                                     | 530 $\mu$ A    |
| off                 | 0   | 0              |

**7.2 FM receiver**

The FM receiver (see Fig.3) has a single frequency conversion architecture with integrated image rejection mixer that makes an external RF filter unnecessary. The Side Band Select (SBS) feature allows choice of frequency for RXLO to be in or out of the ISM band allowing use of the same IC type for both base station and handset. IF channel filtering (a compromise between price and performance) can be implemented simply using two or three external 10.7 MHz filters. The integrated FM PLL demodulator with limiter decreases significantly the number of pins and external components required.

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FCA295

Fig.3 FM receiver block diagram.

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7.2.1 DATA COMPARATOR

The data comparator is an inverting hysteresis comparator. An external bandpass filter is connected between pins DETO and DATI (AC-coupled). The open-collector output is current limited to control the output signal slew rate. An external resistor of 180 kΩ should be connected between pin DATO and V<sub>CC</sub>. An external capacitor in parallel with this resistor will reduce the slew rate.

7.3 Transmitter

The transmitter architecture is of the direct modulation type. The transmit VCO can be frequency modulated by speech or data (see Fig.4). An amplifier sums the modulating signal with the data TX signal before the VCO. Frequency control is affected by integrated variable capacitance diodes. To obtain the correct frequency, external inductors in series with the bonding wires and leadframe are required. The power amplifier is capable of driving a 50 Ω load. The level of the output signal PAO is programmed with two bits via the serial bus interface.

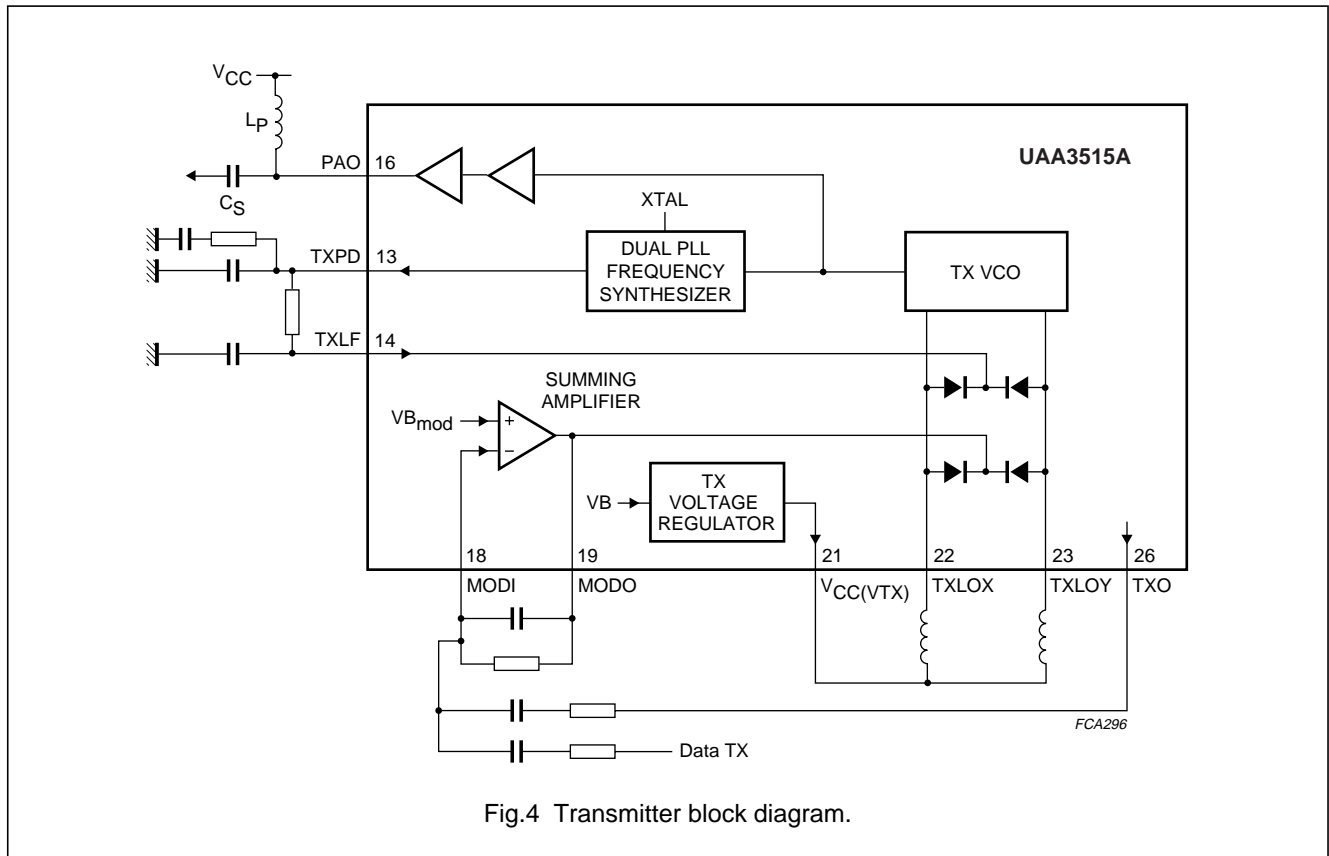


Fig.4 Transmitter block diagram.

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## 7.4 Synthesizer

The crystal local oscillator and reference divider (see Fig.5) provide the reference frequency for the RX and TX PLLs. The 10-bit reference divider is programmed with respect to the crystal frequency and the desired RX and TX frequencies. The microcontroller operating frequency of 4.096 MHz is derived from a 16.384 MHz crystal frequency. The clock divider ratio can be programmed to 1, 2, 2.5, 4 or to 128; ratio 128 is chosen in sleep mode to save current in the microcontroller section. Clock output (pin CLKOUT) is an emitter follower output.

The 16-bit TX counter is programmed for the desired transmit channel frequency. Similarly, the 16-bit RX counter is programmed for the desired local oscillator frequency. The divider counter comprises a 6-bit prescaler with division ratios (R) from 64 to 127, and a 10-bit CMOS divider with division ratios (C) from 8 to 1023. The full counter provides division ratios from 512 to 65535. Settings of RX and TX counters are calculated as follows:

$$C = \text{int} \frac{M}{64}$$

$$R = M - C \times 64$$

(where M is the division ratio between VCO frequency and the reference frequency).

## 7.4.1 CALCULATION EXAMPLE

Given:

RF input frequency  $f_{i(RF)} = 903 \text{ MHz}$

VCO RX  $f_{VCO(RX)} = 892.3 \text{ MHz}$

$f_{IF} = 10.7 \text{ MHz}$

VCO TX  $f_{VCO(TX)} = 925.6 \text{ MHz}$

Internal comparison frequency = 20 kHz  
( $f_{XTAL} = 10.24 \text{ MHz}$ )

We have:

Reference divider = 512 (1000000000)

$$M_{RX} = \frac{892.3 \times 10^6}{20 \times 10^3} = 44615$$

C RX = 697 (1010111001) and R RX = 7 (000111)

and

$$M_{TX} = \frac{925.6 \times 10^6}{20 \times 10^3} = 46280$$

C TX = 723 (1011010011) and R TX = 8 (001000)

VCOs and variable capacitance diodes are integrated. Resonance inductors are shared between bonding wires, leadframe of the package and external inductors. Costs can be reduced by etching external inductors directly onto the printed-circuit board.

An on-chip selectable voltage doubler is provided to enable a larger tuning range of both VCOs. The phase detectors have current drive type outputs with selection possibilities between 400 and 800  $\mu\text{A}$ .

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Fig.5 Synthesizer block diagram.

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## 7.5 Receiver baseband

This section covers the RX audio path from pins RXAI to EARO (see Fig.6). The RXAI input signal is AC-coupled.

The microcontroller sets the value of the RX gain in 32 linear steps of 0.5 dB. The RX baseband has a mute function and an expander with characteristics as shown in Fig.7.

For audio level adjustment and, potentially for software volume control, setting the RX gain provides a dynamic range of 31 dB. This is achieved by the expander slope that multiplies the RX gain by a factor of two for each gain step thus giving 1 dB steps measured at the earpiece amplifier output.

The earpiece amplifier is a rail-to-rail inverting operational amplifier. The non-inverting input is connected to the internal reference voltage at pin VB. Software volume control on the earpiece amplifier is achieved by using an integrated switched feedback resistor  $R_{int}$ . The volume control tuning range is 14 dB. Hardware volume control is achieved by switching externally the earpiece feedback resistor  $R_{ext}$ .



Fig.6 RX baseband block diagram.

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**7.6 TX baseband**

This section covers the TX audio path from pins MIC1 to TXO (see Fig.8). The input signal at pin MIC1 is AC-coupled. There is another AC-coupling at the microphone amplifier output.

The microphone amplifier is an inverting operational amplifier whose gain can be set by external resistors. The non-inverting input is connected to the internal reference voltage VB. External resistors are used to set the gain and frequency response.

The TX baseband has a compressor with the characteristic shown in Fig.9. The ALC provides a 'soft' limit to the output signal swing as the input voltage increases slowly (i.e. a sine wave is maintained at the output). A hard limiter clamps the compressor output voltage at 1.26 V (peak-to-peak). The ALC and the hard limiter can be disabled via the microcontroller interface. The hard limiter is followed by a mute circuit. The TX gain is digitally programmable in 32 steps of 0.5 dB.

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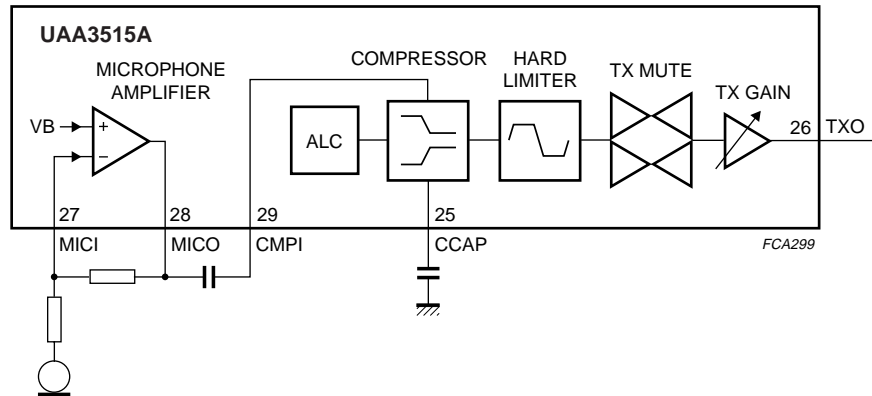
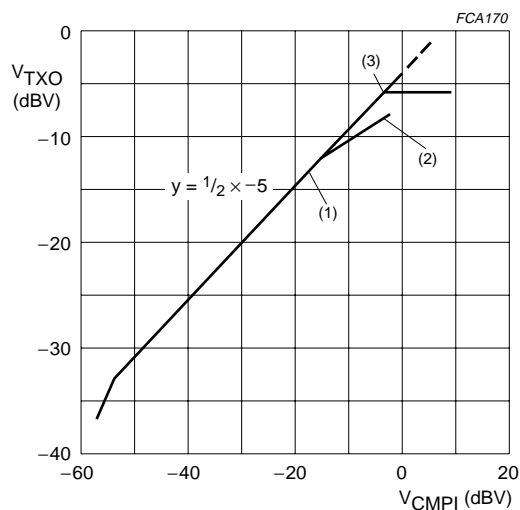


Fig.8 TX baseband block diagram.



- (1) Slowly changing ALC signals:  
 $V_{CPMI} = -16$  dBV;  
 $V_{TXO} = -13$  dBV.
- (2)  $V_{CPMI} = -2.5$  dBV;  
 $V_{TXO} = -11.5$  dBV.
- (3) Hard limiting signals:  
 $V_{CPMI} = -4$  dBV;  
 $V_{TXO} = -1.26$  V (p-p).

Fig.9 Compressor characteristic showing TXO as a function of CMPI.



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### 7.7 Voltage regulator

Pin  $V_{REG}$  provides the internal supply voltage for the RX and TX PLLs. It is regulated at 2.7 V nominal voltage. Two capacitors of 4.7  $\mu$ F and 100 nF must be connected to pin  $V_{REG}$  to filter and stabilize this regulated voltage. The tolerance of the regulated voltage is initially  $\pm 8\%$  but is improved to  $\pm 2\%$  after the internal bandgap voltage reference is adjusted through the microcontroller.

### 7.8 Low-battery detection

The low-battery detector measures the voltage level of the  $V_{CC}$  using a resistance divider and a comparator. One input of the comparator is connected to VB, the other to the middle point of the resistance divider. The comparator has a built-in hysteresis to prevent spurious switching. The precision of the detection depends on the divider accuracy, the comparator offset and the accuracy of the reference voltage VB. The output is multiplexed at pin CDLBD. When the battery voltage level is under the threshold voltage the output CDLBD is going LOW.

### 7.9 Microcontroller interface

The DATA, CLK and EN pins provide a 3-wire unidirectional serial interface for programming the reference counters, the transmit and receive channel divider-counters and the control functions.

The interface consists of 19-bit shift registers connected to a matrix of registers organized as 7 words of 16 bits (all are control registers). The leading 16 bits include the data D15 to D0. The trailing 3 bits set up the address AD2 to AD0. The data is entered with the most significant bit D15 first and the last bit is AD0.

Pins DATA and CLK are used to load data into the shift register. Figure 10 shows the timing required on all pins. Data is clocked into the shift registers on negative clock transitions.

A new clock divider ratio is enabled using an extra EN rising edge. Minimum hold time is 50 ns and during this time no clock cycle is allowed. These extra EN edges can be applied to all the data programmed but will have no effect on the serial interface programming.

The pins DATA, CLK and EN are supplied by  $V_{REG}$ . The ESD protection diodes on these pins are connected to  $V_{CC}$ .

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## 7.9.1 DATA REGISTERS

Table 5 shows the data latches and addresses that select each of the registers; bit D15 is the MSB, this is written and loaded first.

**Table 5** Data register addresses: note 1

| ADDR | D15                                    | D14                    | D13    | D12                    | D11                      | D10                               | D9 | D8 | D7                 | D6                  | D5                  | D4                         | D3                       | D2                 | D1     | D0 |
|------|--|------------------------|--------|------------------------|--------------------------|-----------------------------------|----|----|--------------------|---------------------|---------------------|----------------------------|--------------------------|--------------------|--------|----|
| 000  | SBS                                    | VCTL[1 and 0]          |        | ear piece enable       | RX gain control [4 to 0] |                                   |    |    |                    | SFS                 | DATA phase          | FM PLL VCO tuning [4 to 0] |                          |                    |        |    |
| 001  | RX prescaler [5 to 0]                  |                        |        |                        |                          | RX main divider [9 to 0]          |    |    |                    |                     |                     |                            |                          |                    |        |    |
| 010  | note 2                                 |                        |        |                        |                          | reference divider [9 to 0]        |    |    |                    |                     |                     |                            |                          |                    |        |    |
| 011  | TX prescaler [5 to 0]                  |                        |        |                        |                          | TX main divider [9 to 0]          |    |    |                    |                     |                     |                            |                          |                    |        |    |
| 100  | note 2                                 | CLKO level             | note 2 | doubler enable         | TX gain control [4 to 0] |                                   |    |    |                    | TX mute             | hard limiter enable | ALC disable                | Xtal active              | RX mute            | note 2 |    |
| 101  | V <sub>REG</sub> enable <sup>(3)</sup> | active modes [1 and 0] |        | Xtal high              | CD levels [4 to 0]       |                                   |    |    |                    | LBD levels [2 to 0] |                     |                            | LBD active               | clock div [2 to 0] |        |    |
| 110  | PA output [2 to 0]                     |                        |        | TX charge pump current | RX charge pump current   | voltage reference adjust [2 to 0] |    |    | test mode [2 to 0] |                     |                     | note 2                     | Xtal tuning cap [3 to 0] |                    |        |    |

**Notes**

1. With a 10 kΩ pull-up resistor connected to pin EN or the microcontroller, guarantees that  $V_{IH} > 0.9V_{CC}$  for the EN signal
2. Undefined zone; should always be programmed with 0.
3. In the inactive mode programming V<sub>REG</sub> enable from 1 to 0 might reset all of the registers. We therefore recommend that this register be set to 1 and not to change it.

**Table 6** Data register default values at power-on (undefined zones shown programmed with 0)

| ADDR | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|------|-----|-----|-----|-----|-----|-----|----|----|----|----|----|----|----|----|----|----|
| 000  | 0   | 0   | 0   | 0   | 0   | 1   | 1  | 1  | 1  | 1  | 0  | 0  | 1  | 1  | 1  | 1  |
| 001  | 0   | 0   | 0   | 0   | 0   | 1   | 0  | 0  | 1  | 1  | 0  | 1  | 1  | 0  | 1  | 0  |
| 010  | 0   | 0   | 0   | 0   | 0   | 0   | 0  | 1  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |
| 011  | 0   | 0   | 1   | 0   | 0   | 0   | 0  | 0  | 1  | 1  | 1  | 0  | 0  | 0  | 1  | 0  |
| 100  | 0   | 0   | 0   | 0   | 0   | 1   | 1  | 1  | 1  | 1  | 0  | 0  | 1  | 1  | 0  | 0  |
| 101  | 0   | 0   | 1   | 1   | 0   | 0   | 0  | 0  | 0  | 0  | 0  | 0  | 1  | x  | x  | x  |
| 110  | 0   | 1   | 0   | 0   | 0   | 0   | 1  | 1  | 0  | 0  | 0  | 0  | 0  | 1  | 1  | 1  |

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**Table 7** Data register content description

| DATA REGISTER NAME            | BIT | DESCRIPTION  |
|-------------------------------|-----|--|
| SBS <sup>(1)</sup>            | 1   | sideband select: (LO + IF) frequency is rejected   |
|                               | 0   | sideband select: (LO – IF) frequency is rejected   |
| SFS                           | 1   | second filter select: the second IF filter is selected                                       |
|                               | 0   | second filter select: the second IF filter is deselected; note 2                             |
| CLKO level <sup>(3)</sup>     | 1   | clock output signal is regulated with respect to $V_{REG}$ ; $V_{CLKOUT(p-p)} = 1\text{ V}$  |
|                               | 0   | clock output signal is regulated with respect to $V_{CC}$ ; $V_{CLKOUT(p-p)} = 1.4\text{ V}$ |
| Xtal active                   | 1   | crystal oscillator is active   |
|                               | 0   | crystal oscillator is disable  |
| Xtal high <sup>(4)</sup>      | 1   | oscillator is in normal operation  |
|                               | 0   | oscillator is in low current consumption mode  |
| DATA phase <sup>(5)</sup>     | 1   | DATA signal is inverted  |
|                               | 0   | DATA signal is not inverted (inverter bypassed)  |
| ALC disable                   | 1   | ALC disabled   |
|                               | 0   | normal operation   |
| Hard limiter enable           | 1   | hard limiter enabled   |
|                               | 0   | hard limiter disabled  |
| RX mute                       | 1   | RX channel muted   |
|                               | 0   | normal operation   |
| TX mute                       | 1   | TX channel muted   |
|                               | 0   | normal operation   |
| $V_{REG}$ enable              | 1   | $V_{REG}$ enabled  |
|                               | 0   | $V_{REG}$ disabled and tied to $V_{CC}$ (in inactive mode)                                   |
| Doubler enable <sup>(6)</sup> | 1   | voltage doubler is enabled   |
|                               | 0   | voltage doubler is disabled  |
| Earpiece enable               | 1   | earpiece enabled (can be used in RX mode for specific features)                              |
|                               | 0   | earpiece disabled  |

**Notes**

- Sideband select enables the user to have the RX local oscillator in or out of the ISM band and to use the same IC in both handset and base.
- A 4.5 dB insertion loss in the filter is assumed.
- The clock output signal will be AC-coupled with the XTALI pin of the microcontroller. The external resonator from the microcontroller can be removed. Caution needs to be taken that no radiation is present on the PCB
- In inactive mode, the crystal oscillator is a major contributor to the full current consumption. When Xtal high = 0, the current mode can be programmed to save current and in inactive mode this comes to full current consumption at 230  $\mu\text{A}$  (see Section 7.1.3). When Xtal high = 1, the crystal oscillator current is increased by 100  $\mu\text{A}$ .
- Depending on the SBS-bit and the protocol chosen, the data may be inverted between the base and handset data transmission.
- Minimum supply voltage for the IC is 2.9 V which limits the voltage swing on both charge pumps to approximately 2.3 V. With the voltage doubler or with an external high supply voltage on pin  $V_{CC(CP)}$ , the extra voltage availability can be used to enhance the tuning range of the VCOs variable capacitance diodes. To save current in inactive mode, voltage doubler clock is the same as CLKO clock (can be programmed to  $\frac{XTAL}{128}$ ); in other modes the voltage doubler clock is XTALI divided by two.

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## 7.9.2 ACTIVE MODES

**Table 8** Active mode bit selection; note 1

| BIT 1 | BIT 0 | DESCRIPTION   |
|-------|-------|---------------|
| 0     | X     | inactive mode |
| 1     | 0     | RX mode       |
| 1     | 1     | active mode   |

**Note**

1. See details on activated blocks in Section 7.1.2.

## 7.9.3 CLOCK OUTPUT DIVIDER

The crystal oscillator produces a reference frequency that is divided and buffered to drive a microcontroller. Table 9 gives the division ratios. The buffer is a CMOS output which can drive up to 20 pF at 10 MHz in both CLKO level modes.

**Table 9** Clock division register

| BIT 2 | BIT 1 | BIT 0 | SELECT | CLOCK DIVISION RATIO |
|-------|-------|-------|--------|----------------------|
| 0     | 0     | 0     | 0      | output disabled      |
| 0     | 0     | 1     | 1      | 2                    |
| 0     | 1     | 0     | 2      | 2.5                  |
| 0     | 1     | 1     | 3      | 4                    |
| 1     | 0     | 0     | 4      | 1                    |
| 1     | 0     | 1     | 5      | 128                  |

When the clock output signal is used, an external RC filter connected to pin CLKOUT can be added to limit clock waveform edges and therefore clock radiation on the printed-circuit board.

To supply the clock to the microcontroller and save current in the handset, an external low power resonator may be used and the clock output disabled (000) as well as the crystal oscillator (Xtal active = 0). In power saving mode, the divider ratio can be programmed down to 128 to reduce the microcontroller power consumption.

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## 7.9.4 FM-PLL CENTRE FREQUENCY

This register allows the centre frequency of the VCO to be calibrated within the FM PLL to align the frequency as close as possible to the nominal 10.7 MHz frequency.

**Table 10** FM-PLL VCO tuning register

| BIT 4 | BIT 3 | BIT 2 | BIT 1 | BIT 0 | SELECT | CENTRE FREQUENCY SHIFT (MHz) |
|-------|-------|-------|-------|-------|--------|------------------------------|
| 0     | 0     | 0     | 0     | 0     | 0      | 3.0                          |
| 0     | 0     | 0     | 0     | 1     | 1      | 2.8                          |
| 0     | 0     | 0     | 1     | 0     | 2      | 2.6                          |
| 0     | 0     | 0     | 1     | 1     | 3      | 2.4                          |
| 0     | 0     | 1     | 0     | 0     | 4      | 2.2                          |
| 0     | 0     | 1     | 0     | 1     | 5      | 2.0                          |
| 0     | 0     | 1     | 1     | 0     | 6      | 1.8                          |
| 0     | 0     | 1     | 1     | 1     | 7      | 1.6                          |
| 0     | 1     | 0     | 0     | 0     | 8      | 1.4                          |
| 0     | 1     | 0     | 0     | 1     | 9      | 1.2                          |
| 0     | 1     | 0     | 1     | 0     | 10     | 1.0                          |
| 0     | 1     | 0     | 1     | 1     | 11     | 0.8                          |
| 0     | 1     | 1     | 0     | 0     | 12     | 0.6                          |
| 0     | 1     | 1     | 0     | 1     | 13     | 0.4                          |
| 0     | 1     | 1     | 1     | 0     | 14     | 0.2                          |
| 0     | 1     | 1     | 1     | 1     | 15     | 0                            |
| 1     | 0     | 0     | 0     | 0     | 16     | -0.2                         |
| 1     | 0     | 0     | 0     | 1     | 17     | -0.4                         |
| 1     | 0     | 0     | 1     | 0     | 18     | -0.6                         |
| 1     | 0     | 0     | 1     | 1     | 19     | -0.8                         |
| 1     | 0     | 1     | 0     | 0     | 20     | -1.0                         |
| 1     | 0     | 1     | 0     | 1     | 21     | -1.2                         |
| 1     | 0     | 1     | 1     | 0     | 22     | -1.4                         |
| 1     | 0     | 1     | 1     | 1     | 23     | -1.6                         |
| 1     | 1     | 0     | 0     | 0     | 24     | -1.8                         |
| 1     | 1     | 0     | 0     | 1     | 25     | -2.0                         |
| 1     | 1     | 0     | 1     | 0     | 26     | -2.2                         |
| 1     | 1     | 0     | 1     | 1     | 27     | -2.4                         |
| 1     | 1     | 1     | 0     | 0     | 28     | -2.6                         |
| 1     | 1     | 1     | 0     | 1     | 29     | -2.8                         |
| 1     | 1     | 1     | 1     | 0     | 30     | -3.0                         |
| 1     | 1     | 1     | 1     | 1     | 31     | -3.2                         |

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## 7.9.5 TX AND RX GAIN CONTROL REGISTERS

The TX and RX audio signal paths each have a programmable gain block. If a TX or RX voltage gain other than the nominal power-up default is desired it can be programmed through the microcontroller interface. The gain blocks can be used during final telephone testing to adjust electronically gain tolerances in the telephone system. The RX gain and the TX gain controls have steps of 0.5 dB covering a dynamic range of  $-7.5$  to  $+8.0$  dB. Measured on the earpiece amplifier output, RX gain steps are multiplied by 2 due to the expander slope. A dynamic range of  $-15$  to  $+16$  dB at the earpiece amplifier supports a volume control feature that can be implemented in the telephone and compensate for gain tolerances. Volume control can also be performed externally with hardware switches on various resistor values.

**Table 11** RX and TX gain control registers

| BIT 4 | BIT 3 | BIT 2 | BIT 1 | BIT 0 | GAIN CONTROL | RX GAIN (dB) | EARO (dB) | TX GAIN (dB) |
|-------|-------|-------|-------|-------|--------------|--------------|-----------|--------------|
| 0     | 0     | 0     | 0     | 0     | 0            | -7.5         | -15.0     | -7.5         |
| 0     | 0     | 0     | 0     | 1     | 1            | -7.0         | -14.0     | -7.0         |
| 0     | 0     | 0     | 1     | 0     | 2            | -6.5         | -13.0     | -6.5         |
| 0     | 0     | 0     | 1     | 1     | 3            | -6.0         | -12.0     | -6.0         |
| 0     | 0     | 1     | 0     | 0     | 4            | -5.5         | -11.0     | -5.5         |
| 0     | 0     | 1     | 0     | 1     | 5            | -5.0         | -10.0     | -5.0         |
| 0     | 0     | 1     | 1     | 0     | 6            | -4.5         | -9.0      | -4.5         |
| 0     | 0     | 1     | 1     | 1     | 7            | -4.0         | -8.0      | -4.0         |
| 0     | 1     | 0     | 0     | 0     | 8            | -3.5         | -7.0      | -3.5         |
| 0     | 1     | 0     | 0     | 1     | 9            | -3.0         | -6.0      | -3.0         |
| 0     | 1     | 0     | 1     | 0     | 10           | -2.5         | -5.0      | -2.5         |
| 0     | 1     | 0     | 1     | 1     | 11           | -2.0         | -4.0      | -2.0         |
| 0     | 1     | 1     | 0     | 0     | 12           | -1.5         | -3.0      | -1.5         |
| 0     | 1     | 1     | 0     | 1     | 13           | -1.0         | -2.0      | -1.0         |
| 0     | 1     | 1     | 1     | 0     | 14           | -0.5         | -1.0      | -0.5         |
| 0     | 1     | 1     | 1     | 1     | 15           | 0            | 0         | 0            |
| 1     | 0     | 0     | 0     | 0     | 16           | 0.5          | 1.0       | 0.5          |
| 1     | 0     | 0     | 0     | 1     | 17           | 1.0          | 2.0       | 1.0          |
| 1     | 0     | 0     | 1     | 0     | 18           | 1.5          | 3.0       | 1.5          |
| 1     | 0     | 0     | 1     | 1     | 19           | 2.0          | 4.0       | 2.0          |
| 1     | 0     | 1     | 0     | 0     | 20           | 2.5          | 5.0       | 2.5          |
| 1     | 0     | 1     | 0     | 1     | 21           | 3.0          | 6.0       | 3.0          |
| 1     | 0     | 1     | 1     | 0     | 22           | 3.5          | 7.0       | 3.5          |
| 1     | 0     | 1     | 1     | 1     | 23           | 4.0          | 8.0       | 4.0          |
| 1     | 1     | 0     | 0     | 0     | 24           | 4.5          | 9.0       | 4.5          |
| 1     | 1     | 0     | 0     | 1     | 25           | 5.0          | 10.0      | 5.0          |
| 1     | 1     | 0     | 1     | 0     | 26           | 5.5          | 11.0      | 5.5          |
| 1     | 1     | 0     | 1     | 1     | 27           | 6.0          | 12.0      | 6.0          |
| 1     | 1     | 1     | 0     | 0     | 28           | 6.5          | 13.0      | 6.5          |
| 1     | 1     | 1     | 0     | 1     | 29           | 7.0          | 14.0      | 7.0          |
| 1     | 1     | 1     | 1     | 0     | 30           | 7.5          | 15.0      | 7.5          |
| 1     | 1     | 1     | 1     | 1     | 31           | 8.0          | 16.0      | 8.0          |

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## 7.9.6 CARRIER DETECTOR THRESHOLD PROGRAMMING

When the LBD active register = 0, the carrier detector is enabled and the signal CDout is sent to the output pin CDLBD. If RSSI is above the programmed RSSI level, CDLBD = 0; if RSSI is below the programmed level then CDLBD = 1. The carrier detector gives an indication if a carrier signal is present on the selected channel. The carrier detector has a nominal value and tolerance, if a different carrier detect threshold value is desired, this can be programmed through the microcontroller interface. If the carrier detect range is to be scaled, an external resistor should be connected between pin RSSI and ground. CD control = 10011 which corresponds to RSSI = 0.86 V (typical DC value).

**Table 12** CD levels register

| BIT 4 | BIT 3 | BIT 2 | BIT 1 | BIT 0 | SELECT | RSSI VOLTAGE THRESHOLD DETECT (V) |
|-------|-------|-------|-------|-------|--------|-----------------------------------|
| 0     | 0     | 0     | 0     | 0     | 0      | 0.1                               |
| 0     | 0     | 0     | 0     | 1     | 1      | 0.14                              |
| 0     | 0     | 0     | 1     | 0     | 2      | 0.18                              |
| 0     | 0     | 0     | 1     | 1     | 3      | 0.22                              |
| 0     | 0     | 1     | 0     | 0     | 4      | 0.26                              |
| 0     | 0     | 1     | 0     | 1     | 5      | 0.3                               |
| 0     | 0     | 1     | 1     | 0     | 6      | 0.34                              |
| 0     | 0     | 1     | 1     | 1     | 7      | 0.38                              |
| 0     | 1     | 0     | 0     | 0     | 8      | 0.42                              |
| 0     | 1     | 0     | 0     | 1     | 9      | 0.46                              |
| 0     | 1     | 0     | 1     | 0     | 10     | 0.5                               |
| 0     | 1     | 0     | 1     | 1     | 11     | 0.54                              |
| 0     | 1     | 1     | 0     | 0     | 12     | 0.58                              |
| 0     | 1     | 1     | 0     | 1     | 13     | 0.62                              |
| 0     | 1     | 1     | 1     | 0     | 14     | 0.66                              |
| 0     | 1     | 1     | 1     | 1     | 15     | 0.7                               |
| 1     | 0     | 0     | 0     | 0     | 16     | 0.74                              |
| 1     | 0     | 0     | 0     | 1     | 17     | 0.78                              |
| 1     | 0     | 0     | 1     | 0     | 18     | 0.82                              |
| 1     | 0     | 0     | 1     | 1     | 19     | 0.86                              |
| 1     | 0     | 1     | 0     | 0     | 20     | 0.9                               |
| 1     | 0     | 1     | 0     | 1     | 21     | 0.94                              |
| 1     | 0     | 1     | 1     | 0     | 22     | 0.98                              |
| 1     | 0     | 1     | 1     | 1     | 23     | 1.02                              |
| 1     | 1     | 0     | 0     | 0     | 24     | 1.06                              |
| 1     | 1     | 0     | 0     | 1     | 25     | 1.1                               |
| 1     | 1     | 0     | 1     | 0     | 26     | 1.14                              |
| 1     | 1     | 0     | 1     | 1     | 27     | 1.18                              |
| 1     | 1     | 1     | 0     | 0     | 28     | 1.22                              |
| 1     | 1     | 1     | 0     | 1     | 29     | 1.26                              |
| 1     | 1     | 1     | 1     | 0     | 30     | 1.3                               |
| 1     | 1     | 1     | 1     | 1     | 31     | 1.34                              |



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## 7.9.7 LOW-BATTERY DETECTION

When the LBD active register = 1, the low battery detector is enabled and the signal BDout passes to the output CDLBD. If  $V_{CC}$  is below the programmed LBD level, CDLBD = 0; if not below the programmed level, CDLBD = 1. The power-up default value is 110.

**Table 13** LBD level register

| BIT 2 | BIT 1 | BIT 0 | SELECT | LOW BATTERY VOLTAGE DETECTION; NOMINAL VALUE (V) |
|-------|-------|-------|--------|--|
| 0     | 0     | 0     | 0      | 3.5  |
| 0     | 0     | 1     | 1      | 3.4  |
| 0     | 1     | 0     | 2      | 3.3  |
| 0     | 1     | 1     | 3      | 3.2  |
| 1     | 0     | 0     | 4      | 3.1  |
| 1     | 0     | 1     | 5      | 3.0  |
| 1     | 1     | 0     | 6      | 2.9  |
| 1     | 1     | 1     | 7      | 2.8  |

## 7.9.8 POWER AMPLIFIER OUTPUT LEVEL

The power amplifier output register has two bits to modify the output power and one bit to disable the power amplifier (PA output bit 2 = 0). Duplexer matching ( $300\ \Omega$  to  $50\ \Omega$ ) is performed using a parallel inductive/series capacitive network. Output power on  $50\ \Omega$  is specified in Table 14. To get power on the antenna, duplexer insertion loss should be removed. At maximum power, 3 mA extra DC current is consumed compared with the current at the minimum power settings.

**Table 14** PA output register

| BIT 2 | BIT 1 | BIT 0 | SELECT | PA OUTPUT POWER (dBm) | 2nd HARMONIC (dBm) | 3rd HARMONIC (dBm) | 4th HARMONIC (dBm) |
|-------|-------|-------|--------|-----------------------|--------------------|--------------------|--------------------|
| 0     | X     | X     | –      | PA inactive           | –                  | –                  | –                  |
| 1     | 0     | 0     | 0      | 1.0                   | –17                | –327               | –34                |
| 1     | 0     | 1     | 1      | 1.9                   | –19                | –29                | –34                |
| 1     | 1     | 0     | 2      | 2.5                   | –23                | –33                | –36                |
| 1     | 1     | 1     | 3      | 3.1                   | –23                | –36                | –40                |

## 7.9.9 PLL CHARGE PUMP CURRENT

Performance of the PLLs can be improved by increasing charge pump current. Then a programmable current on both RX and TX charge pump can be programmed. RX and TX charge pump currents are programmed independently. When the RX or TX charge pump current register = 0, charge pump current is  $400\ \mu\text{A}$ ; when it is set to 1, charge pump current is  $800\ \mu\text{A}$ .

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## 7.9.10 VOLUME CONTROL

The register VCTL enables the volume control of the earpiece amplifier to be set to a predefined gain. This is achieved by switched feedback resistor  $R_{int}$ . The optional resistor  $R_{ext}$ , connected between pins EARI and EARO provides the hardware control.

**Table 15** Volume control bit selection

| BIT 1 | BIT 0 | $R_{int}$ (k $\Omega$ ) | $R_{ext}$ (k $\Omega$ ) | $G_{EAR}$ (dB) |
|-------|-------|-------------------------|-------------------------|----------------|
| 0     | 0     | 14                      | none                    | 0              |
| 0     | 1     | 24                      | none                    | 4.7            |
| 1     | 0     | 41                      | none                    | 9.3            |
| 1     | 1     | 70.2                    | none                    | 14             |
| 1     | 1     | 70.2                    | 100                     | 9.4            |
| 1     | 1     | 70.2                    | 33                      | 4.1            |
| 1     | 1     | 70.2                    | 15                      | -1             |

## 7.9.11 CRYSTAL TUNING CAPACITORS

On-chip crystal reference tuning is provided to compensate for frequency spread over process and temperature changes. An external capacitor should be connected at pin XTALI; the value of the capacitor should be approximately 3 pF less than the capacitance of pin XTALO. Internally, a programmable capacitance is available in parallel with the XTALI pin. Tuning capacitance values are in the range 0 to 4.5 pF; see Table 16.

**Table 16** Xtal tuning cap register

| BIT 3 | BIT 2 | BIT 1 | BIT 0 | SELECT | CAPACITANCE (pF) |
|-------|-------|-------|-------|--------|------------------|
| 0     | 0     | 0     | 0     | 0      | 0.2              |
| 0     | 0     | 0     | 1     | 1      | 0.5              |
| 0     | 0     | 1     | 0     | 2      | 0.8              |
| 0     | 0     | 1     | 1     | 3      | 1.1              |
| 0     | 1     | 0     | 0     | 4      | 1.4              |
| 0     | 1     | 0     | 1     | 5      | 1.7              |
| 0     | 1     | 1     | 0     | 6      | 2.0              |
| 0     | 1     | 1     | 1     | 7      | 2.3              |
| 1     | 0     | 0     | 0     | 8      | 2.6              |
| 1     | 0     | 0     | 1     | 9      | 2.9              |
| 1     | 0     | 1     | 0     | 10     | 3.2              |
| 1     | 0     | 1     | 1     | 11     | 3.5              |
| 1     | 1     | 0     | 0     | 12     | 3.8              |
| 1     | 1     | 0     | 1     | 13     | 4.1              |
| 1     | 1     | 1     | 0     | 14     | 4.4              |
| 1     | 1     | 1     | 1     | 15     | 4.7              |

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## 7.9.12 VOLTAGE REFERENCE ADJUSTMENT

An internal 1.5 V bandgap voltage reference provides the voltage reference for the low battery detect circuits, the  $V_{REG}$  voltage regulator, the  $V_B$  reference and all internal analog references. In inactive mode, the adjustment is disabled.

**Table 17** Voltage reference adjust register

| BIT 2 | BIT 1 | BIT 0 | SELECT | NOMINAL VOLTAGE REFERENCE |
|-------|-------|-------|--------|---------------------------|
| 0     | 0     | 0     | 0      | -7%                       |
| 0     | 0     | 1     | 1      | -5%                       |
| 0     | 1     | 0     | 2      | -3%                       |
| 0     | 1     | 1     | 3      | -1%                       |
| 1     | 0     | 0     | 4      | 1%                        |
| 1     | 0     | 1     | 5      | 3%                        |
| 1     | 1     | 0     | 6      | 5%                        |
| 1     | 1     | 1     | 7      | 7%                        |

## 7.9.13 TEST MODE

Test mode bits are used only for test in production and application tuning. The test bits must be set to 0 for normal operation. Out-of-lock of synthesizers RX or TX can be monitored indirectly on pin CDLBD: the width of the 'glitch' that occurs with out-of-lock gives a direct indication of the phase error on the PLL RX and/or TX. To tune the external inductors of the RX and TX VCOs, a defined division ratio has to be programmed into the dividers, and then the image frequency of the VCO can be read on pin CDLBD. Test mode can also be used to check the division ratio: a frequency can be forced on the VCO or crystal pins and the programmed frequency can be read on pin CDLBD. There is a divide-by-2 stage before the CDLBD pin, therefore all frequencies are divided-by-2. When both charge pumps are in the high-impedance state, the VCOs can be measured as stand alone.

**Table 18** Test mode register

| BIT 2 | BIT 1 | BIT 0 | SELECT  |
|-------|-------|-------|---|
| 0     | 0     | 0     | normal operation  |
| 0     | 0     | 1     | XOR between internal signals 'up' and 'down' of the RX synthesizer        |
| 0     | 1     | 0     | XOR between internal signals 'up' and 'down' of the TX synthesizer        |
| 0     | 1     | 1     | XOR between internal signals 'up' and 'down' of the RX or TX synthesizers |
| 1     | 0     | 0     | reference divider output divided by 2                                     |
| 1     | 0     | 1     | prescaler and main divider RX divided by 2                                |
| 1     | 1     | 0     | prescaler and main divider TX divided by 2                                |
| 1     | 1     | 1     | both synthesizer charge pumps are in high-impedance-state                 |

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**8 LIMITING VALUES**

In accordance with the Absolute Maximum Rating System (IEC 60134).

| SYMBOL    | PARAMETER           | MIN. | MAX. | UNIT |
|-----------|---------------------|------|------|------|
| $V_{CC}$  | supply voltage      | -0.3 | +6.0 | V    |
| $T_{stg}$ | storage temperature | -55  | +125 | °C   |
| $T_{amb}$ | ambient temperature | -20  | +80  | °C   |

**9 HANDLING**

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices. Do not operate or store near strong electrostatic fields.

Meets Class 1 ESD test requirements (human body model) in accordance with "EIA/JESD22-A114-B (June 2001)" and class A ESD test requirements (machine model) in accordance with "EIA/JESD22-A115-B (October 1997)".

**10 THERMAL CHARACTERISTICS**

| SYMBOL        | PARAMETER                                   | CONDITIONS  | VALUE | UNIT |
|---------------|---|-------------|-------|------|
| $R_{th(j-a)}$ | thermal resistance from junction to ambient | in free air | 68    | K/W  |

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## 11 CHARACTERISTICS

$V_{CC} = V_{CC(PS)} = V_{CC(ATX)} = V_{CC(ARX)} = V_{CC(IF)} = V_{CC(BLO)} = V_{CC(MIX)} = V_{CC(LNA)} = 3.3 \text{ V}$ ;  $T_{amb} = 25 \text{ }^\circ\text{C}$ ; unless otherwise specified.

| SYMBOL   | PARAMETER   | CONDITIONS   | MIN.                    | TYP.                          | MAX.                    | UNIT             |
|--|---|--|-------------------------|-------------------------------|-------------------------|------------------|
| <b>Supplies</b>  |   |  |                         |                               |                         |                  |
| $V_{CC}$   | positive supply voltage to pins $V_{CC(PS)}$ ; $V_{CC(ATX)}$ ; $V_{CC(ARX)}$ ; $V_{CC(IF)}$ ; $V_{CC(BLO)}$ ; $V_{CC(MIX)}$ ; $V_{CC(LNA)}$ |  | 2.9                     | 3.3                           | 5.5                     | V                |
| <b>PLL VOLTAGE REGULATOR</b>   |   |  |                         |                               |                         |                  |
| $V_{O(VREG)}$  | regulated output voltage  | $V_{REG} \text{ enable} = 0$<br>$V_{REG} \text{ enable} = 1$<br>inactive mode<br>before $V_{ref}$ adjustment<br>after $V_{ref}$ adjustment | –<br>2.5<br>2.5<br>2.65 | $V_{CC}$<br>2.7<br>2.7<br>2.7 | –<br>2.9<br>2.9<br>2.75 | V<br>V<br>V<br>V |
| $I_{O(VREG)}$  | output current  | $C_{VREG} = 1 \mu\text{F}$   | –                       | –                             | 3                       | mA               |
| <b>LOW BATTERY DETECTION: LBD active = 1</b>                                   |   |  |                         |                               |                         |                  |
| $V_{LBD}$  | detection voltage range   |  | 2.8                     | –                             | 3.5                     | V                |
| $\Delta V_{LBD}$   | number of detection voltage steps   |  | –                       | 8                             | –                       | steps            |
| $V_{hys}$  | comparator hysteresis   | $[V_{CC(high)} - V_{CC(low)}] \times \frac{V_{VB}}{V_{th}}$  | –                       | 18                            | –                       | mV               |
| $\Delta V_{CC}/V_{CC}$   | LBD accuracy  | measured after $V_{ref}$ adjusted; LBD = 010   | –                       | 0.5                           | 5                       | %                |
| <b>Receiver section</b>  |   |  |                         |                               |                         |                  |
| <b>LNA AND IMAGE REJECTION MIXER; <math>f_{i(RX)} = 903 \text{ MHz}</math></b> |   |  |                         |                               |                         |                  |
| $R_{i(RX)}$  | RF input resistance   | balanced   | –                       | 110                           | –                       | $\Omega$         |
| $C_{i(RX)}$  | RF input capacitance  | balanced   | –                       | 0.7                           | –                       | pF               |
| $f_{i(RX)}$  | RF input frequency  |  | 902                     | 903                           | 928                     | MHz              |
| $RL_{i(RX)}$   | return loss on match RF input   | note 1   | 10                      | –                             | –                       | dB               |
| $G_{conv(p)(RX)}$  | conversion power gain   | balun input to MIXO pin; matched to $330 \Omega$   | –                       | 22                            | –                       | dB               |
| $CP1_{RX}$   | 1 dB input compression point  | note 1   | –                       | –23                           | –                       | dBm              |
| $IP3_{RX}$   | 3 <sup>rd</sup> order intercept point   |  | –                       | –13                           | –                       | dBm              |
| $NF_{RX}$  | overall noise figure, RF front end  | IF section excluded  | –                       | 4                             | 5                       | dB               |
| IR   | image frequency rejection   | in band of interest  | 26                      | 45                            | –                       | dB               |
| $R_{L(RX)}$  | IF resistive output load  | on pin MIXO  | –                       | 330                           | –                       | $\Omega$         |
| $C_{L(RX)}$  | IF capacitive output load   | on pin MIXO  | –                       | –                             | 3                       | pF               |

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| SYMBOL  | PARAMETER                                    | CONDITIONS   | MIN.   | TYP.           | MAX.     | UNIT       |
|---|--|--|--------|----------------|----------|------------|
| IF AMPLIFIER SECTION: $f_0 = 10.7$ MHz  |  |  |        |                |          |            |
| $G_{IFAMP1}$  | voltage or power gain of first IF amplifier  | 330 $\Omega$ matched input and output; SFS = 1; measured at amplifier output   | –      | 22.5           | –        | dB         |
| $NF_{IFAMP1}$   | noise figure of first IF amplifier           | 330 $\Omega$ matched input and output  | –      | 7              | –        | dB         |
| $G_{IFAMP2}$  | voltage or power gain of second IF amplifier | 330 $\Omega$ matched input and output; SFS = 1; measured at amplifier output   | –      | 25             | –        | dB         |
| $NF_{IFAMP2}$   | noise figure of second IF amplifier          | 330 $\Omega$ matched input and output  | –      | 14             | –        | dB         |
| $G_{IFAMP}$   | gain of IF amplifier section                 | 330 $\Omega$ matched input and output; SFS = 0   | –      | 43             | –        | dB         |
| $NF_{IFAMP}$  | noise figure of IF amplifier section         |  | –      | 7.5            | –        | dB         |
| PLL DEMODULATOR: $f_0 = 10.7$ MHz; $f_{dev} = \pm 25$ kHz; $f_{mod} = 1$ kHz  |  |  |        |                |          |            |
| $\Delta f_{VCO}/\Delta V$   | VCO gain                                     | after calibration  | –      | 760            | –        | kHz/V      |
| $f_{VCO}$   | VCO centre frequency (free running)          | open loop; all conditions  | 7.0    | 10.7           | 15.0     | MHz        |
| $\Delta f_{VCO}$  | VCO frequency adjustment                     | see Table 10   | –      | 32             | –        | steps      |
| $f_{VCO(step)}$   | VCO centre frequency step size               |  | –      | 200            | –        | kHz        |
| $BW_{demod}$  | demodulator –3 dB bandwidth                  | loop filter: see note 2  | 10     | –              | –        | kHz        |
| $f_{dev(max)}$  | maximum frequency deviation                  |  | –      | –              | $\pm 75$ | kHz        |
| $R_{L(DETO)}$   | demodulator external load on pin DETO        |  | 5      | –              | –        | k $\Omega$ |
| $V_{o(DETO)(RMS)}$  | PLL output voltage on pin DETO (RMS value)   | TX mode; $R_{L(DETO)} = 10$ k $\Omega$ ; amplifier gain = 10; note 3   | –      | 100            | 350      | mV         |
| $V_{o(DETO)(DC)}$   | PLL output DC voltage on pin DETO            | microcontroller adjustable DC component  | 1.2    | 1.4            | 1.6      | V          |
| FM RECEIVER: $f_0 = 903$ MHz; $f_{dev} = \pm 25$ kHz; $f_{mod} = 1$ kHz; $R_{L(EARO)} = 150$ $\Omega$ in series with 10 $\mu$ F (all with CCITT filter) |  |  |        |                |          |            |
| $SR_{FI}$   | receiver sensitivity                         | measured at antenna; duplexer insertion loss = 3 dB; input level for 12 dB SINAD; bandwidth = 100 kHz<br>RX mode<br>TX mode; PA = 10;<br>$V_{EARO(RMS)} = 200$ mV;<br>TX to RX duplexer isolation is 35 dB minimum | –<br>– | –115<br>–113.5 | –<br>–   | dBm<br>dBm |

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| SYMBOL                                    | PARAMETER   | CONDITIONS   | MIN.        | TYP.           | MAX.        | UNIT       |
|---|---|--|-------------|----------------|-------------|------------|
| $S/N_{FM}$                                | signal-to-noise ratio                             | TX mode;<br>$V_{i(RF)} = -80$ and $-40$ dBm;<br>PA = 10; CLKO level = 0;<br>$V_{EARO(RMS)} = 200$ mV   | 40          | 45             | –           | dB         |
| $THD_{FM}$                                | total harmonic distortion                         | TX mode; $f_{dev} = \pm 60$ kHz;<br>$V_{i(RF)} = -80$ and $-40$ dBm;<br>PA = 10; CLKO level = 0;<br>$V_{EARO(RMS)} = 500$ mV;<br>measured without CCITT filter | –           | 0.6            | 2           | %          |
| RSSI AND CARRIER DETECTION: $V_B = 1.5$ V |   |  |             |                |             |            |
| RSSI                                      | output current dynamic range                      |  | –           | 68             | –           | dB         |
| $V_{OH}$                                  | HIGH-level output voltage at pin CDLBD            | $V_{i(LIM)(RMS)} = 0$ mV; CD = 10011   | $0.9V_{CC}$ | –              | –           | V          |
| $V_{OL}$                                  | LOW-level output voltage at pin CDLBD             | $V_{i(LIM)} = 0.1$ V (RMS);<br>CD = 10011  | –           | –              | $0.1V_{CC}$ | V          |
| $R_{int}$                                 | internal resistance between pin RSSI and $V_{CC}$ |  | –           | 175            | –           | k $\Omega$ |
| $V_{det}$                                 | voltage detection range                           |  | 0.05        | –              | 1.6         | V          |
| $\Delta V_{det}$                          | voltage detection step                            |  | –           | 40             | –           | mV         |
| $V_{hys}$                                 | hysteresis  |  | –           | 45             | –           | mV         |
| $V_{th(CD)}$                              | carrier sense threshold                           | microcontroller programmable   | –           | 32             | –           | steps      |
| DATA COMPARATOR                           |   |  |             |                |             |            |
| $V_{i(DATC)(p-p)}$                        | comparator input signal (peak-to-peak value)      |  | 100         | –              | –           | mV         |
| $V_{hys(DATC)}$                           | hysteresis  |  | 25          | 40             | 75          | mV         |
| $V_{th(DATC)}$                            | pin DATI threshold voltage                        |  | –           | $V_{CC} - 0.9$ | –           | V          |
| $Z_{i(DATC)}$                             | pin DATI input impedance                          |  | 150         | 240            | –           | k $\Omega$ |
| $V_{OH}$                                  | HIGH-level output voltage                         | $V_{i(DATI)} = V_{CC} - 1.4$ V   | $0.9V_{CC}$ | –              | –           | V          |
| $V_{OL}$                                  | LOW-level output voltage                          | $V_{i(DATI)} = V_{CC} - 0.4$ V   | –           | –              | $0.1V_{CC}$ | V          |
| $I_{OHsink}$                              | pin DATO output sink current                      | $V_{i(DATI)} = V_{CC} - 0.4$ V;<br>$V_{o(DATO)} = 0.1V_{CC}$   | –           | 40             | –           | $\mu$ A    |
| <b>Transmitter section</b>                |   |  |             |                |             |            |
| SUMMING AMPLIFIER                         |   |  |             |                |             |            |
| $V_{o(p-p)}$                              | pin MODO output voltage (peak-to-peak value)      |  | –           | 94             | 240         | mV         |
| $R_{fb}$                                  | external feedback resistor                        | between pins MODI and MODO   | 10          | –              | –           | k $\Omega$ |
| $V_{bias}$                                | pin MODI bias voltage                             |  | –           | 2.2            | –           | V          |

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| SYMBOL   | PARAMETER   | CONDITIONS  | MIN.           | TYP.               | MAX.        | UNIT                           |
|--|---|---|----------------|--------------------|-------------|--------------------------------|
| <b>TX VOLTAGE-CONTROLLED OSCILLATOR AND POWER AMPLIFIER</b>  |   |   |                |                    |             |                                |
| $f_{VCO(TX)}$  | VCO free running frequency                                | note 1  | –              | 910                | –           | MHz                            |
| $Q_{L(VCO)(TX)}$   | quality factor of external inductor                       | $L = 3.9 \text{ nH}$ ;<br>$f_{VCO} = 902 \text{ to } 928 \text{ MHz}$   | 30             | –                  | –           |                                |
| $\frac{\Delta f_{VCO(TX)}}{\Delta V_{TXLF}}$   | VCO gain  | $V_{TXLF} = 0.5 \text{ V}$  | –              | 50                 | –           | MHz/V                          |
|  |   | $V_{TXLF} = 1.5 \text{ V}$  | –              | 25                 | –           | MHz/V                          |
| $\frac{\Delta f_{VCO(TX)}}{\Delta V_{mod}}$  | VCO modulation gain                                       | $V_{MOD0} = 2.2 \text{ V}$  | –              | 530                | –           | kHz/V                          |
| $N_{VCO(TX)}$  | VCO and power amplifier phase noise                       | $P_o = 0 \text{ dBm}$ ;<br>$f_{carrier} = 925.6 \text{ MHz}$ ;<br>TX to RX duplexer isolation is 35 dB minimum; $L_{ext} = 3.9 \text{ nH}$ (both base and handset); loop filter: see note 4<br><br>$f_{offset} = 20 \text{ MHz}$<br>$f_{offset} = 10 \text{ kHz}$<br>$f_{offset} = 1 \text{ kHz}$ | –139<br>–<br>– | –150<br>–85<br>–60 | –<br>–<br>– | <br>dBc/Hz<br>dBc/Hz<br>dBc/Hz |
| $P_{o(PA)}$  | PA output power range                                     | $R_o = 50 \Omega$ , $L_p = 22 \text{ nH}$ ;<br>$C_s = 1.6 \text{ pF}$ (see Fig.4)   | –              | 2                  | –           | dB                             |
| $\Delta P_{o(PA)}$   | PA output power adjustment                                |   | –              | 4                  | –           | steps                          |
| $P_{o(PA)(max)}$   | PA maximum output power                                   | $R_o = 50 \Omega$ , $L_p = 22 \text{ nH}$ ,<br>$C_s = 1.6 \text{ pF}$ (see Fig.4); remove duplexer insertion loss to get power on the antenna   | –              | 1                  | –           | dBm                            |
| <b>TRANSMIT SYSTEM</b>   |   |   |                |                    |             |                                |
| $THD_{TX}$   | total harmonic distortion after demodulation              | $f_{dev} = \pm 60 \text{ kHz}$ ;<br>$V_{MOD0} = 225 \text{ mV (p-p)}$ ;<br>CCITT filter included  | –              | 1                  | 2           | %                              |
| $\alpha_{ct(RX-TX)}$   | RXVCO crosstalk on PA output with respect to output power | note 1  | –              | –45                | –           | dBc                            |
| <b>Synthesizer</b>   |   |   |                |                    |             |                                |
| CRYSTAL OSCILLATOR: external capacitor on pin XTALO is 8.2 pF; on pin XTALI is 5.6 pF (indicative) |   |   |                |                    |             |                                |
| $f_{(i)XTAL}$  | crystal input frequency                                   |   | 4              | 10.24              | 20          | MHz                            |
| $C_{XTALI}$  | input capacitance on pin XTALI                            | indicative; XTAL tuning cap = 8 (see Table 5)   | –              | 4                  | –           | pF                             |
| $C_{XTALO}$  | input capacitance on pin XTALO                            | indicative  | –              | 1.5                | –           | pF                             |
| $\Delta C_{TUNE}$  | crystal tuning capacitance range                          | on XTALI pin  | –              | 4.5                | –           | pF                             |



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| SYMBOL                                       | PARAMETER   | CONDITIONS   | MIN. | TYP.            | MAX. | UNIT   |
|--|---|--|------|-----------------|------|--------|
| N <sub>TUNE</sub>                            | number of capacitance tuning steps                            |  | –    | 16              | –    | steps  |
| REFERENCE AND CLOCK DIVIDER                  |   |  |      |                 |      |        |
| RDR  | reference divider ratio                                       |  | 8    | –               | 1023 |        |
| CDR  | clock divider ratio   | 5 steps (2, 2.5, 4, 1 and 128)   | 1    | –               | 128  |        |
| C <sub>L(CLKOUT)</sub>                       | clock output load capacitance                                 | external to pin CLKOUT   | –    | –               | 20   | pF     |
| V <sub>CLKOUT(p-p)</sub>                     | CLKOUT voltage swing (peak-to-peak value)                     | CLKO level = 0   | –    | 1.4             | –    | V      |
|  |   | CLKO level = 1   | –    | 1               | –    | V      |
| t <sub>sw(f1-f2)</sub>                       | switching time from frequency f1 to f2                        |  | –    | $\frac{2}{f_2}$ | –    | s      |
| RF TX AND RX PRESCALER AND MAIN DIVIDERS     |   |  |      |                 |      |        |
| f <sub>RF</sub>                              | RF input frequency  |  | 902  | 903             | 928  | MHz    |
| R <sub>PDR</sub>                             | prescaler divider ratio                                       |  | 64   | –               | 127  |        |
| R <sub>MDR</sub>                             | main divider ratio  |  | 8    | –               | 1023 |        |
| <i>Charge pump current</i>                   |   |  |      |                 |      |        |
| I <sub>RXCPSink</sub>                        | RX charge pump sink current                                   | RXCPI = 0  | –    | 400             | –    | μA     |
|  |   | RXCPI = 1  | –    | 800             | –    | μA     |
| I <sub>RXCPSource</sub>                      | RX charge pump source current                                 | RXCPI = 0  | –    | –400            | –    | μA     |
|  |   | RXCPI = 1  | –    | –800            | –    | μA     |
| I <sub>TXCPSink</sub>                        | TX charge pump sink current                                   | TXCPI = 0  | –    | 400             | –    | μA     |
|  |   | TXCPI = 1  | –    | 800             | –    | μA     |
| I <sub>TXCPSource</sub>                      | TX charge pump source current                                 | TXCPI = 0  | –    | –400            | –    | μA     |
|  |   | TXCPI = 1  | –    | –800            | –    | μA     |
| RX VCO                                       |   |  |      |                 |      |        |
| f <sub>VCO</sub>                             | oscillator free running frequency                             | note 1   | –    | 910             | –    | MHz    |
| Q <sub>L(VCO)(RX)</sub>                      | external inductor quality factor                              | f = 920 MHz; L = 3.9 nH  | 30   | –               | –    |        |
| $\frac{\Delta f_{VCO(RX)}}{\Delta V_{RXLF}}$ | VCO gain  | L <sub>ext</sub> = 4.7 nH at 890 MHz<br>(3.9 nH for 935 MHz operation)   | –    | 55              | –    | MHz/V  |
|  |   | V <sub>RXLF</sub> = 0.5 V<br>V <sub>RXLF</sub> = 1.5 V   | –    | 30              | –    | MHz/V  |
| N <sub>VCO(RX)</sub>                         | VCO RX phase noise; (indicative: cannot be measured directly) | f <sub>carrier</sub> = 892.3 MHz;<br>L <sub>ext</sub> = 4.7 nH<br>(3.9 nH for 935 MHz operation);<br>loop filter: see note 5 | –    | –58             | –    | dBc/Hz |
|  |   | f <sub>offset</sub> = 1 kHz  | –    | –82             | –    | dBc/Hz |
|  |   | f <sub>offset</sub> = 100 kHz  | –    | –102            | –    | dBc/Hz |

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| SYMBOL   | PARAMETER   | CONDITIONS  | MIN. | TYP. | MAX. | UNIT          |
|--|---|---|------|------|------|---------------|
| VOLTAGE DOUBLER (Doubler enable = 1)   |   |   |      |      |      |               |
| $V_{CC(CP)}$   | charge pump supply voltage from voltage doubler   | $V_{CC} = 3\text{ V}$   | –    | 5.2  | –    | V             |
| $I_{CC(CP)}$   | voltage doubler current consumption   | PLL locked  | –    | 300  | –    | $\mu\text{A}$ |
|  |   | RX or TX mode<br>CDR = 128  | –    | 130  | –    | $\mu\text{A}$ |
| <b>RX baseband</b>   |   |   |      |      |      |               |
| RX AUDIO PATH (see Fig.6): $V_{VB} = 1.5\text{ V}$ ; $f_{\text{mod}} = 1\text{ kHz}$ ; RX gain set for 0 dB at $V_{i(\text{RXAI})} = -20\text{ dBV}$ ; earpiece amplifier gain set by VCTL to 4.7 dB; with no external resistor and $C_{\text{ext}} = 560\text{ pF}$ ; measured with a CCITT filter, except THD; $Z_{L(\text{EARO})} = 150\ \Omega$ in series with $10\ \mu\text{F}$ |   |   |      |      |      |               |
| $\Delta G_{\text{RX}}$   | RX gain adjustment range  | on RX gain amplifier  | -7.5 | –    | +8   | dB            |
|  |   | on EARO   | -15  | –    | +16  | dB            |
| $\Delta G_{\text{RX(steps)}}$  | RX gain adjustment steps  | programmable through microcontroller interface  | –    | 32   | –    | steps         |
| $\Delta G_{\text{RX(mute)}}$   | RX gain with mute on  | $V_{i(\text{RXAI})} = -20\text{ dBV}$   | –    | -70  | -60  | dB            |
| $G_{\text{EXP}}$   | expander gain   | $V_{i(\text{RXAI})} = -20\text{ dBV}$   | -1   | 0    | +1   | dB            |
|  |   | $V_{i(\text{RXAI})} = -30\text{ dBV}$   | -22  | -20  | -18  | dB            |
|  |   | $V_{i(\text{RXAI})} = -35\text{ dBV}$   | -34  | -30  | -26  | dB            |
| $V_{i(\text{RXAI})(\text{max})}$   | maximum input voltage   | THD < 4%  | –    | -13  | –    | dBV           |
| $V_{o(\text{EXP})(\text{max})}$  | maximum expander output voltage (indicative; cannot be measured directly)   | indicative; THD < 4%  | –    | -7   | –    | dBV           |
| $N_{\text{RX}}$  | RX audio path noise   | BW = 300 Hz to 3.4 kHz  | –    | -83  | –    | dBVp          |
| $Z_{i(\text{RXAI})}$   | input impedance   | note 3  | –    | 15   | –    | k $\Omega$    |
|  |   | TX mode   | –    | 15   | –    | k $\Omega$    |
|  |   | RX mode   | 100  | –    | –    | k $\Omega$    |
| $t_{\text{att(EXP)}}$  | expander attack time  | $C_{\text{ECAP}} = 0.47\ \mu\text{F}$   | –    | 2.0  | –    | ms            |
| $t_{\text{rel(EXP)}}$  | expander release time   | $C_{\text{ECAP}} = 0.47\ \mu\text{F}$   | –    | 5.0  | –    | ms            |
| $\alpha_{\text{ct(TX-RX)}}$  | TX compressor to RX expander crosstalk attenuation  | measured between pins CMPI and EARO; $V_{\text{RXAI}} = 0$ ; $V_{\text{CMPI}} = -20\text{ dBV}$ | –    | 80   | –    | dB            |
| $V_{\text{EARO}(\text{max})(\text{p-p})}$  | maximum output voltage (peak-peak value)  | THD < 4%  | –    | 2.2  | –    | V             |
| $R_{L(\text{EARO})}$   | load resistance on pin EARO for stable earpiece amplifier   | in series with $10\ \mu\text{F}$ capacitor  | –    | 0.15 | 100  | k $\Omega$    |
| $G_{\text{EAR}}$   | earpiece amplifier gain set by internal resistors without external components ( $R_{\text{ext}}$ and $C_{\text{ext}}$ ) | $R_{\text{int}} = 14\text{ k}\Omega$  | -1   | 0    | +1   | dB            |
|  |   | $R_{\text{int}} = 24\text{ k}\Omega$  | 3.7  | 4.7  | 5.7  | dB            |
|  |   | $R_{\text{int}} = 41\text{ k}\Omega$  | 8.3  | 9.3  | 10.3 | dB            |
|  |   | $R_{\text{int}} = 70.2\text{ k}\Omega$  | 13   | 14   | 15   | dB            |

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| SYMBOL   | PARAMETER   | CONDITIONS   | MIN. | TYP.  | MAX. | UNIT       |
|--|---|--|------|-------|------|------------|
| $G_{\text{EAR(dyn)}}$  | dynamic earpiece amplifier gain                                     |  | 13   | 14    | 15   | dB         |
| $\text{THD}_{\text{ARX}}$  | audio receiver total harmonic distortion                            | $V_{i(\text{RXAI})} = -20$ dBV   | –    | 0.2   | 2    | %          |
| <b>TX baseband</b>   |   |  |      |       |      |            |
| MICROPHONE AMPLIFIER: $V_{\text{VB}} = 1.5$ V; $f_{\text{mod}} = 1$ kHz  |   |  |      |       |      |            |
| $V_{\text{MICO(max)}}$   | maximum output voltage  | $R_{\text{L}} = 10$ k $\Omega$ ; $\text{THD} < 4\%$  | –12  | –     | –    | dBV        |
| $\Delta G_{\text{V}}$  | voltage gain range  |  | 0    | –     | 34   | dB         |
| TX AUDIO PATH (see Fig.8): $V_{\text{VB}} = 1.5$ V; $f_{\text{mod}} = 1$ kHz; TX gain set for 10 dB at $V_{\text{CMPI}} = -30$ dBV |   |  |      |       |      |            |
| $G_{\text{COMP}}$  | compressor gain level   | ALC disable = 1;<br>hard limiter enable = 0  | 9    | 10    | 11   | dB         |
| $\Delta G_{\text{COMP}}$   | change in compressor gain referenced to $V_{\text{CMPI}} = -30$ dBV | $V_{\text{CMPI}} = -10$ dBV  | 8    | 10    | 12   | dB         |
|  |   | $V_{\text{CMPI}} = -50$ dBV  | –12  | –10   | –8   | dB         |
| $G_{\text{COMP(max)}}$   | maximum compressor gain   | $V_{\text{CMPI}} = -70$ dBV  | –    | 23    | –    | dB         |
| $V_{\text{HLIM(p-p)}}$   | hard limiter output voltage (peak-to-peak value)                    | ALC disable = 1;<br>hard limiter enable = 1;<br>$V_{\text{CMPI}} = -4$ dBV                 | –    | 1.26  | –    | V          |
| $V_{\text{TXO(max)}}$  | maximum output voltage range  | ALC disable = 0  | –    | –     | –    | –          |
|  |   | $V_{\text{CMPI}} = -12$ dBV  | –    | –12.5 | –    | dBV        |
|  |   | $V_{\text{CMPI}} = -10$ dBV  | –    | –12.3 | –    | dBV        |
|  |   | $V_{\text{CMPI}} = -2.5$ dBV   | –    | –11.5 | –    | dBV        |
| $\text{THD}_{\text{COMP}}$   | compressor total harmonic distortion                                | ALC disable = 1;<br>$V_{\text{CMPI}} = -10$ dBV  | –    | 0.3   | 1    | %          |
| $Z_{\text{CMPI}}$  | input impedance on pin CMPI   |  | –    | 15    | –    | k $\Omega$ |
| $t_{\text{att(COMP)}}$   | compressor attack time  | $C_{\text{CCAP}} = 0.47$ $\mu\text{F}$   | –    | 4.0   | –    | ms         |
| $t_{\text{rel(COMP)}}$   | compressor release time   | $C_{\text{CCAP}} = 0.47$ $\mu\text{F}$   | –    | 8.0   | –    | ms         |
| $\alpha_{\text{ct(RX-TX)}}$  | RX expander to TX compressor crosstalk attenuation                  | measured between pins RXAI and TXO; $V_{\text{CMPI}} = 0$ ;<br>$V_{\text{RXAI}} = -10$ dBV | –    | 65    | –    | dB         |
| $\Delta G_{\text{TX}}$   | TX gain adjustment range  | programmable through microcontroller interface   | –7.5 | –     | +8   | dB         |
| $\Delta G_{\text{TX(steps)}}$  | TX gain adjustment steps  | programmable through microcontroller interface   | –    | 32    | –    | steps      |
| $\Delta G_{\text{TX(mute)}}$   | TX gain with mute on  | ALC disable = 1;<br>$V_{\text{CMPI}} = -10$ dBV  | –    | –70   | –60  | dB         |
| $Z_{\text{o(TXO)}}$  | output impedance at pin TXO   |  | –    | 500   | –    | $\Omega$   |

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| SYMBOL   | PARAMETER                               | CONDITIONS                                      | MIN.                   | TYP. | MAX.        | UNIT    |
|--|---|---|------------------------|------|-------------|---------|
| <b>Microcontroller interface</b>                       |   |   |                        |      |             |         |
| DC CHARACTERISTICS FOR DIGITAL PINS                    |   |   |                        |      |             |         |
| $V_{IL}$   | LOW-level input voltage                 | serial interface                                | –                      | –    | 0.5         | V       |
| $V_{IH}$   | HIGH-level input voltage                | serial interface                                | $\frac{V_{VREG}}{1.5}$ | –    | $V_{CC}$    | V       |
| $I_{IL}$   | LOW-level input current                 | serial interface; $V_{IL} = 0.3$ V              | –5                     | –    | –           | $\mu$ A |
| $I_{IH}$   | HIGH-level input current                | serial interface;<br>$V_{IH} = V_{REG} - 0.3$ V | –                      | –    | 5           | $\mu$ A |
| $I_{OL}$   | LOW-level output current                | pin CDLBD                                       | 20                     | –    | –           | $\mu$ A |
| $V_{OL}$   | LOW-level output voltage                | pin CDLBD; $R_L = 470$ k $\Omega$               | –                      | –    | $0.1V_{CC}$ | V       |
| $V_{OH}$   | HIGH-level output voltage               | pin CDLBD; $R_L = 470$ k $\Omega$               | $0.9V_{CC}$            | –    | –           | V       |
| $C_i$  | input capacitance                       | serial bus                                      | –                      | –    | 8           | pF      |
| $C_o$  | output capacitance                      | pins RXPB and TXPD                              | –                      | –    | 8           | pF      |
| SERIAL INTERFACE TIMING; CLK, DATA and EN (see Fig.10) |   |   |                        |      |             |         |
| $t_{su(CLK-EN)}$                                       | clock to enable set-up time             | 50% signal level                                | 50                     | –    | –           | ns      |
| $t_{su(DATA-CLK)}$                                     | input data to clock set-up time         | 50% signal level                                | 50                     | –    | –           | ns      |
| $t_h(EN-CLK)$  | enable to clock hold time               | 50% signal level                                | 50                     | –    | –           | ns      |
| $f_{CLK}$  | clock frequency                         |   | –                      | –    | 3           | MHz     |
| $t_r$  | input rise time                         | 10% to 90%                                      | –                      | –    | 50          | ns      |
| $t_f$  | input fall time                         | 10% to 90%                                      | –                      | –    | 50          | ns      |
| $t_{END}$  | delay from last falling clock edge      |   | 100                    | –    | –           | ns      |
| $t_w$  | enable pulse width                      | see Fig.10                                      | $\frac{1}{f_{comp}}$   | –    | –           | ns      |
| $t_{strt}$   | microcontroller interface start-up time | 90% of $V_{VREG}$ to DATA, CLK and EN present   | –                      | –    | 200         | $\mu$ s |

**Notes**

1. Measured and guaranteed only on the Philips UAA3515A test board.
2. Loop filter:  $C_1 = 1.8$  nF;  $R_2 = 4.7$  k $\Omega$ ;  $C_2 = 150$  nF (see "Report CTT01001", available on request).
3. RXAI level will be higher in RX mode than in TX mode.
4. Loop filter:  $C_1 = 3.9$  nF;  $R_2 = 6.8$  k $\Omega$ ;  $C_2 = 47$  nF (see "Report CTT01001", available on request).
5. Loop filter:  $C_1 = 470$  nF;  $R_2 = 1.8$  k $\Omega$ ;  $C_2 = 4.7$   $\mu$ F (see "Report CTT01001", available on request).

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12 PACKAGE OUTLINE

LQFP64: plastic low profile quad flat package; 64 leads; body 10 x 10 x 1.4 mm

SOT314-2



DIMENSIONS (mm are the original dimensions)

| UNIT | A max. | A <sub>1</sub> | A <sub>2</sub> | A <sub>3</sub> | b <sub>p</sub> | c            | D <sup>(1)</sup> | E <sup>(1)</sup> | e   | H <sub>D</sub> | H <sub>E</sub> | L   | L <sub>p</sub> | v   | w    | y   | Z <sub>D</sub> <sup>(1)</sup> | Z <sub>E</sub> <sup>(1)</sup> | θ        |
|------|--------|----------------|----------------|----------------|----------------|--------------|------------------|------------------|-----|----------------|----------------|-----|----------------|-----|------|-----|-------------------------------|-------------------------------|----------|
| mm   | 1.60   | 0.20<br>0.05   | 1.45<br>1.35   | 0.25           | 0.27<br>0.17   | 0.18<br>0.12 | 10.1<br>9.9      | 10.1<br>9.9      | 0.5 | 12.15<br>11.85 | 12.15<br>11.85 | 1.0 | 0.75<br>0.45   | 0.2 | 0.12 | 0.1 | 1.45<br>1.05                  | 1.45<br>1.05                  | 7°<br>0° |

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

| OUTLINE VERSION | REFERENCES |        |      |  | EUROPEAN PROJECTION | ISSUE DATE           |
|-----------------|------------|--------|------|--|---------------------|----------------------|
|                 | IEC        | JEDEC  | EIAJ |  |                     |                      |
| SOT314-2        | 136E10     | MS-026 |      |  |                     | 99-12-27<br>00-01-19 |

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**13 SOLDERING****13.1 Introduction to soldering surface mount packages**

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"Data Handbook IC26; Integrated Circuit Packages"* (document order number 9398 652 90011).

There is no soldering method that is ideal for all surface mount IC packages. Wave soldering can still be used for certain surface mount ICs, but it is not suitable for fine pitch SMDs. In these situations reflow soldering is recommended.

**13.2 Reflow soldering**

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several methods exist for reflowing; for example, convection or convection/infrared heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 to 250 °C. The top-surface temperature of the packages should preferably be kept below 220 °C for thick/large packages, and below 235 °C for small/thin packages.

**13.3 Wave soldering**

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):
  - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;
  - smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

The footprint must incorporate solder thieves at the downstream end.
- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time is 4 seconds at 250 °C.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

**13.4 Manual soldering**

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

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## 13.5 Suitability of surface mount IC packages for wave and reflow soldering methods

| PACKAGE   | SOLDERING METHOD                  |                       |
|---|-----------------------------------|-----------------------|
|   | WAVE                              | REFLOW <sup>(1)</sup> |
| BGA, HBGA, LFBGA, SQFP, TFBGA                       | not suitable                      | suitable              |
| HBCC, HLQFP, HSQFP, HSOP, HTQFP, HTSSOP, HVQFN, SMS | not suitable <sup>(2)</sup>       | suitable              |
| PLCC <sup>(3)</sup> , SO, SOJ                       | suitable                          | suitable              |
| LQFP, QFP, TQFP                                     | not recommended <sup>(3)(4)</sup> | suitable              |
| SSOP, TSSOP, VSO                                    | not recommended <sup>(5)</sup>    | suitable              |

**Notes**

1. All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the *"Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods"*.
2. These packages are not suitable for wave soldering as a solder joint between the printed-circuit board and heatsink (at bottom version) can not be achieved, and as solder may stick to the heatsink (on top version).
3. If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.
4. Wave soldering is only suitable for LQFP, TQFP and QFP packages with a pitch (e) equal to or larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.
5. Wave soldering is only suitable for SSOP and TSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.

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## 14 DATA SHEET STATUS

| DATA SHEET STATUS <sup>(1)</sup> | PRODUCT STATUS <sup>(2)</sup> | DEFINITIONS  |
|----------------------------------|-------------------------------|--|
| Objective data                   | Development                   | This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.  |
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