## Low Cost Dual Power Distribution Controller

The HIP1013 is a low cost HOT SWAP dual supply power distribution controller. Two external N-Channel MOSFETs are driven to distribute power while providing load fault isolation. At turn-on, the gate of each external N-Channel MOSFET is charged with a 10µA current source. Capacitors on each gate (see the Typical Application Diagram), create a programmable ramp (soft turn-on) to control inrush currents. A built in charge pump supplies the gate drive for the 12V supply N-Channel MOSFET switch.

Over current protection is facilitated by two external current sense resistors. When the current through either resistor exceeds the user programmed value the N-Channel MOSFETs are latched off by the HIP1013. The controller is reset by a rising edge on either $\overline{\text{PWRON}}$ pin.

Choosing the voltage selection mode the HIP1013 controls either +12V/5V or +3.3V/+5V supplies.

Although pin compatible with the HIP1012 device, the HIP1013 does not offer current regulation during an OC event.

## Ordering Information

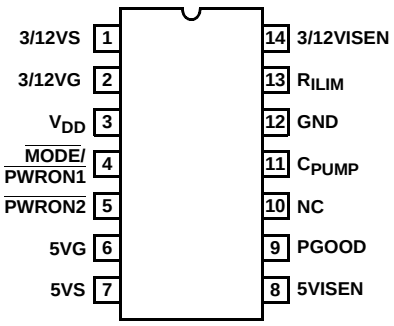
| PART NUMBER | TEMP. RANGE (°C) | PACKAGE | PKG. DWG. # |
|---|---|---|---|
| HIP1013CB | -0 to 70 | 14 Ld SOIC | M14.15 |
| HIP1013CBZA (Note) | -0 to 70 | 14 Ld SOIC (Pb-free) | M14.15 |

NOTE: Intersil Pb-free products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which is compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J Std-020B.

*Tape & Reel packaging available with "-T" suffix..

## Pinout

**HIP1013 (SOIC)**
TOP VIEW



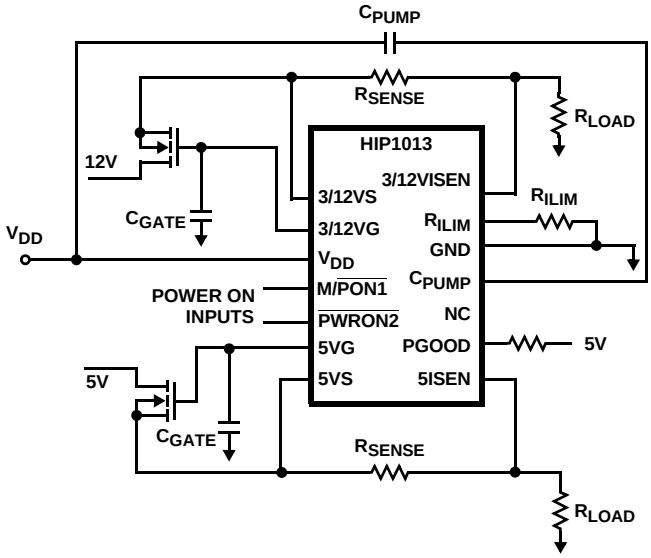

## Features

- HOT SWAP Dual Power Distribution Control for +5V and +12V or +5V and +3.3V
- Provides Fault Isolation
- Charge Pump Allows the Use of N-Channel MOSFETs
- Redundant Power On Controls
- Power Good and Over Current Latch Indicators
- Adjustable Turn-On Ramp
- Protection During Turn-On
- Pb-free Available

## Applications

- Power Distribution Control
- Hot Plug™ Components

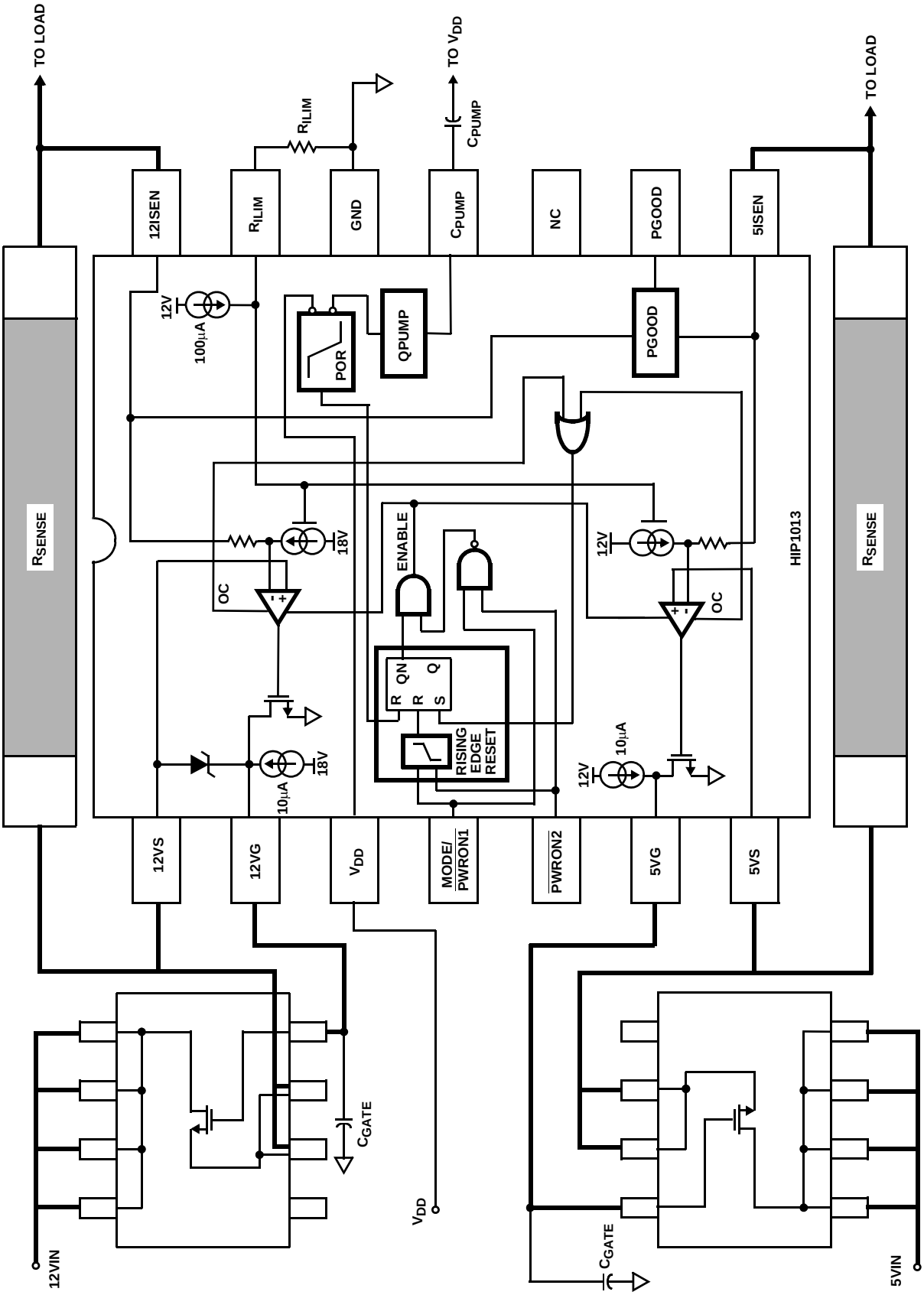
## Typical Application Diagram






CAUTION: These devices are sensitive to electrostatic discharge; follow proper IC Handling Procedures.
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## Functional Diagram



## Pin Description

| PIN NO. | SYMBOL | FUNCTION | DESCRIPTION |
|---|---|---|---|
| 1 | 12VS | 12V Source | Connect to source of associated external N-Channel MOSFET switch to sense output voltage. |
| 2 | 12VG | 12V Gate | Connect to the gate of associated N-Channel MOSFET switch. A capacitor from this node to ground sets the turn-on ramp. At turn-on this capacitor will be charged to ≈17.4V by a 10µA current source when in 5V/12V mode of operation, otherwise capacitor will be charged to ≈11.4V. |
| 3 | $V_{DD}$ | Chip Supply | Connect to 12V supply. This can be either connected directly to the +12V rail supplying the load voltage or to a dedicated $V_{DD}$ +12V supply. |
| 4 | MODE/ $\overline{\text{PWRON1}}$ | Power ON/ Reset invokes 3.3V operation when shorted to $V_{DD}$, Pin 3. | $\overline{\text{PWRON1}}$ and $\overline{\text{PWRON2}}$ are used to turn-on and reset the chip. Both outputs turn-on when either pin is driven low. After an over current limit fault, the chip is reset by the rising edge of a reset signal applied to either $\overline{\text{PWRON}}$ pin. Each input has 100µA pull up capability which is compatible with 3V and 5V open drain and standard logic. $\overline{\text{PWRON1}}$ is also used to invoke 3.3V control operation in preference to +12V control. By tying pin 4 to pin 3 the charge pump is disabled and the UV threshold also shifts to ≈2.8V. |
| 5 | $\overline{\text{PWRON2}}$ | Power ON/Reset | |
| 6 | 5VG | 5V Gate | Connect to the gate of the external 5V N-Channel MOSFET. A capacitor from this node to ground sets the turn-on ramp. At turn-on this capacitor will be charged to ≈11.4V by a 10µA current source. |
| 7 | 5VS | 5V Source | Connect to the source side of 5V external N-Channel MOSFET switch to sense output voltage. |
| 8 | 5VISEN | 5V Current Sense | Connect to the load side of the 5V sense resistor to measure the voltage drop across this resistor between 5VS and 5VISEN pins. |
| 9 | PGOOD | Power Good Indicator | PGOOD is driven by an open drain N-Channel MOSFET. It is pulled low when either output voltage is not within specification or and OC condition exists. |
| 10 | | | No Connection. |
| 11 | $C_{PUMP}$ | Charge Pump Capacitor | Connect a 0.1µF capacitor between this pin and $V_{DD}$ (Pin 3). |
| 12 | GND | Chip Ground | |
| 13 | $R_{ILIM}$ | Current Limit Set Resistor | A resistor connected between this pin and ground determines the current level at which current limit is activated. This current is determined by the ratio of the $R_{ILIM}$ resistor to the sense resistor ($R_{SENSE}$). The current at current limit onset is equal to 10µA x ($R_{ILIM}/R_{SENSE}$). |
| 14 | 12VISEN | 12V Current Sense | Connect to the load side of sense resistor to measure the voltage drop across this resistor. |

## Absolute Maximum Ratings $T_A = 25°C$

$V_{DD}$ . . . . . -0.3V to +17V
3/12VG, $C_{PUMP}$ . . . . . -0.3V to 25V
3/12VISEN, 3/12VS . . . . . -5V to $V_{DD}$ + 0.3V
5VISEN, 5VS . . . . . -5V to 7.5V
PGOOD, $R_{ILIM}$ . . . . . -0.3V to 7.5V
MODE/$\overline{PWRON1}$, $\overline{PWRON2}$, 5VG . . . . . -0.3V to $V_{DD}$ + 0.3V
ESD Classification . . . . . 2kV (Class 2)

## Thermal Information

| Thermal Resistance (Typical, Note 1) | $\theta_{JA}$ (°C/W) |
|---|---|
| SOIC Package | 120 |

Maximum Junction Temperature (Plastic Package) . . . . . 150°C
Maximum Storage Temperature Range . . . . . -65°C to 150°C
Maximum Lead Temperature (Soldering 10s) . . . . . 300°C
(SOIC - Lead Tips Only)

## Operating Conditions

$V_{DD}$ Supply Voltage Range . . . . . +10.5V to +16V
Temperature Range ($T_A$) . . . . . 0°C to 70°C

*CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.*

NOTES:

1. $\theta_{JA}$ is measured with the component mounted on an evaluation PC board in free air.
2. All voltages are relative to GND, unless otherwise specified.

## Electrical Specifications

$V_{DD}$ = 12V, $C_{VG}$ = 0.01µF, $R_{SENSE}$ = 0.1Ω, $C_{BULK}$ = 220µF, ESR = 0.5Ω, $T_A = T_J$ = 0°C to 70°C, Unless Otherwise Specified

| PARAMETER | SYMBOL | TEST CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| **CONTROL SECTION** | | | | | | |
| Current Limit Threshold Voltage (Voltage Across Sense Resistor) | $V_{IL}$ | $R_{ILIM}$ = 10kΩ | 85 | 100 | 115 | mV |
| Over Current Limit Response Time | $OC_{Lrt}$ | Current Overload, $R_{ILIM}$ = 10kΩ, $R_{SHORT}$ = 6.0Ω | - | 2 | - | µs |
| Response Time To Dead Short | $RT_{SHORT}$ | $C_{VG}$ = 0.01µF | - | 500 | 1000 | ns |
| 12V Gate Turn-On Time | $t_{ON12V}$ | $C_{VG}$ = 0.01µF | - | 12 | - | ms |
| 5V Gate Turn-On Time | $t_{ON5V}$ | $C_{VG}$ = 0.01µF | - | 5 | - | ms |
| Gate Turn-On Current | $I_{ON}$ | $C_{VG}$ = 0.01µF | 8 | 10 | 12 | µA |
| 12V Under Voltage Threshold | $12V_{VUV}$ | | 10.5 | 10.8 | 11.0 | V |
| 5V Under Voltage Threshold | $5V_{VUV}$ | | 4.35 | 4.5 | 4.65 | V |
| 3.3V Under Voltage Threshold | $3.3V_{VUV}$ | | 2.65 | 2.8 | 2.95 | V |
| Charge pumped 12VG Voltage | V12VG | $C_{PUMP}$ = 0.1µF | 16.8 | 17.3 | 17.9 | V |
| 3/5VG High Voltage | 3/5VG | | 11.2 | 11.9 | - | V |
| **SUPPLY CURRENT AND IO SPECIFICATIONS** | | | | | | |
| $V_{DD}$ Supply Current | $I_{VDD}$ | | 4 | 8 | 10 | mA |
| $V_{DD}$ POR Rising Threshold | $POR_{rvth}$ | | 9.5 | 10.0 | 10.5 | V |
| $V_{DD}$ POR Falling Threshold | $POR_{fvth}$ | | 9.3 | 9.8 | 10.3 | V |
| $\overline{PWRON}$ Pull-up Voltage | PWRN_V | $\overline{PWRON}$ pins open | 1.8 | 2.4 | 3.2 | V |
| $\overline{PWRON}$ Rising Threshold | PWR_Vth | | 1.1 | 1.5 | 2 | V |
| $\overline{PWRON}$ Hysteresis | PWR_hys | | 0.1 | 0.2 | 0.3 | V |
| $\overline{PWRON}$ Pull-Up Current | PWRN_I | | 60 | 80 | 100 | µA |
| $R_{ILIM}$ Pin Current Source Output | $R_{ILIM}$_Io | | 90 | 100 | 110 | µA |
| Charge Pump Output Current | Qpmp_Io | $C_{PUMP}$ = 0.1µF, $C_{PUMP}$ = 16V | 400 | 590 | 800 | µA |
| Charge Pump Output Voltage | Qpmp_Vo | No load | 17.2 | 17.4 | - | V |
| Charge Pump Output Voltage - Loaded | Qpmp_VIo | Load current = 100µA | 16.2 | 16.7 | - | V |
| Charge Pump POR Rising Threshold | Qpmp+Vth | | 15.6 | 16 | 16.5 | V |
| Charge Pump POR Falling Threshold | Qpmp-Vth | | 15.2 | 15.7 | 16.2 | V |

## Typical Performance Curves

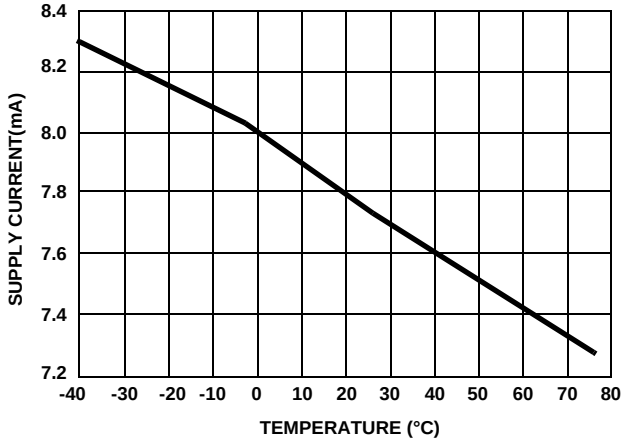



FIGURE 1. SUPPLY CURRENT

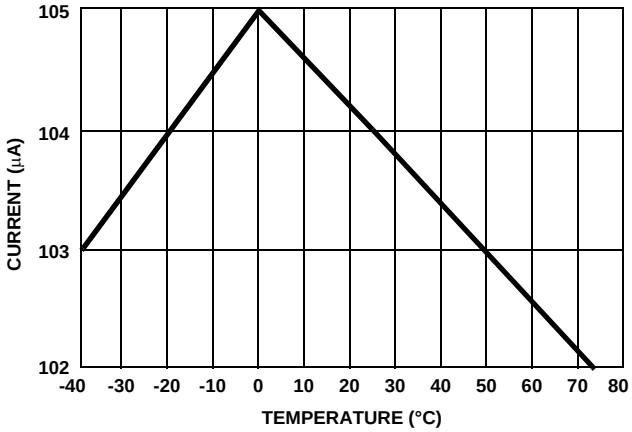



FIGURE 2. $R_{ILIM}$ SOURCE CURRENT

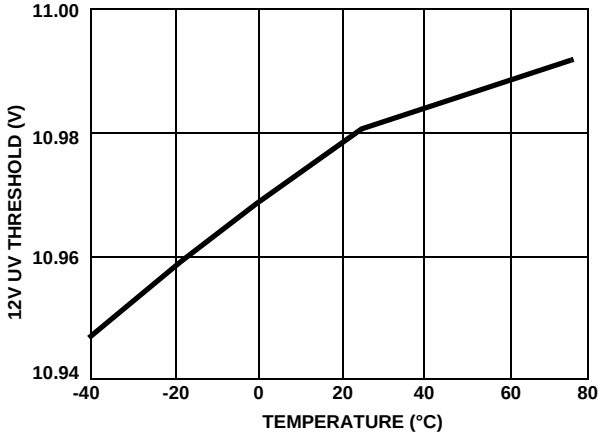



FIGURE 3. 12V UV THRESHOLD

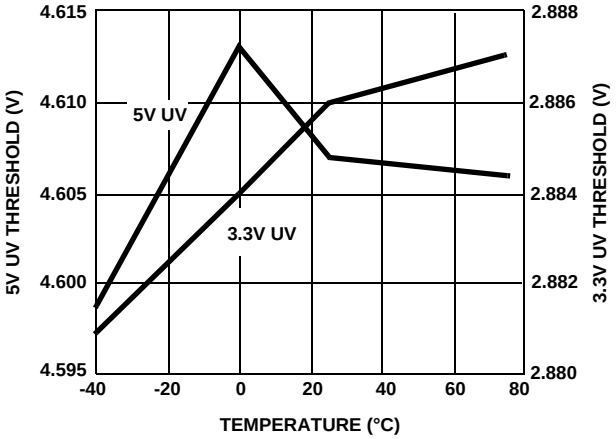



FIGURE 4. 3.3V/5V UV THRESHOLD

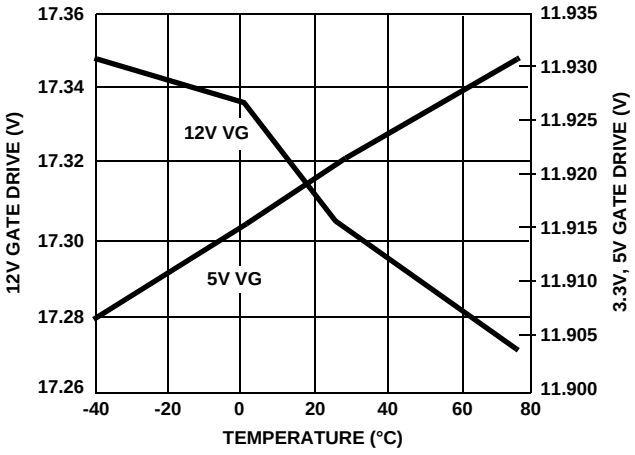



FIGURE 5. 12V, 5V GATE DRIVE

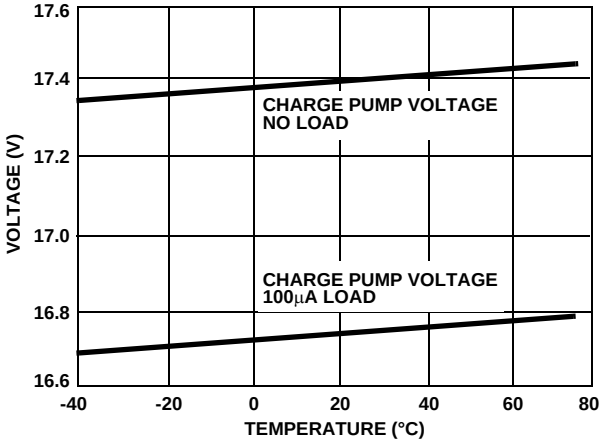



FIGURE 6. CHARGE PUMP VOLTAGE

## Typical Performance Curves (Continued)

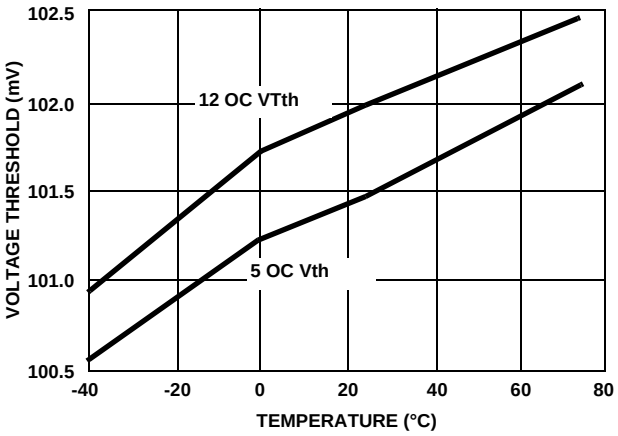



FIGURE 7. OC VOLTAGE THRESHOLD WITH = $R_{ILIM}$ 10kΩ

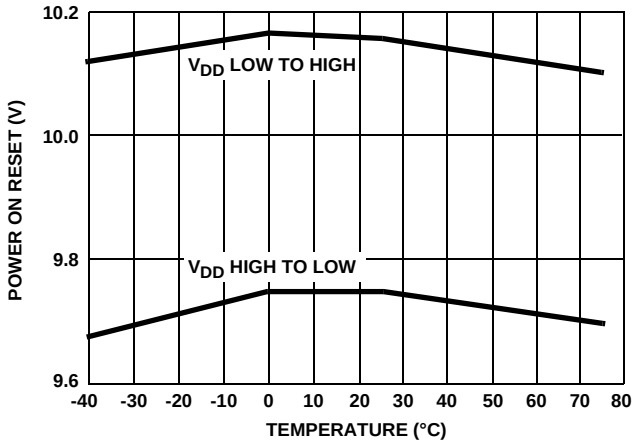



FIGURE 8. POWER ON RESET VOLTAGE THRESHOLD

## HIP1013 Description and Operation

The HIP1013 offers the designer a cost efficient 5V and 12V true hot plug controller. This device drives two external N-Channel MOSFET switches and uses a charge pump to provide ≈17V to drive the gate of the 12V supply switch. The HIP1013 features Over Current (OC) programing with a single external resistor, $R_{ILIM}$ and during turn-on, the gate capacitor of each external N-Channel MOSFET is charged with a 10μA current source. These capacitors create a programmable ramp (soft turn-on).

Upon initial power up, the HIP1013 can either isolate the voltage supply from the load by holding the external N-Channel MOSFET switches off or apply the supply rail voltage directly to the load for true hot swap capability. In either case the HIP1013 turns on in a soft start mode protecting the supply rail from sudden current loading.

The load currents pass through two external current sense resistors. When the voltage across either resistor exceeds the user programmed Over Current (OC) voltage threshold value, (see Table 1) the HIP1013 controller turns both N-Channel MOSFETs off in ≈ 2μs.

**TABLE 1.**

| $R_{ILIM}$ RESISTOR | NOMINAL OC VTH |
|---|---|
| 15K | 150mv |
| 10K | 100mV |
| 7.5K | 75mV |
| 4.99K | 50mV |

NOTE: Nominal OC Vth = $R_{ILIM}$ x 10 μA

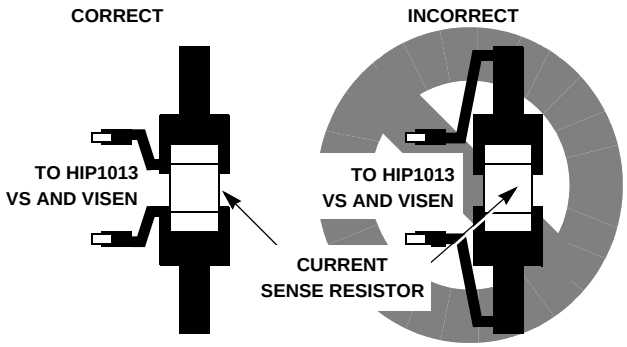
The HIP1013 is reset by a rising edge on either $\overline{PWRON}$ pin and is turned on by either $\overline{PWRON}$ pin being driven low. The HIP1013 can control either +12V/5V or +3.3V/+5V supplies. Tying the $\overline{PWRON1}$ pin to $V_{DD}$, invokes the +3.3V/+5V voltage mode. In this mode, the external charge pump capacitor is not needed and $C_{PUMP}$, pin 11 is also tied directly to $V_{DD}$. Upon any OC or Under Voltage (UV) condition the PGOOD fault indicating signal will pull low when tied high through a resistor to the logic supply.

## HIP1013 Application Considerations

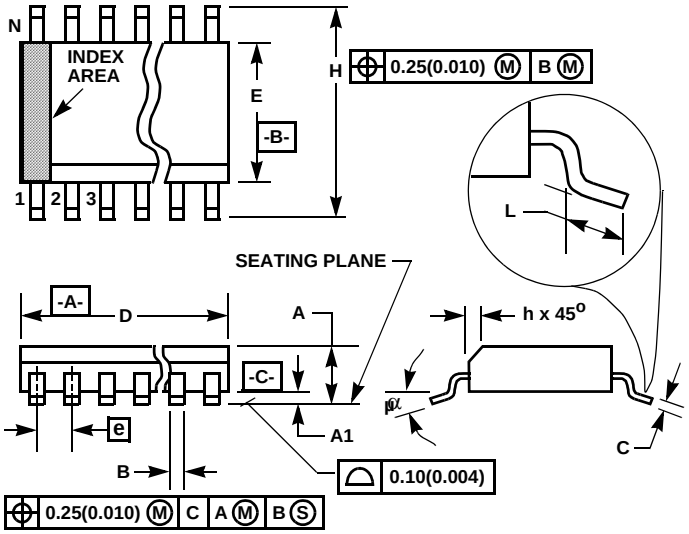
**There is no unique and specific HIP1013 application evaluation board**. Since the HIP1013 is pin compatible with the HIP1012 device, you can substitute a HIP1013 for the existing HIP1012 in either of the HIP1012EVAl1 or EVAL2 boards. Otherwise contact your Intersil Corporation sales office and an already modified board will be provided. Although pin compatible to the HIP1012, the HIP1013 is a less featured dual power supply distribution controller and does not include programmable current limiting regulation and delay time to latch off.

**Random resets** can also occur if the HIP1013 (PINS 8 and 14) sense pins are pulled below ground when turning off a highly inductive load. Place a large load capacitor (10-50µF) on the output to eliminate unintended resets.

**Physical layout of $R_{SENSE}$ resistors** is critical to avoid the possibility of false over current occurrences. Ideally trace routing between the $R_{SENSE}$ resistors and the HIP1013 VS and VISEN pins are direct and as short as possible with zero current in the sense lines.



## Small Outline Plastic Packages (SOIC)




**M14.15 (JEDEC MS-012-AB ISSUE C)**
**14 LEAD NARROW BODY SMALL OUTLINE PLASTIC PACKAGE**

| SYMBOL | INCHES | | MILLIMETERS | | NOTES |
|---|---|---|---|---|---|
| | MIN | MAX | MIN | MAX | |
| A | 0.0532 | 0.0688 | 1.35 | 1.75 | - |
| A1 | 0.0040 | 0.0098 | 0.10 | 0.25 | - |
| B | 0.013 | 0.020 | 0.33 | 0.51 | 9 |
| C | 0.0075 | 0.0098 | 0.19 | 0.25 | - |
| D | 0.3367 | 0.3444 | 8.55 | 8.75 | 3 |
| E | 0.1497 | 0.1574 | 3.80 | 4.00 | 4 |
| e | 0.050 BSC | | 1.27 BSC | | - |
| H | 0.2284 | 0.2440 | 5.80 | 6.20 | - |
| h | 0.0099 | 0.0196 | 0.25 | 0.50 | 5 |
| L | 0.016 | 0.050 | 0.40 | 1.27 | 6 |
| N | 14 | | 14 | | 7 |
| $\alpha$ | $0^o$ | $8^o$ | $0^o$ | $8^o$ | - |

Rev. 0 12/93

NOTES:

1. Symbols are defined in the “MO Series Symbol List” in Section 2.2 of Publication Number 95.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension “D” does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension “E” does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. “L” is the length of terminal for soldering to a substrate.
7. “N” is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. The lead width “B”, as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch).
10. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.

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Intersil Corporation’s quality certifications can be viewed at www.intersil.com/design/quality

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