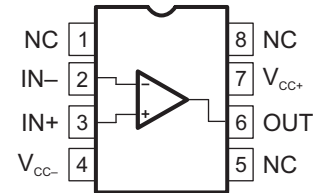


LOW-POWER SINGLE OPERATIONAL AMPLIFIER

FEATURES

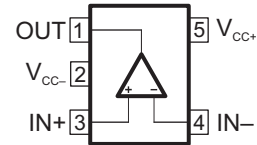
- **Wide Power-Supply Range**
 - Single Supply...3 V to 30 V
 - Dual Supply... ± 1.5 V to ± 15 V
- **Large Output Voltage Swing...**
0 V to 3.5 V (Min) ($V_{CC} = 5$ V)
- **Low Supply Current...**500 μ A (Typ)
- **Low Input Bias Current...**20 nA (Typ)
- **Stable With High Capacitive Loads**

**D (SOIC) PACKAGE
(TOP VIEW)**



NC – No internal connection

**DBV (SOT-23-5) PACKAGE
(TOP VIEW)**



DESCRIPTION/ORDERING INFORMATION

The TS321 is a bipolar operational amplifier for cost-sensitive applications in which space savings are important.

ORDERING INFORMATION

T_A	PACKAGE ⁽¹⁾		ORDERABLE PART NUMBER	TOP-SIDE MARKING ⁽²⁾
–40°C to 125°C	SOIC – D	Tube of 75	TS321ID	SR321I
		Reel of 2500	TS321IDR	
	SOT-23-5 – DBV	Reel of 3000	TS321IDBVR	9C1_
		Reel of 250	TS321IDBVT	

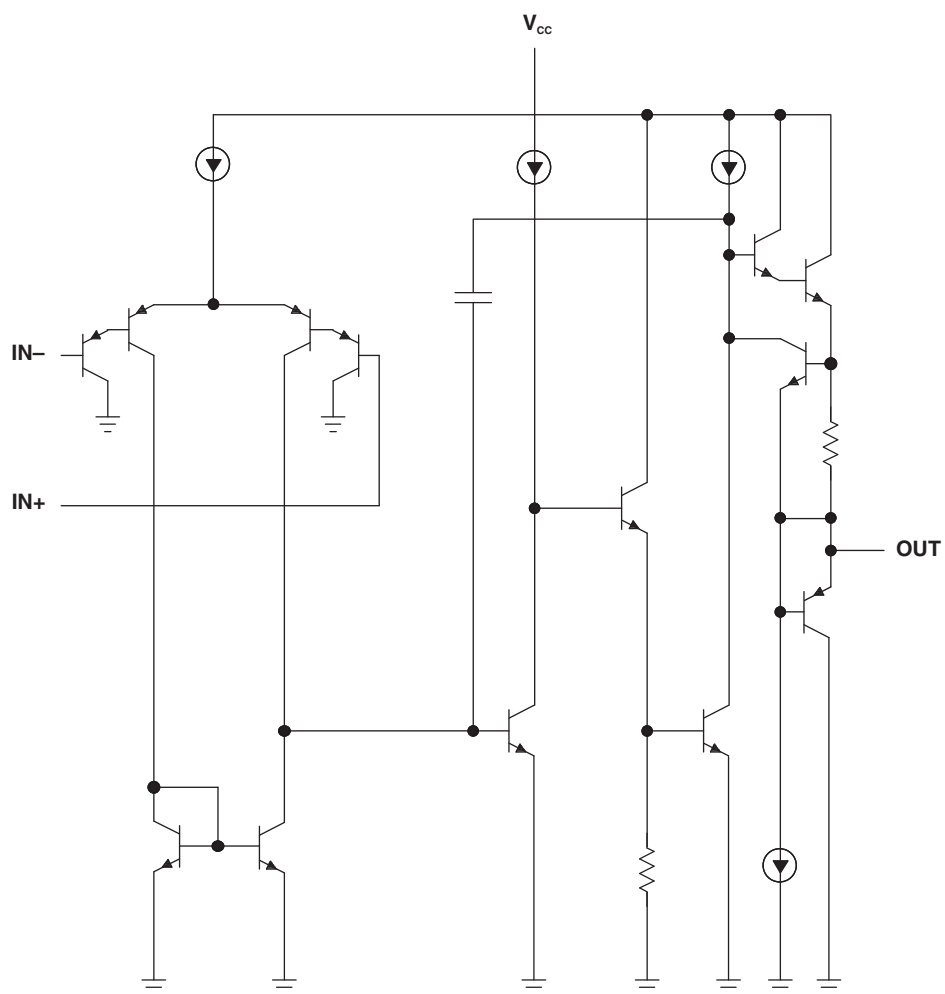
(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

(2) DBV: The actual top-side marking has one additional character that designates the assembly/test site.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

SCHEMATIC DIAGRAM



Absolute Maximum Ratings⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{CC}	Supply voltage ⁽²⁾	Single		32	V
		Dual		±16	
V_{ID}	Differential input voltage ⁽³⁾			32	V
V_I	Input voltage range ⁽²⁾⁽⁴⁾		–0.3	32	V
I_I	Input current ⁽⁴⁾			50	mA
t_{short}	Duration of output short circuit to ground			Unlimited	
θ_{JA}	Package thermal impedance, junction to free air ⁽⁵⁾⁽⁶⁾	D package		97	°C/W
		DBV package		206	
T_J	Operating virtual junction temperature			150	°C
T_{stg}	Storage temperature range		–65	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) These voltage values are with respect to the midpoint between V_{CC+} and V_{CC-} .
- (3) Differential voltages are at $IN+$ with respect to $IN-$.
- (4) Neither input must ever be more positive than V_{CC+} or more negative than V_{CC-} .
- (5) Maximum power dissipation is a function of $T_J(max)$, θ_{JA} , and T_A . The maximum allowable power dissipation at any allowable ambient temperature is $P_D = (T_J(max) - T_A)/\theta_{JA}$. Selecting the maximum of 150°C can affect reliability.
- (6) The package thermal impedance is calculated in accordance with JESD 51-7.

Recommended Operating Conditions

			MIN	MAX	UNIT
V_{CC}	Supply voltage	Single supply	3	30	V
		Dual supply	±1.5	±15	
T_A	Operating free-air temperature		–40	125	°C

Electrical Characteristics

$V_{CC+} = 5\text{ V}$, $V_{CC-} = \text{GND}$, $V_O = 1.4\text{ V}$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T _A	MIN	TYP	MAX	UNIT
V _{IO}	Input offset voltage	R _S = 0, 5 V < V _{CC+} < 30 V, 0 < V _{IC} < (V _{CC+} − 1.5 V)		25°C		0.5	4	mV
				Full range			5	
I _{IO}	Input offset current			25°C		2	30	nA
				Full range			50	
I _{IB}	Input bias current ⁽¹⁾			25°C		20	150	nA
				Full range			200	
A _{VD}	Large-signal differential voltage amplification	V _{CC} = 15 V, R _L = 2 kΩ, V _O = 1.4 V to 11.4 V		25°C	50	100		V/mV
				Full range	25			
V _{ICR}	Common-mode input voltage ⁽²⁾	V _{CC} = 30 V		25°C	0	V _{CC+} − 1.5		V
				Full range	0	V _{CC+} − 2		
V _{OH}	High-level output voltage	V _{CC} = 30 V	R _L = 2 kΩ	25°C	26	27		V
				Full range	25.5			
			R _L = 10 kΩ	25°C	27	28		
				Full range	26.5			
		V _{CC} = 5 V	R _L = 2 kΩ	25°C	3.5			
				Full range	3			
V _{OL}	Low-level output voltage	R _L = 10 kΩ		25°C		5	15	V
				Full range			20	
GBP	Gain bandwidth product	V _{CC} = 30 V, V _I = 10 mV, R _L = 2 kΩ, f = 100 kHz, C _L = 100 pF		25°C		0.8		MHz
SR	Slew rate	V _{CC} = 15 V, V _I = 0.5 V to 3 V, R _L = 2 kΩ, C _L = 100 pF, unity gain		25°C		0.4		V/μs
φ _m	Phase margin			25°C		60		°
CMRR	Common-mode rejection ratio	R _S ≤ 10 kΩ		25°C	65	85		dB
I _{SOURCE}	Output source current	V _{CC} = 15 V, V _O = 2 V, V _{ID} = 1 V		25°C	20	40		mA
I _{SINK}	Output sink current	V _{CC} = 15 V, V _{ID} = 1 V	V _O = 2 V	25°C	10	20		mA
			V _O = 0.2 V	25°C	12	50		μA
I _O	Short-circuit to GND	V _{CC} = 15 V		25°C		40	60	mA
SVR	Supply-voltage rejection ratio	V _{CC} = 5 V to 30 V		25°C	65	110		dB
I _{CC}	Total supply current	No load	V _{CC} = 5 V	25°C		500	800	μA
			V _{CC} = 30 V			600	900	
			V _{CC} = 5 V	Full range		600	900	
			V _{CC} = 30 V				1000	
THD	Total harmonic distortion	V _{CC} = 30 V, V _O = 2 V _{pp} , A _V = 20 dB, R _L = 2 kΩ, f = 1 kHz, C _L = 100 pF		25°C		0.015		%
e _N	Equivalent input noise voltage	V _{CC} = 30 V, f = 1 kHz, R _S = 100 Ω		25°C		50		nV/√Hz

- (1) The direction of the input current is out of the device. This current essentially is constant, independent of the state of the output, so no loading change exists on the input lines.
- (2) The input common-mode voltage of either input signal should not be allowed to go negative by more than 0.3 V. The upper end of the common-mode voltage range is $V_{CC+} - 1.5\text{ V}$, but either or both inputs can go to 32 V without damage.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
TS321ID	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	SR321I	Samples
TS321IDBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	(9C1G ~ 9C1S)	Samples
TS321IDBVRE4	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	(9C1G ~ 9C1S)	Samples
TS321IDBVRG4	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	(9C1G ~ 9C1S)	Samples
TS321IDBVT	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	(9C1G ~ 9C1S)	Samples
TS321IDBVTE4	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	(9C1G ~ 9C1S)	Samples
TS321IDBVTG4	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	(9C1G ~ 9C1S)	Samples
TS321IDE4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	SR321I	Samples
TS321IDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	SR321I	Samples
TS321IDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	SR321I	Samples
TS321IDRE4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	SR321I	Samples
TS321IDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	SR321I	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBsolete: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

⁽⁴⁾ Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

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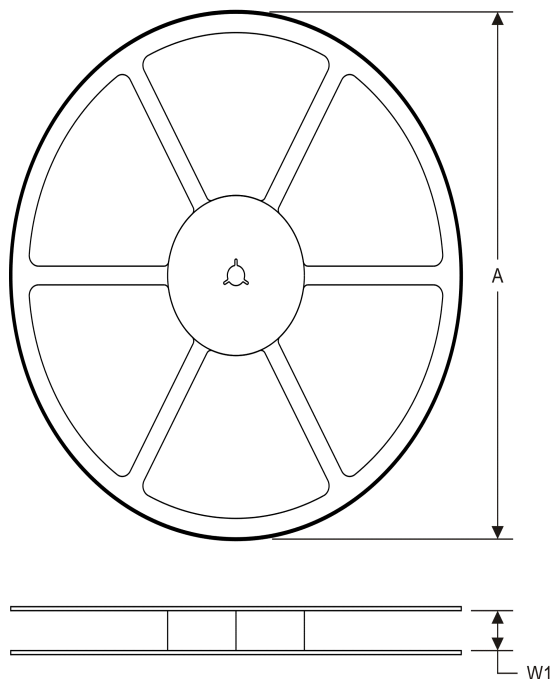
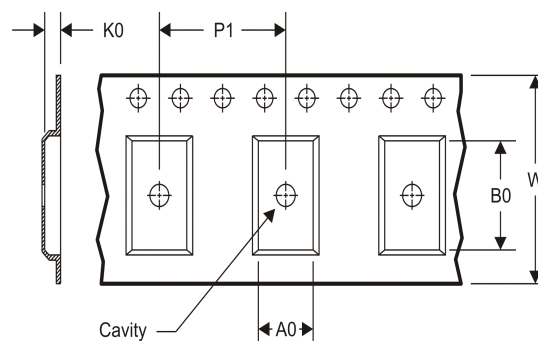
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OTHER QUALIFIED VERSIONS OF TS321 :

- Automotive: [TS321-Q1](#)

NOTE: Qualified Version Definitions:

- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION
REEL DIMENSIONS

TAPE DIMENSIONS


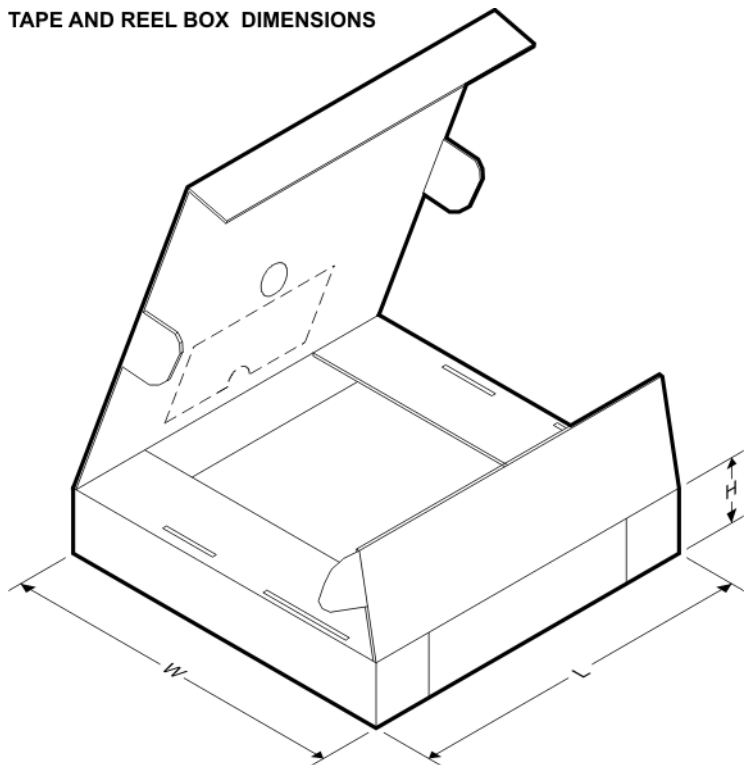
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TS321IDBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TS321IDBVT	SOT-23	DBV	5	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TS321IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS

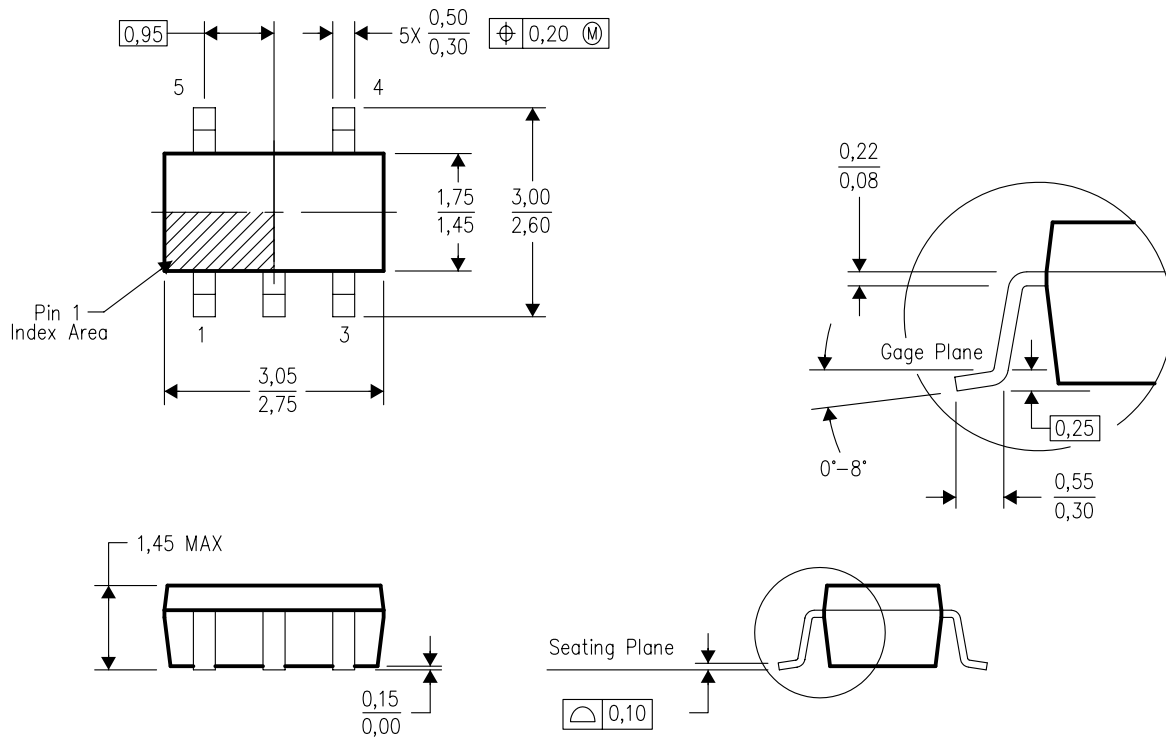


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TS321IDBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TS321IDBVT	SOT-23	DBV	5	250	180.0	180.0	18.0
TS321IDR	SOIC	D	8	2500	340.5	338.1	20.6

DBV (R-PDSO-G5)

PLASTIC SMALL-OUTLINE PACKAGE

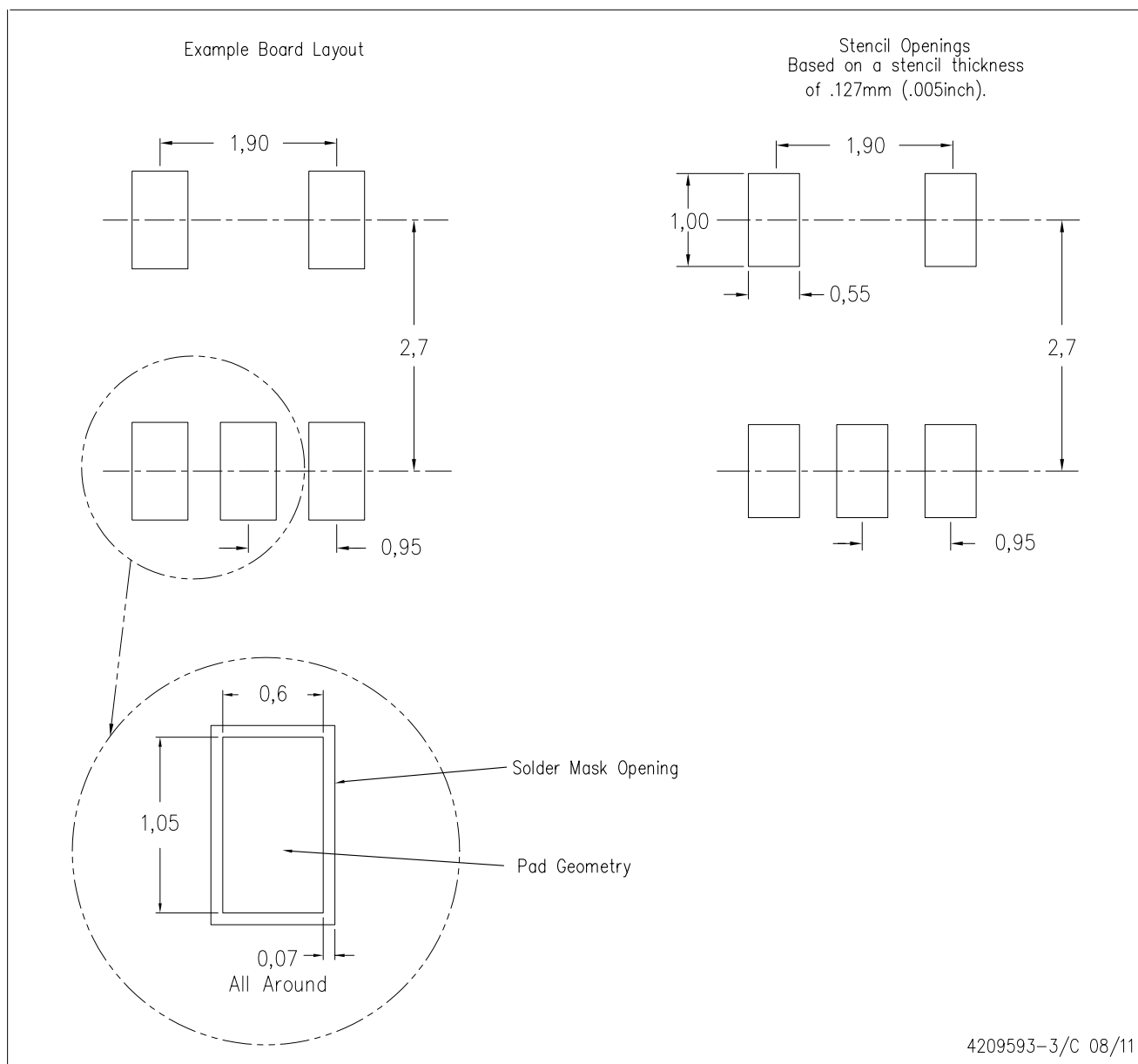


4073253-4/K 03/2006

- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
 - D. Falls within JEDEC MO-178 Variation AA.

DBV (R-PDSO-G5)

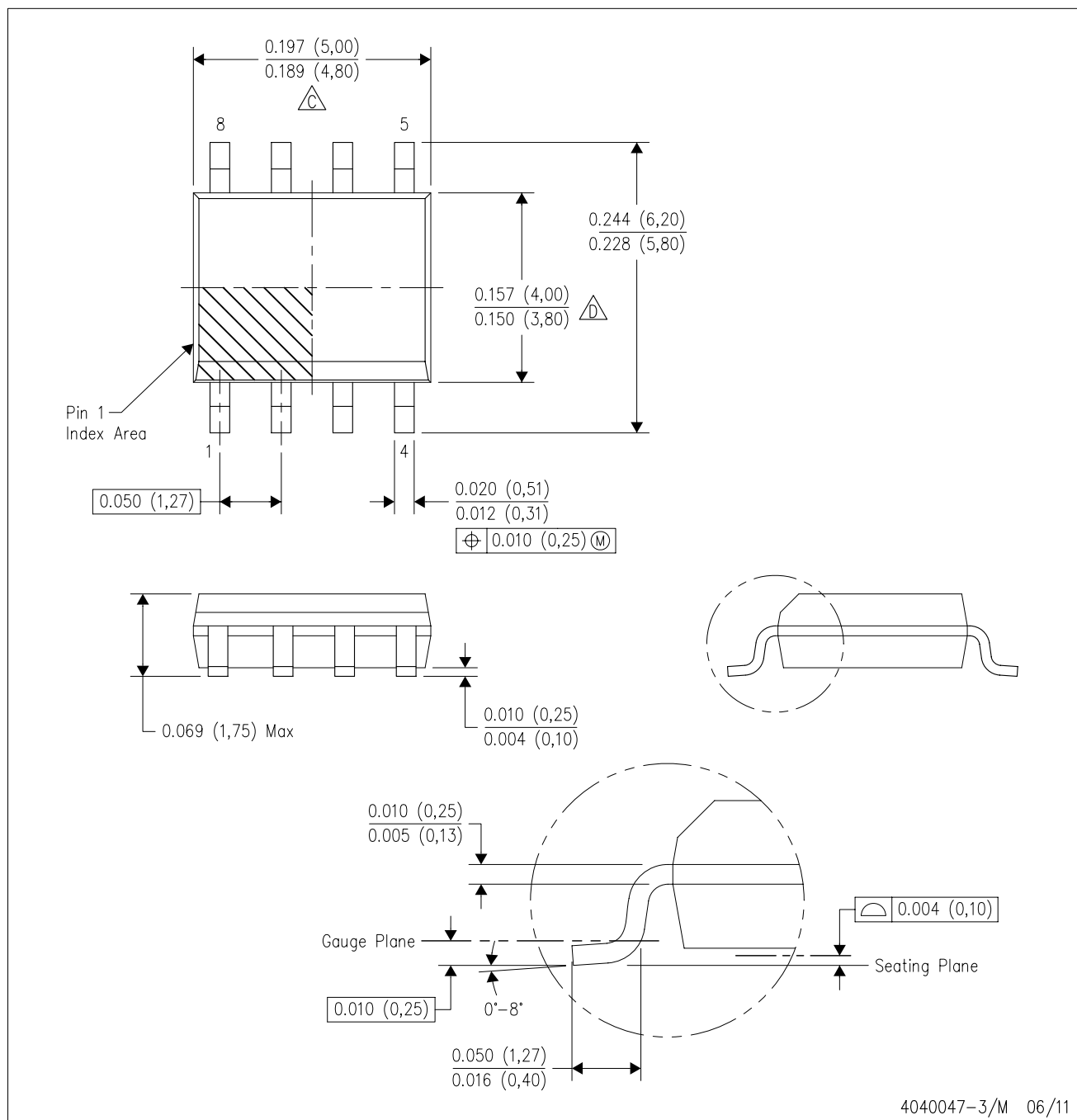
PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
 - D. Publication IPC-7351 is recommended for alternate designs.
 - E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.

D (R-PDSO-G8)

PLASTIC SMALL OUTLINE

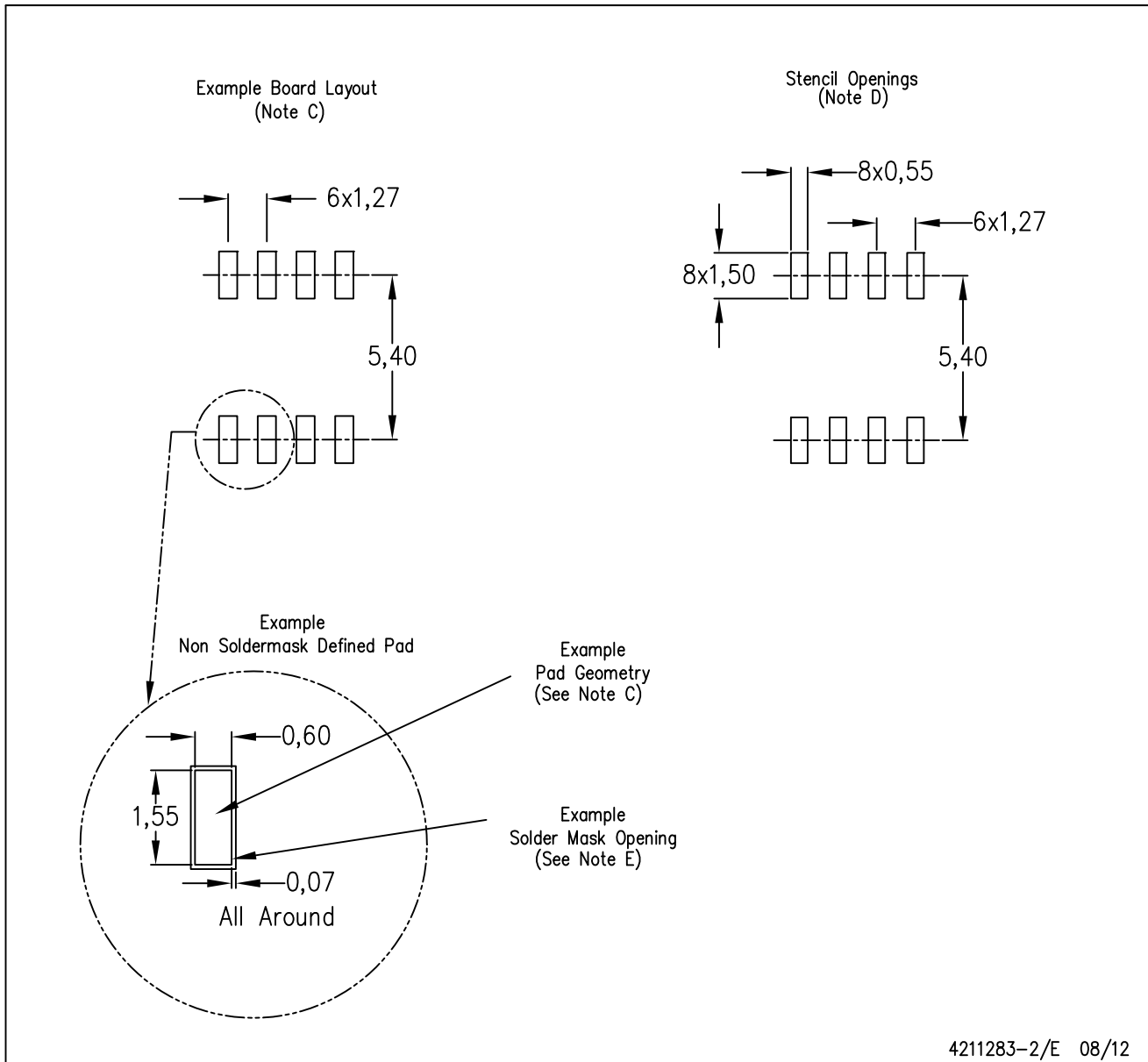


NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- $\triangle C$ Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- $\triangle D$ Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AA.

D (R-PDSO-G8)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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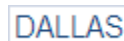
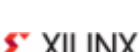
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