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December 4, 2008 FN9192.2

## Digital Multiphase Controller

The ISL6595 digital multiphase controller provides core power for today's high current microprocessors by driving up to six synchronous-rectified buck-converter channels in parallel. Interleaved timing of the channels results in a higher ripple frequency, reducing input and output ripple. With up to six phases, each capable of up to 2MHz operation, the ISL6595 can be used to build DC/DC converters that provide up to 200A with excellent efficiency, low ripple, and the lowest component count.

The ISL6595 utilizes digital technology to implement all control functions, providing the ultimate in flexibility and stability. The ISL6595 incorporates an industry standard $I^2C$ serial interface for control and monitoring. Through the serial interface, the power supply designer can quickly optimize designs and monitor parameters. The interface allows the ISL6595 to provide digitized information for real time system monitoring and control.

The ISL6595 provides superior loadline accuracy through internal calibration that measures and corrects current sense error sources upon start-up. The ISL6595 has programmable current sense temperature compensation that allows the designer to tailor the response for best loadline accuracy over-temperature. Superior loadline accuracy reduces component count and solution cost.

To further reduce component count the ISL6595 incorporates patented Active Transient Response (ATR) technology, allowing the fastest response to transient events for reduced output capacitance.

The flexibility of the ISL6595 allows the power supply designer to implement a wide range of solutions. When used with industry standard power train components, the ISL6595 provides the highest performance with lowest component count and cost.

## Ordering Information

| PART NUMBER (Note) | PART MARKING | TEMP RANGE (°C) | PACKAGE (Pb-Free) | PKG. DWG # |
|---|---|---|---|---|
| ISL6595DRZ* | ISL6595 DRZ | 0 to +85 | 48 Ld 7x7 QFN | L48.7x7P |

*Add "-T" or "-TK" suffix for tape and reel. Please refer to TB347 for details on reel specifications.

NOTE: These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

## Features

- Multiphase Power Conversion
  - 1-Phase to 6-Phase Operation
- 100kHz to 2MHz Switching Frequency
- Supports Intel™ VR10.x and VR11.0 VID Codes
- Supports AMD™ 5-bit and 6-bit VID Codes
- Internal High Precision Voltage Reference
  - ±10mV Voltage Setpoint Accuracy
- Precision Digital Current Sense Calibration
- Precise Digital Current Balancing with Programmable Offsets for Thermal Balancing
- Digitally Programmable Loadline and Loop Compensation
- Differential Voltage Sense
- Digital Temperature Sensor Compensation
- Active Transient Response (ATR) Enables Meeting Transient Requirements With Reduced Output Capacitance
- $I^2C$ Interface for Monitoring, Control and Configuration
- Internal Non-Volatile Memory (NVM) to Store Custom Configurations
- Extensive Fault Detection Capability With Two User Configurable Output Fault Pins (FAULT1, FAULT2)
  - Input Undervoltage
  - Output Under/Overvoltage
  - High Side Short
  - Per Phase and Total Output Current
  - Multiple internal and External Temperature Limits
  - NVM Configuration
  - Calibration Range and Time-Out
- Configurable Latched Fault or Autonomous Recovery Shutdown
- Single +3.3V Supply Operation
- Pb-Free (RoHS compliant)
- 48 Ld QFN Plastic Package

## Applications

- Core Power Regulation For Intel™ and AMD™ Micro-Processors
- Intelligent Point-of-Load (POL) Power Regulation



CAUTION: These devices are sensitive to electrostatic discharge; follow proper IC Handling Procedures.
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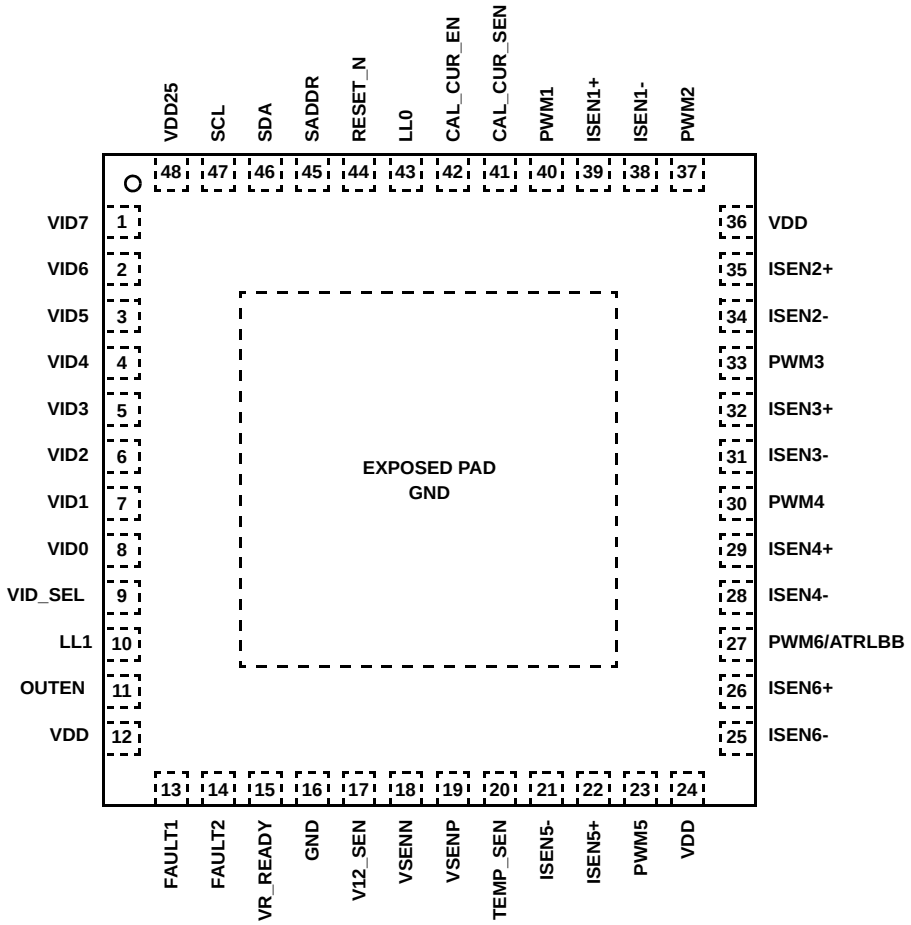
## Pinout

**ISL6595**
**(48 LD QFN)**
TOP VIEW



## Functional Block Diagram (Differential I-Sense Inputs)

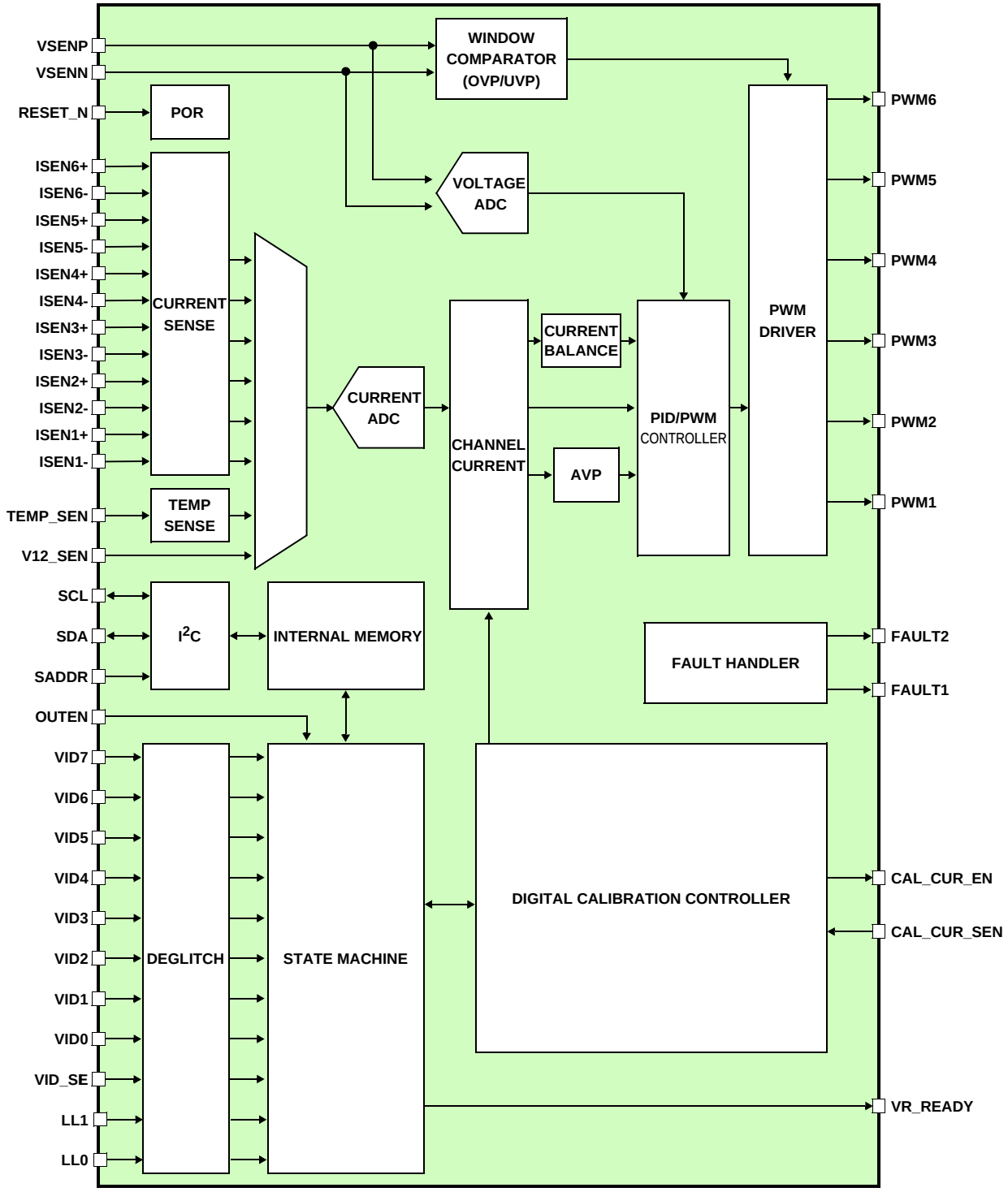



FIGURE 1. BLOCK DIAGRAM FOR DIFFERENTIAL I-SENSE, PWM-ONLY OUTPUT

## Typical VRD Application

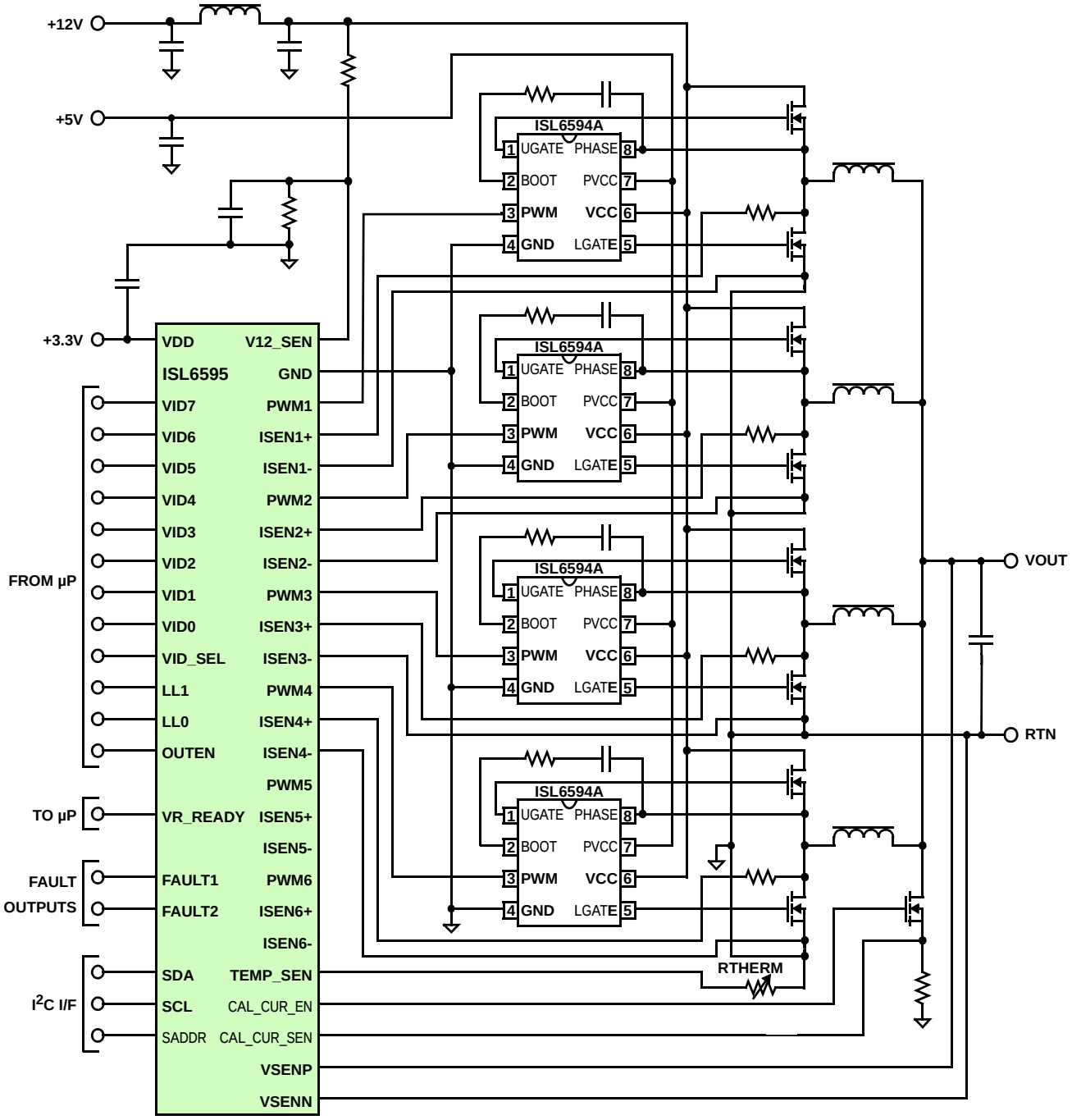



FIGURE 2. 4-PHASE VRD DESIGN

## Absolute Maximum Ratings

Supply Voltage, $V_{DD}$ . . . . . -0.50V to 4.25V
All Pins Except ISENx, VSENP, VSENN and GND . . . . . -0.50V to 4.25V
All ISENx, VSENP, VSENN Pins . . . . . -0.50V to 3.0V
All Ground Pins . . . . . -0.50V to 0.50V
Vapor Phase (60s), $T_{VAPOR}$ . . . . . +215°C
Infrared (15s), $T_{IR}$ . . . . . +220°C

## Thermal Information

| Thermal Resistance (Typical, Notes 1, 2) | $\theta_{JA}$ (°C/W) | $\theta_{JC}$ (°C/W) |
|---|---|---|
| 48 Ld QFN Package. . . . . | 31 | 3 |

Maximum Junction Temperature (Plastic Package) . 0°C to +150°C
Maximum Storage Temperature Range . . . . . -65°C to +150°C
Pb-free reflow profile . . . . . .see link below
http://www.intersil.com/pbfree/Pb-FreeReflow.asp

## Recommended Operating Conditions

Temperature Range . . . . . 0°C to +85°C
Supply Voltage Range . . . . . +3.0V to +3.60V
Operating Case Temperature . . . . . 0°C to +125°C
Operating Ambient Temperature . . . . . 0°C to +85°C

*CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.*

1. $\theta_{JA}$ is measured in free air with the component mounted on a high effective thermal conductivity test board with “direct attach” features. See Tech Brief TB379.
2. For $\theta_{JC}$, the “case temp” location is the center of the exposed metal pad on the package underside.

## Electrical Specifications

$V_{DD}$ = +3.3V, $T_C$ = +25°C, unless otherwise specified. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested

| PARAMETER | SYMBOL | TEST CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| **VDD SUPPLY** | | | | | | |
| Nominal Supply Current | $I_{VDD}$ | | - | 100 | 140 | mA |
| **RESET_N** | | | | | | |
| Input LOW Voltage | | | -0.3 | - | 0.5 | V |
| Input HIGH Voltage | | | 2.8 | - | 3.6 | V |
| Input Current, Input Voltage LOW | | VIN = 0.0V | -75 | - | -10 | µA |
| Input Current, Input Voltage HIGH | | VIN = 3.5V | - | - | - | µA |
| **VID[7:0], OUTEN, LL0, LL1, VID_SEL (Note 3)** | | | | | | |
| Input Low Voltage | | | -0.3 | - | 0.4 | V |
| Input High Voltage (Note 4) | | | 0.8 | - | 5.5 | V |
| Input Current, Input Voltage Low | | VIN = 0.0V | - | -20 | -30 | µA |
| Input Current, Input Voltage High | | VIN = 3.5V | - | 15 | 25 | µA |
| **OUTEN INPUT** | | | | | | |
| Input Threshold | $V_{T_VR_EN}$ | | 0.8 | 0.85 | 0.9 | V |
| Input Hysteresis | $V_{H_VR_EN}$ | | - | 100 | - | mV |
| Input Bandwidth | | | - | - | 20 | MHz |
| **SDA, SCL INPUTS** | | | | | | |
| Input LOW Voltage | $V_{IL_S}$ | | -0.3 | - | 0.8 | V |
| Input HIGH Voltage | $V_{IH_S}$ | | 2.4 | - | 5.5 | V |
| Input Current, Input Voltage Low | $I_{IL_S}$ | VIN = 0.0V | -10 | - | 10 | µA |
| Input Current, Input Voltage High | $I_{IH_S}$ | VIN = 3.5V | -10 | - | 10 | µA |
| Output LOW Voltage | | | - | - | 0.4 | V |
| **VSENP, VSENN INPUTS** | | | | | | |
| VSENN Voltage (Note 5) | | | -0.3 | - | 0.3 | V |

**Electrical Specifications** $V_{DD}$ = +3.3V, $T_C$ = +25°C, unless otherwise specified. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested **(Continued)**

| PARAMETER | SYMBOL | TEST CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| Bandwidth | | | - | - | 1.5 | MHz |
| VSENP | | VSENP = 1.6V | -10 | - | 10 | µA |
| VSENN | | VSENN = 0V | -10 | - | 10 | µA |
| **ISEN[6:1]+ INPUTS** | | | | | | |
| Input Current Range | | | -275 | - | -10 | µA |
| Input Resistance | | | - | 100 | - | Ω |
| Clamp Voltage | | | - | 1.65 | - | V |
| I-sense Amplifier Linearity Error | | $T_A$ = +25°C | - | - | 1.6 | % |
| | | $T_A$ = 0°C to +85°C | - | - | 2 | % |
| Current Conversion ADC Error | | $T_A$ = +25°C | - | - | 2 | % |
| | | $T_A$ = 0°C to +85°C | - | - | 2.2 | % |
| Single-Ended $r_{DS(ON)}$ Mode Bias Voltage | | Programmable from 25mV to 100mV | -18 | - | 18 | mV |
| Differential $r_{DS(ON)}$ Mode Bias Voltage | | Programmable from 25mV to 100mV | -18 | - | 18 | mV |
| **ISEN[6:1]- DCR SENSE MODE** | | | | | | |
| Bias Current Accuracy | | Programmable from 0µA to 37.5µA | - | - | - | µA |
| 0µA Setting | | | -2.5 | - | 2.5 | µA |
| -12.5µA Setting | | | -16 | - | 9 | µA |
| -25µA Setting | | | -30 | - | 20 | µA |
| -37.5µA Setting | | | -45 | - | 30 | µA |
| **CAL_CUR_SEN INPUT** | | | | | | |
| Sensed Voltage | | $R_{SEN}$ = 20mΩ, Ical = 10A | 0.19 | - | 0.22 | V |
| **TEMP_SEN INPUT** | | | | | | |
| Bias Voltage | | $I_{IN}$ = -20µA | - | 295 | - | mV |
| Input Current Range | | | -275 | - | -10 | µA |
| Input Resistance | | | - | 200 | - | Ω |
| **V12_SEN INPUT** | | | | | | |
| Voltage Threshold (Turn-On) | | $T_A$ = +25°C | 1.15 | - | 1.25 | V |
| | | $T_A$ = 0°C to +85°C | 1.14 | - | 1.26 | V |
| Voltage Threshold (Turn-Off) | | $T_A$ = +25°C | 0.95 | - | 1.05 | V |
| | | $T_A$ = 0°C to +85°C | 0.94 | - | 1.05 | V |
| **SADDR INPUT** | | | | | | |
| Input LOW Voltage | | | -0.3 | - | 0.1 | V |
| Input HIGH Voltage | | | VDD-0.1 | - | 3.6 | V |
| Input Current, Input Voltage LOW | | | -800 | - | -400 | µA |
| Input Current, Input Voltage HIGH | | | 400 | - | 800 | µA |
| Tri-State Input Bias Voltage | | | 1.5 | - | 1.8 | V |

## Electrical Specifications

$V_{DD}$ = +3.3V, $T_C$ = +25°C, unless otherwise specified. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested **(Continued)**

| PARAMETER | SYMBOL | TEST CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| **PWM[6:1] OUTPUTS** | | | | | | |
| Output LOW Voltage | $V_{OL}$ | Open drain output, $I_{LOAD}$ = +5mA | - | - | 0.4 | V |
| Output LOW Voltage | $V_{OL}$ | Open drain output, $I_{LOAD}$ = +16mA | - | 0.5 | - | V |
| **FAULT1, FAULT2 OUTPUTS** | | | | | | |
| Output LOW Voltage | $V_{OL}$ | $I_{LOAD}$ = +5mA | - | - | 0.4 | V |
| Output LOW Voltage | $V_{OL}$ | Open drain output, $I_{LOAD}$ = +16mA | - | 0.5 | - | V |
| Output HIGH Voltage | $V_{OH}$ | $I_{LOAD}$ = -5mA | 2.4 | - | - | V |
| Output Current in Hi-Z State | $I_{OZ}$ | $V_{OUT}$ = 1.65V | -10 | - | 10 | µA |
| **CAL_CUR_EN OUTPUT** | | | | | | |
| Output LOW Voltage | $V_{OL}$ | $I_{LOAD}$ = +500µA | - | - | 0.4 | V |
| Output HIGH Voltage | $V_{OH}$ | $I_{LOAD}$ = -1mA | 2.8 | - | - | V |
| **VR_READY OUTPUT** (Note 3) | | | | | | |
| Output Low Voltage | $V_{OL}$ | $I_{LOAD}$ = ±500µA | 0 | - | 0.3 | V |
| Output High Voltage | $V_{OH}$ | $I_{LOAD}$ = ±500µA | 0.8 | - | 3.3 | V |
| Transition Edge Rate | | From 10% to 90% | - | - | 150 | ns |
| **SETPOINT ACCURACY** | | | | | | |
| Setpoint Accuracy (Note 5) | $V_{REF}$ | VID = 1.20V, $T_A$ = +25°C | -8 | - | +8 | mV |
| | | VID = 0.85V to 1.65V, $T_A$ = 0°C to +85°C | -10 | - | +10 | mV |
| Voltage Conversion Gain Error (Note 5) | $G_{REF3}$ | $T_A$ = +25°C | - | - | 0.4 | % |
| | | $T_A$ = 0°C to +85°C | - | - | 0.75 | % |
| Voltage Conversion ADC Error INL (Note 5) | INLVADC | $T_A$ = +25°C | - | - | 8.5 | mV |
| | | $T_A$ = 0°C to +85°C | - | - | 9 | mV |
| **SWITCHING FREQUENCY, RANGE 100kHz TO 2MHz (Note 6)** | | | | | | |
| Frequency Accuracy (Note 6) | | $T_A$ = +25°C | -5 | - | 5 | % |
| | | $T_A$ = 0°C to +85°C, VDD = 3.0V to 3.6V | -10 | - | 10 | % |
| **FAULT MONITORS** | | | | | | |
| OUVP Threshold Voltage | $V_{OUVP}$ | | 0.35 | 0.40 | 0.45 | V |
| OOVP Threshold Accuracy (Note 5) | | Programmable from 0.225V to 1.8V | -50 | - | 50 | mV |
| Internal OTP Threshold Range | | See PTAT shut_down in Table 4 | - | - | - | |
| Internal OTP Threshold Accuracy | | | -10 | - | 10 | °C |
| IUVP Rising Threshold Voltage | $V_{IUVP_LH}$ | | 1.15 | - | 1.25 | V |
| IUVP Falling Threshold Voltage | $V_{IUVP_HL}$ | | 0.95 | - | 1.05 | V |

NOTES:

3. An open input will float to the logic-1 state. This feature is not intended as a replacement for an external pull-up resistor when the input is driven by an open-drain driver.
4. VIH(max) is guaranteed but not tested. Input current is typically less than 2mA at VIH = +4V. In applications requiring +5.5V tolerance, the device must be driven by a source impedance greater than 1kΩ.
5. Limits established by characterization and are not production tested.
6. Setting is programmable.

## Pin Description

| PIN # | NAME | I/O | TYPE | DESCRIPTION |
|---|---|---|---|---|
| 1 | VID7 | I | 1.2V CMOS | Bit 7 of processor voltage identification word (MSB of 8-bit VID word). |
| 2 | VID6 | I | 1.2V CMOS | Bit 6 of processor voltage identification word. |
| 3 | VID5 | I | 1.2V CMOS | Bit 5 of processor voltage identification word. |
| 4 | VID4 | I | 1.2V CMOS | Bit 4 of processor voltage identification word. |
| 5 | VID3 | I | 1.2V CMOS | Bit 3 of processor voltage identification word. |
| 6 | VID2 | I | 1.2V CMOS | Bit 2 of processor voltage identification word. |
| 7 | VID1 | I | 1.2V CMOS | Bit 1 of processor voltage identification word. |
| 8 | VID0 | I | 1.2V CMOS | Bit 0 of processor voltage identification word (LSB of 8-bit VID word). |
| 9 | VID_SEL | I | 1.2V CMOS | VID table selection input.<br>“1” → VR11 VID table selected<br>“0” → VR10 VID table selected |
| 10 | LL1 | I | 1.2V CMOS | Processor load line select input control signal (MSB). Selects regulator load line resistance. |
| 11 | OUTEN | I | 1.2V CMOS | Processor output enable input signal used to command the regulator output.<br>“1” → Regulator output voltage enabled<br>“0” → Regulator output voltage disabled |
| 12 | VDD | I | VDD | 3.3V power supply connection; decoupling cap should be placed close to pin. |
| 13 | FAULT1 | O | 3.3V CMOS | Programmable fault indicator #1. |
| 14 | FAULT2 | O | 3.3V CMOS | Programmable fault indicator #2. |
| 15 | VR_READY | O | Open Drain | Digital Controller output signal to indicate the regulator output voltage is within the specified range.<br>“1” → µP VCC within 10% of target regulation voltage<br>“0” → µP VCC outside 10% of target regulation voltage |
| 16 | GND | | | Pin used in test mode only, tie to Ground for normal operation. |
| 17 | V12_SEN | I | Analog | 12V voltage divider input. Used to guarantee valid input power supply before starting up (undervoltage lockout). |
| 18 | VSENN | I | Analog | Negative voltage sense input. |
| 19 | VSENP | I | Analog | Positive voltage sense input. |
| 20 | TEMP_SEN | I | Analog | External thermistor temperature sense. Connected to ground through a negative TC thermistor, with series and shunt resistance added to achieve desired range. See “External Temperature Sense” on page 13 for more information. |
| 21 | ISEN5- | I | | Phase channel #5 ADC current sense (-) input, tie to ground if the phase is unused. |
| 22 | ISEN5+ | I | Analog | Phase channel #5 ADC current sense (+) input. |
| 23 | PWM5 | O | 3.3V CMOS | Phase channel #5 PWM output. |
| 24 | VDD | I | VDD | 3.3V power supply connection; decoupling cap should be placed close to pin. |
| 25 | ISEN6- | I | | Phase channel #6 ADC current sense (-) input, tie to ground if the phase is unused. |
| 26 | ISEN6+ | I | Analog | Phase channel #6 ADC current sense (+) input. |
| 27 | PWM6/ATRLBB | O | 3.3V CMOS | Phase channel #6 PWM output or optional external ATRL output. |
| 28 | ISEN4- | I | | Phase channel #4 ADC current sense (-) input, tie to ground if the phase is unused. |
| 29 | ISEN4+ | I | Analog | Phase channel #4 ADC current sense (+) input. |
| 30 | PWM4 | O | 3.3V CMOS | Phase channel #4 PWM output. |
| 31 | ISEN3- | I | | Phase channel #3 ADC current sense (-) input, tie to ground if the phase is unused. |
| 32 | ISEN3+ | I | Analog | Phase channel #3 ADC current sense (+) input. |
| 33 | PWM3 | O | 3.3V CMOS | Phase channel #3 PWM output. |

## Pin Description (Continued)

| PIN # | NAME | I/O | TYPE | DESCRIPTION |
|---|---|---|---|---|
| 34 | ISEN2- | I | | Phase channel #2 ADC current sense (-) input, tie to ground if the phase is unused. |
| 35 | ISEN2+ | I | Analog | Phase channel #2 ADC current sense (+) input. |
| 36 | VDD | I | VDD | 3.3V power supply connection, decoupling cap should be placed close to pin. |
| 37 | PWM2 | O | 3.3V CMOS | Phase channel #2 PWM output. |
| 38 | ISEN1- | I | | Phase channel #1 ADC current sense (-) input, tie to ground if the phase is unused. |
| 39 | ISEN1+ | I | Analog | Phase channel #1 ADC current sense (+) input. |
| 40 | PWM1 | O | 3.3V CMOS | Phase channel #1 PWM output. |
| 41 | CAL_CUR_SEN | I | Analog | Calibration current sense input. Measures the voltage across the calibration sense resistor and adjusts CAL_CUR_EN via an op amp loop such that the voltage across the resistor is 200mV. |
| 42 | CAL_CUR_EN | O | Analog | Calibration current enable output. Drives the calibration FET gate voltage to adjust its $r_{DS(ON)}$ such that voltage across the sense resistor is set at 200mV. |
| 43 | LL0 | I | 1.2V CMOS | Processor load line select input control signal (LSB). Selects regulator load line resistance and loadline offset voltage. |
| 44 | RESET_N | I | 3.3V CMOS | Active LOW asynchronous system reset to place ISL6595 into default state.<br>“1” → asynchronous reset disabled<br>“0” → asynchronous reset enabled |
| 45 | SADDR | I | 3.3V CMOS | $I^2C$ address LSB select.<br>“1” → Address 1110001 selected<br>“0” → Address 1110000 selected |
| 46 | SDA | I | 3.3V CMOS | $I^2C$ interface serial data line. |
| 47 | SCL | I | 3.3V CMOS | $I^2C$ interface serial clock line. |
| 48 | VDD25 | I | Analog | Decoupling capacitor for 2.5V internally generated voltage, recommend 0.01µF, 0.1µF max. |

## General Description

The ISL6595 is a digital multiphase pulse width modulation controller integrated circuit for use in 2-phase to 6-phase synchronous buck converter CPU core supply power switching regulators. The device is optimized for delivering voltages from 0.5V to 1.6V at high current levels (120A+) with programmable PWM switching frequencies between 100kHz and 2MHz. The ISL6595 brings the benefit of digital control to voltage regulators targeting Intel™ VRD/VRM 10.x, 11.0 and similar applications.

The ISL6595 is designed to maximize value to the user by providing features, monitoring and performance to minimize the number of required off-chip components, work with a variety of widely available standard components, and to accommodate wider device tolerance mismatches than competing analog controller solutions.

The ISL6595 provides both ease-of-use and flexibility to the user. Major features include:

- **Internal Voltage and Temperature Reference –** An internal factory trimmed ±0.5% voltage reference sets the VID DAC, voltage ADC and current ADC range. In addition, a proportional-to-absolute-temperature (PTAT) reference is generated and digitized to serve as the controller temperature sensor.
- **Internal Oscillator –** Provides a factory trimmed 156.25MHz ±10% clock reference. Fixed and programmable dividers generate all the needed internal clocks to configure the controller’s switching frequency and number of active phases.
- **Dedicated Voltage ADC –** A high precision differential input voltage ADC digitizes the differential remote sense voltage. An integrated anti-alias filter and ripple frequency null filter minimize the impact of high frequency noise on the system.
- **Multiplexed Current Sense ADC –** The average currents from each phase are sensed as a voltage across the low side FET using the multiplexed current ADC. Each phase is sampled at the middle of its cycle, with timing optimized through a programmable delay line. The internal temperature reference and external thermistor temperature are also digitized using the multiplexed current ADC. Gain and offset of the sensor and ADC are compensated through either a one time factory calibration, or through a power-up calibration each time the output voltage is reset.

- **Digital Control Loop and AVP –** An over-sampled digital Proportional-Integral-Derivative (PID) compensator provides flexible loop compensation with programmable coefficients. A digital post-filter provides additional phase lead and/or high frequency filtering to optimize the transient response and ripple of the system. A high accuracy Active Voltage Positioning (AVP) loadline is computed using the calibrated current sense measurements. The AVP bandwidth is also programmable to allow it to be optimized for dynamic performance.
- **Window comparators –** Window comparators with fixed thresholds for input undervoltage lockout (IUVP), output undervoltage and overvoltage protection (OUVP and OOVP). In addition a second OOVP comparator is provided with a programmable threshold with respect to the VID.
- **Active Transient Response (ATR) –** ATR comparators with programmable thresholds are used to provide fast response to dynamic load transients, minimizing spike overshoot and droop undershoot.
- **Configurable PWM Generators –** 1 to 6 PWM waveforms are digitally generated ensuring low jitter and high linearity. PWM outputs are configurable as either single tri-valent outputs or dual outputs with programmable non-overlap delay. Phases can be fully overlapped, with programmable duty cycle limiting.
- **Integrated NVM -** Digital configuration is stored in an integrated NVM, allowing fully independent (stand-alone) operation. NVM is fully accessible to user so that a completely new parameter set can be written. Vendor and user defined memory locations are provided, allowing version control and part identification. NVM integrity is checked every configuration cycle through a cyclic redundancy check (CRC) comparison.
- **Serial Interface –** Intersil PowerCode software provides easy access to all configuration, telemetry, and testability features over a 2 wire $I^2C$ serial interface.

The Intersil PowerCode interface allows full accessibility to regulator telemetry during system operation including:

- Internal Controller Temperature
- External (via optional thermistor) System Temperature
- Per Phase Current
- Total Output Current
- Output Voltage
- Input Voltage
- Configurable latched and unlatched individual fault status
- Microprocessor Leakage Current
- User Defined Memory Space

Fault reporting and shutdown behavior are also fully configurable. Two individual fault outputs are provided (FAULT1, FAULT2), both of which can be masked independently. The outputs can be configured as either latched or unlatched, active high or active low polarity, and CMOS or open drain outputs. The shutdown operation also allows all faults to be individually masked and for the shutdown operation to be either latched or unlatched. Individual status registers allow fault reporting over the serial bus to identify the specific fault event. Fault detection includes the following:

- Input Undervoltage (IUVP)
- Output Overvoltage (OOVP)
- Output Undervoltage (OUVP)
- Per Phase Overcurrent
- Total Output Overcurrent (OCP)
- Two levels of Internal Temperature Protection
- Four levels of External Temperature Protection
- Configuration Failure
- Calibration Time-out Failure

## Theory of Operation

### Power-Up and Initialization

The ISL6595 is designed to provide supply sequence independence and graceful turn-on and turn-off operation. It operates from a single +3.3V supply, while an on-chip low drop-out (LDO) regulator generates an internal +2.5V supply. Power-up controller configuration is initialized by either an internal threshold based power-on reset, or by an external reset pin (RESET_N). During controller configuration, the contents of the NVM are read into the controller's registers. During configuration, all outputs are three-stated, allowing board pull-up or pull-down resistors to set the correct default level.

Once configuration is completed, the controller enters an inactive state. Outputs assume their default values, which may be low, high or three-state. During the inactive state, the controller can communicate over the serial bus, report configuration or inactive state faults. The controller will leave the inactive state and begin soft-start once it has a valid VID, VR_EN is asserted, and the 12V power input is valid. The 12V input is sensed through a resistive divider on the board, and a fixed threshold comparator must be tripped if the input undervoltage lockout is enabled. The sense circuit can be easily modified to also sense an independent or sequenced lower drive voltage typically used to optimize the efficiency of the power stage low side FET.

### Soft-Start and Calibration

Prior to entering an active regulating state, the ISL6595 performs a well-controlled, monotonic initial ramp or "soft-start". Soft-start is performed by actively regulating the load voltage while digitally ramping the target voltage from 0 to the voltage set. During this time, the optional power-up system calibration can be performed. The calibration

algorithm compensates for variations in low-side FET $r_{DS(ON)}$, parasitic inductance and resistance by regulating to a low voltage level, putting a known current load through each phase individually and compensating for the current sense gain and offset error, as well as changes in temperature. Alternatively, default compensation values can be used, or the compensation values can be computed during system test and stored in memory. The external current load needed to perform calibration can be implemented with a precision resistor and N-Channel FET. The voltage across the resistor is sensed and the N-Channel FET gate voltage is adjusted through an internal op amp loop to provide the desired precision current. The calibration current level and the voltage level at which the calibration is performed are both programmable.

After the soft-start ramp is completed, the regulator enters the active regulation state and the VR_READY pin transitions from “0” to “1”, indicating that the microprocessor voltage is within ±10% of the target value.

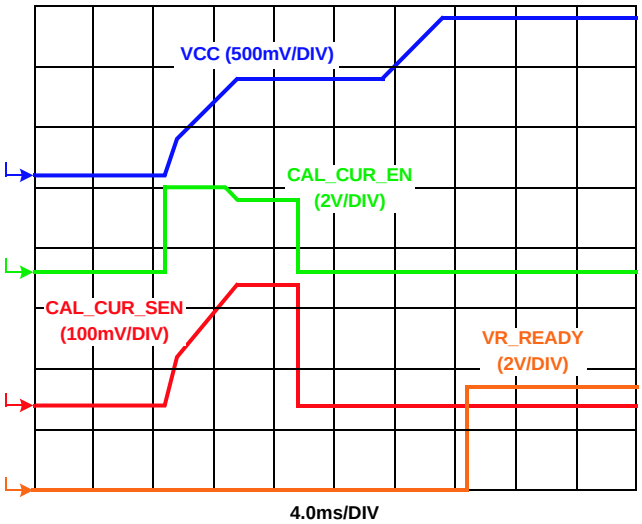



**FIGURE 3. SOFT-START/CALIBRATION SEQUENCE (3-PHASE)**

### *Shutdown*

The ISL6595 also performs a controlled shutdown response to minimize any voltage undershoot. The shutdown state can be entered from the soft-start or active regulation states either through user intervention (de-asserting VR_EN or all one’s VID), or through a detected fault such as over-temperature or output overvoltage. During shutdown, the PWM width is reduced at a steady programmable rate, and then the power stage is three-stated once the pulse width reaches 0.

After shutdown is complete, the controller re-enters the inactive state after a fixed delay. This delay minimizes the duty cycle associated with autonomous restarts if the fault that caused the shutdown disappears once the output is disabled. Alternatively, the fault can be configured so that it is latched and clearing requires user intervention such as toggling VR_EN, toggling RESET_N, or cycling power. If this method is used, the user should ensure adequate delay is provided to complete the shutdown prior to the start of a new start-up. The delay may be as short as 2ms, although longer delays are recommended to minimize the duty cycle in case there is a fault which causes the start-up and shutdown cycle to be repeated indefinitely.

### *Switching Frequency*

Timing is provided by an on-chip, factory trimmed, temperature compensated oscillator.

The ISL6595 operates with a fixed switching frequency (i.e. the switching frequency is fixed independent of load) that is configurable between 100kHz and 2MHz. A programmable divider is used to generate the switching frequency, where the frequency is given by Equation 1:

$$f_{SW} = \frac{156.25\text{MHz}}{2 \times \text{div_sel} \times \text{Nph}} \qquad \text{(EQ. 1)}$$

where $f_{SW}$ is the switching frequency, 156.25MHz is the nominal frequency of the timing reference oscillator, div_sel is the programmable divider ratio between 6 and 127, and Nph is the number of phases between 1 and 6.

Switching frequencies of less than 300kHz and greater than 1.5MHz are supported only for some number of phases used.

### *Output Voltage Sensing and Voltage ADC*

The ISL6595 is built around a high performance digital feedback control loop that senses the differential voltage at the load. This is used to generate the appropriate pulse width modulated (PWM) waveforms to drive the power stages and regulate the load voltage.

The differential sense voltage is digitized with a high speed, high precision analog-to-digital converter (ADC). The on-chip factory trimmed temperature compensated bandgap voltage reference ensures the ADC accuracy is well within the regulator setpoint accuracy requirements. The ADC is sampled synchronously so that there are 2 ADC samples per phase per switching cycle, at a frequency given by Equation 2:

$$f_S = \frac{156.25\text{MHz}}{\text{div_sel}} \qquad \text{(EQ. 2)}$$

The ADC also includes a post-filter which provides a null at $f_{SW}$ * (Nph/2), which is the ripple frequency. This ripple null filter works in conjunction with an internal analog anti-alias filter. The anti-alias filter is a single pole, 2MHz low pass filter. The corner frequency can be lowered by adding series resistors in the board.

### *Current Sensing and Current ADC*

The ISL6595 provides for precise current monitoring in each power stage, allowing for industry-leading loadline accuracy for active voltage positioning (AVP). The current in each power stage is sensed through one of three methods

supported by the ISL6595. These are single-ended $r_{DS(ON)}$ sense of the low-side FET, differential $r_{DS(ON)}$ sense of the low-side FET, or differential DCR sense of the buck inductor. The sensed current is digitized using a multiplexed current ADC.

For low-side $r_{DS(ON)}$ current sense applications, the ISENx+ pin is held at virtual ground with a programmable offset from 25mV to 100mV. An external sense resistor is connected to the drain of the low side FET to monitor the current in this device. The current sourced from the input is then given in Equation 3:

$$ISEN = \frac{(V_{OFFSET} - Vr_{DS(ON)})}{R_{SEN1}} \quad \text{(EQ. 3)}$$

where input current is digitized with the ADC with an effective ADC range of 0µA to 275µA in 4.3µA steps.

For DCR current sense applications, a resistor in series with a capacitor is placed across the inductor for each phase. In this configuration, the resistor is tied to the FET side of the inductor while the capacitor is tied to the load side of the inductor. If the RC values are chosen such that the RC time constant matches the L/DCR time constant, the resultant voltage appearing across the capacitor will equal the voltage across the inductor series resistance and thus represent the current flowing through the inductor. In this application, a sense resistor is then placed from the ISENx+ pin to the load side of the capacitor while the ISENx- pin in placed on the FET side of the capacitor. The current sourced from the input is then given in Equation 4:

$$ISEN = \frac{(V_{OFFSET} - V_{DCR})}{R_{SEN}} \quad \text{(EQ. 4)}$$

where Input current is digitized with the ADC with an effective ADC range of 0µA to 275µA in 4.3µA steps.

### *Differential $r_{DS(ON)}$ Current Sense*

The positive current sense inputs (ISEN1+ to ISEN6+) are held at a virtual ground with a programmable offset from 25mV to 100mV, in 25mV steps. The negative current sense inputs (ISEN1- to ISEN6-) should be tied to the ground plane local to the low side FET being sensed to eliminate the effects of ground differences between the FET and the ISL6595. The large voltage swing at the drain of the low side FET is eliminated by using a series resistor, converting the signal to a current equal to that in Equation 5:

$$ISENSE = \frac{(V_{OFFSET} - V_{DS})}{R_{SENSE}} \quad \text{(EQ. 5)}$$

where $I_{SENSE}$ is the current sourced by the sense input, Voffset is the programmable offset, $V_{DS}$ is the voltage across the low side FET, and $R_{SENSE}$ is an external resistor whose value is chosen to scale the input depending on the expected $r_{DS(ON)}$.

The input current is mirrored and multiplexed, then digitized by the 6-bit current ADC with an effective input range of 0µA to 275µA in 4.3µA steps. The ADC samples the current in each phase once per switching cycle, and the sampling instant can be varied using a programmable delay, such that sampling in the middle of the ON-cycle can be guaranteed.

The current in the power stage can then be inferred from the current ADC measurement if the drain-source resistance ($r_{DS(ON)}$) of the FET is known. The $r_{DS(ON)}$ of each FET can be either programmed as a default value, or it can be determined by running the calibration routine either one time at system test or every time the system starts up. Calibration is performed by providing a known current load while the regulator is on and correcting the gain and offset of the current measurement. This requires the use of a precision external current source consisting of a dedicated calibration FET and sense resistor. The ISL6595 senses the voltage across the resistor and provides a variable voltage to drive the gate of the calibration FET, varying its $r_{DS(ON)}$ such that the current through the FET and resistor are under closed loop control. The calibration current and voltage level at which calibration occurs are programmable, and the calibration routine can be bypassed if the default values are to be used. The $r_{DS(ON)}$ value is compensated for temperature drift using either the on-chip temperature sense or an external thermistor that can be placed close to the power stage.

### *Differential DCR Current Sense*

For DCR current sense applications, a resistor in series with a capacitor is placed across the inductor for each phase. In this configuration, the resistor is tied to the FET side of the inductor while the capacitor is tied to the load side of the inductor. If the RC values are chosen such that the RC time constant matches the L/DCR time constant, the resultant voltage appearing across the capacitor will equal the voltage across the inductor series resistance and thus represent the current flowing through the inductor. In this application, a sense resistor is then placed from the ISENX+ pin to the load side of the capacitor while the ISENX- pin in placed on the FET side of the capacitor. The current sourced from the input is then given in Equation 6:

$$ISEN = \frac{(V_{OFFSET} - V_{DCR})}{R_{SENSE}} \quad \text{(EQ. 6)}$$

where input current is digitized with the ADC with an effective ADC range of 0µA to 275µA in 4.3µA steps.

### External Temperature Sense

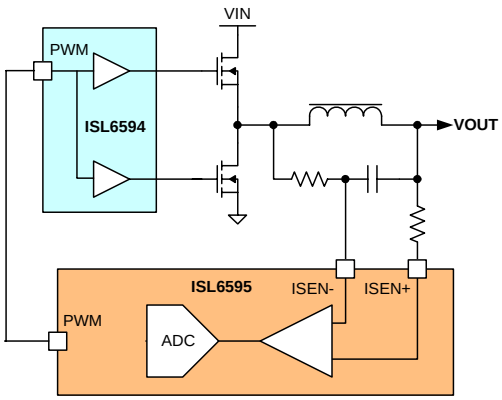



**FIGURE 4. DIFFERENTIAL DCR SENSE**

When configured to sense temperature from an external thermistor, the temperature sense input, TEMP_SEN, is set at virtual ground with a fixed offset of 300mV. An external negative TC thermistor is tied to ground, generating the input current for the measurement. A series and shunt resistor network should be used to scale the resultant current to the proper range. The current range is the same as the current sense inputs, from 0µA to 275µA in 4.3µA steps.

The ADC measurements are converted to temperature using a programmable 4-segment piece-wise linear table while the internal proportional-to-absolute temperature (PTAT) reference is digitized directly, using a linear curve fit. Both internal and external temperature measurements are multiplexed through the current ADC at a low frequency, providing run-time internal and external temperature information to perform temperature compensation, reporting, alerts and shutdown.

### Digital Control Loop and PWM Generation

The digital control loop uses a proportional, integral, and derivative (PID) compensator to drive the digitized sense voltage to the desired target. An additional second derivative gain term and a 2nd order post-filter provide additional high order zeros and poles to further refine the wideband characteristics of the loop. All loop parameters are programmable over a wide range of values, allowing loop bandwidths of 10kHz to 300kHz to be attained depending on the number and type of power stages used.

The effective transfer function of the compensator is given by Equation 7:

$$H(z) = \left(\frac{K_i}{1-z^{-1}} + K_p + K_d((1-z^{-1}) + K_{d2}(1-z^{-1})^2)\right)$$

$$\left(\frac{(1+K_{fd1}+K_{fd2})}{1+K_{fd1}z^{-1}+K_{fd1}z^{-2}}\right)\left(\frac{K_{mod}}{N_{ph}\cdot div_sel}\right)\left(\frac{V_{IN}}{Q}\right) \quad \text{(EQ. 7)}$$

where:

$K_i$, $K_p$, $K_d$, and $K_{d2}$ are the integral, proportional, derivative, and second derivative gain terms

$K_{fd1}$ and $K_{fd2}$ are the coefficients of a second order all pole low pass post-filter

$K_{mod}$ is a programmable maximum duty cycle scaling term

$N_{ph}$ is the number of phases and div_sel is the divider ratio setting the switching frequency

$V_{IN}$ is the power stage input voltage, typically 12V

Q is the ADC step size, 3.125mV

The control loop operates at the same frequency as the voltage ADC, which is synchronous to the switching frequency and given by Equation 8:

$$F_S = 2*Nph*fsw = 156.25MHz/div_sel \quad \text{(EQ. 8)}$$

The compensator digital output is converted to a pulse width using a digital counter based pulse width modulator. The pulse width modulator uses two successive samples to modulate the leading edge and then the trailing edge of a pulse. The modulator provides for monotonic edge placements with a resolution of 100ps. The next two samples are then used to modulate the next phase in the firing sequence. The pulse width modulator is capable of setting a maximum duty cycle limit, overlapping adjacent phases, a minimum pulse width of 13ns, and also producing zero pulse width with minimal glitching.

### Voltage Identification Codes

The target voltage is provided by external parallel 8-bit voltage identification (VID) inputs. The ISL6595 is fully compliant with VRD/VRM 11.0 deglitching and dynamic VID stepping requirements.

**TABLE 1. Intel™ VR10 VID TABLE (WITH 6.25mV EXTENSION, Note 7)**

| $VID_{HI}$ (HEX) | $VID_{LO}$ (HEX) | VOLTAGE (V) | $VID_{HI}$ (HEX) | $VID_{LO}$ (HEX) | VOLTAGE (V) | $VID_{HI}$ (HEX) | $VID_{LO}$ (HEX) | VOLTAGE (V) |
|---|---|---|---|---|---|---|---|---|
| 2 | B | 1.60000 | 5 | 4 | 1.33125 | 0 | 1 | 1.08750 |
| 2 | A | 1.59375 | 5 | 7 | 1.32500 | 0 | 0 | 1.08125 |
| 2 | D | 1.5875 | 5 | 6 | 1.31875 | 0 | 3 | 1.07500 |
| 2 | C | 1.58125 | 5 | 9 | 1.31250 | 0 | 2 | 1.06875 |
| 2 | F | 1.57500 | 5 | 8 | 1.30625 | 0 | 5 | 1.06250 |
| 2 | E | 1.56875 | 5 | B | 1.30000 | 0 | 4 | 1.05625 |
| 3 | 1 | 1.56250 | 5 | A | 1.29375 | 0 | 7 | 1.05000 |
| 3 | 0 | 1.55625 | 5 | D | 1.28750 | 0 | 6 | 1.04375 |
| 3 | 3 | 1.55000 | 5 | C | 1.28125 | 0 | 9 | 1.03750 |
| 3 | 2 | 1.54375 | 5 | F | 1.27500 | 0 | 8 | 1.03125 |
| 3 | 5 | 1.53750 | 5 | E | 1.26875 | 0 | B | 1.02500 |
| 3 | 4 | 1.53125 | 6 | 1 | 1.26250 | 0 | A | 1.01875 |
| 3 | 7 | 1.52500 | 6 | 0 | 1.25625 | 0 | D | 1.01250 |
| 3 | 6 | 1.51875 | 6 | 3 | 1.25000 | 0 | C | 1.00625 |
| 3 | 9 | 1.51250 | 6 | 2 | 1.24375 | 0 | F | 1.00000 |
| 3 | 8 | 1.50625 | 6 | 5 | 1.23750 | 0 | E | 0.99375 |
| 3 | B | 1.50000 | 6 | 4 | 1.23125 | 1 | 1 | 0.98750 |
| 3 | A | 1.49375 | 6 | 7 | 1.22500 | 1 | 0 | 0.98125 |
| 3 | D | 1.4875 | 6 | 6 | 1.21875 | 1 | 3 | 0.97500 |
| 3 | C | 1.48125 | 6 | 9 | 1.21250 | 1 | 2 | 0.96875 |
| 3 | F | 1.47500 | 6 | 8 | 1.20625 | 1 | 5 | 0.96250 |
| 3 | E | 1.46875 | 6 | B | 1.20000 | 1 | 4 | 0.95625 |
| 4 | 1 | 1.46250 | 6 | A | 1.19375 | 1 | 7 | 0.95000 |
| 4 | 0 | 1.45625 | 6 | D | 1.18750 | 1 | 6 | 0.94375 |
| 4 | 3 | 1.45000 | 6 | C | 1.18125 | 1 | 9 | 0.93750 |
| 4 | 2 | 1.44375 | 6 | F | 1.17500 | 1 | 8 | 0.93125 |
| 4 | 5 | 1.43750 | 6 | E | 1.16875 | 1 | B | 0.92500 |
| 4 | 4 | 1.43125 | 7 | 1 | 1.16250 | 1 | A | 0.91875 |
| 4 | 7 | 1.42500 | 7 | 0 | 1.15625 | 1 | D | 0.91250 |
| 4 | 6 | 1.41875 | 7 | 3 | 1.15000 | 1 | C | 0.90625 |
| 4 | 9 | 1.41250 | 7 | 2 | 1.14375 | 1 | F | 0.90000 |
| 4 | 8 | 1.40625 | 7 | 5 | 1.13750 | 1 | E | 0.89375 |
| 4 | B | 1.40000 | 7 | 4 | 1.13125 | 2 | 1 | 0.88750 |
| 4 | A | 1.39375 | 7 | 7 | 1.12500 | 2 | 0 | 0.88125 |
| 4 | D | 1.3875 | 7 | 6 | 1.11875 | 2 | 3 | 0.87500 |
| 4 | C | 1.38125 | 7 | 9 | 1.11250 | 2 | 2 | 0.86875 |
| 4 | F | 1.37500 | 7 | 8 | 1.10625 | 2 | 5 | 0.86250 |

**TABLE 1. Intel™ VR10 VID TABLE (WITH 6.25mV EXTENSION, Note 7) (Continued)**

| $VID_{HI}$ (HEX) | $VID_{LO}$ (HEX) | VOLTAGE (V) | $VID_{HI}$ (HEX) | $VID_{LO}$ (HEX) | VOLTAGE (V) | $VID_{HI}$ (HEX) | $VID_{LO}$ (HEX) | VOLTAGE (V) |
|---|---|---|---|---|---|---|---|---|
| 4 | E | 1.36875 | 7 | B | 1.1 | 2 | 4 | 0.85625 |
| 5 | 1 | 1.36250 | 7 | A | 1.09375 | 2 | 7 | 0.85000 |
| 5 | 0 | 1.35625 | 7 | D | OFF | 2 | 6 | 0.84375 |
| 5 | 3 | 1.35000 | 7 | C | OFF | 2 | 9 | 0.83750 |
| 5 | 2 | 1.34375 | 7 | F | OFF | 2 | 8 | 0.83125 |
| 5 | 5 | 1.33750 | 7 | E | OFF | | | |

NOTE:

7. $VID_{HI}$ = (VID4, VID3, VID2), $VID_{LO}$ = (VID1, VID0, VID5, VID6.25).

TABLE 2. Intel™ VR10 VID TABLE (8-BIT, Note 8)

| $VID_{HI}$ (HEX) | $VID_{LO}$ (HEX) | VOLTAGE (V) | $VID_{HI}$ (HEX) | $VID_{LO}$ (HEX) | VOLTAGE (V) |
|---|---|---|---|---|---|
| 0 | 0 | OFF | 3 | 0 | 1.31250 |
| 0 | 1 | OFF | 3 | 1 | 1.30625 |
| 0 | 2 | 1.60000 | 3 | 2 | 1.30000 |
| 0 | 3 | 1.59375 | 3 | 3 | 1.29375 |
| 0 | 4 | 1.58750 | 3 | 4 | 1.28750 |
| 0 | 5 | 1.58125 | 3 | 5 | 1.28125 |
| 0 | 6 | 1.57500 | 3 | 6 | 1.27500 |
| 0 | 7 | 1.56875 | 3 | 7 | 1.26875 |
| 0 | 8 | 1.56250 | 3 | 8 | 1.26250 |
| 0 | 9 | 1.55625 | 3 | 9 | 1.25625 |
| 0 | A | 1.55000 | 3 | A | 1.25000 |
| 0 | B | 1.54375 | 3 | B | 1.24375 |
| 0 | C | 1.53750 | 3 | C | 1.23750 |
| 0 | D | 1.53125 | 3 | D | 1.23125 |
| 0 | E | 1.52500 | 3 | E | 1.22500 |
| 0 | F | 1.51875 | 3 | F | 1.21875 |
| 1 | 0 | 1.51250 | 4 | 0 | 1.21250 |
| 1 | 1 | 1.50625 | 4 | 1 | 1.20625 |
| 1 | 2 | 1.50000 | 4 | 2 | 1.20000 |
| 1 | 3 | 1.49375 | 4 | 3 | 1.19375 |
| 1 | 4 | 1.48750 | 4 | 4 | 1.18750 |
| 1 | 5 | 1.48125 | 4 | 5 | 1.18125 |
| 1 | 6 | 1.47500 | 4 | 6 | 1.17500 |
| 1 | 7 | 1.46875 | 4 | 7 | 1.16875 |
| 1 | 8 | 1.46250 | 4 | 8 | 1.16250 |
| 1 | 9 | 1.45625 | 4 | 9 | 1.15625 |
| 1 | A | 1.45000 | 4 | A | 1.15000 |
| 1 | B | 1.44375 | 4 | B | 1.14375 |
| 1 | C | 1.43750 | 4 | C | 1.13750 |
| 1 | D | 1.43125 | 4 | D | 1.13125 |
| 1 | E | 1.42500 | 4 | E | 1.12500 |
| 1 | F | 1.41875 | 4 | F | 1.11875 |
| 2 | 0 | 1.41250 | 5 | 0 | 1.11250 |
| 2 | 1 | 1.40625 | 5 | 1 | 1.10625 |
| 2 | 2 | 1.40000 | 5 | 2 | 1.10000 |
| 2 | 3 | 1.39375 | 5 | 3 | 1.09375 |
| 2 | 4 | 1.38750 | 5 | 4 | 1.08750 |
| 2 | 5 | 1.38125 | 5 | 5 | 1.08125 |
| 2 | 6 | 1.37500 | 5 | 6 | 1.07500 |

TABLE 2. Intel™ VR10 VID TABLE (8-BIT, Note 8) (Continued)

| $VID_{HI}$ (HEX) | $VID_{LO}$ (HEX) | VOLTAGE (V) | $VID_{HI}$ (HEX) | $VID_{LO}$ (HEX) | VOLTAGE (V) |
|---|---|---|---|---|---|
| 2 | 7 | 1.36875 | 5 | 7 | 1.06875 |
| 2 | 8 | 1.36250 | 5 | 8 | 1.06250 |
| 2 | 9 | 1.35625 | 5 | 9 | 1.05625 |
| 2 | A | 1.35000 | 5 | A | 1.05000 |
| 2 | B | 1.34375 | 5 | B | 1.04375 |
| 2 | C | 1.33750 | 5 | C | 1.03750 |
| 2 | D | 1.33125 | 5 | D | 1.03125 |
| 2 | E | 1.32500 | 5 | E | 1.02500 |
| 2 | F | 1.31875 | 5 | F | 1.01875 |
| 6 | 0 | 1.01250 | 9 | 0 | 0.71250 |
| 6 | 1 | 1.00625 | 9 | 1 | 0.70625 |
| 6 | 2 | 1.00000 | 9 | 2 | 0.70000 |
| 6 | 3 | 0.99375 | 9 | 3 | 0.69375 |
| 6 | 4 | 0.98750 | 9 | 4 | 0.68750 |
| 6 | 5 | 0.98125 | 9 | 5 | 0.68125 |
| 6 | 6 | 0.97500 | 9 | 6 | 0.67500 |
| 6 | 7 | 0.96875 | 9 | 7 | 0.66875 |
| 6 | 8 | 0.96250 | 9 | 8 | 0.66250 |
| 6 | 9 | 0.95625 | 9 | 9 | 0.65625 |
| 6 | A | 0.95000 | 9 | A | 0.65000 |
| 6 | B | 0.94375 | 9 | B | 0.64375 |
| 6 | C | 0.93750 | 9 | C | 0.63750 |
| 6 | D | 0.93125 | 9 | D | 0.63125 |
| 6 | E | 0.92500 | 9 | E | 0.62500 |
| 6 | F | 0.91875 | 9 | F | 0.61875 |
| 7 | 0 | 0.91250 | A | 0 | 0.61250 |
| 7 | 1 | 0.90625 | A | 1 | 0.60625 |
| 7 | 2 | 0.90000 | A | 2 | 0.60000 |
| 7 | 3 | 0.89375 | A | 3 | 0.59375 |
| 7 | 4 | 0.88750 | A | 4 | 0.58750 |
| 7 | 5 | 0.88125 | A | 5 | 0.58125 |
| 7 | 6 | 0.87500 | A | 6 | 0.57500 |
| 7 | 7 | 0.86875 | A | 7 | 0.56875 |
| 7 | 8 | 0.86250 | A | 8 | 0.56250 |
| 7 | 9 | 0.85625 | A | 9 | 0.55625 |
| 7 | A | 0.85000 | A | A | 0.55000 |
| 7 | B | 0.84375 | A | B | 0.54375 |
| 7 | C | 0.83750 | A | C | 0.53750 |
| 7 | D | 0.83125 | A | D | 0.53125 |

TABLE 2. Intel™ VR10 VID TABLE (8-BIT, Note 8) (Continued)

| $VID_{HI}$ (HEX) | $VID_{LO}$ (HEX) | VOLTAGE (V) | $VID_{HI}$ (HEX) | $VID_{LO}$ (HEX) | VOLTAGE (V) |
|---|---|---|---|---|---|
| 7 | E | 0.82500 | A | E | 0.52500 |
| 7 | F | 0.81875 | A | F | 0.51875 |
| 8 | 0 | 0.81250 | B | 0 | 0.51250 |
| 8 | 1 | 0.80625 | B | 1 | 0.50625 |
| 8 | 2 | 0.80000 | B | 2 | 0.50000 |
| 8 | 3 | 0.79375 | B | 3 | 0.49375 |
| 8 | 4 | 0.78750 | B | 4 | 0.48750 |
| 8 | 5 | 0.78125 | B | 5 | 0.48125 |
| 8 | 6 | 0.77500 | B | 6 | 0.47500 |
| 8 | 7 | 0.76875 | B | 7 | 0.46875 |
| 8 | 8 | 0.76250 | B | 8 | 0.46250 |
| 8 | 9 | 0.75625 | B | 9 | 0.45625 |
| 8 | A | 0.75000 | B | A | 0.45000 |
| 8 | B | 0.74375 | B | B | 0.44375 |
| 8 | C | 0.73750 | B | C | 0.43750 |
| 8 | D | 0.73125 | B | D | 0.43125 |
| 8 | E | 0.72500 | B | E | 0.42500 |
| 8 | F | 0.71875 | B | F | 0.41875 |
| C | 0 | 0.41250 | E | 0 | 0.21250 |
| C | 1 | 0.40625 | E | 1 | 0.20625 |
| C | 2 | 0.40000 | E | 2 | 0.20000 |
| C | 3 | 0.39375 | E | 3 | 0.19375 |
| C | 4 | 0.38750 | E | 4 | 0.18750 |
| C | 5 | 0.38125 | E | 5 | 0.18125 |
| C | 6 | 0.37500 | E | 6 | 0.17500 |
| C | 7 | 0.36875 | E | 7 | 0.16875 |
| C | 8 | 0.36250 | E | 8 | 0.16250 |
| C | 9 | 0.35625 | E | 9 | 0.15625 |
| C | A | 0.35000 | E | A | 0.15000 |
| C | B | 0.34375 | E | B | 0.14375 |
| C | C | 0.33750 | E | C | 0.13750 |
| C | D | 0.33125 | E | D | 0.13125 |
| C | E | 0.32500 | E | E | 0.12500 |
| C | F | 0.31875 | E | F | 0.11875 |
| D | 0 | 0.31250 | F | 0 | 0.11250 |
| D | 1 | 0.30625 | F | 1 | 0.10625 |
| D | 2 | 0.30000 | F | 2 | 0.10000 |
| D | 3 | 0.29375 | F | 3 | 0.09375 |
| D | 4 | 0.28750 | F | 4 | 0.08750 |

TABLE 2. Intel™ VR10 VID TABLE (8-BIT, Note 8) (Continued)

| $VID_{HI}$ (HEX) | $VID_{LO}$ (HEX) | VOLTAGE (V) | $VID_{HI}$ (HEX) | $VID_{LO}$ (HEX) | VOLTAGE (V) |
|---|---|---|---|---|---|
| D | 5 | 0.28125 | F | 5 | 0.08125 |
| D | 6 | 0.27500 | F | 6 | 0.07500 |
| D | 7 | 0.26875 | F | 7 | 0.06875 |
| D | 8 | 0.26250 | F | 8 | 0.06250 |
| D | 9 | 0.25625 | F | 9 | 0.05625 |
| D | A | 0.25000 | F | A | 0.05000 |
| D | B | 0.24375 | F | B | 0.04375 |
| D | C | 0.23750 | F | C | 0.03750 |
| D | D | 0.23125 | F | D | 0.03125 |
| D | E | 0.22500 | F | E | OFF |
| D | F | 0.21875 | F | F | OFF |

NOTE:

8. VID_SEL=1, $VID_{HI}$ = (VID7, VID6, VID5, VID4), $VID_{LO}$ = (VID3, VID2, VID1, VID0)

### *Active Voltage Positioning (AVP)*

The ISL6595 allows selection of both the AVP loadline slope and the VID setpoint offset. The loadline slope is selectable from 0mΩ to 4mΩ, and the setpoint offset is selectable from 0mV to 50mV in 1.56mV steps.

The total current is computed by adding the current measured from each phase, then filtering with a single pole programmable filter to set the AVP bandwidth.

### *Current Balancing/Thermal Balancing*

The ISL6595 also uses the channel current measurements to perform current balancing. To minimize thermal gradient effects, each channel adaptively adjusts its current to match the average channel current.

The current balance function can also be used to induce a thermal gradient if, for example, some channels have greater cooling capability due to better proximity to airflow. The ISL6595 allows the user to independently force an offset current to each channel, creating a current gradient. This causes the current balance to force the channels with greater cooling capability to supply a higher percentage of the total current, creating a net thermal equilibrium amongst all channels.

### *Active Transient Response (ATR)*

Active Transient Response (ATR) is supported through load-line tracking comparators with programmable thresholds. Both internal- and external-loop ATR are supported. Internal-loop ATR engages multiple phases to maximize output current slew rate and minimize spike and droop due to large transient events. Three independent window comparators allows for variation in the number of phases that sink or source. If the transient is slight, only one

phase will respond. If the transient is severe, (up to three phases) respond. This avoids a dramatic sinking or sourcing event, which can cause oscillation. The ISL6595 controller itself uses hysteretic control algorithms after the transient event to ensure that the power stages return to normal operation smoothly with minimal ringing. External-loop ATR (overshoot only) provides an output to engage an additional low latency low side stage capable of quickly discharging the load. This consists of a small low-side FET with a very fast gate driver. Internal- and external-loop ATR can be used independently or in conjunction to optimize transient performance.

### Output Configurations

The ISL6595 provides 6 configurable outputs that are used to drive up to 6-phase power stages. The PWM6 output may also be configured to provide the external loop ATRL output to drive a low side overshoot control FET.

For driving external MOSFETs, tri-valent FET drivers must be used. The driver input circuit has two thresholds (upper and lower) along with a bias network such that its input is centered between the two thresholds when the ISL6595 output driver is three-stated. This allows three values to be defined for the signal, depending whether the output is high, low, or high impedance. If the input signal is high, the gate driver turns the high-side switch on. If the input signal is low, the gate driver turns the low-side switch on. If the input signal is three-state, the driver does not turn either high-side or low-side switches on and the power stage is high impedance or three-stated. Intersil's ISL6594A, ISL6594B and ISL6596 FET drivers are optimized to operate with the ISL6595.

The output drive signals are generated using a 3.3V tri-valent driver. All outputs are tri-stated during reset, configuration, and inactive state. This allows the user to set the appropriate level to tri-state the power stage, using external pull-up or pull-down resistors.

### Output Firing Sequence

The PWM output and current sense (ISEN) pins of the ISL6595 have been assigned such that they can be placed sequentially for PC board layouts (i.e. phase 2 next to 1, phase 3 next to 2, etc...). The output phases are set in a pre-wired firing order to facilitate layout of high phase count systems. For high phase count systems, the VRD layout in the motherboard will likely require the power components to be laid out across two sides of the processor. The firing sequence shown in the table below ensures that for a highly distributed power array, the maximum spatial distribution can be obtained between sequential phases.

**TABLE 3. OUTPUT FIRING SEQUENCE AND NUMBER OF PHASES**

| #P | FIRING SEQUENCE |
|---|---|
| 2 | 1 → 2 → 1 → 2 → 1 → 2 → 1 → 2 → 1 → 2 → 1 → 2 ... |
| 3 | 1 → 2 → 3 → 1 → 2 → 3 → 1 → 2 → 3 → 1 → 2 → 3 ... |
| 4 | 1 → 4 → 2 → 3 → 1 → 4 → 2 → 3 → 1 → 4 → 2 → 3 ... |
| 5 | 1 → 4 → 2 → 5 → 3 → 1 → 4 → 2 → 5 → 3 → 1 → 4 ... |
| 6 | 1 → 4 → 2 → 5 → 3 → 6 → 1 → 4 → 2 → 5 → 3 → 6 ... |

### Fault Detection and Fault Handling

The ISL6595 provides a very flexible fault detection reporting and handling mechanism. Fault detection capability includes:

- Input Undervoltage Protection (IUVP)
- Output Overvoltage Protection (OOVP)
- Output Undervoltage Protection (OUVP)
- Per Phase Overcurrent Protection (OCP)
- Total Output Overcurrent
- Two levels of Internal Temperature Protection
- Four levels of External Temperature Protection
- Configuration Failure
- Calibration Time-out Failure

All individual faults are latched and reported over the serial interface. Two configurable fault outputs are provided (FAULT1, FAULT2). Each output allows independent masking of all faults, allowing a subset of faults to be reported over that pin. The outputs can also be configured as either latched or unlatched, active high or active low polarity, and CMOS or open drain outputs.

Typical usage of the configurable fault pins would be as a crowbar signal to drive an external crowbar device, temperature alert to notify the system a thermal shutdown is imminent, or as an interrupt to cause a micro-controller to poll the fault registers.

Shutdown operation also allows a subset of faults to be individually masked. Additionally, the shutdown recovery can be either autonomous or latched. For autonomous recovery, the faults are not latched, so if the fault condition is eliminated when the controller returns to an inactive state, it will wait for a programmable time period, and then attempt a new soft-start. If the fault condition reoccurs, the controller will recommence the shutdown sequence, continuing this cycle indefinitely until the fault conditions is eliminated. The programmable delay ensures a sufficiently low duty cycle to prevent the regulator components from being damaged from power cycling, assuming the fault condition itself is not immediately destructive.

For latched shutdown, user intervention to clear the latched fault is required before a new soft-start can be attempted. User intervention must come in the form of VR_EN toggle, RESET_N toggle, or controller power cycle.

In addition to fault reporting, there are additional fault handling capabilities specific to each fault type that attempts to provide more graceful fault handling than a shutdown, but more active than simply reporting. The specific fault detection capability and alternate fault handling capability is as follows:

**IUVP:** The V12_SEN input continuously senses the +12V supply through a nominally TBD:1 resistive divider. A comparator with a programmable threshold is used to indicate an undervoltage condition. IUVP can be used to independently provide either an undervoltage lockout prior to soft-start, or to both provide a lockout and force a shutdown during active regulation.

**OOVP/OUVP:** Programmable comparators continuously monitor the VSEN inputs to detect an output overvoltage or undervoltage condition. The OOVP voltage threshold is set relative to VID while OUVP uses a fixed threshold. OOVP is enabled during soft-start and active regulation, while OUVP is enabled only during active regulation.

**OCP:** The OCP (overcurrent protection) continuously monitors all channel currents to determine whether any of the currents are greater than a programmable threshold. Two mechanisms work independently to control overcurrent conditions. A cycle-by-cycle current limit operates by disabling a channel for one cycle when its current exceeds the threshold. A second mechanism monitors the average current for an overcurrent condition. A programmable threshold sets a current limit at which a steeper loadline is implemented, quickly reducing the output voltage downward as the current increases. Both of these mechanisms allow hiccup mode overcurrent protection, where the controller continues to try to provide a regulated output voltage while in overcurrent. Alternatively, a threshold can be set where the overcurrent condition will cause the controller to initiate shutdown.

**Over-Temperature Alert/Shutdown:** Both the internal and external temperature monitors are able to provide fault telemetry in order to shut down the VR in an over-temperature condition. Two programmable thresholds are available for temperature faults. Crossing of the first threshold can be used to only generate a fault report. Crossing the second threshold can be used to cause a shutdown to occur.

**CRC Failure:** The integrity of loading the configuration from the NVM to the controller's registers is checked through a cyclic redundancy code (CRC) check of the data contents. A CRC failure prevents the controller from leaving the inactive state.

**Calibration Failure:** Calibration failure is detected as the inability to achieve a regulation target in the given time-frame. These failures typically indicate a component is damaged or missing.

### *$I^2C$ Interface*

All operating parameters in the ISL6595 are configurable via the $I^2C$ interface. Status can also be read back via the same interface. The ISL6595 operates as a slave at a standard speed of 100kHz.

Three transactions are supported on the $I^2C$ interface:

1. Set current address,
2. Write register,
3. Read register from current address.

All transactions start with a control byte sent from the $I^2C$ master device. The control byte begins with a Start condition, followed by 7-bits of slave address. The last bit sent by the master is the R/W bit and is 0 for a write. If any slaves on the $I^2C$ bus recognize their address, they will Acknowledge by pulling the serial data line low for the last clock cycle in the control byte. If no slaves exist at that address or are not ready to communicate, the data line will be 1, indicating a Not Acknowledge condition. The ISL6595 address on the $I^2C$ bus is 1110_000 or 1110_001, with the LSB set by the input pin SADDR.

To write a register in the ISL6595, the master sends a control byte with the R/W bit set to 0, indicating a write. If it receives an Acknowledge from the ISL6595 it sends a byte representing the address MSB. The ISL6595 will respond with an Acknowledge. The master then sends a byte representing the address LSB. The ISL6595 will respond with an Acknowledge. The master then sends a byte representing the data MS-byte to be written at the current address. The ISL6595 will respond with an Acknowledge. The master then sends a byte representing the data LS-byte to be written at the current address. The ISL6595 will respond with an Acknowledge. The master then issues a Stop condition, indicating to the ISL6595 that the current transaction is complete.

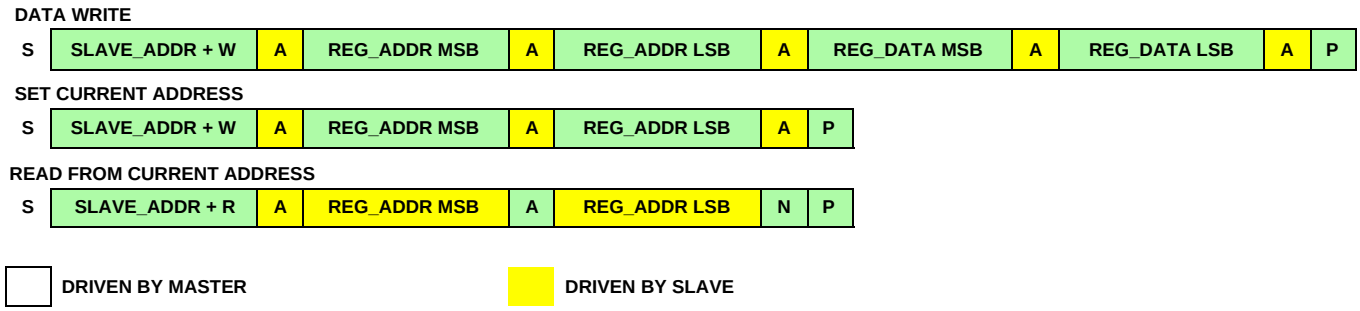
To set the current 16-bit address in the ISL6595, the master sends a control byte with the R/W bit set to 0, indicating a write. If it receives an Acknowledge from the ISL6595 it sends a byte representing the address MS-byte. The ISL6595 will respond with an Acknowledge. The master then sends a byte representing the address LS-byte. The ISL6595 will respond with an Acknowledge. The master then issues a Stop condition, indicating to the ISL6595 that the current transaction is complete. Any read commands issued to the ISL6595 will return data from this address.

To read a register from the ISL6595, the master first sets the address to read from. It then sends a control byte with the R/W-bit set to 1, indicating a read. If it receives an Acknowledge from the ISL6595 it send 8-clocks but does not

drive the serial data line. The ISL6595 will respond with the MS-byte at the current address. The master will respond with an Acknowledge to indicate to the ISL6595 that the transaction is not yet complete. The master again sends 8-clocks but does not drive the serial data line. The ISL6595 will respond with the LS-byte at the current address. The master will respond with a Not Acknowledge to indicate to the ISL6595 that the transaction is complete. The ISL6595 will stop driving the serial data line. The master then issues a Stop condition to indicate that the transaction is complete.

If the ISL6595 has started an internal operation in response to a transaction on the $I^2C$ bus (register read/write, flash write, flash page erase) but the operation has not completed before the last Acknowledge slot in the $I^2C$ bus protocol, the ISL6595 will add wait states by stretching the low portion of the last clock cycle. This also occurs in response to read/write requests to addresses that do not support physical memory in the ISL6595. In this case, the ISL6595 will add wait states until an internal watchdog timer expires, and the $I^2C$ bus is guaranteed to be released.

## $I^2C$ Read and Write Protocol




## Key Registers

Table 4 provides brief descriptions of several key configuration (R/W – read/write) and status (RO – read only) registers available on the ISL6595 Digital Multiphase Controller.

**TABLE 4. KEY REGISTERS**

| REGISTER | DESCRIPTION | FORMAT | RANGE | | RESOLUTION |
|---|---|---|---|---|---|
| | | | MIN | MAX | |
| isum_avg[18:0] | **VR load current.** Averaged sum of all channel current data over a user programmable averaging window (default = 16ms). | RO | 0.00A | 524.288A | 1mA |
| vavp_avg_mon[9:0] | **AVP output voltage.** Averaged VAVP monitored value ADC voltage. | RO | 0.0mV | 3,196.875mV | 3.125mV |
| kavp [9:0] | **AVP loadline slope.** Nominal value of load line slope resistance. | R/W | 0.0Ω | 3.902mΩ | 0.003815mΩ |
| load_line_offset [4:0] | **AVP loadline VID offset.** VID set-point load-line offset tolerance voltage. | R/W | 0.0V | 48.4375mV | 1.5625mV |
| isum_max [7:0] | **Overcurrent limit.** Max load current threshold for over current shutdown. | R/W | 0.0A | +204.0A | 0.800A |
| ptat_mon[5:0] | **PTAT Temperature.** Averaged PTAT calibration temperature output. | RO | 0°C | 157.5°C | 2.5°C |
| ptat_alert_ref[5:0] | **PTAT alert temperature.** PTAT sensor alert temperature reference. | R/W | 0°C | 157.5°C | 2.5°C |
| ptat_shutdown_ref[5:0] | **PTAT shutdown temperature.** PTAT sensor shutdown temperature reference. | R/W | 0°C | 157.5°C | 2.5°C |
| temp_mon[5:0] | **Thermistor temperature.** Averaged Thermistor monitor temperature output. | RO | 0°C | 157.5°C | 2.5°C |
| therm_alert_ref[5:0] | **Thermistor alert temperature.** Thermistor sensor alert temperature reference. | R/W | 0°C | 157.5°C | 2.5°C |
| therm_shutdown_ref[5:0] | **Thermistor shutdown temperature.** Thermistor sensor shutdown temperature reference. | R/W | 0°C | 157.5°C | 2.5°C |

TABLE 4. KEY REGISTERS (Continued)

| REGISTER | DESCRIPTION | FORMAT | RANGE | | RESOLUTION |
|---|---|---|---|---|---|
| | | | MIN | MAX | |
| oovp_limit [5:0] | **Output overvoltage protect threshold.** Tracking VID over voltage threshold. | R/W | 0.0mV | 787.5mV | 12.5mV |
| fault1_mask[12:0]<br>fault2_mask[12:0] | **FAULT1, FAULT2 pin output masks.** Inputs are enabled for reporting when set to logic 1. If multiple inputs are selected, output is “OR” of selected input signals.<br>15 = Current ADC over range<br>14 = Load current monitor<br>13 = Average total current fault<br>12 = NVM fault<br>11 = Internal bus fault<br>10 = IUVP<br>9 = OUVP<br>8 = OOVP<br>7 = VR_HOT alert<br>6 = VR_FAN alert<br>5 = External (thermistor) temp alert<br>4 = External (thermistor) temp shutdown<br>3 = Internal (PTAT) temp alert<br>2 = Internal (PTAT) temp shutdown<br>1 = MHz controller fault<br>0 = Calibration fault | | | | |
| shutdown_mask[10:0] | **Shutdown control mask.** Inputs are enabled for shutdown when set to logic 1. If multiple inputs are selected, output is “OR” of selected input signals.<br>11= Averal total current fault<br>10 = Total current fault during active regulation<br>9 = Total current fault during soft-start<br>8 = Individual phase current fault during active regulation<br>7 = Individual phase current fault during soft-start<br>6 = Current ADC over range fault<br>5 = IUVP<br>4 = OUVP<br>3 = OOVP<br>2 = Thermistor temp shutdown<br>1 = PTAT temp shutdown 0 = Calibration fault<br>0 = Calibration fault | R/W | | | |
| ch_mask[6:1] | **Channel mask.** Selects number of active phases. Phases must be selected in sequential order.<br>000011 = 2-phase operation<br>000111 = 3-phase operation<br>001111 = 4-phase operation<br>011111 = 5-phase operation<br>111111 = 6-phase operation | R/W | | | |

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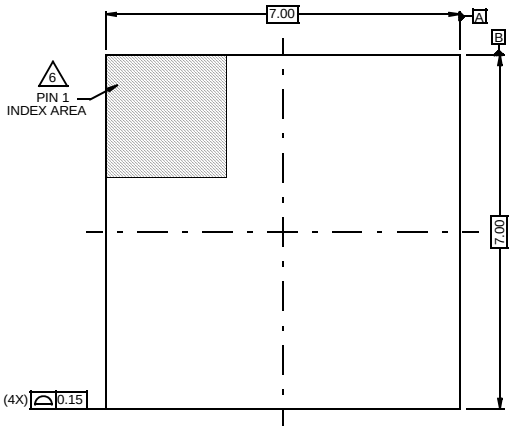
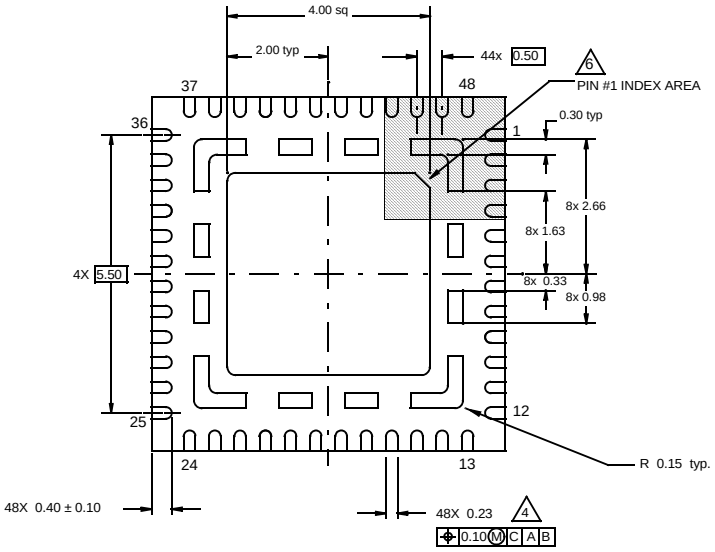
# Package Outline Drawing

## L48.7x7P

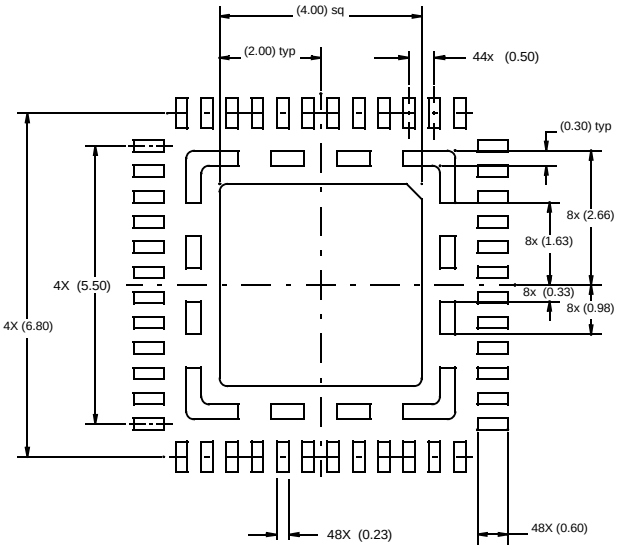
**48 LEAD QUAD FLAT NO-LEAD PLASTIC PACKAGE**
**Rev 1, 7/08**



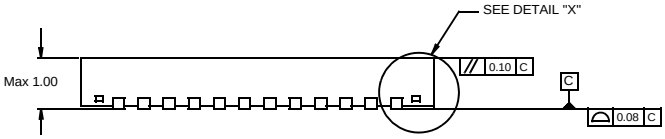

TOP VIEW



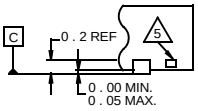

BOTTOM VIEW




TYPICAL RECOMMENDED LAND PATTERN




SIDE VIEW




DETAIL "X"

NOTES:

1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to AMSE Y14.5m-1994.
3. Unless otherwise specified, tolerance : Decimal ± 0.05
4. Dimension b applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
5. Tiebar shown (if present) is a non-functional feature.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.

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