FAIRCHILD SEMICONDUCTOR®

November 2006

FAN4800
Low Start-Up Current PFC/PWM Controller Combos

Features

- Low start-up current (100µA typical)
- Low operating current (2.5mA typical)
- Low total harmonic distortion, high power factor
- Pin-compatible upgrade for the ML4800
- Average current, continuous or discontinuous boost, leading-edge PFC
- Slew rate enhanced transconductance error amplifier for ultra-fast PFC response
- Internally synchronized leading edge PFC and trailing-edge PWM
- Reduction of ripple current in the storage capacitor between the PFC and PWM sections
- PWM configurable for current-mode or voltage-mode operation
- Additional folded-back current limit for PWM section
- 20V BiCMOS process
- V_{IN} OK guaranteed turn-on PWM at 2.25V
- V_{CC} OVP comparator, low-power detect comparator
- Current-fed gain modulator for improved noise immunity
- Brownout control, over-voltage protection, UVLO, soft-start, and reference OK
- Available in 16-DIP, 16-SOIC (wide) packages

Applications

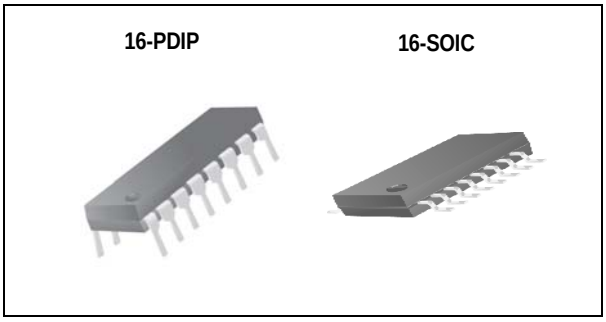
- Desktop PC Power Supply
- Internet Server Power Supply
- Uninterruptible Power Supply (UPS)
- Battery Charger
- DC Motor Power Supply
- Monitor Power Supply
- Telecom System Power Supply
- Distributed Power

Description

The FAN4800 is a controller for power-factor-corrected, switched-mode power supplies. Power Factor Correction (PFC) allows the use of smaller, lower-cost bulk capacitors, reduces power line loading and stress on the switching FETs, and results in a power supply that fully complies with IEC-1000-3-2 specifications. Intended as a BiCMOS version of the industry-standard ML4800, the FAN4800 includes circuits for the implementation of leading edge, average current, boost-type power factor correction, and a trailing-edge Pulse Width Modulator (PWM). A gate driver with 1A capabilities minimizes the need for external driver circuits. Low-power requirements improve efficiency and reduce component costs.

An over-voltage comparator shuts down the PFC section in the event of a sudden decrease in load. The PFC section also includes peak current limiting and input voltage brownout protection. The PWM section can be operated in current or voltage mode, at up to 250kHz, and includes an accurate 50% duty cycle limit to prevent transformer saturation.

The FAN4800 includes a folded-back current limit for the PWM section to provide short-circuit protection.



Ordering Information

Part Number	Operating Temp. Range	Pb-Free	Package	Packing Method	Marking Code
FAN4800IN	-40°C to +125°C	Yes	16-PDIP	Rail	FAN4800
FAN4800IM	-40°C to +125°C	Yes	16-SOIC	Rail	FAN4800
FAN4800IMX	-40°C to +125°C	Yes	16-SOIC	Tape & Reell	FAN4800

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Block Diagram

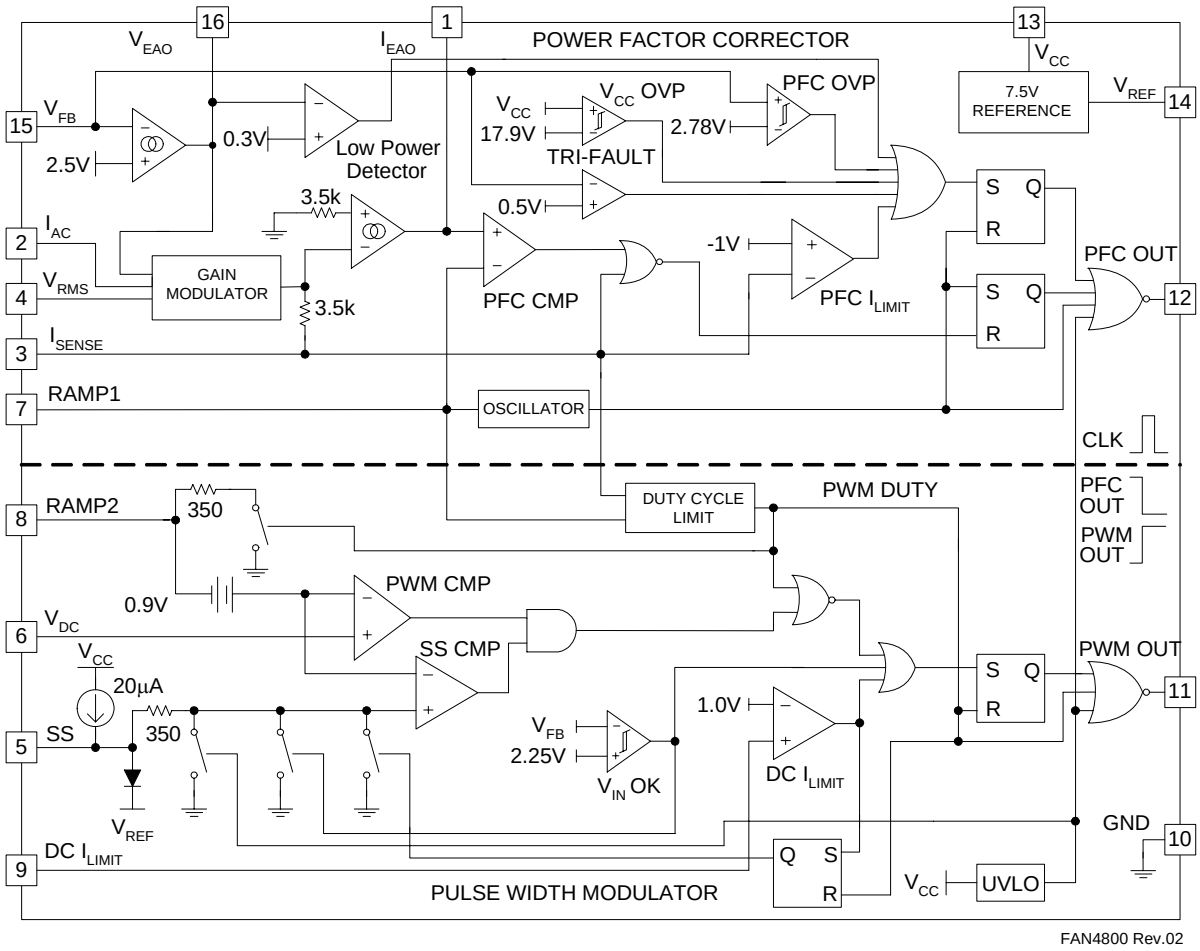


Figure 1. Internal Block Diagram

Pin Configuration

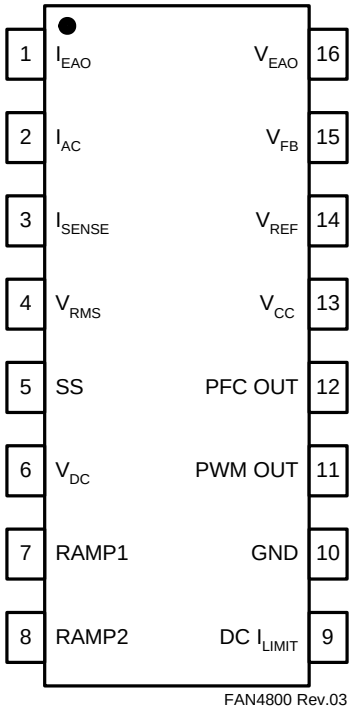


Figure 2. Pin Configuration (Top View)

Pin Definitions

Pin #	Name	Description
1	I_{EAO}	PFC transconductance current error amplifier output
2	I_{AC}	PFC gain control reference input
3	I_{SENSE}	Current sense input to the PFC current limit comparator
4	V_{RMS}	Input for PFC RMS line voltage compensation
5	SS	Connection point for the PWM soft-start capacitor
6	V_{DC}	PWM voltage feedback input
7	RAMP1 (RtCt)	Oscillator timing node; timing set by RT, CT
8	RAMP2 (PWM RAMP)	In current mode, this pin functions as the current sense input; in voltage mode, it is the PWM input from the PFC output (feed forward ramp)
9	DC I_{LIMIT}	PWM current limit comparator input
10	GND	Ground
11	PWM OUT	PWM driver output
12	PFC OUT	PFC driver output
13	V_{CC}	Positive supply
14	V_{REF}	Buffered output for the internal 7.5V reference
15	V_{FB}	PFC transconductance voltage error amplifier input
16	V_{EAO}	PFC transconductance voltage error amplifier output

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Absolute Maximum Ratings

The “Absolute Maximum Ratings” are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the absolute maximum ratings.

Symbol	Parameter	Min.	Max.	Unit
V_{CC}	Positive Supply Voltage		20	V
I_{EAO}	PFC transconductance current error amplifier output	0	5.5	V
V_{ISENSE}	I_{SENSE} Voltage	-3.0	0.7	V
	Voltage on Any Other Pin	GND-0.3	V_{CC}+0.3	V
I_{REF}	I_{REF} Current		10	mA
I_{AC}	I_{AC} Input Current		1	mA
I_{PFC_OUT}	Peak PFC OUT Current, Source or Sink		1	A
I_{PWM_OUT}	Peak PWM OUT Current, Source or Sink		1	A
	PFC OUT, PWM OUT Energy per Cycle		1.5	µJ
T_J	Junction Temperature		150	°C
T_{STG}	Storage Temperature Range	-65	150	°C
T_A	Operating Temperature Range	-40	125	°C
T_L	Lead Temperature (Soldering,10 seconds)		260	°C
θ_{JA}	Thermal Resistance (θ_{JA}) Plastic DIP		80	°C/W

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Electrical Characteristics

Unless otherwise stated, these specifications apply: V_{CC} = 15V, R_T = 52.3KΩ, C_T = 470pF, T_A = -40°C to 125°C.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
VOLTAGE ERROR AMPLIFIER						
V_{FB}	Input Voltage Range(1)		0		6	V
gm1	Transconductance		50	70	90	µmho
V_{ref}(PFC)	Feedback Reference Voltage	T_A = 25°C	2.45	2.50	2.55	V
$I_b(V_{EAO})$	Input Bias Current(2)		-1.00	-0.05		mA
V_{EAO}(H)	Output High-Voltage		5.8	6.0		V
V_{EAO}(L)	Output Low-Voltage			0.1	0.4	V
I_{sink}(V)	Sink Current	T_A = 25°C, V_{FB} = 3V V_{EAO} = 6.0V		-35	-20	µA
I_{source}(V)	Source Current	T_A = 25°C, V_{FB} = 1.5V V_{EAO} = 1.5V	30	40		µA
G_V	Open Loop Gain(1)(3)		50	60		dB
PSRR1	Power Supply Rejection Ratio(1)	11V < V_{CC} < 16.5V	50	60		dB
CURRENT ERROR AMPLIFIER						
V_{IEAO}	Input Voltage Range(1)		-1.5		0.7	V
gm2	Transconductance		50	85	100	µmho
V_{offset}	Input Offset Voltage	T_A = 25°C			25	mV
I_{beao}	Input Bias Current(1)		-1			µA
I_{EAO}(H)	Output High-Voltage		4.00	4.25		V
I_{EAO}(L)	Output Low-Voltage			1.0	1.2	V
I_{sink}(I)	Sink Current	I_{SENSE} = +0.5, I_{EAO} = 4.0V		-65	-35	µA
I_{source}(I)	Source Current	I_{SENSE} = -0.5, I_{EAO} = 1.5V	35	75		µA
Gi	Open Loop Gain(1)		60	70		dB
PSRR2	Power Supply Rejection Ratio(1)	11V < V_{CC} < 16.5V	60	75		dB
PFC OVP COMPARATOR						
Vovp	Threshold Voltage	T_A = 25°C	2.70	2.78	2.90	V
HY(ovp)	Hysteresis	T_A = 25°C	230		350	mV
LOW-POWER DETECT COMPARATOR						
V_{th}(lp)	Threshold Voltage	T_A = 25°C	0.15	0.30	0.40	V
VCC OVP COMPARATOR						
V_{CC_OVP}	Threshold Voltage	T_A = 25°C	17.5	17.9	18.5	V
HY(V_{CC_OVP})	Hysteresis	T_A = 25°C	1.40	1.50	1.65	V
TRI-FAULT DETECT						
$t_{d(F)}$	Time to Fault Detect HIGH(1)	V_{FB} = V_{Fault} Detect LOW to V_{FB} = Open. 470pF from V_{FB} to GND		2	4	ms
F(L)	Fault Detect LOW		0.4	0.5	0.6	V

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Electrical Characteristics (Continued)

Unless otherwise stated, these specifications apply: V_{CC} = 15V, R_T = 52.3kΩ, C_T = 470pF, T_A = -40°C to 125°C.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
PFC I_{LIMIT} COMPARATOR						
$V_{th(cs)}$	Threshold Voltage		-1.10	-1.00	-0.90	V
$V_{th(cs)}$-V_{gm}	(PFC I_{LIMIT} V_{TH} – Gain Modulator Output)		5	100		mV
$t_{d(pfc_off)}$	Delay to Output(1)			250		ns
DC I_{LIMIT} COMPARATOR						
$V_{th(DC)}$	Threshold Voltage		0.95	1.00	1.05	V
t_d(pwm_off)	Delay to Output(1)			250		ns
V_{IN} OK COMPARATOR						
$V_{th(OK)}$	Threshold Voltage		2.10		2.45	V
HY(OK)	Hysteresis		0.8	1.0	1.2	V
GAIN MODULATOR						
G1	Gain(3)	I_{AC} = 100μA, V_{RMS} = 0, V_{FB} = 1V, T_A = 25°C	0.70	0.84	0.95	Gain(3)
G2		I_{AC} = 100μA, V_{RMS} = 1.1V, V_{FB} = 1V, T_A = 25°C	1.80	2.00	2.20	
G3		I_{AC} = 150μA, V_{RMS} = 1.8V, V_{FB} = 1V, T_A = 25°C	0.90	1.00	1.10	
G4		I_{AC} = 300μA, V_{RMS} = 3.3V, V_{FB} = 1V, T_A = 25°C	0.25	0.32	0.40	
BW	Band Width(1)	I_{AC} = 100μA		10		MHz
Vo(gm)	Output Voltage = 3.5kΩ x (I_{SENSE} – I_{OFFSET})	I_{AC} = 250μA, V_{RMS} = 1.1V, V_{FB} = 2V, T_A = 25°C	0.80	1.00	1.20	V
OSCILLATOR						
f_{osc1}	Initial Accuracy	T_A = 25°C	68		81	kHz
Δf_{osc1}	Voltage Stability	11V < V_{CC} < 16.5V		1		%
Δf_{osc2}	Temperature Stability			2		%
f_{osc2}	Total Variation	Line, Temp	66		84	kHz
V_{ramp}	Ramp Valley to Peak Voltage(1)			2.75		V
t_{dead}	PFC Dead Time			685		ns
I_{dis}	CT Discharge Current	V_{RAMP2} = 0V, V_{RAMP1} = 2.5V	6.5		15.0	mA
REFERENCE						
V_{ref1}	Output Voltage	T_A = 25°C, I(V_{REF}) = 1mA	7.4	7.5	7.6	V
ΔV_{ref1}	Line Regulation	11V < V_{CC} < 16.5V		10	25	mV
ΔV_{ref2}	Load Regulation	0mA < I(V_{REF}) < 7mA		10	20	mV
ΔV_{ref4}	Temperature Stability			0.4		%
V_{ref2}	Total Variation(1)	Line, Load, Temperature	7.35		7.65	V
ΔV_{ref5}	Long Term Stability(1)	T_J = 125°C, 1000 hours	5		25	mV

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Electrical Characteristics (Continued)

Unless otherwise stated, these specifications apply: V_{CC} = 15V, R_T = 52.3kΩ, C_T = 470pF, T_A = -40°C to 125°C.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
PFC						
$D_{min.}$	Minimum Duty Cycle	V_{IEAO} > 4.0V			0	%
$D_{max.}$	Maximum Duty Cycle	V_{IEAO} < 1.2V	92	95		%
R_{ON}(low)1	Output Low R_{dson}	I_{OUT} = -20mA at T_A = 25°C			15	Ω
R_{ON}(low)2		I_{OUT} = -100mA at T_A = 25°C			15	Ω
Vol1	Output Low Voltage(1)	I_{OUT} = -10mA, V_{CC} = 9V, T_A = 25°C		0.4	0.8	V
R_{ON}(high)1	Output High R_{dson}	I_{OUT} = 20mA at T_A = 25°C		15	20	Ω
R_{ON}(high)2		I_{OUT} = 100mA at T_A = 25°C		15	20	Ω
$t_{r(pfc)}$	Rise/Fall Time(1)	C_L = 1000pF		50		ns
PWM						
D	Duty Cycle Range		0-42	0-47	0-49	%
R_{ON}(low)3	Output Low R_{dson}	I_{OUT} = -20mA at T_A = 25°C			15	Ω
R_{ON}(low)4		I_{OUT} = -100mA at T_A = 25°C			15	Ω
Vol2	Output Low Voltage	I_{OUT} = -10mA, V_{CC} = 9V, T_A = 25°C		0.4	0.8	V
R_{ON}(high)3	Output High R_{dson}	I_{OUT} = 20mA at T_A = 25°C		15	20	Ω
R_{ON}(high)4		I_{OUT} = 100mA at T_A = 25°C		15	20	Ω
$t_{r(pwm)}$	Rise/Fall Time	C_L = 1000pF(1)		50		ns
PWM(ls)	PWM Comparator Level Shift		0.6	0.9	1.2	V
SUPPLY						
I_{st}	Start-up Current	V_{CC} = 12V, C_L = 0pF		100	200	µA
I_{op}	Operating Current	14V, C_L = 0pF		2.5	7.0	mA
$V_{th(start)}$	Under-Voltage Lockout Threshold		12.74	13.00	13.26	V
$V_{th(hys)}$	Under-Voltage Lockout Hysteresis		2.80	3.00	3.20	V

Notes:

1. This parameter, although guaranteed by design, is not 100% production tested.
2. Includes all bias currents to other circuits connected to the V_{FB} pin.
3. Gain = K × 5.375V; K = $(I_{SENSE} - I_{OFFSET}) \times [I_{AC} \times (V_{EAO} - 0.625)]^{-1}$; $V_{EAO\ (MAX.)}$ = 6V.

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Typical Performance Characteristics

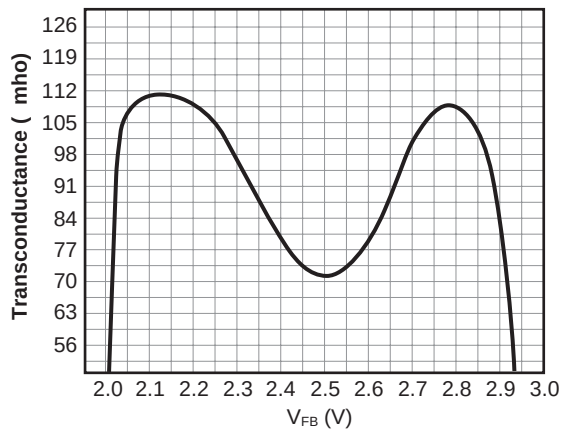


Figure 3. Voltage Error Amplifier (gmv) Transconductance

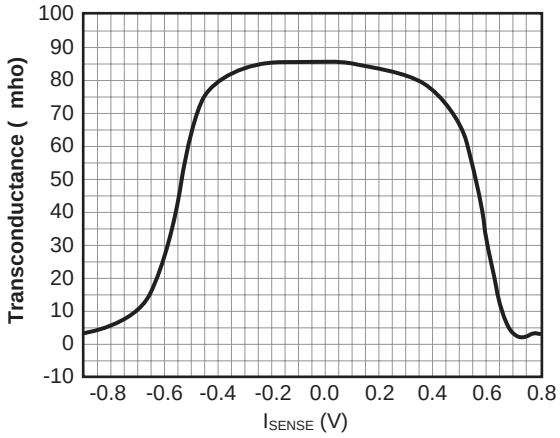


Figure 4. Current Error Amplifier (gmi) Transconductance

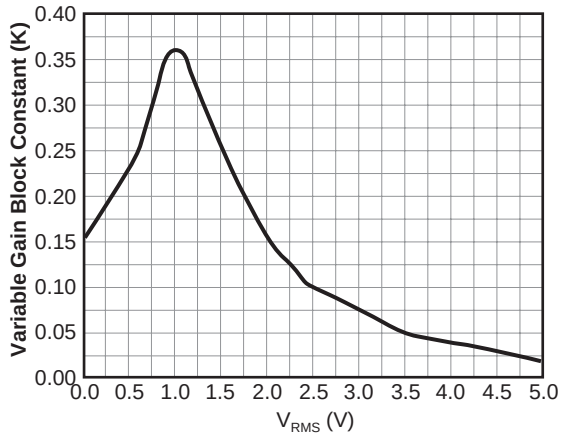


Figure 5. Gain Modulator Transfer Characteristic (K)

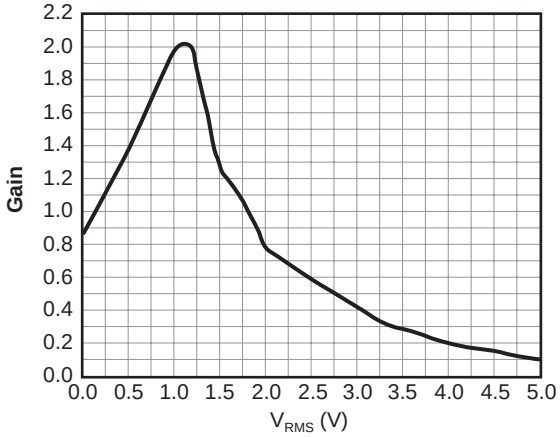


Figure 6. Gain vs. V_{RMS}

$$K = \frac{I_{GAINMOD} - I_{OFFSET}}{I_{AC} \times (6 - 0.625)}\ mV^{-1} \quad (1)$$

$$Gain = \frac{I_{SENSE} - I_{OFFSET}}{I_{AC}} \quad (2)$$

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Functional Description

The FAN4800 consists of an average current controlled, continuous boost Power Factor Correction (PFC) front end and a synchronized Pulse Width Modulator (PWM) back end. The PWM can be used in either current or voltage mode. In voltage mode, feed forward from the PFC output bus can be used to improve the PWM's line regulation. In either mode, the PWM stage uses conventional trailing-edge, duty-cycle modulation. This patented leading/trailing edge modulation results in a higher usable PFC error amplifier bandwidth and can significantly reduce the size of the PFC DC bus capacitor.

The synchronization of the PWM with the PFC simplifies the PWM compensation due to the controlled ripple on the PFC output capacitor (the PWM input capacitor). The PWM section of the FAN4800 runs at the same frequency as the PFC.

In addition to power factor correction, a number of protection features are built into the FAN4800. These include soft-start, PFC over-voltage protection, peak current limiting, brownout protection, duty cycle limiting, and under-voltage lockout (UVLO).

Power Factor Correction

Power Factor Correction treats a nonlinear load like a resistive load to the AC line. For a resistor, the current drawn from the line is in phase with and proportional to the line voltage, so the power factor is unity (one). A common class of nonlinear load is the input of most power supplies, which use a bridge rectifier and capacitive input filter fed from the line.

The peak charging effect, which occurs on the input filter capacitor in these supplies, causes brief, high-amplitude pulses of current to flow from the power line, rather than a sinusoidal current in phase with the line voltage. Such supplies present a power factor to the line of less than one (i.e., they cause significant current harmonics of the power line frequency to appear at the input). If the input current drawn by such a supply (or any nonlinear load) can be made to follow the input voltage in instantaneous amplitude, it appears resistive to the supply.

To hold the input current draw of a device drawing power from the AC line in phase with and proportional to the input voltage, that device must be prevented from loading the line except in proportion to the instantaneous line voltage. To accomplish this, the PFC section of the FAN4800 uses a boost mode DC-DC converter. The input to the converter is the full-wave, rectified, AC line voltage. No bulk filtering is applied following the bridge rectifier, so the input voltage to the boost converter ranges (at twice line the frequency) from zero volts to a peak value of the AC input and back to zero. By forcing the boost converter to meet two simultaneous conditions, it is possible to ensure that the current drawn from the power line is proportional to the input line voltage.

One of these conditions is that the output voltage of the boost converter must be set higher than the peak value of the line voltage. A commonly used value is $385V_{DC}$, to allow for a high line of $270V_{AC}$ rms. The second condition is that the current drawn from the line at any given instant must be proportional to the line voltage. Establishing a suitable voltage control loop for the converter, which in turn drives a current error amplifier and switching output driver, satisfies the first of these requirements. The second requirement is met by using the rectified AC line voltage to modulate the output of the voltage control loop. Such modulation causes the current error amplifier to command a power stage current that varies directly with the input voltage. To prevent ripple, which necessarily appears at the output of boost circuit (typically about $10V_{AC}$ on a $385V_{DC}$ level), from introducing distortion back through the voltage error amplifier, the bandwidth of the voltage loop is deliberately kept low. A final refinement is to adjust the overall gain of the PFC section to be proportional to $1/V_{IN}^2$, which linearizes the transfer function of the system as the AC input voltage.

Since the boost converter in the FAN4800 PFC is current averaging, no slope compensation is required.

1. PFC Section

1.1 Gain Modulator

Figure 1 shows a block diagram of the PFC section of the FAN4800. The gain modulator is the heart of the PFC, as the circuit block controls the response of the current loop to line voltage waveform and frequency, RMS line voltage, and PFC output voltages. There are three inputs to the gain modulator:

1. A current representing the instantaneous input voltage (amplitude and wave shape) to the PFC. The rectified AC input sine wave is converted to a proportional current via a resistor and is then fed into the gain modulator at I_{AC}. Sampling current in this way minimizes ground noise, required in high-power, switching-power conversion environments. The gain modulator responds linearly to this current.
2. A voltage proportional to the long-term RMS AC line voltage, derived from the rectified line voltage after scaling and filtering. This signal is presented to the gain modulator at V_{RMS}. The output of the gain modulator is inversely proportional to V_{RMS}^2 (except at unusually low values of V_{RMS}, where special gain contouring takes over to limit power dissipation of the circuit components under heavy brownout conditions). The relationship between V_{RMS} and gain is called K and is illustrated in Figure 5.

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3. The output of the voltage error amplifier, V_{EAO}. The gain modulator responds linearly to variations in this voltage.

The output of the gain modulator is a current signal, in the form of a full wave rectified sinusoid at twice the line frequency. This current is applied to the virtual ground (negative) input of the current error amplifier. In this way, the gain modulator forms the reference for the current error loop and ultimately controls the instantaneous current draw of the PFC from the power line. The general form of the output of the gain modulator is:

$$I_{GAINMOD} = \frac{I_{AC} \times V_{EAO}}{V^2_{RMS}} \times 1V \quad (3)$$

More precisely, the output current of the gain modulator is given by:

$$I_{GAINMOD} = K \times (V_{EAO} - 0.625) \times I_{AC} \quad (4)$$

where K is in units of V^{-1}.

Note that the output current of the gain modulator is limited around 228.57µA and the maximum output voltage of the gain modulator is limited to 228.57µA x 3.5K = 0.8V.

This 0.8V also determines the maximum input power. However, $I_{GAINMOD}$ cannot be measured directly from I_{SENSE}. $I_{SENSE} = I_{GAINMOD} - I_{OFFSET}$ and I_{OFFSET} can only be measured when V_{EAO} is less than 0.5V and $I_{GAINMOD}$ is 0A. Typical I_{OFFSET} is around 60µA.

1.2 Selecting R_{AC} for I_{AC} pin

I_{AC} pin is the input of the gain modulator. I_{AC} is also a current mirror input and requires current input. Selecting a proper resistor R_{AC} provides a good sine wave current derived from the line voltage and helps program the maximum input power and minimum input line voltage.

$R_{AC} = V_{IN}$ peak x 7.9K. For example, if the minimum line voltage is $80V_{AC}$, the R_{AC} = 80 x 1.414 x 7.9K = 894kΩ.

1.3 Current Error Amplifier, IEAO

The current error amplifier's output controls the PFC duty cycle to keep the average current through the boost inductor a linear function of the line voltage. At the inverting input to the current error amplifier, the output current of the gain modulator is summed with a current, which results from a negative voltage being impressed upon the I_{SENSE} pin.

The negative voltage on I_{SENSE} represents the sum of all currents flowing in the PFC circuit and is typically derived from a current sense resistor in series with the negative terminal of the input bridge rectifier.

The inverting input of the current error amplifier is a virtual ground. Given this fact, and the arrangement of the duty cycle modulator polarities internal to the PFC, an increase in positive current from the gain modulator causes the output stage to increase its duty cycle until the voltage on I_{SENSE} is adequately negative to cancel this increased current. Similarly, if the gain modulator's output decreases, the output duty cycle decreases to achieve a less negative voltage on the I_{SENSE} pin.

1.4 Cycle-By-Cycle Current Limiter and Selecting R_S

As well as being a part of the current feedback loop, the I_{SENSE} pin is a direct input to the cycle-by-cycle current limiter for the PFC section. If the input voltage at this pin is ever less than -1V, the output of the PFC is disabled until the protection flip-flop is reset by the clock pulse at the start of the next PFC power cycle.

R_S is the sensing resistor of the PFC boost converter. During the steady state, line input current x R_S equals $I_{GAINMOD}$ x 3.5K.

Since the maximum output voltage of the gain modulator is $I_{GAINMOD}$ maximum x 3.5k = 0.8V during the steady state, R_S x line input current is limited to below 0.8V as well. Therefore, to choose R_S, use the following equation:

$$R_S = \frac{0.8V \times V_{INPEAK}}{2 \times Line\,Input\,Power} \quad (5)$$

For example, if the minimum input voltage is $80V_{AC}$ and the maximum input RMS power is 200Watt,
R_S = (0.8V x 80V x 1.414) / (2 x 200) = 0.226Ω.

1.5 PFC OVP

In the FAN4800, the PFC OVP comparator serves to protect the power circuit from being subjected to excessive voltages if the load changes suddenly. A resistor divider from the high-voltage DC output of the PFC is fed to V_{FB}. When the voltage on V_{FB} exceeds 2.78V, the PFC output driver is shut down. The PWM section continues to operate. The OVP comparator has 280mV of hysteresis and the PFC does not restart until the voltage at V_{FB} drops below 2.50V. V_{CC} OVP can also serve as a redundant PFC OVP protection. V_{CC} OVP threshold is 17.9V with 1.5V hysteresis.

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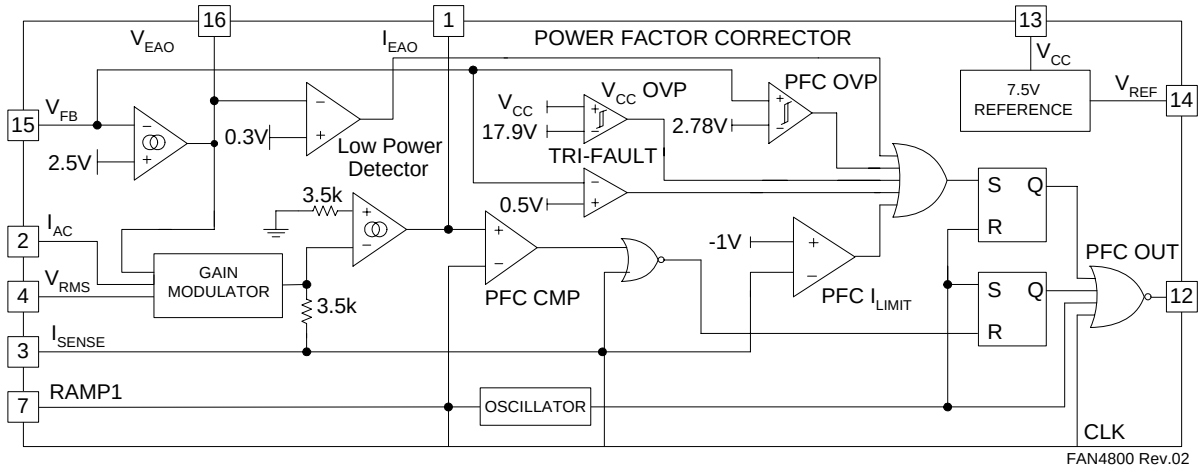


Figure 7. PFC Section Block Diagram

1.6 Error Amplifier Compensation

The PWM loading of the PFC can be modeled as a negative resistor because an increase in the input voltage to the PWM causes a decrease in the input current. This response dictates the proper compensation of the two transconductance error amplifiers.

Figure 8 shows the types of compensation networks most commonly used for the voltage and current error amplifiers, along with their respective return points. The current-loop compensation is returned to V_{REF} to produce a soft-start characteristic on the PFC: As the reference voltage increases from 0V, it creates a differentiated voltage on I_{EAO}, which prevents the PFC from immediately demanding a full duty cycle on its boost converter.

1.7 PFC Voltage Loop

There are two major concerns when compensating the voltage loop error amplifier (V_{EAO}); stability and transient response. Optimizing interaction between transient response and stability requires that the error amplifier's open-loop crossover frequency half that of the line frequency, or 23Hz for a 47Hz line (lowest anticipated international power frequency). The gain vs. input voltage of the FAN4800's voltage error amplifier (V_{EAO}) has a specially shaped non-linearity, so that under steady-state operating conditions, the transconductance of the error amplifier is at a local minimum. Rapid perturbation in line or load conditions causes the input to the voltage error amplifier (V_{FB}) to deviate from its 2.5V (nominal) value. If this happens, the transconductance of the voltage error amplifier increases significantly, as shown in the Figure 4. This raises the gain-bandwidth product of the voltage loop, resulting in a much more rapid voltage loop response to such perturbations than would occur with conventional linear gain characteristics.

The Voltage loop gain(s) is given by:

$$= \frac{\Delta V_{OUT}}{\Delta V_{EAO}} \times \frac{\Delta V_{FB}}{\Delta V_{OUT}} \times \frac{\Delta V_{EAO}}{\Delta V_{FB}} \approx \frac{P_{IN} \times 2.5V}{V^2_{OUTDC} \times \Delta V_{EAO} \times S \times C_{DC}} \times GM_V \times Z_C \quad (6)$$

where:

Z_C: Compensation network for the voltage loop.

GM_V: Transconductance of V_{EAO}.

P_{IN}: Average PFC input power.

V^2_{OUTDC}: PFC boost output voltage (typical designed value is 380V).

C_{DC}: PFC boost output capacitor.

1.8 PFC Current Loop

The compensation of the current amplifier (I_{EAO}) is similar to that of the voltage error amplifier (V_{EAO}) with the exception of the choice of crossover frequency. The crossover frequency of the current amplifier should be at least ten times that of the voltage amplifier to prevent interaction with the voltage loop. It should also be limited to less than one sixth of the switching frequency, e.g., 16.7kHz for a 100kHz switching frequency.

The current loop gain(s) is given by:

$$= \frac{\Delta V_{ISENSE}}{\Delta D_{OFF}} \times \frac{\Delta D_{OFF}}{\Delta I_{EAO}} \times \frac{\Delta I_{EAO}}{\Delta V_{ISENSE}} \approx \frac{V_{OUTDC} \times R_S}{S \times L \times 2.5V} \times GM_I \times Z_{CI} \quad (7)$$

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where:

Z_{CI}: Compensation network for the current loop.

GM_I: Transconductance of I_{EAO}.

V_{OUTDC}: PFC boost output voltage (typical designed value is 380V). The equation uses the worst-case condition to calculate the Z_{CI}.

R_S: Sensing resistor of the boost converter.

2.5V: Amplitude of the PFC leading modulation ramp.

L: Boost inductor.

A modest degree of gain contouring is applied to the transfer characteristic of the current error amplifier to increase its response speed to current-loop perturbations. However, the boost inductor is usually the dominant factor in overall current loop response. Therefore, this contouring is significantly less marked than that of the voltage error amplifier. This is illustrated in Figure 8.

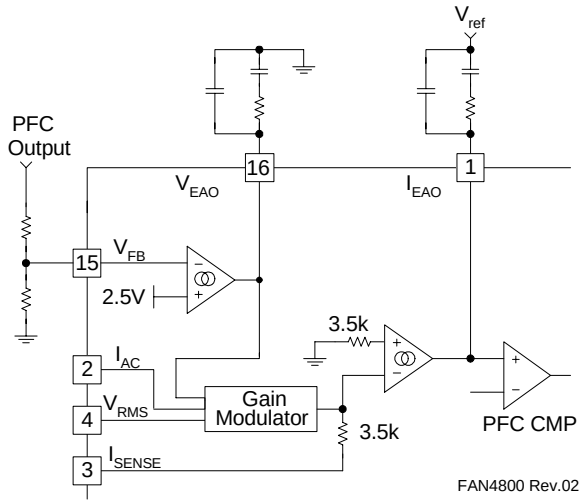


Figure 8. Compensation Network Connection for the Voltage and Current Error Amplifiers

There is an RC filter between R_S and I_{SENSE} pin.

There are two reasons to add a filter at the I_{SENSE} pin:

1) Protection: During start-up or in-rush current conditions, there is a large voltage across R_S, which is the sensing resistor of the PFC boost converter. It requires the I_{SENSE} filter to attenuate the energy.

2) To reduce L, the boost inductor: The I_{SENSE} filter also can reduce the boost inductor value since the I_{SENSE} filter behaves like an integrator before the I_{SENSE} pin, which is the input of the current error amplifier, I_{EAO}.

The I_{SENSE} filter is an RC filter. The resistor value of the I_{SENSE} filter is between 100Ω and 50Ω because $I_{OFF-SET}$ x R_S can generate an offset voltage of I_{EAO}.

Selecting an R_{FILTER} equal to 50Ω keeps the offset of the I_{EAO} less than 5mV. Design the pole of I_{SENSE} filter at $f_{pfc}/6$, one sixth of the PFC switching frequency, so the boost inductor can be reduced six times without disturbing the stability. The capacitor of the I_{SENSE} filter, C_{FILTER}, is approximately 283nF.

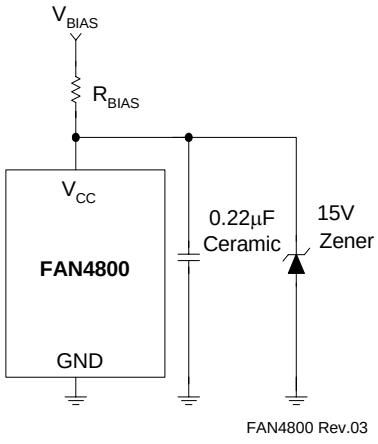


Figure 9. External Component Connection to V_{CC}

1.9 Oscillator (RAMP1)

The oscillator frequency is determined by the values of R_T and C_T, which determine the ramp and off-time of the oscillator output clock:

$$f_{OSC} = \frac{1}{t_{RAMP} + t_{DEAD}} \quad (8)$$

The dead time of the oscillator is derived from the following equation:

$$t_{RAMP} = C_T \times R_T \times ln\left(\frac{V_{REF}\text{-}1.00}{V_{REF}\text{-}3.75}\right) \quad (9)$$

at V_{REF} = 7.5V and $t_{RAMP} = C_T$ x R_T x 0.55.

The dead time of the oscillator may be determined using:

$$t_{DEAD} = \frac{2.75V}{12.11mA} \times C_T = 227 \times C_T \quad (10)$$

The dead time is so small ($t_{RAMP} >> t_{DEAD}$) that the operating frequency can typically be approximated by:

$$f_{OSC} = \frac{1}{t_{RAMP}} \quad (11)$$

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1.10 Example

For the application circuit shown in Figures 12 and 13, with the oscillator running at:

$$f_{OSC} = 100kHz = \frac{1}{t_{RAMP}} \quad (12)$$

solving for C_T x R_T yields 1.96 x 10^{-4}. C_T is 390pF and R_T is 51.1kΩ, selecting standard components values.

The dead time of the oscillator adds to the maximum PWM duty cycle (it is an input to the duty cycle limiter). With zero oscillator dead time, the maximum PWM duty cycle is typically 47%. Take care not to make C_T too large, which could extend the maximum duty cycle beyond 50%. This can be accomplished by using no greater than a 390pF capacitor for C_T.

2. PWM Section

2.1 Pulse Width Modulator (PWM)

The operation of the PWM section of the FAN4800 is straightforward, but there are several points that should be noted. Foremost among these is the inherent synchronization of PWM with the PFC section of the device, from which it also derives its basic timing. The PWM is capable of current-mode or voltage-mode operation. In current-mode applications, the PWM ramp (RAMP2) is usually derived directly from a current sensing resistor or current transformer in the primary of the output stage. it is thereby representative of the current flowing in the converter's output stage. DC I_{LIMIT}, which provides cycle-by-cycle current limiting, is typically connected to RAMP2 in such applications. For voltage-mode operation and certain specialized applications, RAMP2 can be connected to a separate RC timing network to generate a voltage ramp against which V_{DC} is compared. Under these conditions, the use of voltage feed-forward from the PFC bus can assist in line regulation accuracy and response. As in current-mode operation, the DC I_{LIMIT} input is used for output stage over-current protection.

No voltage error amplifier is included in the PWM stage of the FAN4800, as this function is generally performed on the output side of the PWM's isolation boundary. To facilitate the design of opto-coupler feedback circuitry, an offset has been built into the PWM's RAMP2 input that allows V_{DC} to command a 0% duty cycle for input voltages below typical 0.9V.

2.2 PWM Current Limit

The DC I_{LIMIT} pin is a direct input to the cycle-by-cycle current limiter for the PWM section. Should the input voltage at this pin ever exceed 1V, the output flip-flop is reset by the clock pulse at the start of the next PWM power cycle. When the DC I_{LIMIT} triggers the cycle-by-cycle current, it also softly discharges the voltage of the soft-start capacitor. It limits the PWM duty cycle mode and the power dissipation is reduced during the dead-short condition.

2.3 V_{IN} OK Comparator

The V_{IN} OK comparator monitors the DC output of the PFC and inhibits the PWM if the voltage on V_{FB} is less than its nominal 2.25V. Once the voltage reaches 2.25V, which corresponds to the PFC output capacitor being charged to its rated boost voltage, the soft-start begins.

2.4 PWM Control (RAMP2)

When the PWM section is used in current mode, RAMP2 is generally used as the sampling point for a voltage, representing the current in the primary of the PWM's output transformer. The voltage is derived either from a current sensing resistor or a current transformer. In voltage mode, RAMP2 is the input for a ramp voltage generated by a second set of timing components (R_{RAMP2}, C_{RAMP2}) that have a minimum value of 0V and a peak value of approximately 5V. In voltage mode, feed forward from the PFC output bus is an excellent way to derive the timing ramp for the PWM stage.

2.5 Soft-Start (SS)

PWM start-up is controlled by selection of the external capacitor at soft-start. A current source of 20mA supplies the charging current for the capacitor and start-up of the PWM begins at 0.9V. Start-up delay can be programmed by the following equation:

$$C_{SS} = t_{DELAY} \times \frac{20\mu A}{0.9V} \quad (13)$$

where C_{SS} is the required soft-start capacitance and the t_{DELAY} is the desired start-up delay.

It is important that the time constant of the PWM soft-start allows the PFC time to generate sufficient output power for the PWM section. The PWM start-up delay should be at least 5ms.

Solving for the minimum value of C_{SS}:

$$C_{SS} = 5ms \times \frac{20\mu A}{0.9V} = 111nF \quad (14)$$

Use caution when using this minimum soft-start capacitance value because it can cause premature charging of the SS capacitor and activation of the PWM section if V_{FB} is in the hysteresis band of the V_{IN} OK comparator at start-up. The magnitude of V_{FB} at start-up is related both to line voltage and nominal PFC output voltage. Typically, a 1.0µF soft-start capacitor allows time for V_{FB} and PFC_{OUT} to reach their nominal values prior to activation of the PWM section at line voltages between 90Vrms and 265Vrms.

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2.6 Generating V_{CC}

After turning on the FAN4800 at 13V, the operating voltage can vary from 10V to 17.9V. The threshold voltage of the V_{CC} OVP comparator is 17.9V and its hysteresis is 1.5V. When V_{CC} reaches 17.9V, PFC OUT is LOW, and the PWM section is not disturbed. There are two ways to generate V_{CC}: use auxiliary power supply around 15V or use bootstrap winding to self-bias the FAN4800 system. The bootstrap winding can be either taped from the PFC boost choke or from the transformer of the DC-to-DC stage.

The ratio of the bootstrap's winding transformer should be set between 18V and 15V. A filter network is recommended between V_{CC} (pin 13) and bootstrap winding. The resistor of the filter can be set as:

$$\begin{aligned} &R_{FILTER} \times I_{VCC} \approx 2V, \\ &I_{VCC} = I_{OP} + \left(Q_{PFCFET} + Q_{PWMFET}\right) \times f_{SW} I_{OP} \\ &\quad = 2.5A \text{ (typ.)} \end{aligned} \tag{15}$$

If V_{CC} goes beyond 17.9V, the PFC gate (pin 12) drive goes LOW and the PWM gate drive (pin 11) remains working. The resistor's value must be chosen to meet the operating current requirement of the FAN4800 itself (5mA, maximum) in addition to the current required by the two gate driver outputs.

2.7 Example

To obtain a desired V_{BIAS} voltage of 18V, a V_{CC} of 15V, and the FAN4800 driving a total gate charge of 90nC at 100kHz (e.g. one IRF840 MOSFET and two IRF820 MOSFET), the gate driver current required is:

$$I_{GATEDRIVE} = 100kHz \times 90nC = 9mA \tag{16}$$

$$\begin{aligned} R_{BIAS} &= \frac{V_{BIAS} - V_{CC}}{I_{CC} + I_G} \\ &= \frac{18V - 15V}{5mA + 9mA} \end{aligned} \tag{17}$$

$$Choose\ R_{BIAS} = 214\Omega \tag{18}$$

Bypass the FAN4800 locally with a 1.0μF ceramic capacitor. In most applications, an electrolytic capacitor of between 47μF and 220μF is also required across the part both for filtering and as a part of the start-up bootstrap circuitry.

2.8 Leading/Trailing Modulation

Conventional PWM techniques employ trailing-edge modulation, in which the switch turns on right after the trailing edge of the system clock. The error amplifier output is then compared with the modulating ramp up. The effective duty cycle of the trailing edge modulation is determined during the on-time of the switch. Figure 10 shows a typical trailing-edge control scheme.

In the case of leading-edge modulation, the switch is turned off exactly at the leading edge of the system clock. When the modulating ramp reaches the level of the error amplifier output voltage, the switch is turned on. The effective duty-cycle of the leading-edge modulation is determined during off-time of the switch. Figure 11 shows a leading-edge control scheme.

One of the advantages of this control technique is that it requires only one system clock. Switch 1 (SW1) turns off and Switch 2 (SW2) turns on at the same instant to minimize the momentary no-load period, thus lowering ripple voltage generated by the switching action. With such synchronized switching, the ripple voltage of the first stage is reduced. Calculation and evaluation have shown that the 120Hz component of the PFC's output ripple voltage can be reduced by as much as 30% using the leading-edge modulation method.

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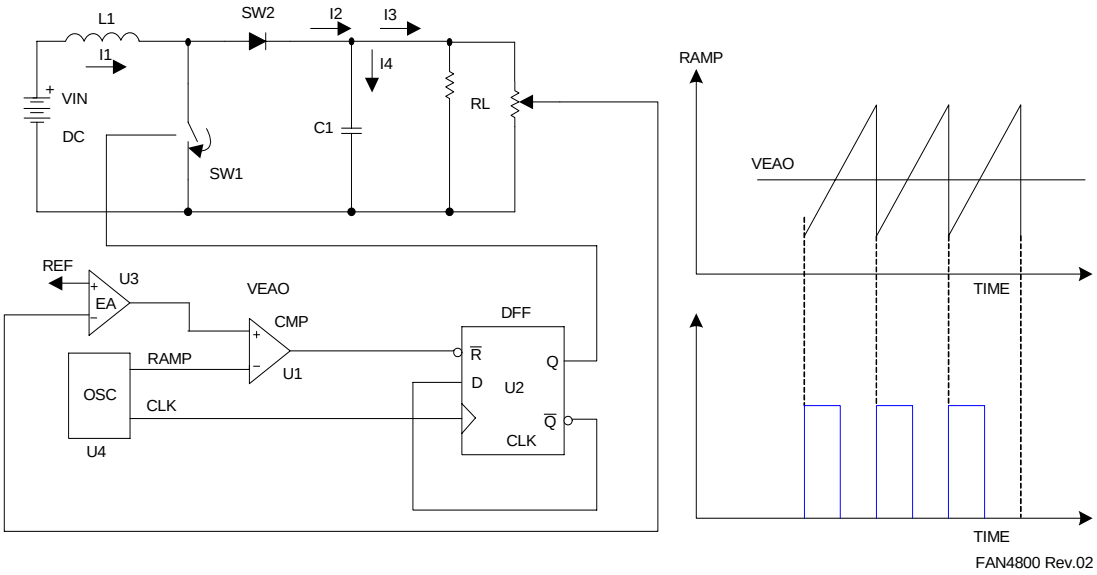


Figure 10. Typical Trailing-Edge Control Scheme

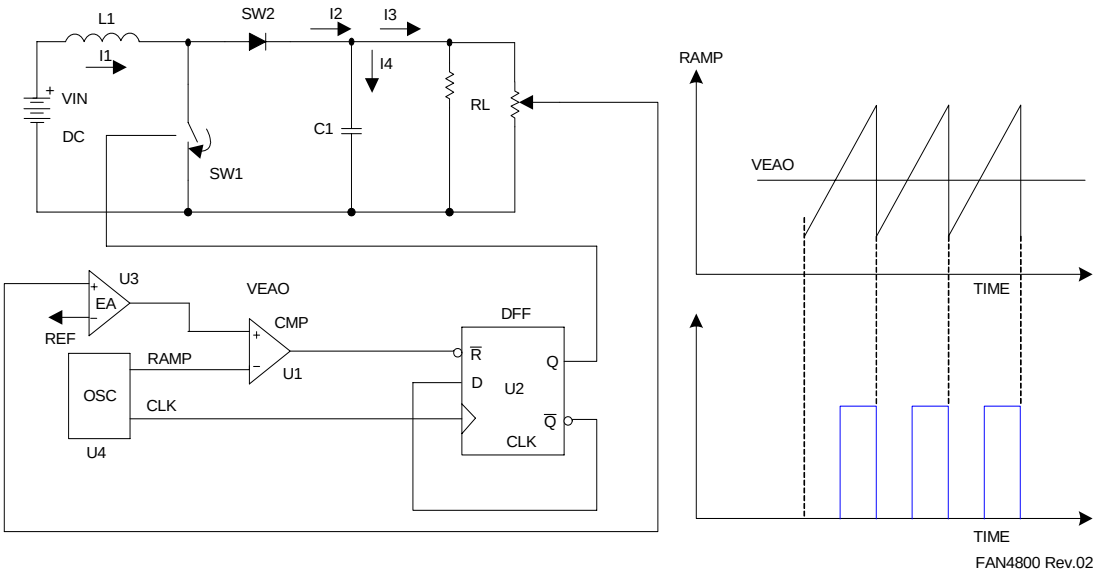


Figure 11. Typical Leading-Edge Control Scheme

Typical Application Circuit

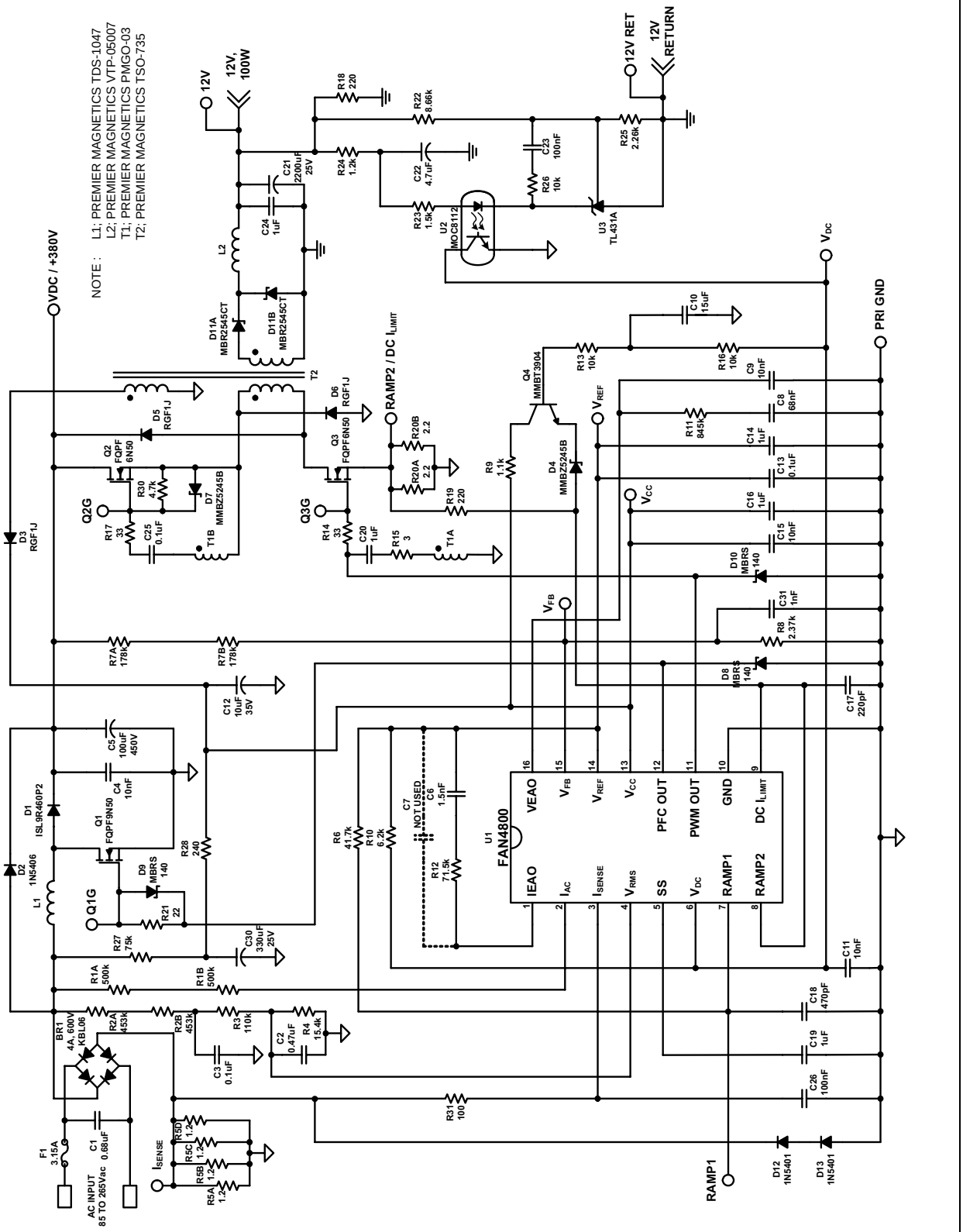


Figure 12. Current-Mode Application

Typical Application Circuit (Continued)

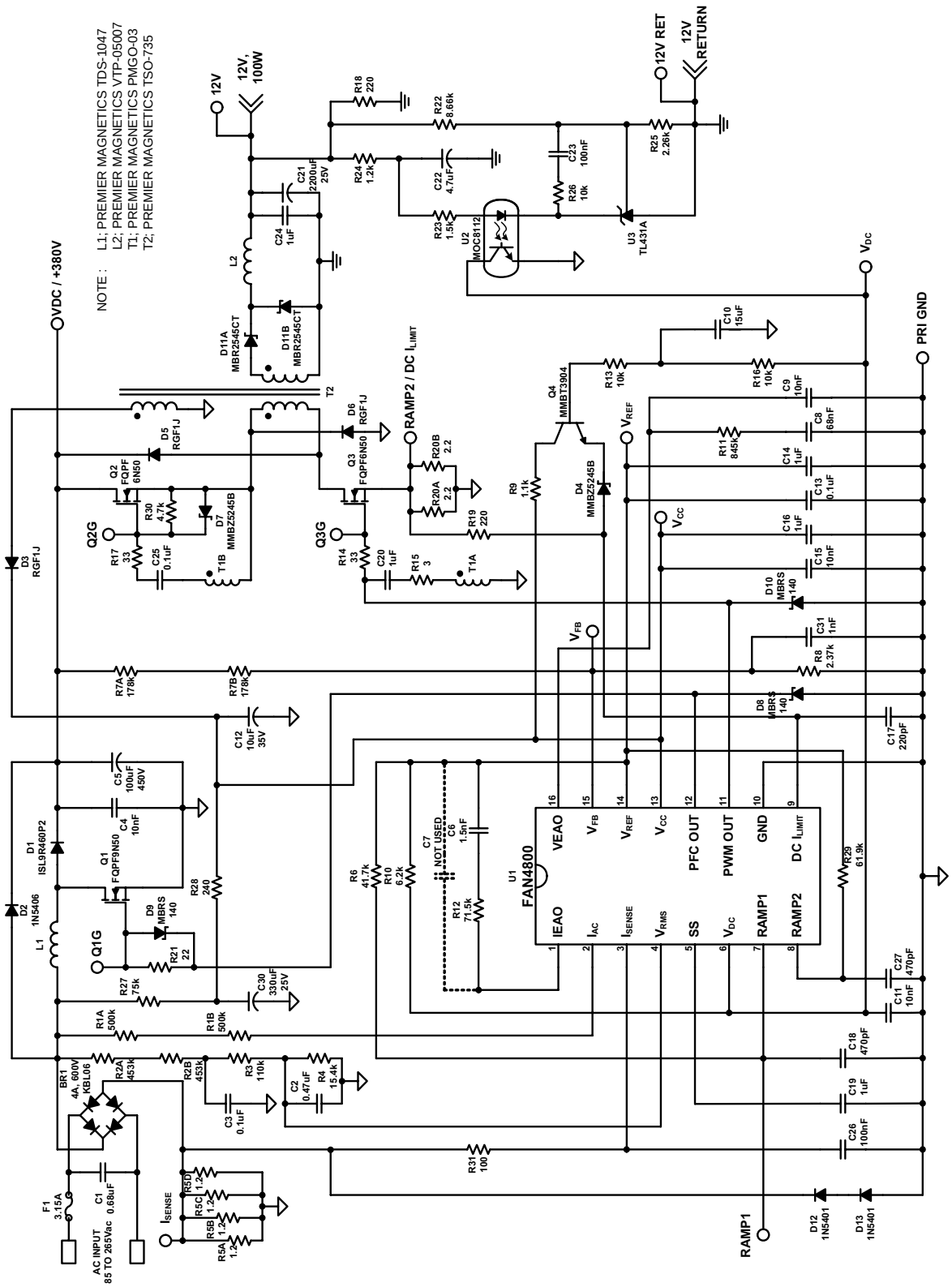


Figure 13. Voltage-Mode Application

Package Dimensions

16-Pin DIP

Dimensions are in inches (millimeters) unless otherwise specified.

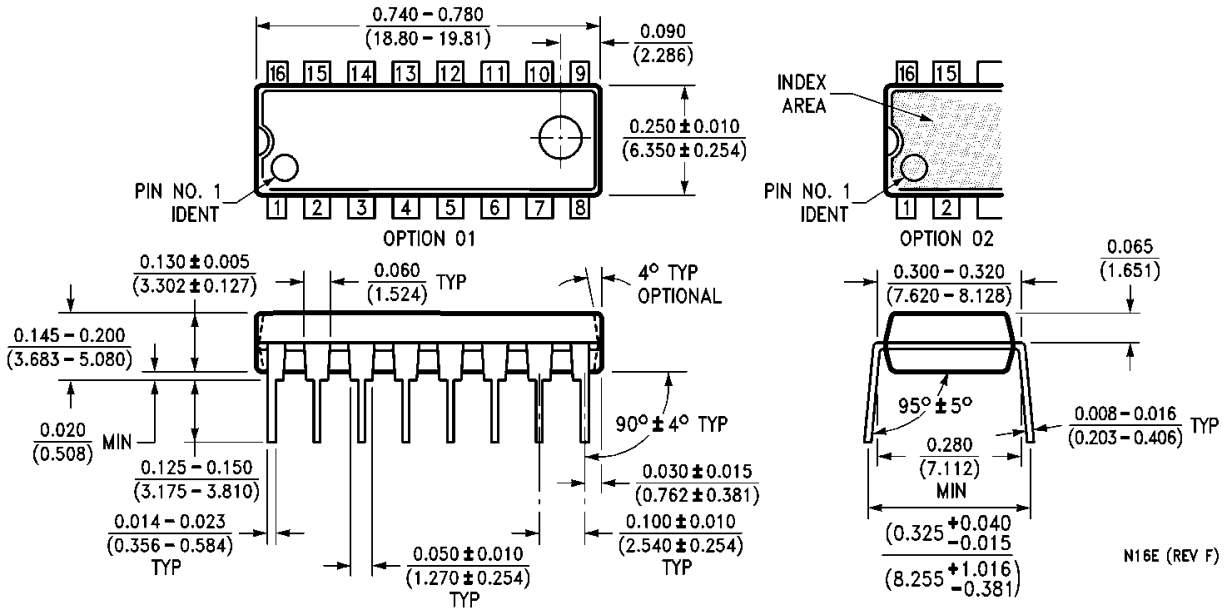


Figure 14. 16-Lead Plastic Dual In-Line Package (DIP)

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Package Dimensions (Continued)

16-Pin SOIC (Wide)

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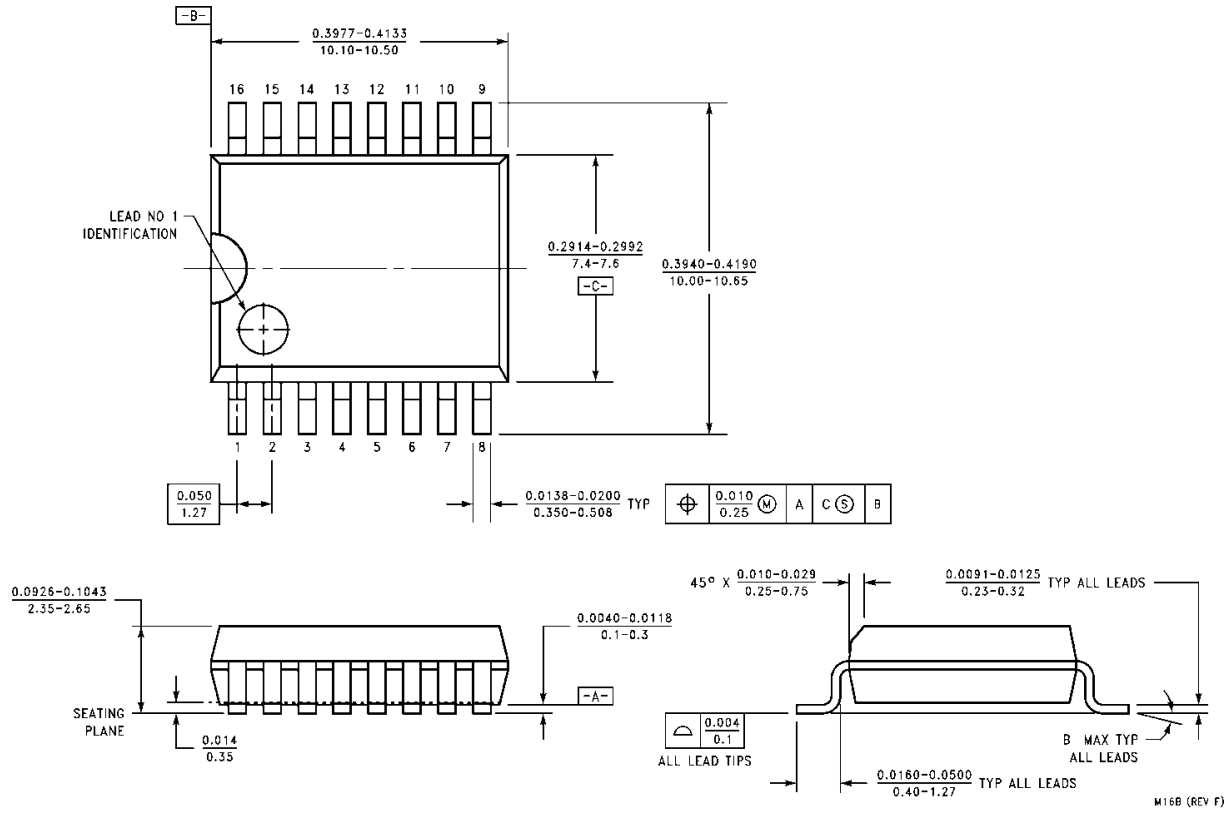


Figure 15. 16-Lead Small Outline Integrated Circuit (SOIC)

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