Full-Bridge Power MOSFET Controller

Not for New Design

The A3940KLPTR-T variant is in production but has been determined to be NOT FOR NEW DESIGN. This classification indicates that sale of this device is currently restricted to existing customer applications. The device should not be purchased for new design applications because obsolescence in the near future is probable. Samples are no longer available.
Date of status change: April 30, 2007

Recommended Substitutions:

For existing customer transition, and for new customers or new applications, refer to the A3941.

NOTE: For detailed information on purchasing options, contact your local Allegro field applications engineer or sales representative.

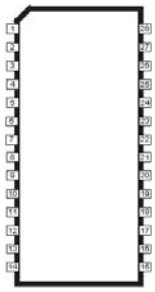
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3940

Data Sheet
29319.100J



A3940KLP
(TSSOP with exposed thermal pad)



A3940KLW
(SOIC)

Approx. 2X actual size.

ABSOLUTE MAXIMUM RATINGS

Load Supply Voltage Range, VBB, VDRAIN, CP1 ..... **-0.6 V to +40 V**
Output Voltage Ranges,
LSS ..... **-2 V to +6.5 V**
GHA/GHB, V_{GHX} ..... **-2 V to +55 V**
SA/SB, V_{SX} ..... **-2 V to +45 V**
GLA/GLB, V_{GLX} ..... **-2 V to +16 V**
CA/CB, V_{CX} ..... **-0.6 V to +55 V**
CP2,VCP, VIN ..... **-0.6 V to +52 V**
Logic Input/Output Voltage Range
V_{IN}, V_{OUT} ..... **-0.3 V to +6.5 V**
Operating Temperature Range,
T_A ..... **-40°C to +135°C**
Junction Temperature, T_J ..... **+150°C***
Storage Temperature Range,
T_S ..... **-55°C to +150°C**

* Fault conditions that produce excessive junction temperature will activate device thermal shutdown circuitry. These conditions can be tolerated, but should be avoided.

The A3940KLP and A3940KLW are designed specifically for automotive applications that require high-power motors. Each provides four high-current gate drive outputs capable of driving a wide range of n-channel power MOSFETs in a full-bridge configuration.

Bootstrap capacitors are utilized to provide the above-battery supply voltage required for n-channel FETs. An internal charge pump for the high side allows for dc (100% duty cycle) operation of the bridge.

Protection features include supply under/overvoltage, thermal shutdown, and motor lead short-to-battery and short-to-ground fault notification, and a programmable dead-time adjustment for cross-conduction prevention. The overvoltage trip point is user adjustable.

The A3940 is supplied in a choice of two power packages, a 28-pin TSSOP with an exposed thermal pad (package type LP), and a 28-pin wide-body SOIC (package type LW). Both package types are available in lead (Pb) free versions, with 100 % matte-tin leadframe plating (suffix –T).

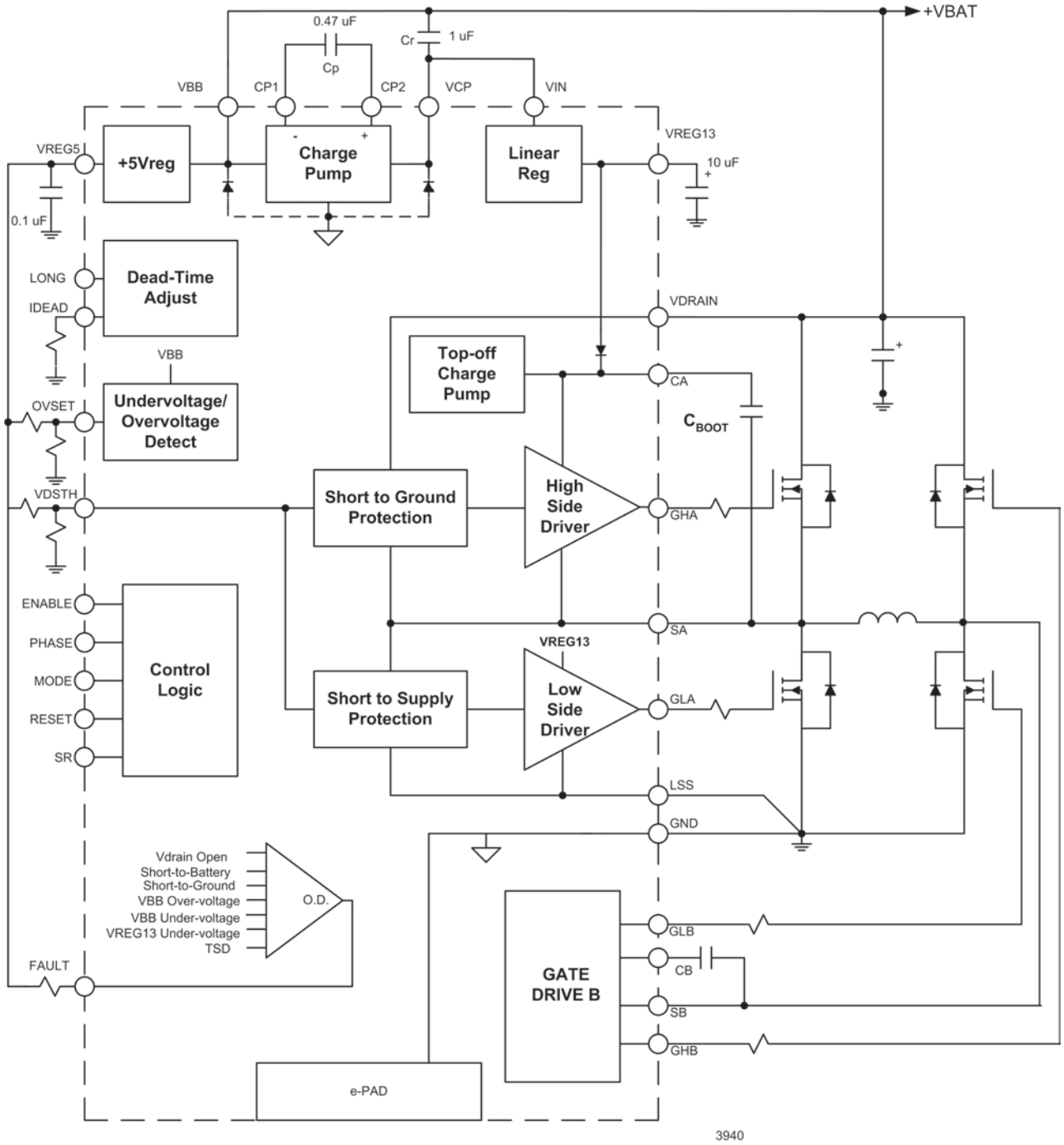
FEATURES

- Drives wide range of n-channel MOSFETs
- Charge pump to boost gate drive at low-battery-input conditions
- Bootstrapped gate drive with charge pump for 100% duty cycle
- Synchronous rectification
- Fault diagnostic output
- Adjustable dead-time cross-conduction protection
- Motor lead short-to-battery and short-to-ground protection
- Undervoltage/overvoltage protection
- -40°C to +150°C, T_J operation
- Thermal shutdown

Always order by complete part number

Part Number	Pb-free	Status	Package	Packing
A3940KLPTR-T	Yes	NND	28-pin TSSOP	4000 pcs/reel
A3940KLPTR	–	LTB	28-pin TSSOP	4000 pcs/reel

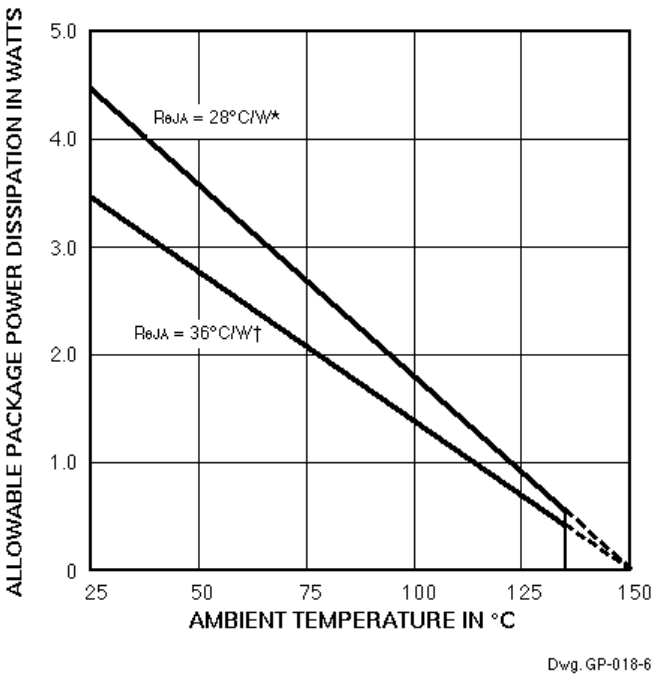
Functional Block Diagram



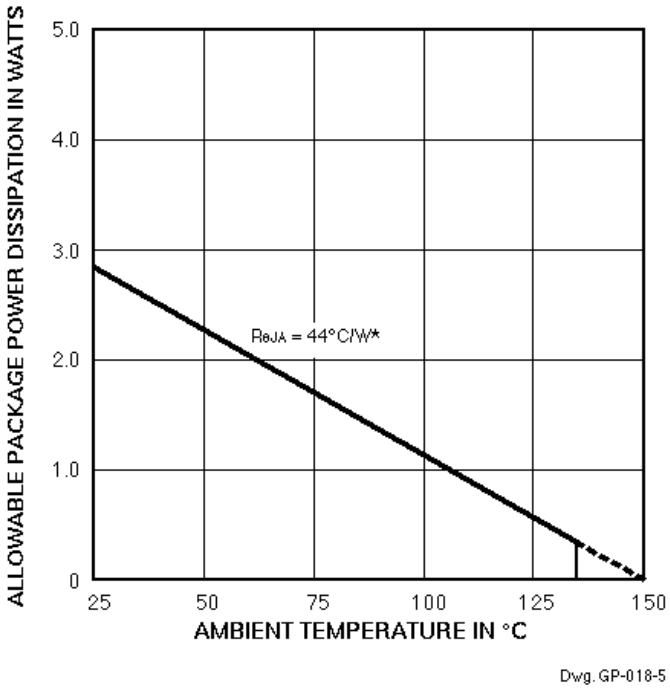
See pages 7 and 8 for terminal assignments and descriptions.

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A3940KLP (TSSOP)



A3940KLW (SOIC)



* Measured on "High-K" multi-layer PWB per JEDEC Standard JESD51-7.
† Measured on typical two-sided PWB .

The products described here are manufactured under one or more U.S. patents or U.S. patents pending.

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ELECTRICAL CHARACTERISTICS: unless otherwise noted at T_A = -40°C to +135°C, T_J = -40°C to +150°C, $V_{IN} \le V_{BB}$ = 7 V to 40 V, C_p = 0.47 µF, C_r = 1 µF, C_{REG5} = 0.1 µF, C_{REG13} = 10 µF, C_{BOOT} = 0.1 µF, PWM = 22.5 kHz square wave.

Characteristics	Symbol	Conditions	Limits			
			Min	Typ	Max	Units
Power Supply						
V_{BB} Quiescent Current	I_{BB}	RESET = 1, $V_{BB} = V_{IN}$ = 40 V, $V_{IN} \neq V_{CP}$, coast, stopped, CP disabled, I_{DEAD} = 170 µA	–	4.8	7.0	mA
		RESET = 1, $V_{BB} = V_{IN}$ = 15 V, $V_{IN} \neq V_{CP}$, coast, stopped, CP disabled, I_{DEAD} = 170 µA	–	4.3	7.0	mA
		RESET = 1, $V_{BB} = V_{IN}$ = 40 V, $V_{IN} \neq V_{CP}$, coast, stopped, I_{DEAD} = 170 µA, I_{CP} = 0 mA	–	5.0	7.0	mA
		RESET = 1, $V_{BB} = V_{IN}$ = 15 V, $V_{IN} \neq V_{CP}$, coast, stopped, I_{DEAD} = 170 µA, I_{CP} = 0 mA	–	4.8	7.0	mA
		RESET = 1, $V_{BB} = V_{IN}$ = 40 V, $V_{IN} \neq V_{CP}$, coast, stopped, I_{DEAD} = 170 µA, I_{CP} = 15 mA	–	35.4	40.0	mA
		RESET = 1, $V_{BB} = V_{IN}$ = 15 V, $V_{IN} \neq V_{CP}$, coast, stopped, I_{DEAD} = 170 µA, I_{CP} = 15 mA	–	35.1	40.0	mA
		RESET = 0	–	–	1.0	µA
VREG5 Output Voltage	V_{REG5}	No load	4.5	5.0	5.5	V
VREG5 Line Regulation	V_{REG5}	I_{REG5} = 4.0 mA	–	5.0	–	mV
VREG5 Load Regulation	V_{REG5}	I_{REG5} = 0 - 4.0 mA, V_{BB} = 40 V	–	5.0	–	mV
VREG5 Short-Circuit Current	I_{REG5M}	V_{BB} = 40 V, V_{REG5} = 0	–	28	–	mA
VCP Output Voltage Level	V_{CP}	V_{BB} = 14 - 40 V, I_{CP} = 15 mA	V_{BB}+9.5	V_{BB}+10.7	V_{BB}+11.8	V
		V_{BB} = 7 V, I_{CP} = 15 mA	11.7	13	13.8	V
VCP Gate Drive	I_{CP}	SR = 1, MODE = 0, ENABLE = PWM	15	–	–	mA
VCP Output Voltage Ripple	$V_{CP(PP)}$	I_{CP} = 15 mA, V_{BB} = 14 V - 40 V	–	500	–	mV
VCP Pump-Up time	t_{up}	$V_{IN} = V_{CP}$, V_{BB} = 14 V - 40 V	–	2.5	–	ms
		$V_{IN} = V_{CP}$, V_{BB} = 7 V	–	3.5	–	ms
VREG13 Quiescent Input Current	I_{REG13}	RESET = 1, $V_{BB} = V_{IN}$ = 40 V, coast, stopped	–	1.4	–	mA
VREG13 Output Voltage	V_{REG13}	V_{IN} = 15 V, no load	12.6	13.3	14.0	V
VREG13 Dropout Voltage	V_{REGDV}	I_{REG13} = 15 mA, V_{IN} = 11 V - 14 V	–	0.7	–	V
VREG13 Line Regulation	V_{REG13}	V_{IN} = 15 V - 40 V, I_{REG13} = 15 mA	–	2.0	–	mV
VREG13 Load Regulation	V_{REG13}	V_{IN} = 40 V, I_{REG13} = 0 - 15 mA	–	2.0	–	mV
VREG13 Short-Circuit Current	I_{REG13M}	V_{IN} = 40 V, V_{REG13} = 0 (pulse)	–	60	–	mA
Go-to-Sleep Response Time	t_{sleep}	RESET = 0 to V_{REG5} = 4 V	10	30	–	µs
Wake-Up Response Time	t_{wake}	RESET = 1 to V_{REG13}, UV cleared	–	1.4	–	ms

NOTES: Typical Data is for design information only.
Negative current is defined as coming out of (sourcing) the specified device terminal.

Continued next page …

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Characteristics	Symbol	Conditions	Limits			
			Min	Typ	Max	Units
Control Logic						
Logic Input Voltage	$V_{IN(1)}$	HIGH level input (Logic 1), except RESET.	2.0	–	–	V
	$V_{IN(1)}$	HIGH level input (Logic 1) for RESET	2.2	–	–	V
	$V_{IN(0)}$	LOW level input (Logic 0)	–	–	0.8	V
Logic Input Current	$I_{IN(1)}$	V_{IN} = 2.0 V	–	40	100	µA
	$I_{IN(0)}$	V_{IN} = 0.8 V, except RESET(0)	–	16	40	µA
	$I_{IN(0)}$	V_{IN} = 0.8 V, RESET(0)	–	–	1.0	µA
Gate Drives, GHx, GLx (internal SOURCE or upper switch stages)						
Output High Voltage	$V_{DSL(H)}$	GHx: I_{xU} = -10 mA, V_{sx} = 0	V_{REG13} - 2.2	–	V_{REG13}	V
		GLx: I_{xU} = -10 mA, V_{lss} = 0	V_{REG13} - 0.2	–	V_{REG13}	V
Source Current (pulsed)	I_{xU}	V_{SDU} = 10 V, T_J = 25°C	–	700	–	mA
		V_{SDU} = 10 V, T_J = 135°C	400	–	–	mA
Source ON Resistance	$r_{SDU(on)}$	I_{xU} = -150 mA, T_J = 25°C	4.0	–	13	Ω
		I_{xU} = -150 mA, T_J = 135°C	7.0	–	23	Ω
Source Load Rise Time	t_r	Measure V_{DSL}, 20% to 80%, C_L = 3300 pF	–	90	–	ns
Gate Drives, GHx, GLx (internal SINK or lower switch stages)						
Output Low Voltage	$V_{DSL(L)}$	GHx: I_{xL} = 10 mA, V_{sx} = 0	–	–	150	mV
		GLx: I_{xL} = 10 mA, V_{lss} = 0	–	–	150	mV
Sink Current (pulsed)	I_{xL}	V_{DSL} = 10 V, T_J = 25°C	–	800	–	mA
		V_{DSL} = 10 V, T_J = 135°C	550	–	–	mA
Sink ON Resistance	$r_{DSL(on)}$	I_{xL} = +150 mA, T_J = 25°C	1.8	–	6.0	Ω
		I_{xL} = +150 mA, T_J = 135°C	3.0	–	7.5	Ω
Sink Load Fall Time	t_f	Measure V_{DSL}, 80% to 20%, C_L = 3300 pF	–	70	–	ns
Gate Drives, GHx, GLx (General)						
Propagation Delay	t_{pd}	Logic input to unloaded GHx, GLx	–	–	225	ns
Output Skew Time	$t_{sk(o)}$	Grouped by rising or falling edge	–	–	50	ns
Dead Time (Shoot-Through Prevention) Between GHx, GLx transitions of same phase	t_{dead}	LONG = 0, R_{DEAD} = 12.1 kΩ (I_{DEAD} = 167 µA)	0.3	–	–	µs
		LONG = 0, R_{DEAD} = 499 kΩ (I_{DEAD} = 4 µA)	–	–	11.0	µs
		LONG = 1, R_{DEAD} = 12.1 kΩ (I_{DEAD} = 167 µA)	8.3	–	–	µs
		LONG = 1, R_{DEAD} = 499 kΩ (I_{DEAD} = 4 µA)	–	–	345	µs

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For GH_X: $V_{SDU} = V_{CX} - V_{GHX}$, $V_{DSL} = V_{GHX} - V_{SX}$, $V_{DSL(H)} = V_{CX} - V_{SDU} - V_{SX}$.
For GL_X: $V_{SDU} = V_{REG} - V_{GLX}$, $V_{DSL} = V_{GLX} - V_{LSS}$, $V_{DSL(H)} = V_{REG} - V_{SDU} - V_{LSS}$.

Continued next page …

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Characteristics	Symbol	Conditions	Limits Min	Typ	Max	Units
Bootstrap Circuit						
Diode Forward Current Limit	I_{CX}	3 V < [(V_{REG13} = 13.5 V) - V_{CX}] < 12 V	140	–	1000	mA
Diode Forward Drop	V_F	I_F = 10 mA	0.8	–	2.0	V
Diode Resistance	R_F	$R_F(100) = [V_F(150) - V_F(50)]/100$	1.5	–	6.5	Ω
Top-off CP Source Current at Cx	Icx	V_{CX} - V_{SX} = 8 V, V_{BB} = 40 V, GHx = 1(no load)	40	–	–	µA
Fault Logic						
VBB Undervoltage	$V_{BB(uv)}$	Decreasing V_{BB}	4.5	5.25	6.0	V
VBB Undervoltage Hysteresis	$\Delta V_{BB(uv)}$	$V_{BB(recovery)}$ - $V_{BB(uv)}$	200	450	700	mV
VREG13 Undervoltage	$V_{REG13(uv)}$	Decreasing V_{IN}	7.5	8.25	9.0	V
VREG13 Undervoltage Hyst.	$\Delta V_{REG13(uv)}$	$V_{REG13(recovery)}$ - $V_{REG13(uv)}$	200	450	700	mV
VBB Overvoltage	$V_{BB(ov)}$	Increasing V_{BB}, FAULT = 0 to 1, V_{OVSET} = 0 V	16	19.6	22	V
		Increasing V_{BB}, FAULT = 0 to 1, V_{OVSET} = 0.45 V	24	28	30.5	V
		Increasing V_{BB}, FAULT = 0 to 1, V_{OVSET} = 0.9 V	32.5	36.4	39	V
VBB Overvoltage Hysteresis	$\Delta V_{BB(ov)}$	$V_{BB(ov)}$ - $V_{BB(recovery)}$	2.1	3.1	4.1	V
OVSET Input Current	$I_{SET(ov)}$	0 V < $V_{SET(ov)}$ < 0.9 V	–	–	1.4	µA
VDSTH Input Current	I_{DSTH}	0.3 V < V_{DSTH} < 3 V	–	–	1.0	µA
Short-to-Ground Threshold	$V_{STG(th)}$	V_{DSTH} = 0.3 V	V_{DSTH}-0.14	–	V_{DSTH}+0.10	V
		V_{DSTH} = 1.0 V	V_{DSTH}-0.18	–	V_{DSTH}+0.13	V
		V_{DSTH} = 3.0 V	V_{DSTH}-0.39	–	V_{DSTH}+0.26	V
Short-to-Battery Threshold	$V_{STB(th)}$	V_{DSTH} = 0.3 V	V_{DSTH}-0.20	–	V_{DSTH}+0.30	V
		V_{DSTH} = 1.0 V	V_{DSTH}-0.24	–	V_{DSTH}+0.30	V
		V_{DSTH} = 3.0 V	V_{DSTH}-0.37	–	V_{DSTH}+0.30	V
V_{DRAIN} /Open Bridge Threshold	$V_{DO(th)}$	If V_{DRAIN} < $V_{DO(th)}$, FAULT = 0 to 1	1.0	–	3.0	V
V_{DRAIN} /Open Bridge Current	I_{VDRAIN}	RESET = 0	–	–	1.0	µA
		RESET = 1, V_{DSTH} < 3 V	–	–	500	µA
Fault Latch Clear Pulsewidth	t_{latch}	RESET = 0, pulse	0.15	–	2.0	µs
Fault Clear Propagation Delay	t_{pd}	From RESET = 1 to FAULT = 0	–	2.0	–	µs
Fault Detection Noise Filter	t_{noise}		–	1.7	–	µs
Fault Output	$V_{out(0)}$	I_{out} = 5 mA, faults negated	–	–	0.4	V
	$I_{out(1)}$	V_{out} = 5 V, open-drain, fault asserted	–	–	1.0	µA
Thermal Shutdown Temperature	T_J	T_J increasing	–	172	–	°C
Thermal Shutdown Hysteresis	ΔT_J	T_J decreasing	–	12	–	°C

NOTES: Typical Data is for design information only.
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Terminal Functions

Terminal Name	Function	Terminal Number
VDRAIN	Kelvin connection to MOSFET high-side drains	1
LSS	Gate-drive source return, low-side	2
GLB	Gate-drive B output, low-side	3
SB	Motor phase B input	4
GHB	Gate-drive B output, high-side	5
CB	Bootstrap capacitor B	6
VIN	Regulated 13 V gate drive supply input	7
VREG13	Regulated 13 V gate drive supply output	8
CA	Bootstrap A capacitor	9
GHA	Gate-drive A output, high-side	10
SA	Motor phase A input	11
GLA	Gate-drive A output, low-side	12
VBB	Battery supply	13
CP2	Charge pump connection for pumping capacitor	14
VCP	Charge pump output	15
CP1	Charge pump connection for pumping capacitor	16
GND	Common ground and dc supply returns Electrically connected to exposed thermal pad of LP package	17
FAULT	Open-drain fault output	18
OVSET	DC input, overvoltage threshold setting for V_{BB}	19
VREG5	Regulated 5 V supply output	20
MODE	Control input	21
SR	Control input	22
ENABLE	Control input	23
PHASE	Control input	24
RESET	Control input	25
LONG	Control input, long or short deadtime	26
IDEAD	Adjust current for basic deadtime	27
VDSTH	DC input, drain-to-source monitor threshold voltage	28

Terminal Descriptions

CA/CB. High-side connection for bootstrap capacitor, positive supply for high-side gate drive. The bootstrap capacitor is charged to V_{REG13} – 1.5 V when the output Sx terminal is low. When the output swings high, the voltage on this terminal rises with the output to provide the boosted gate voltage needed for n-channel power MOSFETs.

RESET. Control input to put device into minimum power consumption mode and to clear latched faults. Logic "1" enables the device; logic "0" triggers the sleep mode. Internally pulled down via 50 kΩ resistor.

ENABLE. Logic "1" enables direct control of the output drivers via the PHASE input, as in PWM controls, and ignores the MODE and SR inputs. Internally pulled down via 50 kΩ resistor.

MODE. Logic input to set the current decay mode. Logic "1" (slow-decay mode) switches off the high-side MOSFET in response to a PWM "off" command. Logic "0" (fast-decay mode) switches off both the high-side and low-side MOSFETs. Internally pulled down via 50 kΩ resistor.

PHASE. Motor direction control. When logic "1", enables gate drive outputs GHA and GLB allowing current flow from SA to SB. When logic "0", enables GHB and GLA allowing current flow from SB to SA. Internally pulled down via 50 kΩ resistor.

SR. When logic "1", enables synchronous rectification; logic "0" disables the synchronous rectification. Internally pulled down via 50 kΩ resistor.

FAULT. Open drain, diagnostic logic output signal. When logic "1", indicates that one or more fault conditions have occurred. Use an external pullup resistor to VREG5 or to digital controller. Internally causes a coast when asserted. See also Functional Description, next page.

IDEAD. Analog current set by resistor (12 kΩ<R_{DEAD}<500 kΩ) to ground. In conjunction with LONG, determines dead time between GHx and GLx transitions of same phase. V_{IDEAD} = 2 V.

LONG. When logic "1", selects long dead time between GHx and GLx transitions of same phase. When logic "0", selects short dead times. Internally pulled down via 50 kΩ resistor.

GHA/GHB. High-side gate-drive outputs for n-channel MOSFET drivers. External series gate resistors can control slew rate seen at the power driver gate.

GLA/GLB. Low-side gate drive outputs for external, n-channel MOSFET drivers. External series gate resistors can control slew rate seen at the power driver gate.

GND. Common ground and dc supply returns. Exposed thermal pad of LP package is NOT internally connected to GND.

LSS. Low-side gate drivers' return. Connects to the common sources in the low-side of the power MOSFET bridge. It is the reference connection for the short-to-battery monitor.

OVSET. A positive, dc level that controls the VBB overvoltage trip point. Usually, provided from precision resistor divider network between V_{REG5} and GND. If connected directly to V_{REG5}, sets unspecified but high overvoltage trip point, effectively eliminating the overvoltage protection.

SA/SB. Directly connected to the motor terminals, these terminals sense the voltages switched across the load and are connected to the negative side of the bootstrap capacitors. Also, are the negative supply connection for the floating, high-side drivers.

VBB. Positive supply voltage. Usually connected to the motor voltage supply. If V_{BB} is above a specified level or below a specified level, a fault will be asserted.

VDRAIN. Kelvin connection for drain-to-source voltage (short-to-ground) monitor and is connected to high-side drains of the MOSFET bridge. Also used to detect "open drain".

VDSTH. A positive, dc level that sets the short-to-ground and short-to-battery monitor threshold voltage. If the drain-source voltage exceeds this level (after the dead time) during an "on" state, a fault will be asserted.

CP1 [CP2]. Charge pump capacitor negative [positive] side. If not using the charge pump, leave both terminals open.

VCP. Charge pump output for VREG13 input. If not using the charge pump, connect this terminal to VBB.

VIN. Positive supply voltage for the V_{REG13} linear regulator. Usually connected to VCP, the charge-pump output gate drive. If not using the charge pump, connect VIN to VBB or other dc supply greater than 11 V.

VREG13. High-side, gate-driver supply. If V_{REG13} falls below a specified level, a fault will be asserted.

VREG5. Regulated 5 V output for internal logic.

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Functional Description

Motor Lead Protection. A fault detection circuit monitors the voltage across the drain to source of the external MOSFETs. A fault is asserted "high" on the output terminal, FAULT, if the drain-to-source voltage of any MOSFET that is instructed to turn on is greater than the voltage applied to the V_{DSTH} input terminal. When a high-side switch is turned on, the voltage from V_{DRAIN} to the appropriate motor phase output, V_{SX}, is examined. If the motor lead is shorted to ground the measured voltage will exceed the threshold and the FAULT terminal will go "high". Similarly, when a low-side MOSFET is turned on, the differential voltage between the motor phase (drain) and the LSS terminal (source) is monitored. V_{DSTH} is set by a resistor divider to V_{REG5}.

To prevent erroneous motor faults during switching, the fault circuitry will wait two dead times after every PWM/phase change before monitoring the drain-to-source voltage; except, it will use one dead time for (1) a long coast to any phase on, or (2) a long hi-Z before on for that phase. This allows time for the motor output voltage to settle before checking for motor fault when using slow rise/fall gate-control waveforms.

The V_{DRAIN} is intended to be a Kelvin connection for the high-side, drain-source monitor circuit. Voltage drops across the power bus are eliminated by connecting an isolated PCB trace from the V_{DRAIN} terminal to the drain of the MOSFET bridge. This allows improved accuracy in setting the V_{DSTH} threshold voltage. The low-side, drain-source monitor uses the LSS terminal, rather than V_{DRAIN}, in comparing against V_{DSTH}.

Fault States. The FAULT terminal provides real time indication of fault conditions after some digital noise filtering. The V_{DRAIN} fault acts as if a short-to-ground fault existed on every motor phase. Bridge (or motor) faults are latched but cleared by a RESET = 0 pulse or by power cycling. GHx = GLx = 0 during RESET = 0. The undervoltage, overvoltage, and thermal shutdown faults are not latched and will not reset until the cause is eliminated. All faults cause, via the FAULT line, a coast and some cause shutdown of the regulators, as in the Fault Responses table (next page).

Note: As a test mode, if the thermal shutdown or SLEEP has not occurred and the FAULT output is externally held low, the coast mode and regulator shutdowns will not occur if motor or voltage faults occur. Do not wire-OR this terminal to other FAULT lines.

Dead Time. The A3940 is intended to drive a wide range of power MOSFETs in applications requiring a wide range of switching times. In order to prevent cross conduction (a.k.a. shoot-through) during direction and PWM changes, a power MOSFET must be turned off before its "phase-pin mate" is turned on.

$$t_{DEAD}(ns) = K([18.8R_{DEAD}(k\Omega)] + 50) + 90$$

where K = 1 for LONG = 0; K = 32 for LONG = 1.

Note: $I_{DEAD}(mA) \approx 2/R_{DEAD}(k\Omega)$, 12 kΩ<$R_{DEAD}$<500 kΩ.

Sleep Mode. RESET = 0 clears any latched motor faults while driving all gate drive outputs low (coast). Eventually, RESET = 0 turns off all circuits to allow minimum current draw. GHx and GLx outputs go high impedance (Z) when V_{REG13} < 4 V. RESET = 1 enables the device after it powers up all circuits. The user should wait the pump-up time, t_{up}, to allow the device to be powered up properly before a gate output is enabled. Please refer to power-up diagram in application note AN295040 for more detail.

Charge Pump. The A3940 is designed to accommodate a wide range of power supply voltages. The charge pump output voltage, V_{CP}, is regulated to V_{BB} + 11 V (or about $2V_{BB}$ if V_{BB} < 11 V).

VREG13. A 13.3 V, low-dropout, linear regulator is used to power the low-side gate drive circuit directly and to provide the current to charge the bootstrap capacitors for the high-side gate drive. The input supply connection to this regulator, VIN, can be externally connected to the charge pump output, VCP, or it can be directly connected to the VBB or VBAT terminal. Internal current limiting protects V_{REG13}.

VREG5. A 5 V, low-dropout, linear regulator is used to power the internal logic, regulators, and thermal detection. This regulator can also power low-current external resistor networks for VDSTH and OVSET, and the FAULT output pull-up. The input supply connection is VBB. Internal current limiting protects V_{REG5}.

Power-Up State. If the input logic is open, internal pull-downs put the system in coast mode on powering up. First, issue a brake command for >10 µs to charge the bootstrap capacitors and avoid a possible short-to-ground fault indication.

Functional Description (cont'd)

Control Logic

PHASE	ENABLE	MODE	SR	GLA	GLB	GHA	GHB	SA	SB	Mode of Operation
0	1	X	X	1	0	0	1	Lo	Hi	Reverse
0	0	0	1	0	1	1	0	Hi	Lo	Fast decay, SR enabled
0	0	1	1	1	1	0	0	Lo	Lo	Slow decay, braking mode
0	0	0	0	0	0	0	0	Z	Z	Fast decay, coast
0	0	1	0	1	0	0	0	Lo	Z	Slow decay, SR disabled
1	1	X	X	0	1	1	0	Hi	Lo	Forward
1	0	0	1	1	0	0	1	Lo	Hi	Fast decay, SR enabled
1	0	1	1	1	1	0	0	Lo	Lo	Slow decay, braking mode
1	0	0	0	0	0	0	0	Z	Z	Fast decay, coast
1	0	1	0	0	1	0	0	Z	Lo	Slow decay, SR disabled

NOTES: All faults will coast the motor, i.e., GHA = GHB = GLA = GLB = 0 to switch off all bridge MOSFETs.
X = Indicates a "don't care".
Z = Indicates a high-impedance state.

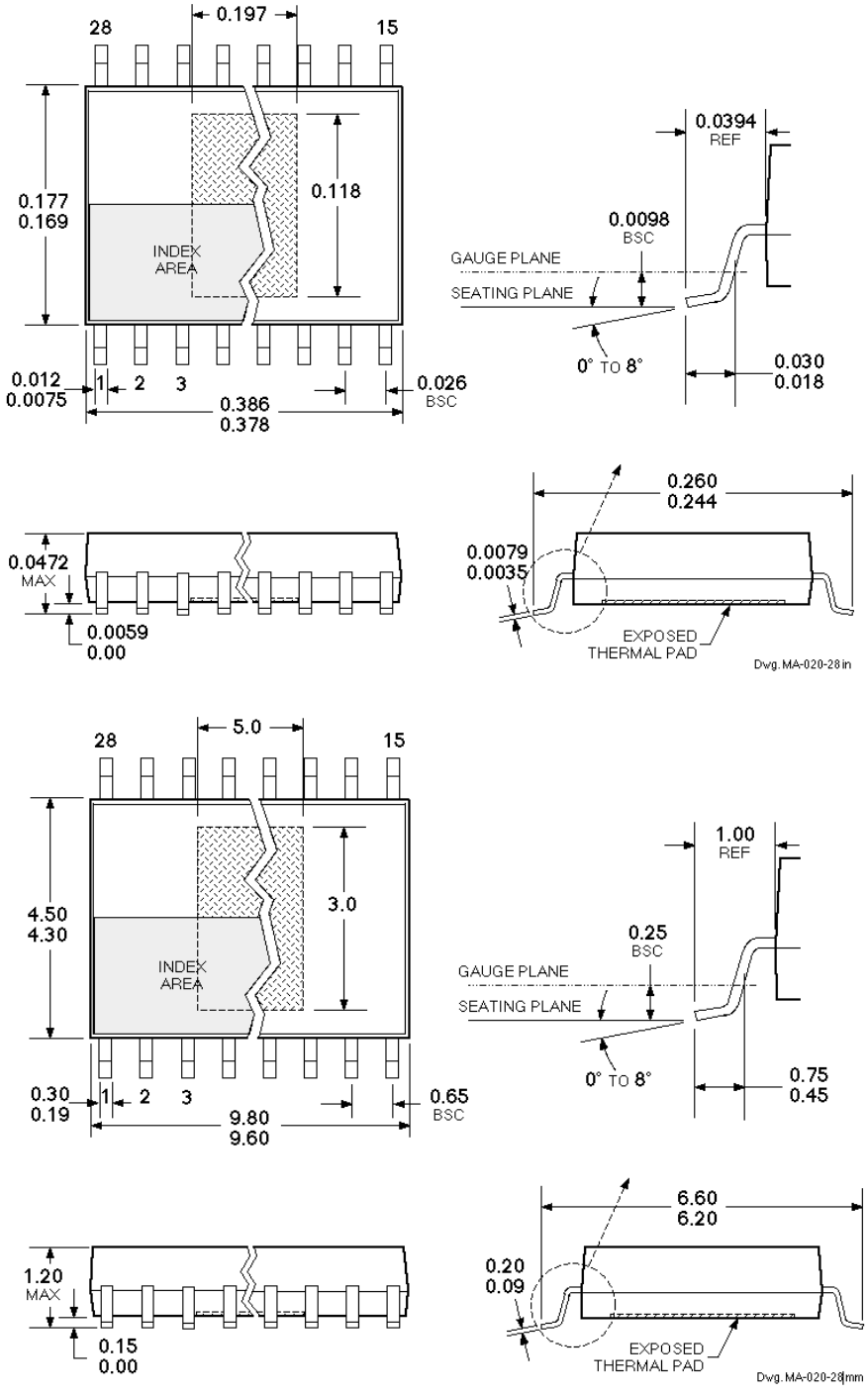
Fault Responses

Fault Mode	RESET	FAULT	CP Reg.	VREG13	VREG5	GHx	GLx
No Fault	1	0	ON	ON	ON	–	–
Short-to-Battery①②	1	1	ON	ON	ON	0	0
Short-to-Ground①③	1	1	ON	ON	ON	0	0
Open Bridge (V_{DRAIN})①④	1	1	ON	ON	ON	0	0
V_{REG13} Undervoltage	1	1	ON	ON⑤	ON	0⑥	0⑥
V_{BB} Overvoltage	1	1	ON	ON	ON	0	0
V_{BB} Undervoltage	1	1	OFF	OFF	ON⑤	0⑥	0⑥
Thermal Shutdown	1	1	OFF	OFF	ON⑤	0⑥	0⑥
Sleep	0	1	OFF	OFF	OFF	Z	Z

NOTES: ① = These faults are latched but will clear during RESET = 0 pulse. GHx = GLx = 0 during RESET = 0, except see ⑥. Other faults will not clear except when their cause is removed.
② = Short-to-battery can only be detected when the corresponding GLx = 1.
③ = Short-to-ground can only be detected when the corresponding GHx = 1.
④ = Bridge fault appears as a short-to-ground fault on all motor phases.
⑤ = Not instructed off but may be low voltage because of the fault indicated.
⑥ = During undervoltage conditions, the low sides of GHx and GLx are instructed to be "on" so that the outputs are low = 0; however, with V_{REG13} < 4 V, the outputs will start to open (become high impedance). See "Sleep Mode".

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A3940KLP (TSSOP)

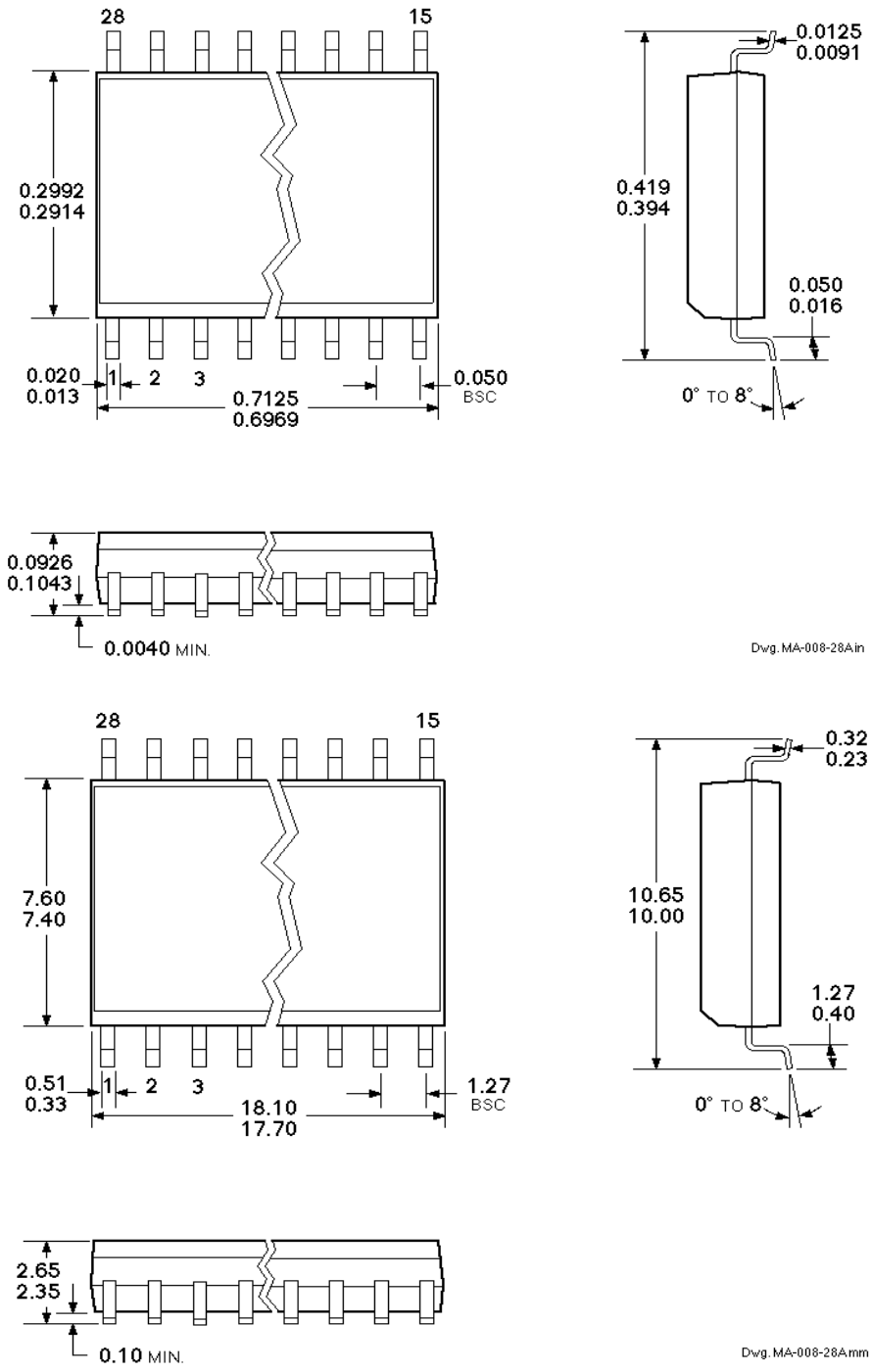


Dimensions in Inches
(for reference only)

Dimensions in Millimeters
(controlling dimensions)

NOTES: 1. Exact body and lead configuration at vendor's option within limits shown.
2. Lead spacing tolerance is non-cumulative.
3. Supplied in standard sticks/tubes of 50 devices or add "TR" to part number for tape and reel.

A3940KLW (SOIC)



Dimensions in Inches
(for reference only)

Dimensions in Millimeters
(controlling dimensions)

NOTES: 1. Lead spacing tolerance is non-cumulative.
2. Exact body and lead configuration at vendor's option within limits shown.
3. Supplied in standard sticks/tubes of 27 devices or add "TR" to part number for tape and reel.

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