

74ABT3284

18-Bit Synchronous Datapath Multiplexer

General Description

The 74ABT3284 is a synchronous datapath buffer designed to transmit four 9-bit bytes of data onto one or two 9-bit bytes in 2:1 or 4:1 multiplexed configurations. In addition, the non-inverting transceiver supports bidirectional data transfer in transparent or registered modes. A data byte from any one of the six ports can be stored during transparent operation for later recall. Data input to any port may also be read back to itself for byte manipulation or system self-diagnostic purposes.

The 74ABT3284 is useful for interleaving data in memory applications or for use in bus-to-bus communications where variations in data word length or construction are required.

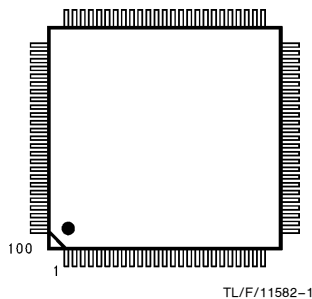
- 18-bit 2:1 or 9-bit 4:1 multiplexed modes
- Registered or transparent datapath operation
- Output enables and select lines have the option of being synchronized for pipelined operation
- Independent input, output register and control synchronizing clocks insure maximum timing flexibility
- Independent control signals insure functional flexibility
- Guaranteed simultaneous switching noise level and dynamic threshold performance
- Guaranteed latchup protection
- High impedance glitch free bus loading during entire power up and power down cycle
- Non-destructive hot insertion capability

Features

- Advanced BiCMOS technology provides high speed at low power consumption

Commercial	Package Number	Package Description
74ABT3284VJG	VJG100A	100-Lead (14mm x 14mm) Molded Plastic Quad Flatpak, JEDEC

Connection Diagram



Pin Assignment

Pin		Pin		Pin		Pin	
1	Mode__SO	26	V _{CC}	51	CP__IN	76	V _{CC}
2	CP__AX	27	A ₈	52	OE _B	77	D ₈
3	OE _C	28	A ₇	53	LDBI	78	D ₇
4	LDCI	29	A ₆	54	LDBO	79	D ₆
5	LDCO	30	GND	55	Mode__W	80	GND
6	SA ₂ X ₁	31	A ₅	56	YSEL	81	D ₅
7	SA ₂ X ₀	32	A ₄	57	OE _Y	82	D ₄
8	X ₀	33	A ₃	58	Y ₈	83	D ₃
9	X ₁	34	A ₂	59	Y ₇	84	D ₂
10	GND	35	GND	60	GND	85	GND
11	X ₂	36	A ₁	61	Y ₆	86	D ₁
12	X ₃	37	A ₀	62	Y ₅	87	D ₀
13	X ₄	38	V _{CC}	63	Y ₄	88	V _{CC}
14	X ₅	39	B ₀	64	Y ₃	89	C ₀
15	X ₆	40	B ₁	65	Y ₂	90	C ₁
16	GND	41	GND	66	GND	91	GND
17	X ₇	42	B ₂	67	Y ₁	92	C ₂
18	X ₈	43	B ₃	68	Y ₀	93	C ₃
19	OE _X	44	B ₄	69	LDDO	94	C ₄
20	XSEL ₀	45	B ₅	70	LDDI	95	C ₅
21	XSEL ₁	46	GND	71	ASEL1	96	GND
22	LDAO	47	B ₆	72	ASEL0	97	C ₆
23	LDAI	48	B ₇	73	OE _D	98	C ₇
24	OE _A	49	B ₈	74	CP__XA	99	C ₈
25	V _{CC}	50	V _{CC}	75	Mode__SC	100	V _{CC}

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Functional Description

The 74ABT3284 is a bi-directional registered data-path routing device which can multiplex/de-multiplex four 9-bit “A-side” data ports (Ports A, B, C, D) onto/from one 9-bit “X-side” port (Port X). Alternatively, it can be configured for mux/demux of two 18-bit data paths (Ports A and C, B and D) onto/from one 18-bit data path (Ports X and Y).

Each of the six 9-bit I/O ports have independent active low TRI-STATE® output enable control logic which can be configured to operate asynchronously or synchronously. With `MODE__SO` low, direct asynchronous output control is provided. With `MODE__SO` high, output enable control is asserted synchronously on the positive edge of the `CP__IN` clock. All I/O port inputs are continuously active allowing output state feedback.

The four A-side ports (A, B, C, D) contain independently enabled input and output data registers for storage of data passing in either direction. The input register (AIR, BIR, CIR, DIR) is loaded/held on the positive edge of `CP__AX` when the respective Load Control pin (LDAI, LDBI, LDCI, LDDI) is asserted high/low. The Input Registers can be loaded with data from the corresponding A-side port. The output register (AOR, BOR, COR, DOR) is loaded/held on the positive edge of `CP__XA` when the respective Load Control pin (LDAO, LDBO, LDCO, LDDO) is asserted high/low. The Output Registers can be loaded with data from Port X when `MODE__WS` is asserted low. When `MODE__WS` is asserted high, the Output Registers A and C can be loaded with Port X data and the B and D Output Registers can be loaded with data from Port Y.

When routing data from A-side to X-side, Data Path Control is provided for the following options via the `SA2X` inputs; Transparent mode where Input Register is bypassed but can simultaneously monitor A-side data; Registered Mode where X-side receives data from the selected Input Registers; Readback Mode where X-side receives data from the selected Output Registers. A-side data from Ports A, B, C, or D can be selected to Port X via the `XSEL` data path select inputs. Ports B or D can be selected to Port Y via the `YSEL` data path select input.

When routing data from X-side to A-side, Data Path Control is provided for the following options via the `ASEL` inputs; Transparent mode where Output Register is bypassed but can simultaneously monitor X-side data; Registered Mode where the A-side Port receives data from the corresponding Output Register; Readback Mode where the A-side Port receives data from the corresponding Input Registers. `MODE__WS` asserted low selects Port X data to be passed to Ports A, B, C, and D. With `MODE__WS` asserted high, Port X data is passed to Ports A and C with Port Y data passed to Ports B and D.

All Data Path Control Inputs and Input/Output Register Load Enable Inputs are active high and can be asserted asynchronously or synchronously. When `MODE__SC` is low, these inputs operate asynchronously. When `MODE__SC` is high, the inputs are asserted synchronously on the positive edge of the `CP__IN` clock.

When operating the Data Path Control and/or the Output Enable Input groups with `MODE__SC` and/or `MODE__SO` “hard wired” high for synchronous mode, a single pre-clock of `CP__IN` will be required following power-up to insure that all internal synchronous control registers are in the appropriate known state. if the application requires “on the fly” changes from asynchronous to synchronous operation, then the respective control/enable pin data must be pre-clocked via `CP__IN` and held steady prior to and during any low to high transition of the `MODE__SO` or `MODE__SC` to properly initiate the sync control registers for synchronous control mode.

Pin Descriptions

Pin Name	Description	Operation
$\overline{OEa}$	Output Enable Inputs (Active Low)	Sync/ Async
LDAI	Load Enable Inputs for the Input Registers	Sync/ Async
LDAO	Load Enable Inputs for the Output Registers	Sync/ Async
ASEL(0,1)	A-Side Data Path Select Inputs	Sync/ Async
SA2X(0,1)	X-Side Data Path Select Inputs	Sync/ Async
XSEL(0,1)	X-Port Data Path Select Inputs	Sync/ Async
YSEL	Y-Port Data Path Select Input	Sync/ Async
MODE__W	Word Mode Select Input for the X/Y to A-Side Direction	Sync/ Async
MODE__SO	Enable Input for Synchronous Output Enable Control	Async
MODE__SC	Enable Input for Synchronous Data Path Control	Async
CP__IN	Clock Input for Synchronous Control (Positive Edge Trigger)	
CP__AX	Clock Input for Input Registers (Positive Edge Trigger)	
CP__XA	Clock Input for Output Registers (Positive Edge Trigger)	

Function Tables

Output Enable Control Table

Inputs			Outputs	Control Mode	Function
$\overline{OE}$ (A, B, C, D, X, Y)	MODE__SO	CP__IN	Port A, B, C, D, X, Y		
L	L	X	ENABLE	ASYN	ENABLED OUTPUT, I/O input always active
H	L	X	DISABLE	ASYN	DISABLED OUTPUT, I/O input always active
(Notes 2, 3)	H (Note 1)		(Note 3)	SYNC	(Note 3)

Note 1: Low to High transitions of MODE__SO must be immediately preceded by a low to high transition (clock edge) on CP__IN while holding Synchronous Control Inputs $\overline{OE}$ (A, B, C, D, X, Y) steady to preset internal registers and assure predictable operation during the control mode change from asynchronous to synchronous.

Note 2: $\overline{OE}$ (A, B, C, D, X, Y) levels are synchronously asserted by the positive transition of CP__IN when MODE__SO is high.

Note 3: Synchronous Control Mode Functions are same as Asynchronous at time T + 1 of CP__IN.

A Side Data Path Select Function Table

Inputs				Data Path		Control Mode	Function
ASEL(1)	ASEL(0)	MODE__SC	CP__IN	From Reg/Port	To Port		
L	L	L	X	(A, B, C, D) IR	A, B, C, D	ASYN	Readback; Contents of Input Register (A, B, C, D) IR to Port (A, B, C, D)
L	H	L	X	(A, B, C, D) OR	A, B, C, D	ASYN	Clocked Path; Contents of Output Register (A, B, C, D) OR to Port (A, B, C, D)
H	L	L	X	Port X	A, B, C, & D	ASYN	Transparent Path; Port X to Port A, B, C, & D
H	H	L	X	Port X Port Y	A & C B & D	ASYN	Transparent Path; Port X to Port A & C Transparent Path; Port Y to Port B & D
(Notes 2, 3)	(Notes 2, 3)	H (Note 1)		(Note 3)	(Note 3)	SYNC	(Note 3)

Note 1: Low to High transitions of MODE__SC must be immediately preceded by a low to high transition (clock edge) on CP__IN while holding Synchronous Control Inputs ASEL(0) and ASEL(1) steady to preset internal registers and assure predictable operation during the control mode change from asynchronous to synchronous.

Note 2: ASEL(0) and ASEL(1) levels are synchronously asserted by the positive transition of CP__IN when MODE__SC is high.

Note 3: Synchronous Control Mode Functions are same as Asynchronous at time T + 1 of CP__IN.

Input Register Control Table

Inputs					Register	Control Mode	Function
Port (A, B, C, D)	LD(A, B, C, D) I	MODE__SC	CP__IN	CP__XA	(A, B, C, D) IR		
X	L	L	X		HOLD	ASYN	HOLD; Input Register holds previous state.
L (H)	H	L	X		L (H)	ASYN	LOAD; Port A, B, C, D clocked to Input Register (A, B, C, D) IR via CP__AX positive edge
(Note 3)	(Notes 2, 3)	H (Note 1)		(Note 3)	(Note 3)	SYNC	(Note 3)

Note 1: Low to High transitions of MODE__SO must be immediately preceded by a low to high transition (clock edge) on CP__IN while holding Synchronous Control Inputs LDAI, LDBI, LDCI, and LDDI steady to preset internal registers and assure predictable operation during the control mode change from asynchronous to synchronous.

Note 2: LDAI, LDBI, LDCI and LDDI levels are synchronously asserted by the positive transition of CP__IN when MODE__SC is high.

Note 3: Synchronous Control Mode Functions are same as Asynchronous at time T + 1 of CP__IN.

Function Tables (Continued)

Output Register Control Table

Inputs							Output Register		Control Mode	Function
Port X	Port Y	LD(A, B, C, D) O	MODE__W	MODE__SC	CP__IN	CP__XA	(A, C) OR	(B, D) OR		
X	X	L	X	L	X		HOLD	HOLD	ASYNC	HOLD OR
L (H)	X	H	L	L	X		L (H)	L (H)	ASYNC	LOAD OR Port X to OR (A, B, C, D)
L (H)	L (H)	H	H	L	X		L (H)	L (H)	ASYNC	LOAD OR Port X to OR (A, C) Port Y to OR (B, D)
(Note 3)	(Note 3)	(Notes 2, 3)	(Notes 2, 3)	H (Note 1)		(Note 3)	(Note 3)	(Note 3)	SYNC	(Note 3)

Note 1: Low to High transitions of MODE__SC must be immediately preceded by a low to high transition (clock edge) on CP__IN while holding Synchronous Control Inputs LDAO, LDBO, LDCO, LDDO and MODE__W steady to preset internal registers and assure predictable operation during the control mode change from asynchronous to synchronous.

Note 2: LDAO, LDBO, LDCO, LDDO and MODE__W levels are synchronously asserted by the positive transition of CP__IN when MODE__SC is high.

Note 3: Synchronous Control Mode Functions are same as Asynchronous at time $T + 1$ of CP__IN.

Function Tables (Continued)

1st Level X Side Data Path Select Function Table

Inputs				Data Path		Control Mode	Function
SA2X(1)	SA2X(0)	MODE__SC	CP__IN	From Reg/Port	To Internal Node		
L	L	L	X	A, B, C, D	(A, B, C, D) X	ASync	Transparent datapath from Port (A, B, C, D) to internal node (A, B, C, D) X
L	H	L	X	(A, B, C, D) IR	(A, B, C, D) X	ASync	Clocked Path; Contents of Input Register (A, B, C, D) IR to internal node (A, B, C, D) X
H	L	L	X	(A, B, C, D) OR	(A, B, C, D) X	ASync	Readback; contents of Output register (A, B, C, D) OR to internal node (A, B, C, D) X
H	H	L	X	GND	(A, B, C, D) X	ASync	D diagnostic; Select all 36 bits as low and pass to the internal node (A, B, C, D) X
(Notes 2, 3)	(Notes 2, 3)	H (Note 1)		(Note 3)	(Note 3)	Sync	(Note 3)

Note 1: Low to High transitions of MODE__SC must be immediately preceded by a low to high transition (clock edge) on CP__IN while holding Synchronous Control Inputs SA2X(0) and SA2X(1) steady to preset internal sync registers and assure predictable operation during the control mode change from asynchronous to synchronous.

Note 2: SA2X(0) and SA2X(1) levels are synchronously asserted by the positive transition of CP__IN when MODE__SC is high.

Note 3: Synchronous Control Mode Functions are same as Asynchronous at time T + 1 of CP__IN.

2nd Level X Side Data Path Select Function Table for Port X

Inputs				Data Path		Control Mode	Function
XSEL(1)	XSEL(0)	MODE__SC	CP__IN	From Internal Node	To Port		
L	L	L	X	AX	X	ASync	Internal Node AX to Port X
L	H	L	X	BX	X	ASync	Internal Node BX to Port X
H	L	L	X	CX	X	ASync	Internal Node CX to Port X
H	H	L	X	DX	X	ASync	Internal Node DX to Port X
(Notes 2, 3)	(Notes 2, 3)	H (Note 1)		(Note 3)	(Note 3)	Sync	(Note 3)

Note 1: Low to High transitions of MODE__SC must be immediately preceded by a low to high transition (clock edge) on CP__IN while holding Synchronous Control Inputs XSEL(0) and XSEL(1) steady to preset internal sync registers and assure predictable operation during the control mode change from asynchronous to synchronous.

Note 2: XSEL(0) and XSEL(1) levels are synchronously asserted by the positive transition of CP__IN when MODE__SC is high.

Note 3: Synchronous Control Mode Functions are same as Asynchronous at time T + 1 of CP__IN.

2nd Level X Side Data Path Select Function Table for Port Y

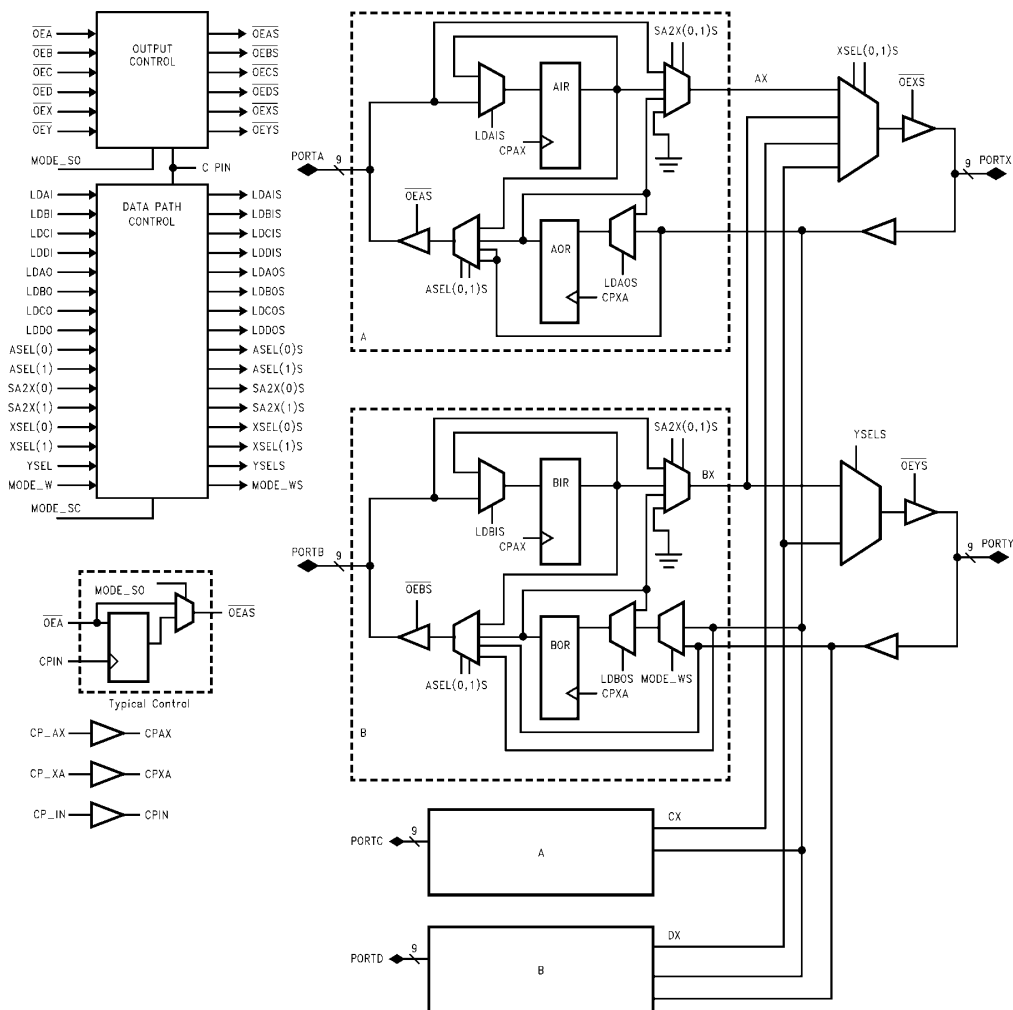
Inputs			Data Path		Control Mode	Function
YSEL	MODE__SC	CP__IN	From Internal Node	To Port		
L	L	X	BX	Y	ASync	Internal Node BX to Port Y
H	L	X	DX	Y	ASync	Internal Node DX to Port Y
(Notes 2, 3)	H (Note 1)		(Note 3)	(Note 3)	Sync	(Note 3)

Note 1: Low to High transitions of MODE__SC must be immediately preceded by a low to high transition (clock edge) on CP__IN while holding Synchronous Control Inputs YSEL steady to preset internal registers and assure predictable operation during the control mode change from asynchronous to synchronous.

Note 2: YSEL levels are synchronously asserted by the positive transition of CP__IN when MODE__SC is high.

Note 3: Synchronous Control Mode Functions are same as Asynchronous at time T + 1 of CP__IN.

Logic Diagrams

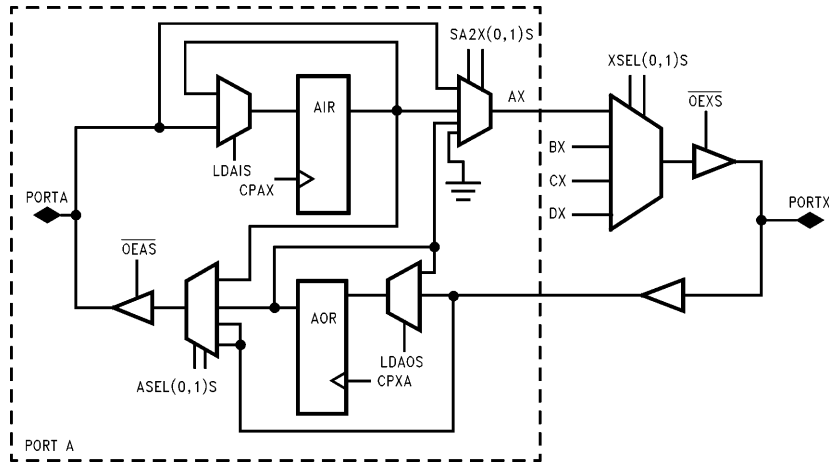


TL/F/11582-2

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

FIGURE 1. 18-Bit Synchronous Datapath Multiplexer

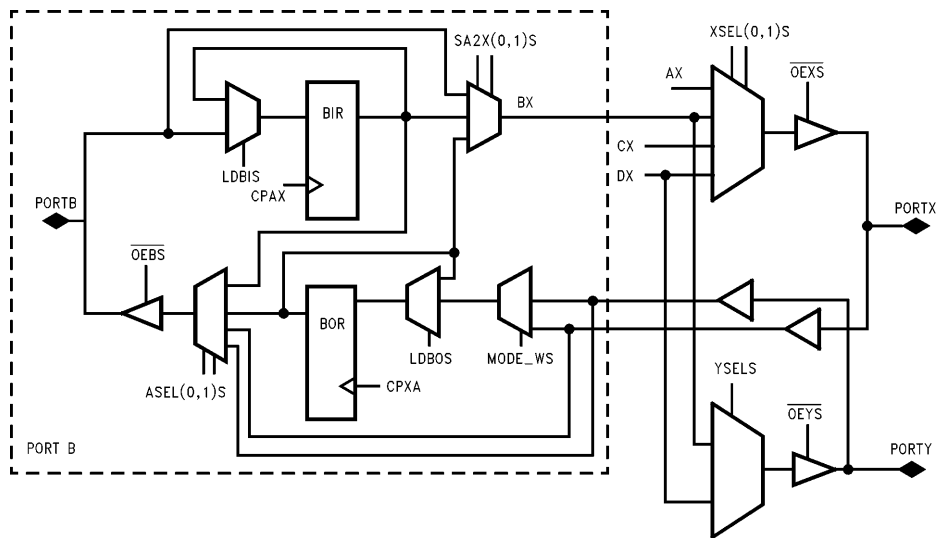
Logic Diagrams (Continued)



Note: Port C configured identical to Port A.

**FIGURE 2. Synchronous Bus Multiplexer
A-X Datapath**

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Note: Port D configured identical to Port B.

**FIGURE 3. Synchronous Bus Multiplexer
B PORT Datapath**

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Absolute Maximum Ratings (Note 1)

Storage Temperature	−65°C to +150°C
Ambient Temperature under Bias	−55°C to +125°C
Junction Temperature under Bias	
Ceramic	−55°C to +175°C
Plastic	−55°C to +150°C
V _{CC} Pin Potential to Ground Pin	−0.5V to +7.0V
Input Voltage (Note 2)	−0.5V to +7.0V
Input Current (Note 2)	−30 mA to +5.0 mA
Voltage Applied to Any Output	
in the Disabled or Power-off State	−0.5V to +5.5V
in the HIGH STATE	−0.5V to V _{CC}
Current Applied to Output	
in LOW State (Max)	twice the rated I _{OL} (mA)

DC Latchup Source Current	−300 mA
Over Voltage Latchup (I/O)	10V

Note 1: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Either voltage limit or current limit is sufficient to protect inputs.

Recommended Operating Conditions

Free Air Ambient Temperature	
Commercial	−40°C to +85°C
Supply Voltage	
Commercial	+4.5V to +5.5V
Minimum Input Edge Rate	(ΔV/Δt)
Data Input	50 mV/ns
Enable Input	20 mV/ns
Clock Input	100 mV/ns

DC Electrical Characteristics

Symbol	Parameter	ABT3284			Units	V _{CC}	Conditions
		Min	Typ	Max			
V _{IH}	Input HIGH Voltage	2.0			V		Recognized HIGH Signal
V _{IL}	Input LOW Voltage		0.8		V		Recognized LOW Signal
V _{CD}	Input Clamp Voltage			−1.2	V	Min	I _{IN} = −18 mA
V _{OH}	Output HIGH Voltage	2.5 2.0			V	Min	I _{OH} = −3 mA I _{OH} = −32 mA (Note 3)
V _{OL}	Output LOW Voltage		0.55		V	Min	I _{OL} = 64 mA (Note 4)
I _{IH}	Input HIGH Current		5		μA	Max	V _{IN} = V _{CC}
I _{BVI}	Input HIGH Current Breakdown Test		7		μA	Max	V _{IN} = 7.0V Control Inputs
I _{BVIT}	Input HIGH Current Breakdown Test (I/O)		100		μA	Max	V _{IN} = 5.5V (A _n , B _n , C _n , D _n , X _n , Y _n)
I _{IL}	Input LOW Current		−5		μA	Max	V _{IN} = 0.5V Control Inputs
V _{ID}	Input Leakage Test	4.75			V	0.0	I _{ID} = 1.9 μA Control Inputs All Data Pins Grounded
I _{IH} + I _{OZH}	Output Leakage Current		50		μA	0–5.5	V _{OUT} = 2.7V (A _n , B _n , C _n , D _n , X _n , Y _n) All Output Enables = 2.0V
I _{IL} + I _{OZL}	Output Leakage Current		−50		μA	0–5.5	V _{OUT} = 0.5V (A _n , B _n , C _n , D _n , X _n , Y _n) All Output Enables = 2.0V
I _{OS}	Output Short-Circuit Current	−100	−275		mA	Max	V _{OUT} = 0.0V (A _n , B _n , C _n , D _n , X _n , Y _n) (Note 5)
I _{CEX}	Output High Leakage Current		50		μA	Max	V _{OUT} = V _{CC} (A _n , B _n , C _n , D _n , X _n , Y _n)
I _{ZZ}	Bus Drainage Test		100		μA	0.0	V _{OUT} = 5.5V (A _n , B _n , C _n , D _n , X _n , Y _n)
I _{CCH}	Power Supply Current		2.5		mA	Max	All Outputs HIGH
I _{CCL}	Power Supply Current		140		mA	Max	36 Outputs LOW
I _{CCZ}	Power Supply Current		2.5		mA	Max	Output Enables = V _{CC} ; All Others at GND
I _{CCT}	Additional I _{CC} /Input		2.5		mA	Max	V _{IN} = V _{CC} − 2.1V All Others at V _{CC} or GND
I _{CCD}	Dynamic I _{CC} No Load		0.35		mA/ MHz	Max	Outputs Open, Transparent Mode Output Enables = GND One Bit Toggling, 50% Duty Cycle

Note 3: Up to 18 outputs can each source 32 mA continuously, or any combination of outputs can source up to a total of 324 mA. For example, 36 outputs can continuously each source 16 mA.

Note 4: Up to 18 outputs can each sink 64 mA continuously, or any combination of outputs can sink up to a total of 648 mA. For example, 36 outputs can continuously each sink 32 mA.

Note 5: One output at a time, duration 1 second maximum.

DC Electrical Characteristics (Continued)

Symbol	Parameter	Min	Typ	Max	Units	V _{CC}	Conditions C _L = 50 pF, R _L = 500Ω
V _{OLP}	Quiet Output Maximum Dynamic V _{OL}		0.7	1.0	V	5.0	T _A = 25°C (Note 1)
V _{OLV}	Quiet Output Minimum Dynamic V _{OL}	−0.8	−0.5		V	5.0	T _A = 25°C (Note 1)
V _{OHV}	Minimum High Level Dynamic Output Voltage	2.5	3.0		V	5.0	T _A = 25°C (Note 3)
V _{IHD}	Minimum High Level Dynamic Input Voltage	2.0	1.7		V	5.0	T _A = 25°C (Note 2)
V _{ILD}	Maximum Low Level Dynamic Input Voltage		1.2	0.8	V	5.0	T _A = 25°C (Note 2)

Note 1: Max number of outputs defined as (n). n − 1 data inputs are driven 0V to 3V. One output at LOW. Guaranteed, but not tested.

Note 2: Max number of data inputs (n) switching. n − 1 inputs switching 0V to 3V. Input-under-test switching: 3V to threshold (V_{ILD}), 0V to threshold (V_{IHD}). Guaranteed, but not tested.

Note 3: Max number of outputs defined as (n). n − 1 data inputs are driven 0V to 3V. One output HIGH. Guaranteed, but not tested.

AC Electrical Characteristics Single Output Switching

Symbol	Parameter	74ABT		74ABT		Units
		$T_A = 25^{\circ}\text{C}$ $V_{CC} = 5.0\text{V}$ $C_L = 50\text{ pF}$		$T_A = -40^{\circ}\text{C to } +85^{\circ}\text{C}$ $V_{CC} = 4.5\text{V to } 5.5\text{V}$ $C_L = 50\text{pF}$		
		Min	Max	Min	Max	
f _{MAX}	Max Operating Frequency	150				
t _{PHL} t _{PLH}	Propagation Delay A, B, C, D or X Inputs to X or A, B, C, D Outputs. Transparent Mode	1.5	5.5	1.5	5.5	ns
t _{PHL} t _{PLH}	Propagation Delay B, D or Y Inputs to Y or B, D Outputs. Transparent Mode	1.0	5.0	1.0	5.0	ns
t _{PHL} t _{PLH}	Propagation Delay CP__XA ↑ to A, B, C, or D. Registered Mode	1.5	6.0	1.5	6.0	ns
t _{PHL} t _{PLH}	Propagation Delay CP__AX ↑ to X. Registered Mode	1.5	7.0	1.5	7.0	ns
t _{PHL} t _{PLH}	Propagation Delay CP__AX ↑ to Y. Registered Mode	1.5	6.5	1.5	6.5	ns
t _{PHL} t _{PLH}	Propagation Delay ASELn to A, B, C or D. Asynchronous Mode	2.0	7.5	2.0	7.5	ns
t _{PHL} t _{PLH}	Propagation Delay CP__IN ↑ to A, B, C or D. ASELn Synchronous Mode	2.5	8.5	2.5	8.5	ns
t _{PHL} t _{PLH}	Propagation Delay SA2Xn to X or Y. Asynchronous Mode	1.5	7.5	1.5	7.5	ns
t _{PHL} t _{PLH}	Propagation Delay CP__IN ↑ to X or Y. SA2Xn Synchronous Mode	2.0	8.5	2.0	8.5	ns
t _{PHL} t _{PLH}	Propagation Delay XSELn to X. Asynchronous Mode	1.5	6.0	1.5	6.0	ns
t _{PHL} t _{PLH}	Propagation Delay CP__IN ↑ to X. XSELn Synchronous Mode	2.0	7.5	2.0	7.5	ns
t _{PHL} t _{PLH}	Propagation Delay YSELn to Y. Asynchronous Mode	1.0	5.5	1.0	5.5	ns
t _{PHL} t _{PLH}	Propagation Delay CP__IN ↑ to Y. YSELn Synchronous Mode	1.5	6.5	1.5	6.5	ns
t _{PZH} t _{PZL}	Asynchronous Enable Time	1.0	6.0	1.0	6.0	ns
t _{PZH} t _{PZL}	Synchronous Enable Time	1.5	7.0	1.5	7.0	ns
t _{PHZ} t _{PLZ}	Asynchronous Disable Time	1.0	7.5	1.0	7.5	ns
t _{PHZ} t _{PLZ}	Synchronous Disable Time	1.5	8.5	1.5	8.5	ns

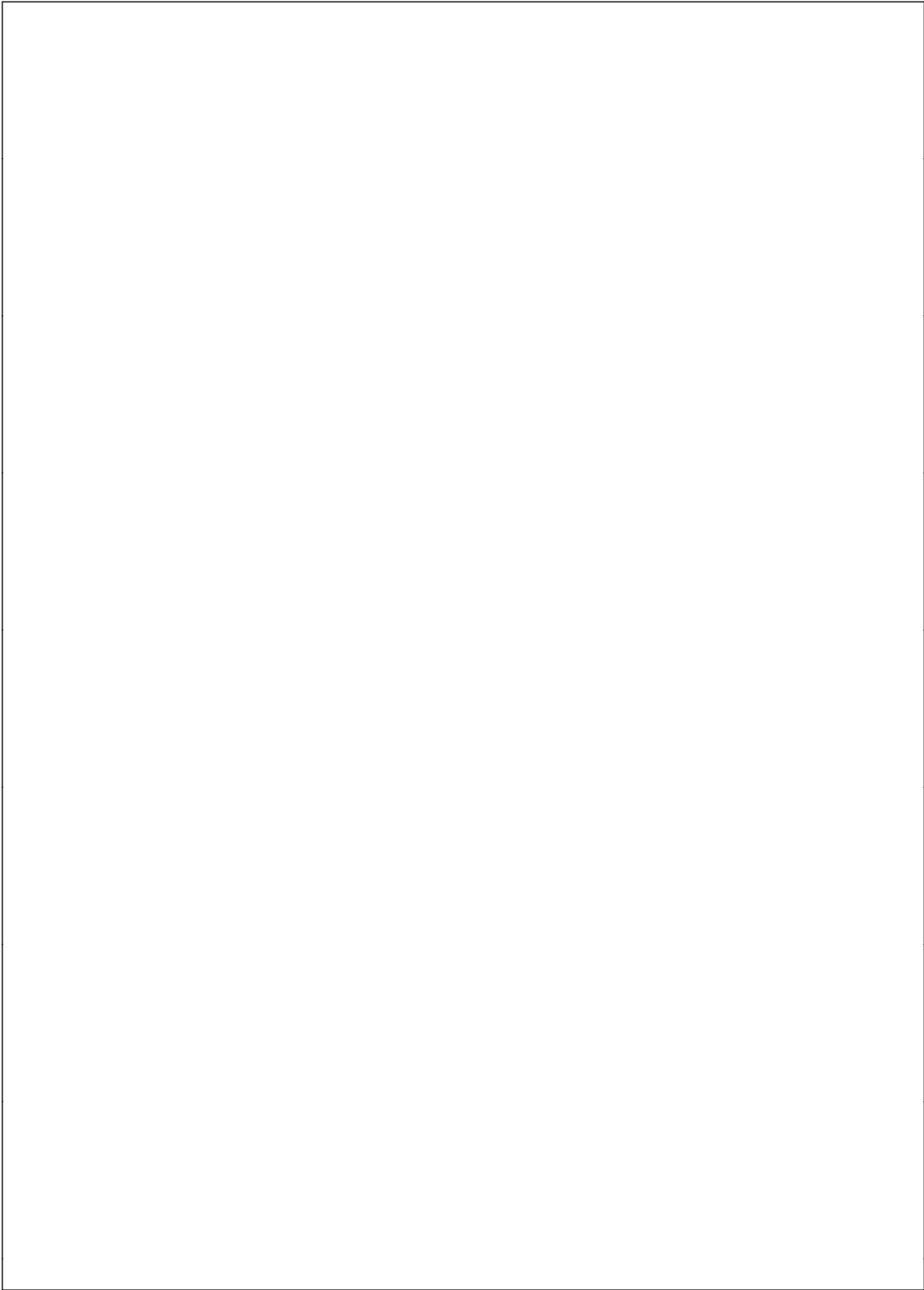
AC Operating Requirements Single Output Switching

Symbol	Parameter	74ABT	74ABT	Units
		$T_A = 25^{\circ}\text{C}$ $V_{CC} = 5.0\text{V}$ $C_L = 50\text{ pF}$	$T_A = -40^{\circ}\text{C to } +85^{\circ}\text{C}$ $V_{CC} = 4.5\text{V to } 5.5\text{V}$ $C_L = 50\text{ pF}$	
		Min	Max	
$t_s(\text{H})$ $t_s(\text{L})$	Setup Time High or Low A, B, C, D X or Y. Data to CP__AX $\uparrow$ or CP__XA $\uparrow$ (Registered Mode)	4.0	4.0	ns
$t_h(\text{H})$ $t_h(\text{L})$	Hold Time High or Low A, B, C, D X or Y. Data to CP__AX $\uparrow$ or CP__XA $\uparrow$ (Registered Mode)	0.0	0.0	ns
$t_s(\text{H})$ $t_s(\text{L})$	Setup Time High or Low Control Inputs to CP__IN $\uparrow$. (Synchronous Mode)	3.0	3.0	ns
$t_h(\text{H})$ $t_h(\text{L})$	Hold Time High or Low Control Inputs to CP__IN $\uparrow$. (Synchronous Mode)	0.0	0.0	ns
$t_s(\text{H})$	Setup Time High, CP__IN $\uparrow$ to CP__AX $\uparrow$ or CP__XA $\uparrow$.	5.0	5.0	ns
$t_h(\text{L})$	Hold Time Low, CP__IN $\uparrow$ to CP__AX $\uparrow$ or CP__XA $\uparrow$.	0.0	0.0	ns
$t_w(\text{H})$ $t_w(\text{L})$	CLK Pulsewidth High CLK Pulsewidth Low	3.0 4.0	3.0 4.0	ns

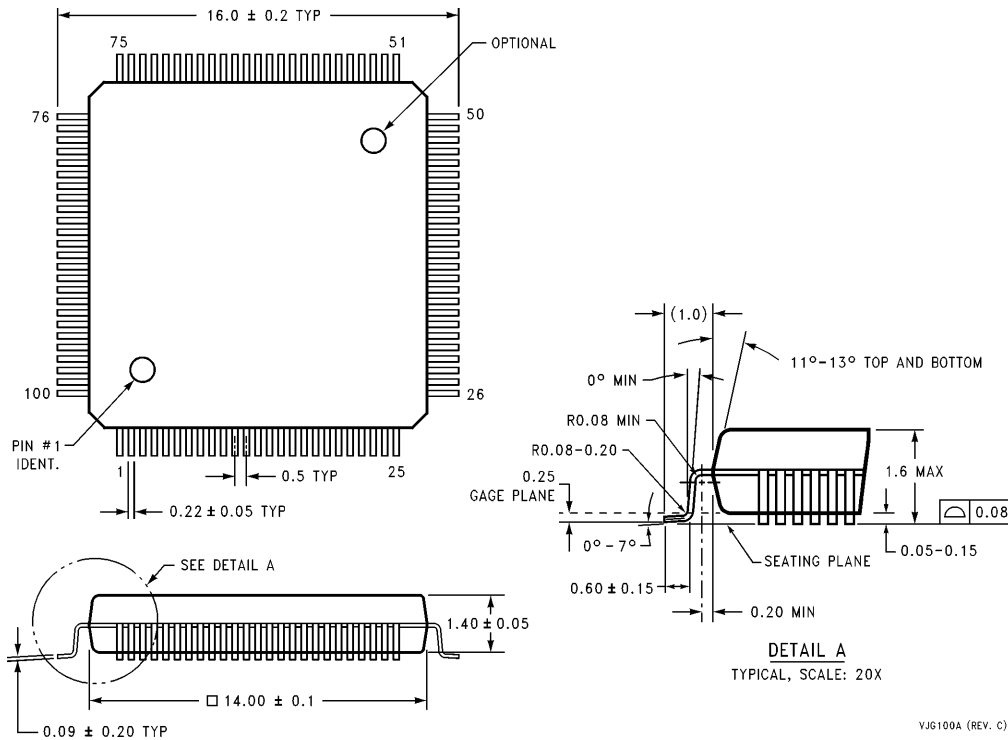
Capacitance

Symbol	Parameter	Typ	Units	Conditions $T_A = 25^{\circ}\text{C}$
C_{IN}	Input Capacitance	5	pF	$V_{CC} = 0\text{V}$ Control Inputs
$C_{I/O}$ (Note 1)	I/O Capacitance	11	pF	$V_{CC} = 5.0\text{V}$ ($A_n, B_n, C_n, D_n, X_n, Y_n$)

Note 1: $C_{I/O}$ is measured at frequency $f = 1\text{ MHz}$, per MIL-STD-883B, Method 3012.



Physical Dimensions inches (millimeters)



100-Lead Thin Quad Flatpak (TQFP)
NS Package Number VJG100A

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