Peregrine Semiconductor

# Product Specification

# PE3238

**1500 MHz UltraCMOS™ Integer-N PLL for Low Phase Noise Applications**

### Features

- 1.5 GHz operation
- ÷10/11 dual modulus prescaler
- Internal phase detector
- Serial, parallel or hardwired programmable
- Low power ¾ 20 mA at 3 V
- Q3236 PLL replacement
- Ultra-low phase noise

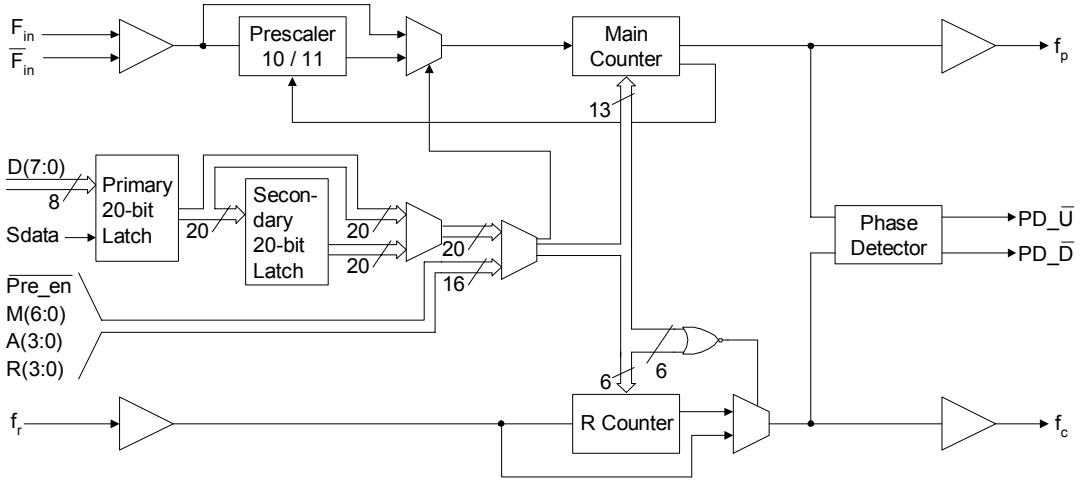
## Product Description

*Peregrine's PE3238 is a high performance integer-N PLL capable of frequency synthesis up to 1.5 GHz. The superior phase noise performance of the PE3238 is ideal for applications such as LMDS / MMDS / WLL basestations and demanding terrestrial systems.*

*The PE3238 features a 10/11 dual modulus prescaler, counters and a phase comparator as shown in Figure 1. Counter values are programmable through either a serial or parallel interface and can also be directly hard wired. This programming flexibility, combined with the dual latch architecture enabling ping-pong loading of the main divide counter, makes these PLLs well suited as the core for fractional-N or sigma-delta implementation.*

*The PE3238 is optimized for terrestrial applications. It is manufactured on Peregrine's UltraCMOS™ process, a patented variation of silicon-on-insulator (SOI) technology on a sapphire substrate, offering the performance of GaAs with the economy and integration of conventional CMOS.*

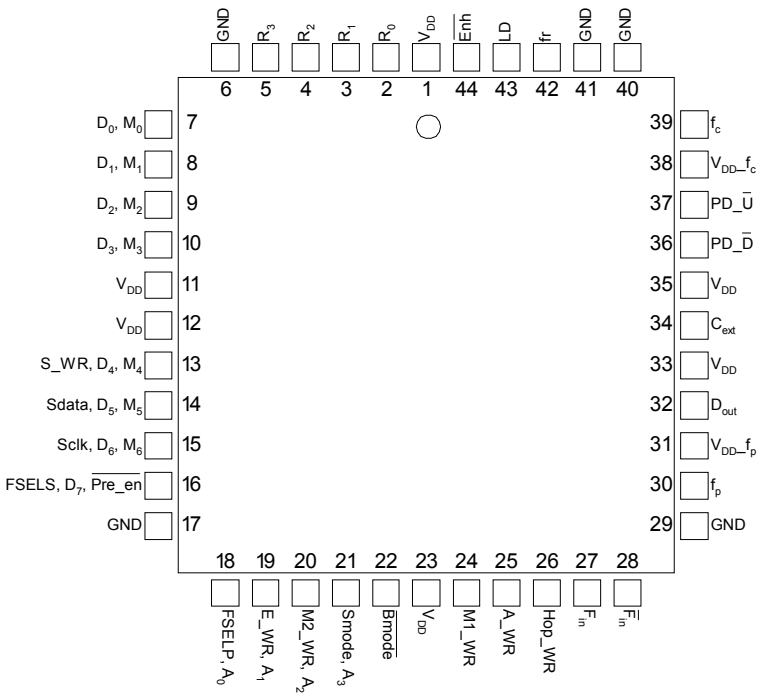
**Figure 1. Block Diagram**





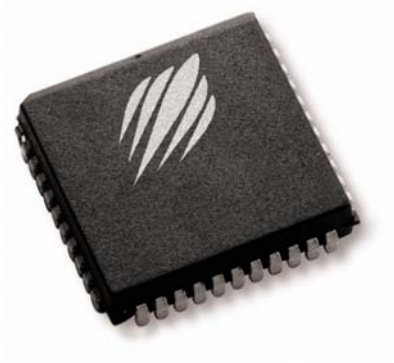
©2003-2005 Peregrine Semiconductor Corp. All rights reserved.

## Figure 2. Pin Configurations (Top View)




## Figure 3. Package Type

44-lead PLCC



## Table 1. Pin Descriptions

| Pin No. | Pin Name | Interface Mode | Type | Description |
|---|---|---|---|---|
| 1 | $V_{DD}$ | ALL | (Note 1) | Power supply input. Input may range from 2.85 V to 3.15 V. Bypassing recommended. |
| 2 | $R_0$ | Direct | Input | R Counter bit0 (LSB). |
| 3 | $R_1$ | Direct | Input | R Counter bit1. |
| 4 | $R_2$ | Direct | Input | R Counter bit2. |
| 5 | $R_3$ | Direct | Input | R Counter bit3. |
| 6 | GND | ALL | (Note 1) | Ground. |
| 7 | $D_0$ | Parallel | Input | Parallel data bus bit0 (LSB). |
| | $M_0$ | Direct | Input | M Counter bit0 (LSB). |
| 8 | $D_1$ | Parallel | Input | Parallel data bus bit1. |
| | $M_1$ | Direct | Input | M Counter bit1. |
| 9 | $D_2$ | Parallel | Input | Parallel data bus bit2. |
| | $M_2$ | Direct | Input | M Counter bit2. |
| 10 | $D_3$ | Parallel | Input | Parallel data bus bit3. |
| | $M_3$ | Direct | Input | M Counter bit3. |
| 11 | $V_{DD}$ | ALL | (Note 1) | Same as pin 1. |
| 12 | $V_{DD}$ | ALL | (Note 1) | Same as pin 1. |

*©2003-2005 Peregrine Semiconductor Corp. All rights reserved.*

## Table 1. Pin Descriptions (continued)

| Pin No. | Pin Name | Interface Mode | Type | Description |
|---|---|---|---|---|
| 13 | S_WR | Serial | Input | Serial load enable input. While S_WR is "low", Sdata can be serially clocked. Primary register data are transferred to the secondary register on S_WR or Hop_WR rising edge. |
| | $D_4$ | Parallel | Input | Parallel data bus bit4. |
| | $M_4$ | Direct | Input | M Counter bit4. |
| 14 | Sdata | Serial | Input | Binary serial data input. Input data entered MSB first. |
| | $D_5$ | Parallel | Input | Parallel data bus bit5. |
| | $M_5$ | Direct | Input | M Counter bit5. |
| 15 | Sclk | Serial | Input | Serial clock input. Sdata is clocked serially into the 20-bit primary register (E_WR "low") or the 8-bit enhancement register (E_WR "high") on the rising edge of Sclk. |
| | $D_6$ | Parallel | Input | Parallel data bus bit6. |
| | $M_6$ | Direct | Input | M Counter bit6. |
| 16 | FSELS | Serial | Input | Selects contents of primary register (FSELS=1) or secondary register (FSELS=0) for programming of internal counters while in Serial Interface Mode. |
| | $D_7$ | Parallel | Input | Parallel data bus bit7 (MSB). |
| | $\overline{\text{Pre_en}}$ | Direct | Input | Prescaler enable, active "low". When "high", $F_{in}$ bypasses the prescaler. |
| 17 | GND | ALL | | Ground. |
| 18 | FSELP | Parallel | Input | Selects contents of primary register (FSELP=1) or secondary register (FSELP=0) for programming of internal counters while in Parallel Interface Mode. |
| | $A_0$ | Direct | Input | A Counter bit0 (LSB). |
| 19 | E_WR | Serial | Input | Enhancement register write enable. While E_WR is "high", Sdata can be serially clocked into the enhancement register on the rising edge of Sclk. |
| | | Parallel | Input | Enhancement register write. D[7:0] are latched into the enhancement register on the rising edge of E_WR. |
| | $A_1$ | Direct | Input | A Counter bit1. |
| 20 | M2_WR | Parallel | Input | M2 write. D[3:0] are latched into the primary register (R[5:4], M[8:7]) on the rising edge of M2_WR. |
| | $A_2$ | Direct | Input | A Counter bit2. |
| 21 | Smode | Serial, Parallel | Input | Selects serial bus interface mode ($\overline{\text{Bmode}}$=0, Smode=1) or Parallel Interface Mode ($\overline{\text{Bmode}}$=0, Smode=0). |
| | $A_3$ | Direct | Input | A Counter bit3 (MSB). |
| 22 | $\overline{\text{Bmode}}$ | ALL | Input | Selects direct interface mode ($\overline{\text{Bmode}}$=1). |
| 23 | $V_{DD}$ | ALL | (Note 1) | Same as pin 1. |
| 24 | M1_WR | Parallel | Input | M1 write. D[7:0] are latched into the primary register ($\overline{\text{Pre_en}}$, M[6:0]) on the rising edge of M1_WR. |
| 25 | A_WR | Parallel | Input | A write. D[7:0] are latched into the primary register (R[3:0], A[3:0]) on the rising edge of A_WR. |
| 26 | Hop_WR | Serial, Parallel | Input | Hop write. The contents of the primary register are latched into the secondary register on the rising edge of Hop_WR. |
| 27 | $F_{in}$ | ALL | Input | Prescaler input from the VCO. 1.5 GHz max frequency. |
| 28 | $\overline{F_{in}}$ | ALL | Input | Prescaler complementary input. A bypass capacitor in series with a 51 ohm resistor should be placed as close as possible to this pin and be connected directly to the ground plane. |
| 29 | GND | ALL | | Ground. |


*©2003-2005 Peregrine Semiconductor Corp. All rights reserved.*

## Table 1. Pin Descriptions (continued)

| Pin No. | Pin Name | Interface Mode | Type | Description |
|---|---|---|---|---|
| 30 | $f_p$ | ALL | Output | Monitor pin for main divider output. Switching activity can be disabled through enhancement register programming or by floating or grounding $V_{DD}$ pin 31. |
| 31 | $V_{DD}$-$f_p$ | ALL | (Note 2) | $V_{DD}$ for $f_p$. |
| 32 | Dout | Serial, Parallel | Output | Data Out. The MSEL signal and the raw prescaler output are available on Dout through enhancement register programming. |
| 33 | $V_{DD}$ | ALL | (Note 1) | Same as pin 1. |
| 34 | Cext | ALL | Output | Logical "NAND" of PD_U and PD_D terminated through an on chip, 2 kohm series resistor. Connecting Cext to an external capacitor will low pass filter the input to the inverting amplifier used for driving LD. |
| 35 | $V_{DD}$ | ALL | (Note 1) | Same as pin 1. |
| 36 | PD_D | ALL | Output | PD_D is pulse down when $f_p$ leads $f_c$. |
| 37 | PD_U | ALL | | PD_U is pulse down when $f_c$ leads $f_p$. |
| 38 | $V_{DD}$-$f_c$ | ALL | (Note 2) | $V_{DD}$ for $f_c$. |
| 39 | $f_c$ | ALL | Output | Monitor pin for reference divider output. Switching activity can be disabled through enhancement register programming or by floating or grounding $V_{DD}$ pin 38. |
| 40 | GND | ALL | | Ground. |
| 41 | GND | ALL | | Ground. |
| 42 | $f_r$ | ALL | Input | Reference frequency input. |
| 43 | LD | ALL | Output, OD | Lock detect and open drain logical inversion of Cext. When the loop is in lock, LD is high impedance, otherwise LD is a logic low ("0"). |
| 44 | $\overline{\text{Enh}}$ | Serial, Parallel | Input | Enhancement mode. When asserted low ("0"), enhancement register bits are functional. |

**Note 1:** $V_{DD}$ pins 1, 11, 12, 23, 31, 33, 35 and 38 are connected by diodes and must be supplied with the same positive voltage level.

**Note 2:** $V_{DD}$ pins 31 and 38 are used to power the $f_p$ and $f_c$ outputs and can alternatively be left floating or connected to GND to disable the $f_p$ and $f_c$ outputs.

*©2003-2005 Peregrine Semiconductor Corp. All rights reserved.*

### Table 2. Absolute Maximum Ratings

| Symbol | Parameter/Conditions | Min | Max | Units |
|---|---|---|---|---|
| $V_{DD}$ | Supply voltage | -0.3 | 4.0 | V |
| $V_I$ | Voltage on any input | -0.3 | $V_{DD}$ + 0.3 | V |
| $I_I$ | DC into any input | -10 | +10 | mA |
| $I_O$ | DC into any output | -10 | +10 | mA |
| $T_{stg}$ | Storage temperature range | -65 | 150 | °C |

### Table 3. Operating Ratings

| Symbol | Parameter/Conditions | Min | Max | Units |
|---|---|---|---|---|
| $V_{DD}$ | Supply voltage | 2.85 | 3.15 | V |
| $T_A$ | Operating ambient temperature range | -40 | 85 | °C |

### Table 4. ESD Ratings

| Symbol | Parameter/Conditions | Level | Units |
|---|---|---|---|
| $V_{ESD}$ | ESD voltage human body model (Note 1) | 1000 | V |

**Note 1:** Periodically sampled, not 100% tested. Tested per MIL-STD-883, M3015 C2

### Electrostatic Discharge (ESD) Precautions

When handling this UltraCMOS™ device, observe the same precautions that you would use with other ESD-sensitive devices. Although this device contains circuitry to protect it from damage due to ESD, precautions should be taken to avoid exceeding the specified rating in Table 4.

### Latch-Up Avoidance

Unlike conventional CMOS devices, UltraCMOS™ devices are immune to latch-up.

### Table 5. DC Characteristics: $V_{DD}$ = 3.0 V, -40° C < $T_A$ < 85° C, unless otherwise specified

| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $I_{DD}$ | Operational supply current; Prescaler enabled | $V_{DD}$ = 2.85 to 3.15 V | | 20 | 35 | mA |
| Digital Inputs: All except $f_r$ , $R_0$, $F_{in}$, $\overline{F_{in}}$ | | | | | | |
| $V_{IH}$ | High level input voltage | $V_{DD}$ = 2.85 to 3.15 V | 0.7 x $V_{DD}$ | | | V |
| $V_{IL}$ | Low level input voltage | $V_{DD}$ = 2.85 to 3.15 V | | | 0.3 x $V_{DD}$ | V |
| $I_{IH}$ | High level input current | $V_{IH}$ = $V_{DD}$ = 3.15 V | | | +1 | µA |
| $I_{IL}$ | Low level input current | $V_{IL}$ = 0, $V_{DD}$ = 3.15 V | -1 | | | µA |
| Reference Divider input: $f_r$ | | | | | | |
| $I_{IHR}$ | High level input current | $V_{IH}$ = $V_{DD}$ = 3.15 V | | | +100 | µA |
| $I_{ILR}$ | Low level input current | $V_{IL}$ = 0, $V_{DD}$ = 3.15 V | -100 | | | µA |
| R0 Input (Pull-up Resistor): $R_0$ | | | | | | |
| $I_{IHRO}$ | High level input current | $V_{IH}$ = $V_{DD}$ = 3.15 V | | | +5 | µA |
| $I_{ILRO}$ | Low level input current | $V_{IL}$ = 0, $V_{DD}$ = 3.15 V | -5 | | | µA |
| Counter and phase detector outputs: $f_c$, $f_p$ | | | | | | |
| $V_{OLD}$ | Output voltage LOW | $I_{out}$ = 6 mA | | | 0.4 | V |
| $V_{OHD}$ | Output voltage HIGH | $I_{out}$ = -3 mA | $V_{DD}$ - 0.4 | | | V |
| Lock detect outputs: Cext, LD | | | | | | |
| $V_{OLC}$ | Output voltage LOW, Cext | $I_{out}$ = 0.1 mA | | | 0.4 | V |
| $V_{OHC}$ | Output voltage HIGH, Cext | $I_{out}$ = -0.1 mA | $V_{DD}$ - 0.4 | | | V |
| $V_{OLLD}$ | Output voltage LOW, LD | $I_{out}$ = 1 mA | | | 0.4 | V |


*©2003-2005 Peregrine Semiconductor Corp. All rights reserved.*

## Table 6. AC Characteristics: $V_{DD}$ = 3.0 V, -40° C < $T_A$ < 85° C, unless otherwise specified

| Symbol | Parameter | Conditions | Min | Max | Units |
|---|---|---|---|---|---|
| Control Interface and Latches (see Figures 4, 5, 6) | | | | | |
| $f_{Clk}$ | Serial data clock frequency | (Note 1) | | 10 | MHz |
| $t_{ClkH}$ | Serial clock HIGH time | | 30 | | ns |
| $t_{ClkL}$ | Serial clock LOW time | | 30 | | ns |
| $t_{DSU}$ | Sdata set-up time to Sclk rising edge, D[7:0] set-up time to M1_WR, M2_WR, A_WR rising edge | | 10 | | ns |
| $t_{DHLD}$ | Sdata hold time after Sclk rising edge, D[7:0] hold time to M1_WR, M2_WR, A_WR, E_WR rising edge | | 10 | | ns |
| $t_{PW}$ | S_WR, M1_WR, M2_WR, A_WR, E_WR pulse width | | 30 | | ns |
| $t_{CWR}$ | Sclk rising edge to S_WR rising edge. S_WR, M1_WR, M2_WR, A_WR falling edge to Hop_WR rising edge | | 30 | | ns |
| $t_{CE}$ | Sclk falling edge to E_WR transition | | 30 | | ns |
| $t_{WRC}$ | S_WR falling edge to Sclk rising edge. Hop_WR falling edge to S_WR, M1_WR, M2_WR, A_WR rising edge | | 30 | | ns |
| $t_{EC}$ | E_WR transition to Sclk rising edge | | 30 | | ns |
| Main Divider (Including Prescaler) | | | | | |
| $F_{in}$ | Operating frequency | | 200 | 1500 | MHz |
| $P_{Fin}$ | Input level range | External AC coupling | -10 | 5 | dBm |
| Main Divider (Prescaler Bypassed) | | | | | |
| $F_{in}$ | Operating frequency | | 20 | 220 | MHz |
| $P_{Fin}$ | Input level range | External AC coupling | -5 | 5 | dBm |
| Reference Divider | | | | | |
| $f_r$ | Operating frequency | (Note 3) | | 100 | MHz |
| $P_{fr}$ | Reference input power (Note 2) | Single ended input | -2 | | dBm |
| Phase Detector | | | | | |
| $f_c$ | Comparison frequency | (Note 3) | | 20 | MHz |
| SSB Phase Noise ($F_{in}$ = 1.3 GHz, $f_r$ = 10 MHz, $f_c$ = 1.25 MHz, LBW = 70 kHz, $V_{DD}$ = 3.0 V, Temp = -40° C) | | | | | |
| | | 100 Hz Offset | | -75 | dBc/Hz |
| | | 1 kHz Offset | | -85 | dBc/Hz |

**Note 1:** Fclk is verified during the functional pattern test. Serial programming sections of the functional pattern are clocked at 10 MHz to verify Fclk specification.

**Note 2:** CMOS logic levels can be used to drive reference input if DC coupled. Voltage input needs to be a minimum of 0.5 Vp-p. For optimum phase noise performance, the reference input falling edge rate should be faster than 80mV/ns.

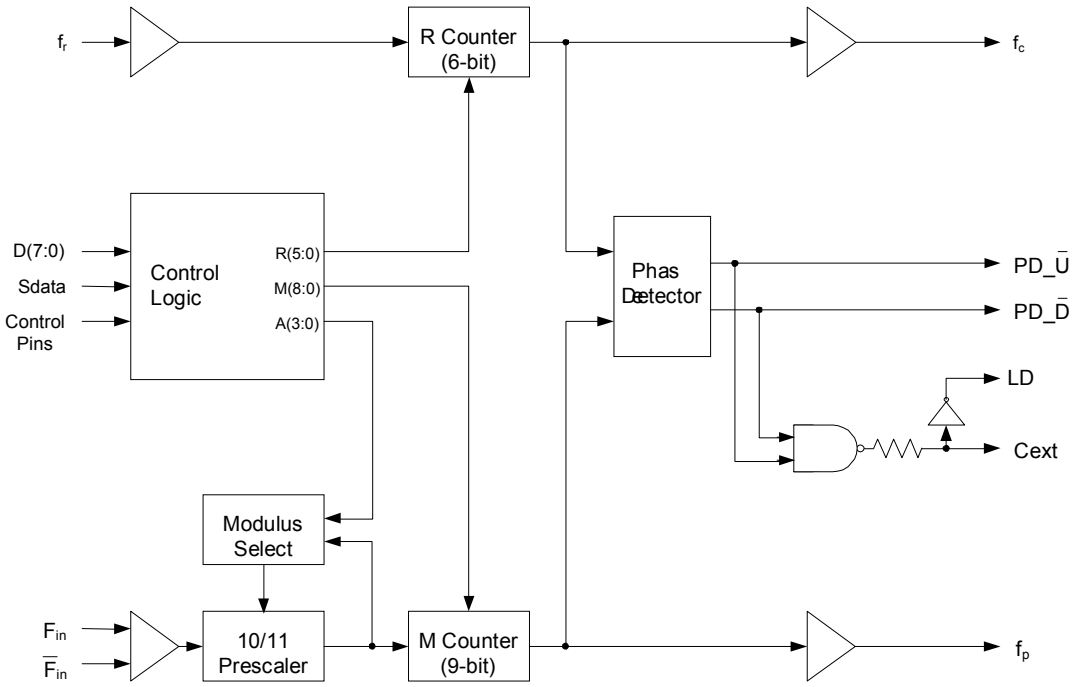
**Note 3:** Parameter is guaranteed through characterization only and is not tested.

*©2003-2005 Peregrine Semiconductor Corp. All rights reserved.*

## Functional Description

The PE3238 consists of a prescaler, counters, a phase detector and control logic. The dual modulus prescaler divides the VCO frequency by either 10 or 11, depending on the value of the modulus select. Counters “R” and “M” divide the reference and prescaler output, respectively, by integer values stored in a 20-bit register. An additional counter (“A”) is used in the modulus select logic. The phase-frequency detector generates up and down frequency control signals. The control logic includes a selectable chip interface. Data can be written via serial bus, parallel bus, or hardwired direct to the pins. There are also various operational and test modes and lock detect.

**Figure 4. Functional Block Diagram**





*©2003-2005 Peregrine Semiconductor Corp. All rights reserved.*

### Main Counter Chain

The main counter chain divides the RF input frequency, $F_{in}$, by an integer derived from the user defined values in the "M" and "A" counters. It is composed of the 10/11 dual modulus prescaler, modulus select logic, and 9 bit M counter. Setting Pre_en "low" enables the 10/11 prescaler. Setting Pre_en "high" allows $F_{in}$ to bypass the prescaler and powers down the prescaler.

The output from the main counter chain, $f_p$, is related to the VCO frequency, $F_{in}$, by the following equation:

$$f_p = F_{in} / [10 \times (M + 1) + A] \quad (1)$$
$$\text{where } A \leq M + 1,\ 1 \leq M \leq 511$$

When the loop is locked, $F_{in}$ is related to the reference frequency, $f_r$, by the following equation:

$$F_{in} = [10 \times (M + 1) + A] \times (f_r / (R+1)) \quad (2)$$
$$\text{where } A \leq M + 1,\ 1 \leq M \leq 511$$

A consequence of the upper limit on A is that Fin must be greater than or equal to 90 x ($f_r$ / (R+1)) to obtain contiguous channels. Programming the M Counter with the minimum value of "1" will result in a minimum M Counter divide ratio of "2".

When the prescaler is bypassed, the equation becomes:

$$F_{in} = (M + 1) \times (f_r / (R+1)) \quad (3)$$
$$\text{where } 1 \leq M \leq 511$$

In Direct Interface Mode, main counter inputs $M_7$ and $M_8$ are internally forced low.

### Reference Counter

The reference counter chain divides the reference frequency, $f_r$, down to the phase detector comparison frequency, $f_c$.

The output frequency of the 6-bit R Counter is related to the reference frequency by the following equation:

$$f_c = f_r / (R + 1) \quad (4)$$
$$\text{where } 0 \leq R \leq 63$$

Note that programming R equal to "0" will pass the reference frequency, $f_r$, directly to the phase detector.

In Direct Interface Mode, R Counter inputs $R_4$ and $R_5$ are internally forced low ("0").

### Register Programming

*Parallel Interface Mode*

Parallel Interface Mode is selected by setting the Bmode input "low" and the Smode input "low".

Parallel input data, D[7:0], are latched in a parallel fashion into one of three, 8-bit primary register sections on the rising edge of M1_WR, M2_WR, or A_WR per the mapping shown in Table 7 on page 9. The contents of the primary register are transferred into a secondary register on the rising edge of Hop_WR according to the timing diagram shown in Figure 5. Data are transferred to the counters as shown in Table 7 on page 9.

The secondary register acts as a buffer to allow rapid changes to the VCO frequency. This double buffering for "ping-pong" counter control is programmed via the FSELP input. When FSELP is "high", the primary register contents set the counter inputs. When FSELP is "low", the secondary register contents are utilized.

Parallel input data, D[7:0], are latched into the enhancement register on the rising edge of E_WR according to the timing diagram shown in Figure 5. This data provides control bits as shown in Table 8 on page 9 with bit functionality enabled by asserting the Enh input "low".

*Serial Interface Mode*

Serial Interface Mode is selected by setting the Bmode input "low" and the Smode input "high".

While the E_WR input is "low" and the S_WR input is "low", serial input data (Sdata input), $B_0$ to $B_{19}$, are clocked serially into the primary register on the rising edge of Sclk, MSB ($B_0$) first. The contents from the primary register are transferred into the secondary register on the rising edge of either S_WR or Hop_WR according to the timing diagram shown in Figures 5-6. Data are transferred to the counters as shown in Table 7 on page 9.

The double buffering provided by the primary and secondary registers allows for "ping-pong" counter control using the FSELS input. When FSELS is "high", the primary register contents set the counter inputs. When FSELS is "low", the secondary register contents are utilized.

While the E_WR input is "high" and the S_WR input is "low", serial input data (Sdata input), $B_0$

©2003-2005 Peregrine Semiconductor Corp. All rights reserved.

to $B_7$, are clocked serially into the enhancement register on the rising edge of Sclk, MSB ($B_0$) first. The enhancement register is double buffered to prevent inadvertent control changes during serial loading, with buffer capture of the serially entered data performed on the falling edge of E_WR according to the timing diagram shown in Figure 5. After the falling edge of E_WR, the data provide control bits as shown in Table 8 with bit functionality enabled by asserting the Enh input "low".

*Direct Interface Mode*

Direct Interface Mode is selected by setting the Bmode input "high".
Counter control bits are set directly at the pins as shown in Table 7. In Direct Interface Mode, main counter inputs $M_7$ and $M_8$, and R Counter inputs $R_4$ and $R_5$ are internally forced low ("0").

**Table 7. Primary Register Programming**

| Interface Mode | $\overline{Enh}$ | $\overline{Bmode}$ | Smode | $R_5$ | $R_4$ | $M_8$ | $M_7$ | $\overline{Pre_en}$ | $M_6$ | $M_5$ | $M_4$ | $M_3$ | $M_2$ | $M_1$ | $M_0$ | $R_3$ | $R_2$ | $R_1$ | $R_0$ | $A_3$ | $A_2$ | $A_1$ | $A_0$ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Parallel | 1 | 0 | 0 | M2_WR rising edge load | | | | M1_WR rising edge load | | | | | | | | A_WR rising edge load | | | | | | | |
| | | | | $D_3$ | $D_2$ | $D_1$ | $D_0$ | $D_7$ | $D_6$ | $D_5$ | $D_4$ | $D_3$ | $D_2$ | $D_1$ | $D_0$ | $D_7$ | $D_6$ | $D_5$ | $D_4$ | $D_3$ | $D_2$ | $D_1$ | $D_0$ |
| Serial* | 1 | 0 | 1 | $B_0$ | $B_1$ | $B_2$ | $B_3$ | $B_4$ | $B_5$ | $B_6$ | $B_7$ | $B_8$ | $B_9$ | $B_{10}$ | $B_{11}$ | $B_{12}$ | $B_{13}$ | $B_{14}$ | $B_{15}$ | $B_{16}$ | $B_{17}$ | $B_{18}$ | $B_{19}$ |
| Direct | 1 | 1 | X | 0 | 0 | 0 | 0 | $\overline{Pre_en}$ | $M_6$ | $M_5$ | $M_4$ | $M_3$ | $M_2$ | $M_1$ | $M_0$ | $R_3$ | $R_2$ | $R_1$ | $R_0$ | $A_3$ | $A_2$ | $A_1$ | $A_0$ |

*Serial data clocked serially on Sclk rising edge while E_WR "low" and captured in secondary register on S_WR rising edge.

MSB (first in) ... (last in) LSB

**Table 8. Enhancement Register Programming**

| Interface Mode | $\overline{Enh}$ | $\overline{Bmode}$ | Smode | Reserved | Reserved | Reserved | Power down | Counter load | MSEL output | Prescaler output | $f_c$, $f_p$ OE |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Parallel | 0 | X | 0 | E_WR rising edge load | | | | | | | |
| | | | | $D_7$ | $D_6$ | $D_5$ | $D_4$ | $D_3$ | $D_2$ | $D_1$ | $D_0$ |
| Serial* | 0 | X | 1 | $B_0$ | $B_1$ | $B_2$ | $B_3$ | $B_4$ | $B_5$ | $B_6$ | $B_7$ |

*Serial data clocked serially on Sclk rising edge while E_WR "high" and captured in the double buffer on E_WR falling edge.

MSB (first in) ... (last in) LSB


©2003-2005 Peregrine Semiconductor Corp. All rights reserved.

**Figure 5. Parallel Interface Mode Timing Diagram**

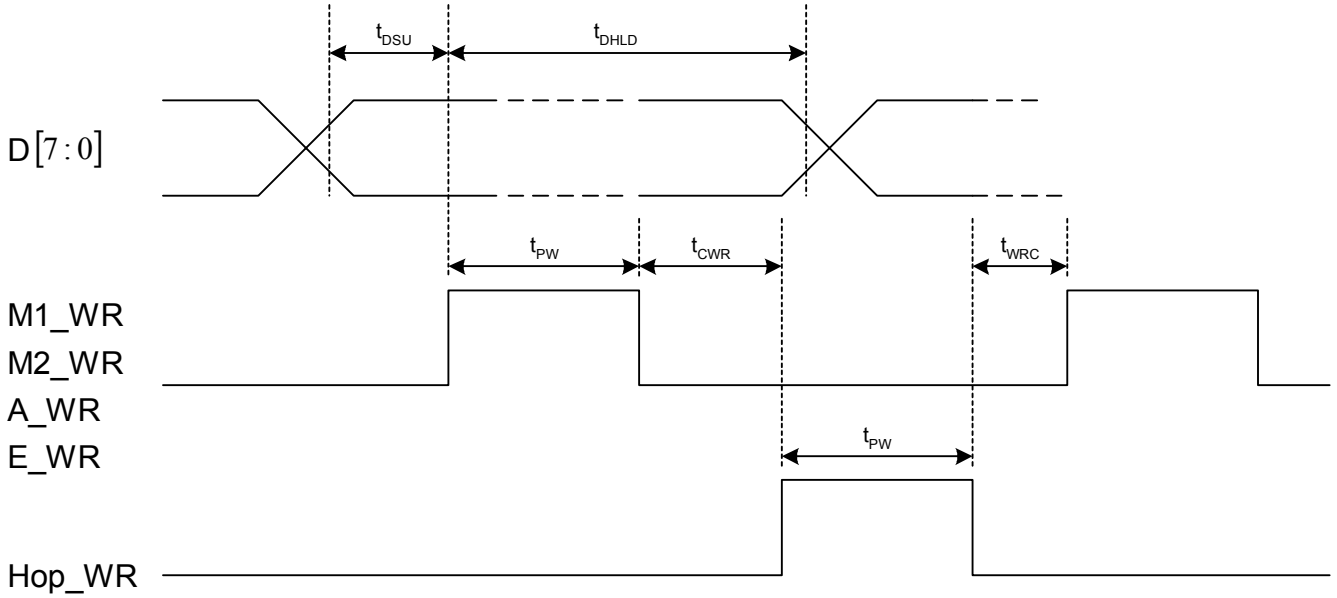
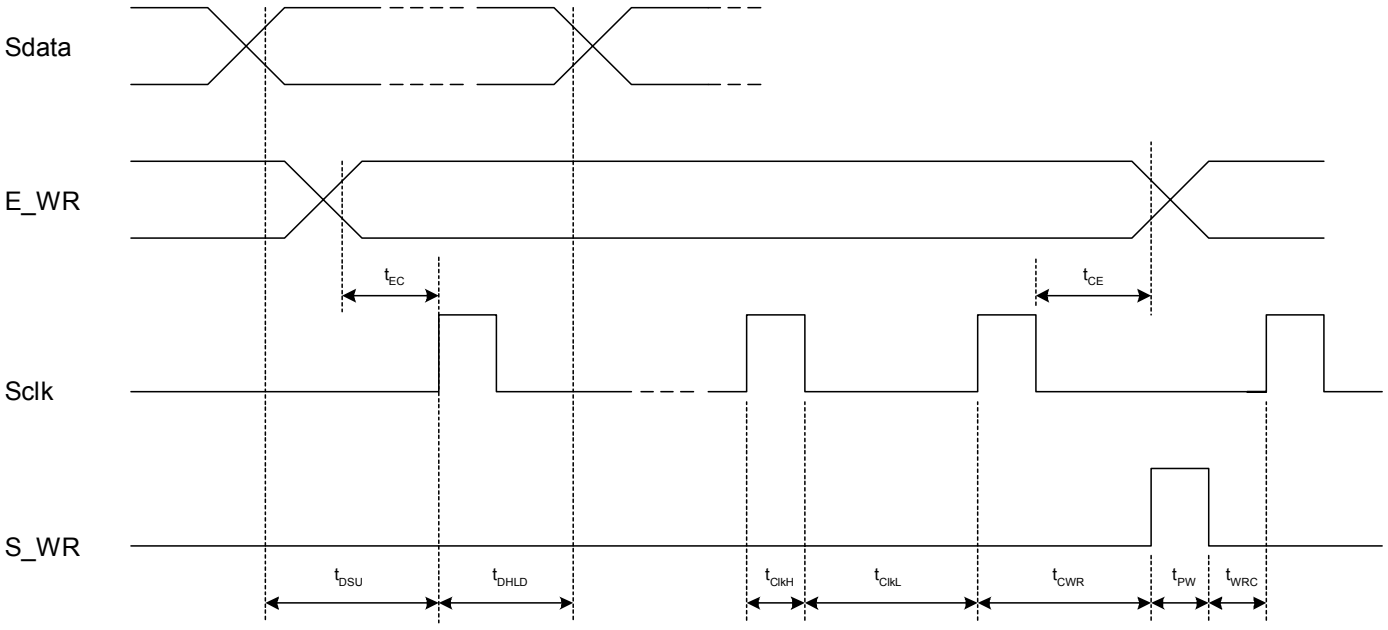



**Figure 6. Serial Interface Mode Timing Diagram**




©2003-2005 Peregrine Semiconductor Corp. All rights reserved.

### Enhancement Register

The functions of the enhancement register bits are shown below in Table 9 with all bits active “high”.

**Table 9. Enhancement Register Bit Functionality**

| Bit Function | | Description |
|---|---|---|
| Bit 0 | Reserved** | |
| Bit 1 | Reserved** | |
| Bit 2 | Reserved** | |
| Bit 3 | Power down | Power down of all functions except programming interface. |
| Bit 4 | Counter load | Immediate and continuous load of counter programming as directed by the $\overline{\text{Bmode}}$ and Smode inputs. |
| Bit 5 | MSEL output | Drives the internal dual modulus prescaler modulus select (MSEL) onto the Dout output. |
| Bit 6 | Prescaler output | Drives the raw internal prescaler output onto the Dout output. |
| Bit 7 | $f_p$, $f_c$ OE | $f_p$, $f_c$ outputs disabled. |

** Program to 0

### Phase Detector

The phase detector is triggered by rising edges from the main Counter ($f_p$) and the reference counter ($f_c$). It has two outputs, namely PD_U, and PD_D. If the divided VCO leads the divided reference in phase or frequency ($f_p$ leads $f_c$), PD_D pulses “low”. If the divided reference leads the divided VCO in phase or frequency ($f_c$ leads $f_p$), PD_D pulses “low”. The width of either pulse is directly proportional to phase offset between the two input signals, $f_p$ and $f_c$.

PD_U and PD_D drive an active loop filter which controls the VCO tune voltage. PD_U pulses result in an increase in VCO frequency and PD_D results in a decrease in VCO frequency.

A lock detect output, LD is also provided, via the pin Cext. Cext is the logical “NAND” of PD_U and PD_D waveforms, which is driven through a series 2 kΩ resistor. Connecting Cext to an external shunt capacitor provides integration. Cext also drives the input of an internal inverting comparator with an open drain output. Thus LD is an “AND” function of PD_U and PD_D.


*©2003-2005 Peregrine Semiconductor Corp. All rights reserved.*

**Figure 7. PE3238 Typical Phase Noise vs. Offset (VDD = 3.0 V, Temp = 25° C)**

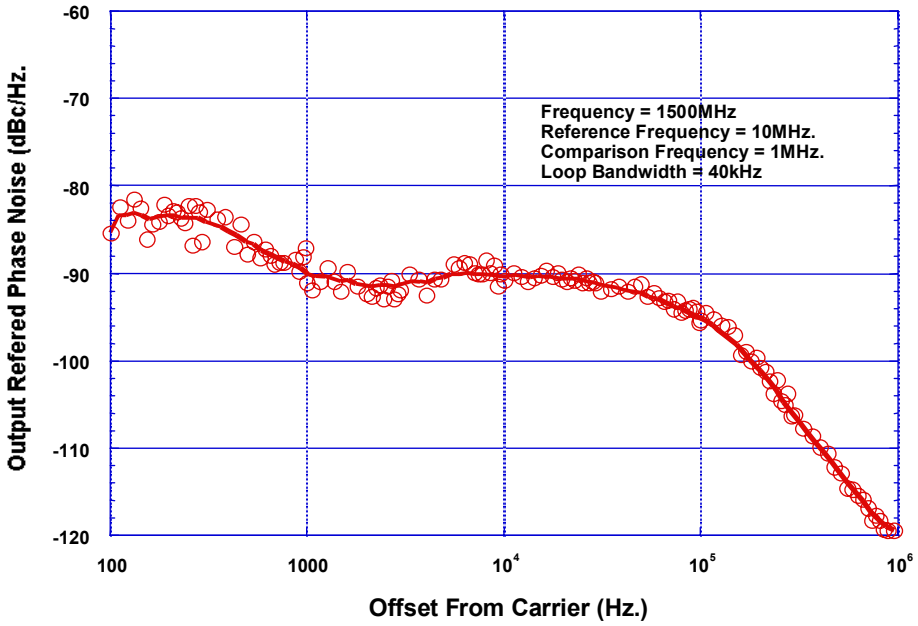
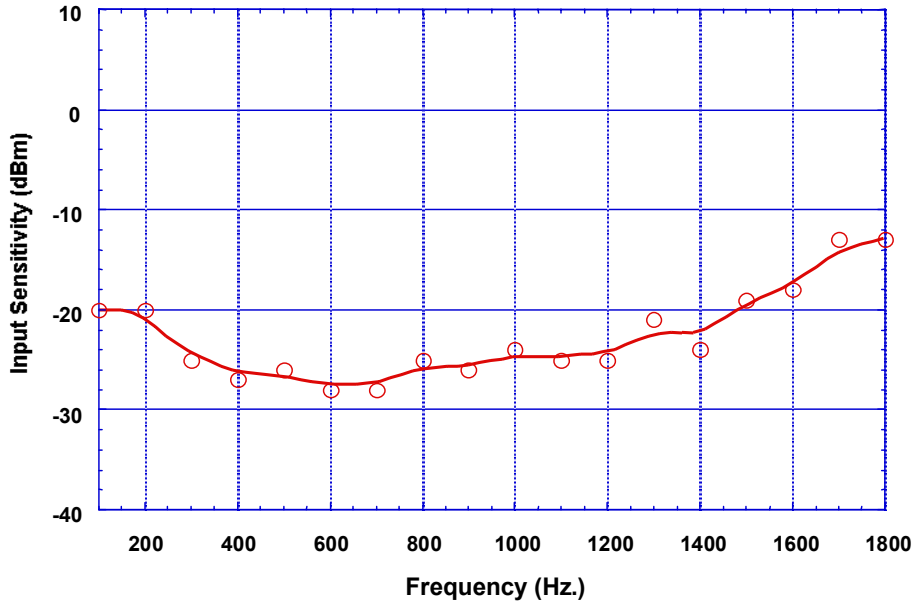



**Figure 8. PE3238 Typical Input Sensitivity vs. Frequency ($V_{DD}$ = 3.0 V, Temp = 25° C)**




©2003-2005 Peregrine Semiconductor Corp. All rights reserved.

## Handling Requirements

All surface mount products which do not meet Level 1 moisture sensitivity requirements are processed through dry bake and pack procedure. The necessary data is recorded on the caution label of each shipment. The 44-lead PLCC package is moisture sensitivity Level 3.

### Level 3 Caution Label

The caution label should contain the following information for Level 3 devices:

1. Calculated shelf life in sealed bag: 12 months at <40 °C and <90% relative humidity (RH)
2. Peak package body temperature is 225 °C.
3. After bag is opened, devices that will be subjected to reflow solder or other high temperature process must
   a) Be mounted within 168 hours of factory conditions <30 °C/60% RH, **or**
   b) Be stored at <10% RH
4. Devices require bake, before mounting, if:
   a) Humidity Indicator Card is > 10% when read at 23 ± 5 °C
   b) 3a or 3b are not met
5. If baking is required, devices may be baked for 48 hours at 125 +5/-0 °C

Note: If device containers cannot be subjected to high temperature or shorter bake times are desired, reference IPC/JEDEC-J-STD-033 for bake procedure.

Level and Body temperature defined by: IPC/JEDEC-J-STD-020

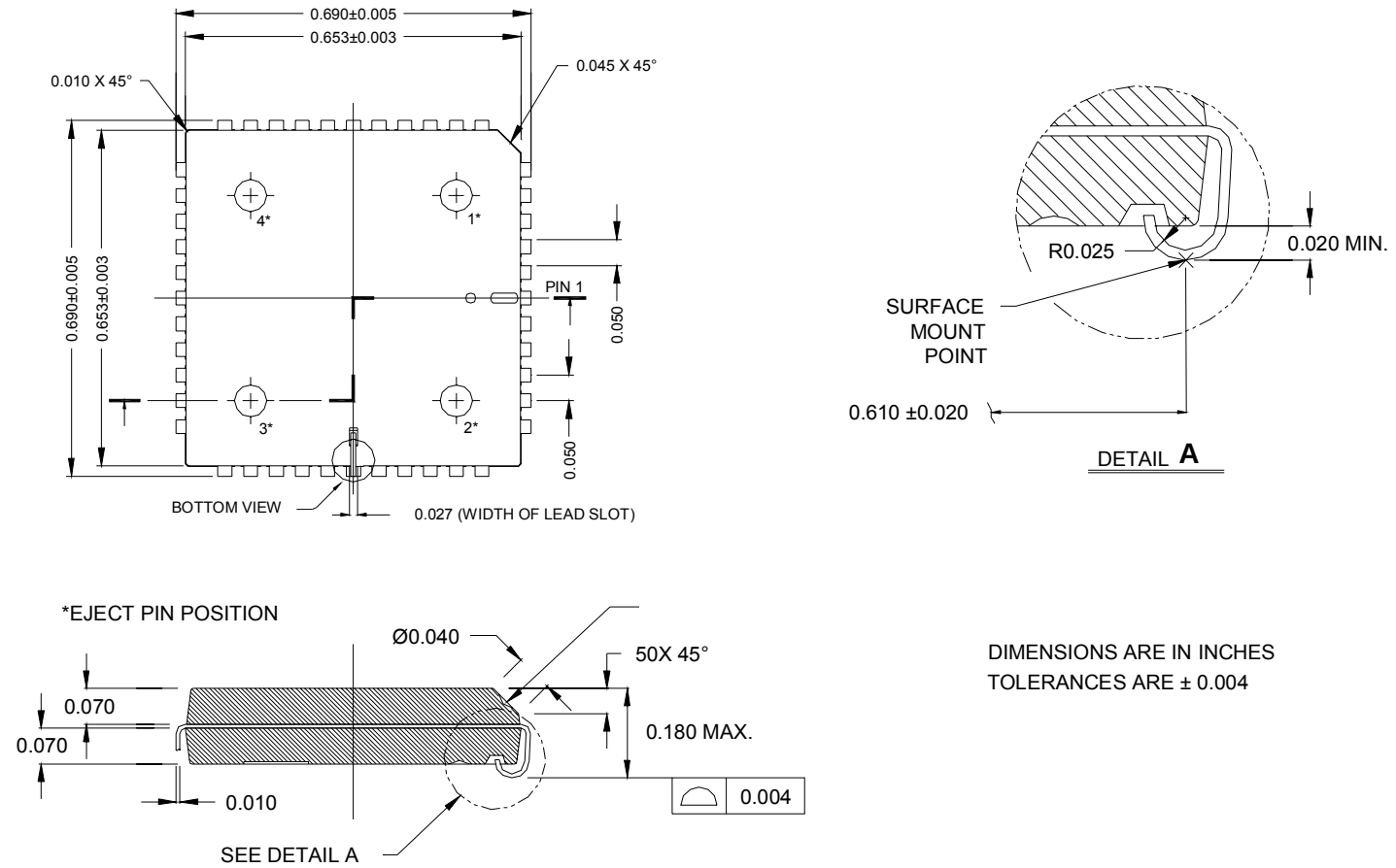
For Dry Bake Procedures, see: IPC/JEDEC-J-STD-033

Operator must observe ESD precautions per ESD Control Procedure and Parts Handling and shipping Procedure.


*©2003-2005 Peregrine Semiconductor Corp. All rights reserved.*

## Figure 9. Package Drawing

44-lead PLCC




## Table 10. Ordering Information

| Order Code | Part Marking | Description | Package | Shipping Method |
|---|---|---|---|---|
| 3238-21 | PE3238 | PE3238-44PLCC-27A | 44-lead PLCC | 27 units / Tube |
| 3238-22 | PE3238 | PE3238-44PLCC-500C | 44-lead PLCC | 500 units / T&R |
| 3238-00 | PE3238EK | PE3238-44PLCC-EVAL KIT | 44-lead PLCC | 1 / Box |

©2003-2005 Peregrine Semiconductor Corp. All rights reserved.

## Sales Offices

### *The Americas*

**Peregrine Semiconductor Corporation**
9450 Carroll Park Drive
San Diego, CA 92121
Tel: 858-731-9400
Fax: 858-731-9499

### *Europe*

**Peregrine Semiconductor Europe**
Bâtiment Maine
13-15 rue des Quatre Vents
F-92380 Garches, France
Tel: +33-1-47-41-91-73
Fax : +33-1-47-41-91-73

**Space and Defense Products**

***Americas:***

Tel: 858-731-9453

***Europe, Asia Pacific:***

180 Rue Jean de Guiramand
13852 Aix-En-Provence Cedex 3, France
Tel: +33(0) 4 4239 3361
Fax: +33(0) 4 4239 7227

### *North Asia Pacific*

**Peregrine Semiconductor K.K.**
Teikoku Hotel Tower 10B-6
1-1-1 Uchisaiwai-cho, Chiyoda-ku
Tokyo 100-0011 Japan
Tel: +81-3-3502-5211
Fax: +81-3-3502-5213

**Peregrine Semiconductor, Korea**
#B-2402, Kolon Tripolis, #210
Geumgok-dong, Bundang-gu, Seongnam-si
Gyeonggi-do, 463-480 S. Korea
Tel: +82-31-728-4300
Fax: +82-31-728-4305

### *South Asia Pacific*

**Peregrine Semiconductor, China**
Shanghai, 200040, P.R. China
Tel: +86-21-5836-8276
Fax: +86-21-5836-7652

For a list of representatives in your area, please refer to our Web site at: ***www.psemi.com***

## Data Sheet Identification

### *Advance Information*

The product is in a formative or design stage. The data sheet contains design target specifications for product development. Specifications and features may change in any manner without notice.

### *Preliminary Specification*

The data sheet contains preliminary data. Additional data may be added at a later date. Peregrine reserves the right to change specifications at any time without notice in order to supply the best possible product.

### *Product Specification*

The data sheet contains final data. In the event Peregrine decides to change the specifications, Peregrine will notify customers of the intended changes by issuing a DCN (Document Change Notice).

The information in this data sheet is believed to be reliable. However, Peregrine assumes no liability for the use of this information. Use shall be entirely at the user's own risk.

No patent rights or licenses to any circuits described in this data sheet are implied or granted to any third party.

Peregrine's products are not designed or intended for use in devices or systems intended for surgical implant, or in other applications intended to support or sustain life, or in any application in which the failure of the Peregrine product could create a situation in which personal injury or death might occur. Peregrine assumes no liability for damages, including consequential or incidental damages, arising out of the use of its products in such applications.

The Peregrine name, logo, and UTSi are registered trademarks and UltraCMOS and HaRP are trademarks of Peregrine Semiconductor Corp.


*©2003-2005 Peregrine Semiconductor Corp. All rights reserved.*

TradeElectronics.ru

гарантия бесперебойности производства и качества выпускаемой продукции

## О компании

ООО "ТрейдЭлектроникс" - это оперативные поставки широкого спектра электронных компонентов отечественного и импортного производства напрямую от производителей и с крупнейших мировых складов. Реализуемая нашей компанией продукция насчитывает более полумиллиона наименований.

Благодаря этому наша компания предлагает к поставке практически не ограниченный ассортимент компонентов как оптовыми, мелкооптовыми партиями, так и в розницу.

Наличие собственной эффективной системы логистики обеспечивает надежную поставку продукции по конкурентным ценам в точно указанные сроки.

Срок поставки со стоков в **Европе и Америке – от 3 до 14 дней.**

Срок поставки из **Азии – от 10 дней.**

Благодаря развитой сети поставщиков, помогаем в поиске и приобретении экзотичных или снятых с производства компонентов.

Предоставляем спец цены на элементы для создания инженерных сэмплов.

**Упорный труд, качественный результат дают нам право быть уверенными в себе и надежными для наших клиентов.**

## Наша компания это:

- Гарантия качества поставляемой продукции
- Широкий ассортимент
- Минимальные сроки поставок
- Техническая поддержка
- Подбор комплектации
- Индивидуальный подход
- Гибкое ценообразование

Наша организация особенно сильна в поставках модулей, микросхем, пассивных компонентов, ксайленсах (XC), EPF, EPM и силовой электроники.

Большой выбор предлагаемой продукции, различные виды оплаты и доставки, позволят Вам сэкономить время и получить максимум выгоды от сотрудничества с нами!

Trade Electronics.ru

гарантия бесперебойности производства и качества выпускаемой продукции

## Перечень производителей, продукцию которых мы поставляем на российский рынок



Trade Electronics.ru

гарантия бесперебойности производства и качества выпускаемой продукции

С удовольствием будем прорабатывать для Вас поставки всех необходимых компонентов по текущим запросам для скорейшего выявления групп элементов, по которым сотрудничество именно с нашей компанией будет для Вас максимально выгодным!

С уважением,

Менеджер отдела продаж ООО

«Трейд Электроникс»

Шишлаков Евгений

8 (495)668-30-28 доб 169

manager28@tradeelectronics.ru

http://www.tradeelectronics.ru/