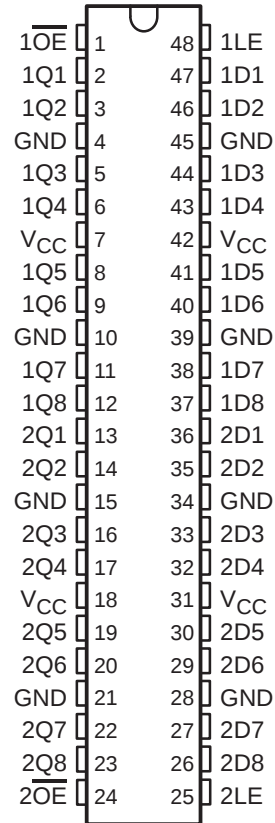


SN54ABT16373, SN74ABT16373 16-BIT TRANSPARENT D-TYPE LATCHES WITH 3-STATE OUTPUTS

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- Members of the Texas Instruments **Widebus™** Family
- State-of-the-Art **EPIC-II B™** BiCMOS Design Significantly Reduces Power Dissipation
- ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17
- Typical V_{OLP} (Output Ground Bounce) < 0.8 V at $V_{CC} = 5$ V, $T_A = 25^\circ\text{C}$
- Distributed V_{CC} and GND Pin Configuration Minimizes High-Speed Switching Noise
- Flow-Through Architecture Optimizes PCB Layout
- High-Drive Outputs (–32-mA I_{OH} , 64-mA I_{OL})
- Packaged in Plastic 300-mil Shrink Small-Outline Packages and 380-mil Fine-Pitch Ceramic Flat Packages Using 25-mil Center-to-Center Spacings

SN54ABT16373 . . . WD PACKAGE
SN74ABT16373 . . . DL PACKAGE
(TOP VIEW)



description

The 4ABT16373 is a 16-bit transparent D-type latch with 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. It is particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The device can be used as two 8-bit latches or one 16-bit latch. When the latch-enable (LE) input is high, the Q outputs follow the data (D) inputs. When LE is taken low, the Q outputs are latched at the levels set up at the D inputs.

A buffered output-enable ($\overline{OE}$) input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and the increased drive provide the capability to drive bus lines without need for interface or pullup components.

The output enable ($\overline{OE}$) does not affect internal operations of the latch. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN74ABT16373 is available in TI's shrink small-outline package (DL), which provides twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The SN54ABT16373 is characterized for operation over the full military temperature range of -55°C to 125°C . The SN74ABT16373 is characterized for operation from -40°C to 85°C .

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INPUTS			OUTPUT Q
OE	LE	D	
L	H	H	H
L	H	L	L
L	L	X	Q ₀
H	X	X	Z

$\overline{1OE}$	1	1EN C3 2EN C4		
	48			
$\overline{2OE}$	24			
2LE	25			
1D1	47	3D	1 ▽	2
1D2	46			3
1D3	44			5
1D4	43			6
1D5	41			8
1D6	40			9
1D7	38			11
1D8	37			12
2D1	36	4D	2 ▽	13
2D2	35			14
2D3	33			16
2D4	32			17
2D5	30			19
2D6	29			20
2D7	27			22
2D8	26			23

2

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V_{CC}	–0.5 V to 7 V
Input voltage range, V_I (see Note 1)	–0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, V_O	–0.5 V to 5.5 V
Current into any output in the low state, I_O : SN54ABT16373	96 mA
SN74ABT16373	128 mA
Input clamp current, I_{IK} ($V_I < 0$)	–18 mA
Output clamp current, I_{OK} ($V_O < 0$)	–50 mA
Maximum power dissipation at $T_A = 55^\circ\text{C}$ (in still air)	0.85 W
Storage temperature range	–65°C to 150°C

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

recommended operating conditions (see Note 2)

		SN54ABT16373		SN74ABT16373		UNIT
		MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage	4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage	2		2		V
V_{IL}	Low-level input voltage		0.8		0.8	V
V_I	Input voltage	0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current		–24		–32	mA
I_{OL}	Low-level output current		48		64	mA
$\Delta t / \Delta v$	Input transition rise or fall rate	Outputs enabled			10	ns/V
T_A	Operating free-air temperature	–55	125	–40	85	°C

NOTE 2: Unused or floating inputs must be held high or low.

SN54ABT16373, SN74ABT16373

16-BIT TRANSPARENT D-TYPE LATCHES

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		T _A = 25°C			SN54ABT16373		SN74ABT16373		UNIT
			MIN	TYP†	MAX	MIN	MAX	MIN	MAX	
V _{IK}	V _{CC} = 4.5 V, I _I = −18 mA		−1.2			−1.2		−1.2		V
V _{OH}	V _{CC} = 4.5 V, I _{OH} = − 3 mA		2.5			2.5		2.5		V
	V _{CC} = 5 V, I _{OH} = − 3 mA		3			3		3		
	V _{CC} = 4.5 V, I _{OH} = −24 mA		2			2				
	V _{CC} = 4.5 V, I _{OH} = − 32 mA		2‡					2		
V _{OL}	V _{CC} = 4.5 V, I _{OL} = 48 mA		0.55			0.55				V
	V _{CC} = 4.5 V, I _{OL} = 64 mA		0.55‡					0.55		
I _I	V _{CC} = 5.5 V, V _I = V _{CC} or GND		±1			±1		±1		μA
I _{OZH}	V _{CC} = 5.5 V, V _O = 2.7 V		50			50		50		μA
I _{OZL}	V _{CC} = 5.5 V, V _O = 0.5 V		−50			−50		−50		μA
I _{off}	V _{CC} = 0, V _I or V _O ≤ 4.5 V		±100					±100		μA
I _{CEX}	V _{CC} = 5.5 V, V _O = 5.5 V	Outputs high	50			50		50		μA
I _O [§]	V _{CC} = 5.5 V, V _O = 2.5 V		−50	−100	−180	−50	−180	−50	−180	mA
I _{CC}	V _{CC} = 5.5 V, I _O = 0, V _I = V _{CC} or GND	Outputs high	2			2		2		mA
		Outputs low	85			85		85		
		Outputs disabled	2			2		2		
ΔI _{CC}	V _{CC} = 5.5 V, One input at 3.4 V, Other inputs at V _{CC} or GND		1.5			1.5		1.5		mA
C _i	V _I = 2.5 V or 0.5 V		3.5							pF
C _O	V _O = 2.5 V or 0.5 V		9.5							pF

† All typical values are at $V_{CC} = 5\text{ V}$.

‡ On products compliant to MIL-STD-883, Class B, this parameter does not apply.

§ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

¶ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

		$V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$		SN54ABT16373		SN74ABT16373		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_w	Pulse duration, LE high	3.3		3.3		3.3		ns
t_{su}	Setup time, data before LE↓	1.5		1.5		1.5		ns
t_h	Hold time, data after LE↓	1		1		1		ns

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switching characteristics over recommended ranges of supply voltage and operating free-air temperature, $C_L = 50$ pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 5$ V, $T_A = 25^\circ\text{C}$			SN54ABT16373		SN74ABT16373		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	D	Q	1.9	4.1	5.3	1.9	6.5	1.9	6.3	ns
t_{PHL}			2.3	4.3	5.4	2.3	6.5	2.3	6.2	
t_{PLH}	LE	Q	2.1	4.5	5.7	2.1	7	2.1	6.7	ns
t_{PHL}			2.6	4.5	5.6	2.6	6.3	2.6	6.1	
t_{PZH}	$\overline{OE}$	Q	1.5	3.9	5	1.5	6.4	1.5	6.1	ns
t_{PZL}			1.8	3.8	4.9	1.8	5.8	1.8	5.6	
t_{PHZ}	$\overline{OE}$	Q	2.4	6.5	8.8	2.4	10.8	2.4	10.3	ns
t_{PLZ}			2.3	5.3	7.6	2.3	8.7	2.3	8.1	

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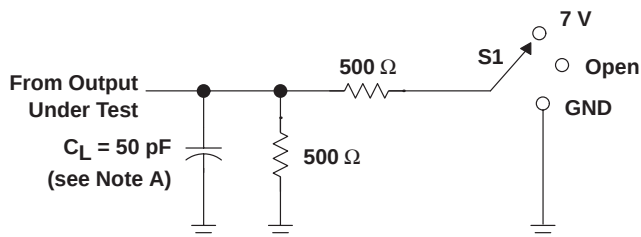
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16-BIT TRANSPARENT D-TYPE LATCHES

WITH 3-STATE OUTPUTS

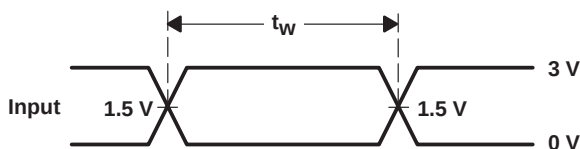
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PARAMETER MEASUREMENT INFORMATION

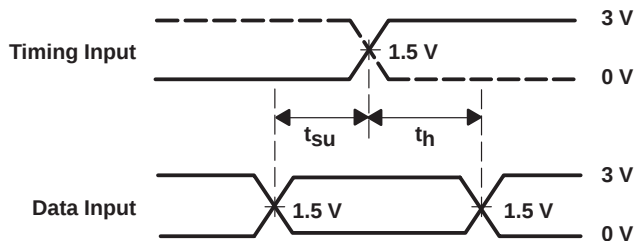


LOAD CIRCUIT FOR OUTPUTS

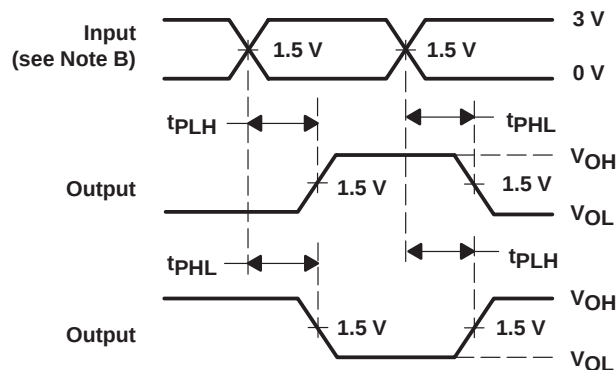
TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open



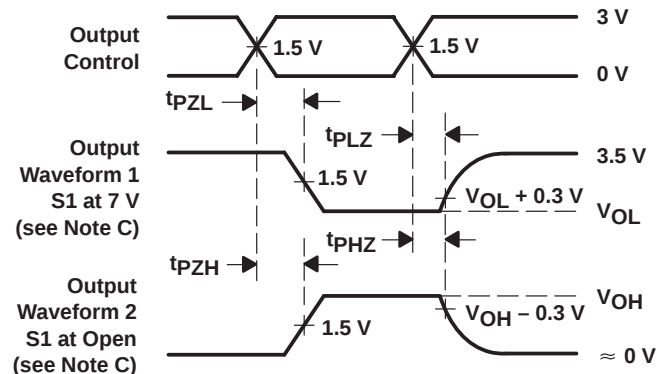
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

- NOTES: A. C_L includes probe and jig capacitance.
- B. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2.5 \text{ ns}$, $t_f \leq 2.5 \text{ ns}$.
- C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
SN74ABT16373DGGR	OBSOLETE	TSSOP	DGG	48		TBD	Call TI	Call TI
SN74ABT16373DL	OBSOLETE	SSOP	DL	48		TBD	Call TI	Call TI
SN74ABT16373DLR	OBSOLETE	SSOP	DL	48		TBD	Call TI	Call TI

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS) or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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