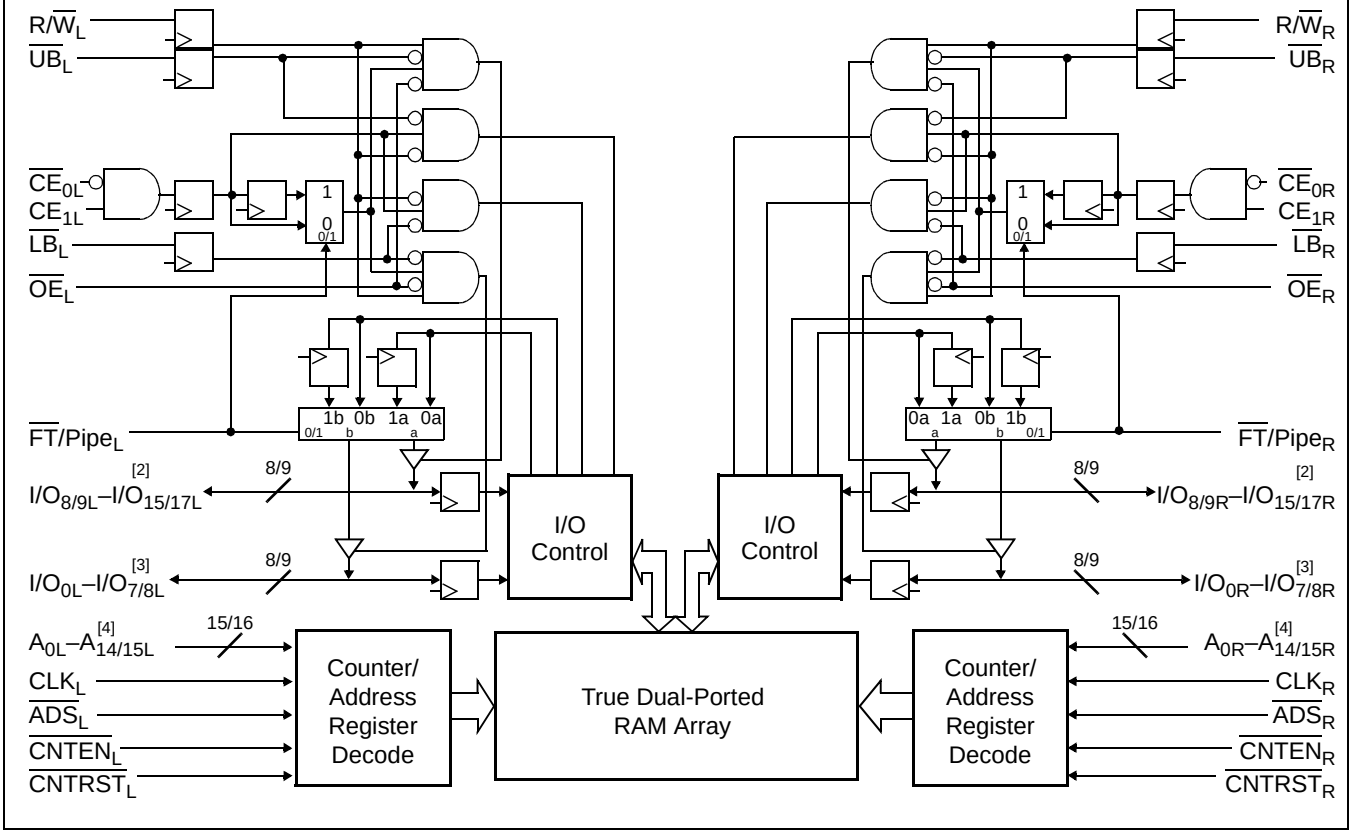
# CY7C09279/89
# CY7C09379/89

## 32K/64K x16/18
## Synchronous Dual Port Static RAM

### Features

- True dual-ported memory cells which allow simultaneous access of the same memory location
- Six Flow-Through/Pipelined devices
  - 32K x 16/18 organization (CY7C09279/379)
  - 64K x 16/18 organization (CY7C09289/389)
- Three Modes
  - Flow-Through
  - Pipelined
  - Burst
- Pipelined output mode on both ports allows fast 100-MHz cycle time
- 0.35-micron CMOS for optimum speed/power
- High-speed clock to data access 6.5[1]/7.5/9/12 ns (max.)
- Low operating power
  - Active = 195 mA (typical)
  - Standby = 0.05 mA (typical)
- Fully synchronous interface for easier operation
- Burst counters increment addresses internally
  - Shorten cycle times
  - Minimize bus noise
  - Supported in Flow-Through and Pipelined modes
- Dual Chip Enables for easy depth expansion
- Upper and Lower Byte Controls for Bus Matching
- Automatic power-down
- Commercial and Industrial temperature ranges
- Available in 100-pin TQFP
- Pin-compatible and functionally equivalent to IDT70927 and IDT709279

### Logic Block Diagram




**Notes:**
1. See page 6 for Load Conditions.
2. $I/O_8$–$I/O_{15}$ for x16 devices; $I/O_9$–$I/O_{17}$ for x18 devices.
3. $I/O_0$–$I/O_7$ for x16 devices. $I/O_0$–$I/O_8$ for x18 devices.
4. $A_0$–$A_{14}$ for 32K; $A_0$–$A_{15}$ for 64K devices.

## Functional Description

The CY7C09279/89 and CY7C09379/89 are high-speed synchronous CMOS 32K, and 64K x 16/18 dual-port static RAMs. Two ports are provided, permitting independent, simultaneous access for reads and writes to any location in memory.[5] Registers on control, address, and data lines allow for minimal set-up and hold times. In pipelined output mode, data is registered for decreased cycle time. Clock to data valid $t_{CD2}$ = 6.5 ns[1] (pipelined). Flow-through mode can also be used to bypass the pipelined output register to eliminate access latency. In flow-through mode data will be available $t_{CD1}$ = 15 ns after the address is clocked into the device. Pipelined output or flow-through mode is selected via the $\overline{FT}$/PIPE pin.

Each port contains a burst counter on the input address register. The internal write pulse width is independent of the LOW-to-HIGH transition of the clock signal. The internal write pulse is self-timed to allow the shortest possible cycle times.

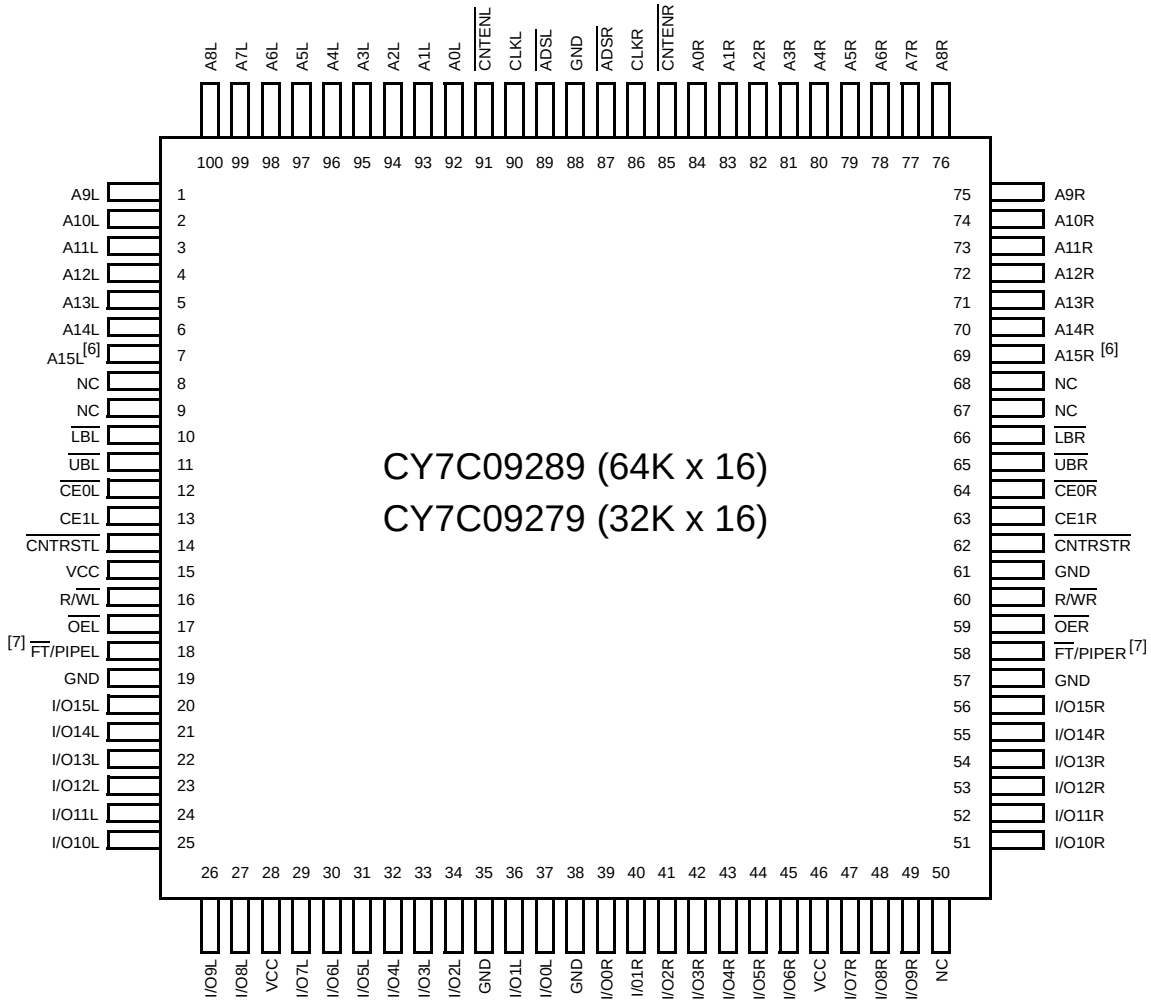
A HIGH on $\overline{CE}_0$ or LOW on $CE_1$ for one clock cycle will power down the internal circuitry to reduce the static power consumption. The use of multiple Chip Enables allows easier banking of multiple chips for depth expansion configurations. In the pipelined mode, one cycle is required with $\overline{CE}_0$ LOW and $CE_1$ HIGH to reactivate the outputs.

Counter enable inputs are provided to stall the operation of the address input and utilize the internal address generated by the internal counter for fast interleaved memory applications. A port's burst counter is loaded with the port's Address Strobe ($\overline{ADS}$). When the port's Count Enable ($\overline{CNTEN}$) is asserted, the address counter will increment on each LOW-to-HIGH transition of that port's clock signal. This will read/write one word from/into each successive address location until $\overline{CNTEN}$ is deasserted. The counter can address the entire memory array and will loop back to the start. Counter Reset ($\overline{CNTRST}$) is used to reset the burst counter.

All parts are available in 100-pin Thin Quad Plastic Flatpack (TQFP) packages.

## Pin Configurations

**100-Pin TQFP (Top View)**

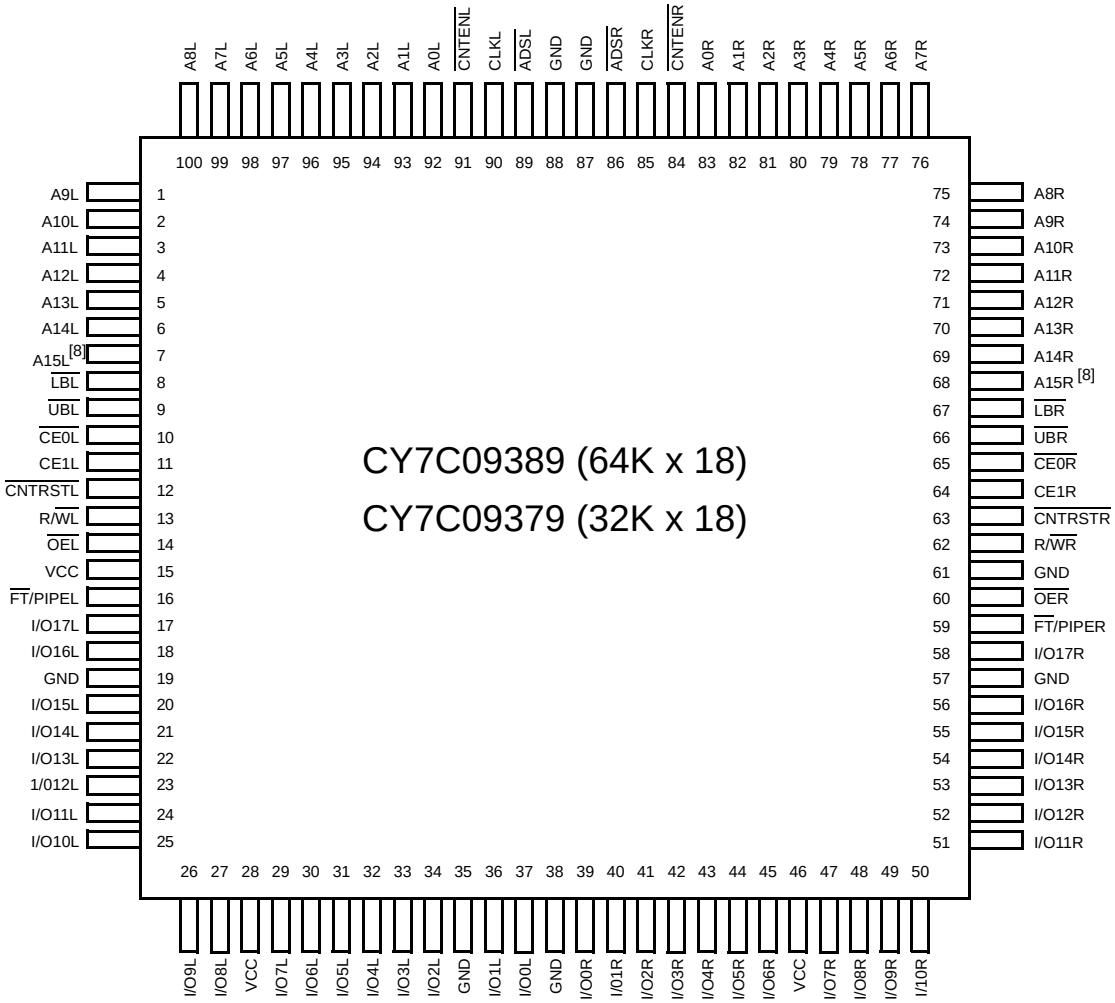



**Notes:**

5. When writing simultaneously to the same location, the final value cannot be guaranteed.
6. This pin is NC for CY7C09279.
7. For CY7C09279, pin #18 connected to $V_{CC}$ is equivalent to an IDT x16 pipelined device; connecting pin #18 and #58 to GND is equivalent to an IDT x16 flow-through device.

## Pin Configurations (continued)

**100-Pin TQFP (Top View)**




## Selection Guide

| | CY7C09279/89 CY7C09379/89 -6[1] | CY7C09279/89 CY7C09379/89 -7 | CY7C09279/89 CY7C09379/89 -9 | CY7C09279/89 CY7C09379/89 -12 |
|---|---|---|---|---|
| $f_{MAX2}$ (MHz) (Pipelined) | 100 | 83 | 67 | 50 |
| Max Access Time (ns) (Clock to Data, Pipelined) | 6.5 | 7.5 | 9 | 12 |
| Typical Operating Current $I_{CC}$ (mA) | 250 | 235 | 215 | 195 |
| Typical Standby Current for $I_{SB1}$ (mA) (Both Ports TTL Level) | 45 | 40 | 35 | 30 |
| Typical Standby Current for $I_{SB3}$ (mA) (Both Ports CMOS Level) | 0.05 | 0.05 | 0.05 | 0.05 |

**Note:**
8. This pin is NC for CY7C09379.

## Pin Definitions

| Left Port | Right Port | Description |
|---|---|---|
| $A_{0L}$–$A_{15L}$ | $A_{0R}$–$A_{15R}$ | Address Inputs ($A_0$–$A_{14}$ for 32K, $A_0$–$A_{15}$ for 64K devices). |
| $\overline{ADS}_L$ | $\overline{ADS}_R$ | Address Strobe Input. Used as an address qualifier. This signal should be asserted LOW to access the part using an externally supplied address. Asserting this signal LOW also loads the burst counter with the address present on the address pins. |
| $\overline{CE}_{0L}$,$CE_{1L}$ | $\overline{CE}_{0R}$,$CE_{1R}$ | Chip Enable Input. To select either the left or right port, both $\overline{CE}_0$ AND $CE_1$ must be asserted to their active states ($\overline{CE}_0 \le V_{IL}$ and $CE_1 \ge V_{IH}$). |
| $CLK_L$ | $CLK_R$ | Clock Signal. This input can be free running or strobed. Maximum clock input rate is $f_{MAX}$. |
| $\overline{CNTEN}_L$ | $\overline{CNTEN}_R$ | Counter Enable Input. Asserting this signal LOW increments the burst address counter of its respective port on each rising edge of CLK. $\overline{CNTEN}$ is disabled if $\overline{ADS}$ or $\overline{CNTRST}$ are asserted LOW. |
| $\overline{CNTRST}_L$ | $\overline{CNTRST}_R$ | Counter Reset Input. Asserting this signal LOW resets the burst address counter of its respective port to zero. $\overline{CNTRST}$ is not disabled by asserting $\overline{ADS}$ or $\overline{CNTEN}$. |
| $I/O_{0L}$–$I/O_{17L}$ | $I/O_{0R}$–$I/O_{17R}$ | Data Bus Input/Output ($I/O_0$–$I/O_{15}$ for x16 devices). |
| $\overline{LB}_L$ | $\overline{LB}_R$ | Lower Byte Select Input. Asserting this signal LOW enables read and write operations to the lower byte. ($I/O_0$–$I/O_8$ for x18, $I/O_0$–$I/O_7$ for x16) of the memory array. For read operations both the $\overline{LB}$ and $\overline{OE}$ signals must be asserted to drive output data on the lower byte of the data pins. |
| $\overline{UB}_L$ | $\overline{UB}_R$ | Upper Byte Select Input. Same function as $\overline{LB}$, but to the upper byte ($I/O_{8/9L}$–$I/O_{15/17L}$). |
| $\overline{OE}_L$ | $\overline{OE}_R$ | Output Enable Input. This signal must be asserted LOW to enable the I/O data pins during read operations. |
| $R/\overline{W}_L$ | $R/\overline{W}_R$ | Read/Write Enable Input. This signal is asserted LOW to write to the dual port memory array. For read operations, assert this pin HIGH. |
| $\overline{FT}/PIPE_L$ | $\overline{FT}/PIPE_R$ | Flow-Through/Pipelined Select Input. For flow-through mode operation, assert this pin LOW. For pipelined mode operation, assert this pin HIGH. |
| GND | | Ground Input. |
| NC | | No Connect. |
| $V_{CC}$ | | Power Input. |

## Maximum Ratings[9]

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... –65°C to +150°C

Ambient Temperature with Power Applied..–55°C to +125°C

Supply Voltage to Ground Potential..... –0.3V to +7.0V

DC Voltage Applied to
Outputs in High Z State..... –0.5V to +7.0V

DC Input Voltage..... –0.5V to +7.0V

Output Current into Outputs (LOW)..... 20 mA

Static Discharge Voltage..... >1100V

Latch-Up Current..... >200 mA

## Operating Range

| Range | Ambient Temperature | $V_{CC}$ |
|---|---|---|
| Commercial | 0°C to +70°C | 5V ± 10% |
| Industrial[10] | –40°C to +85°C | 5V ± 10% |

**Note:**
9. The Voltage on any input or I/O pin cannot exceed the power pin during power-up.
10. Industrial parts are available in CY7C09289 and Cy7C09389 only

## Electrical Characteristics Over the Operating Range

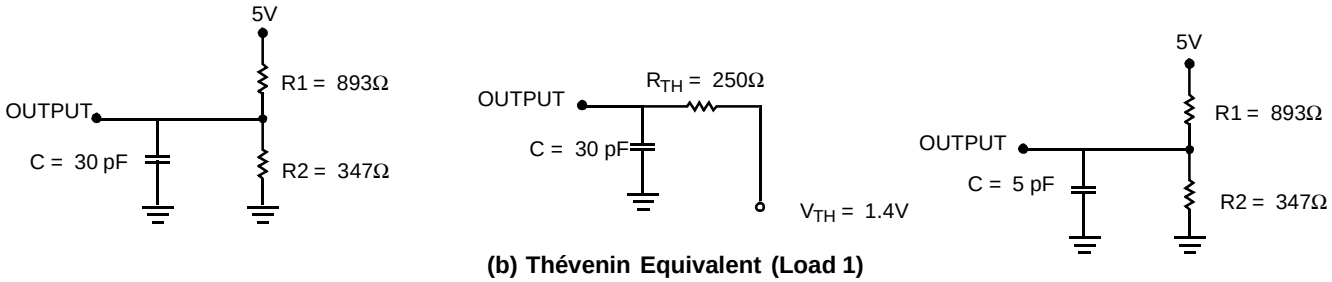
| Parameter | Description | | CY7C09279/89 CY7C09379/89 | | | | | | | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | -6[1] | | | -7 | | | -9 | | | -12 | | | |
| | | | Min. | Typ. | Max. | Min. | Typ. | Max. | Min. | Typ. | Max. | Min. | Typ. | Max. | |
| $V_{OH}$ | Output HIGH Voltage ($V_{CC}$ = Min., $I_{OH}$ = –4.0 mA) | | 2.4 | | | 2.4 | | | 2.4 | | | 2.4 | | | V |
| $V_{OL}$ | Output LOW Voltage ($V_{CC}$ = Min., $I_{OH}$ = +4.0 mA) | | | | 0.4 | | | 0.4 | | | 0.4 | | | 0.4 | V |
| $V_{IH}$ | Input HIGH Voltage | | 2.2 | | | 2.2 | | | 2.2 | | | 2.2 | | | V |
| $V_{IL}$ | Input LOW Voltage | | | | 0.8 | | | 0.8 | | | 0.8 | | | 0.8 | V |
| $I_{OZ}$ | Output Leakage Current | | –10 | | 10 | –10 | | 10 | –10 | | 10 | –10 | | 10 | µA |
| $I_{CC}$ | Operating Current ($V_{CC}$ = Max., $I_{OUT}$ = 0 mA) Outputs Disabled | Com'l. | | 250 | 450 | | 235 | 420 | | 215 | 360 | | 195 | 300 | mA |
| | | Ind.[10] | | | | | | | | 245 | 410 | | | | mA |
| $I_{SB1}$ | Standby Current (Both Ports TTL Level)[11] $\overline{CE}_L$ & $\overline{CE}_R \geq V_{IH}$, f = $f_{MAX}$ | Com'l. | | 45 | 115 | | 40 | 105 | | 35 | 95 | | 30 | 85 | mA |
| | | Ind.[10] | | | | | | | | 50 | 110 | | | | mA |
| $I_{SB2}$ | Standby Current (One Port TTL Level)[11] $\overline{CE}_L$ \| $\overline{CE}_R \geq V_{IH}$, f = $f_{MAX}$ | Com'l. | | 175 | 235 | | 160 | 220 | | 145 | 205 | | 125 | 190 | mA |
| | | Ind.[10] | | | | | | | | 160 | 220 | | | | mA |
| $I_{SB3}$ | Standby Current (Both Ports CMOS Level)[11] $\overline{CE}_L$ & $\overline{CE}_R \geq V_{CC}$ – 0.2V, f = 0 | Com'l. | | 0.05 | 0.5 | | 0.05 | 0.5 | | 0.05 | 0.5 | | 0.05 | 0.5 | mA |
| | | Ind.[10] | | | | | | | | 0.05 | 0.5 | | | | mA |
| $I_{SB4}$ | Standby Current (One Port CMOS Level)[11] $\overline{CE}_L$ \| $\overline{CE}_R \geq V_{IH}$, f = $f_{MAX}$ | Com'l. | | 160 | 200 | | 145 | 185 | | 130 | 170 | | 110 | 150 | mA |
| | | Ind.[10] | | | | | | | | 145 | 185 | | | | mA |

## Capacitance

| Parameter | Description | Test Conditions | Max. | Unit |
|---|---|---|---|---|
| $C_{IN}$ | Input Capacitance | $T_A$ = 25°C, f = 1 MHz, $V_{CC}$ = 5.0V | 10 | pF |
| $C_{OUT}$ | Output Capacitance | | 10 | pF |

**Note:**
11. $\overline{CE}_L$ and $\overline{CE}_R$ are internal signals. To select either the left or right port, both $\overline{CE}_0$ AND $CE_1$ must be asserted to their active states ($\overline{CE}_0 \leq V_{IL}$ and $CE_1 \geq V_{IH}$).

## AC Test Loads




**(a) Normal Load (Load 1)**

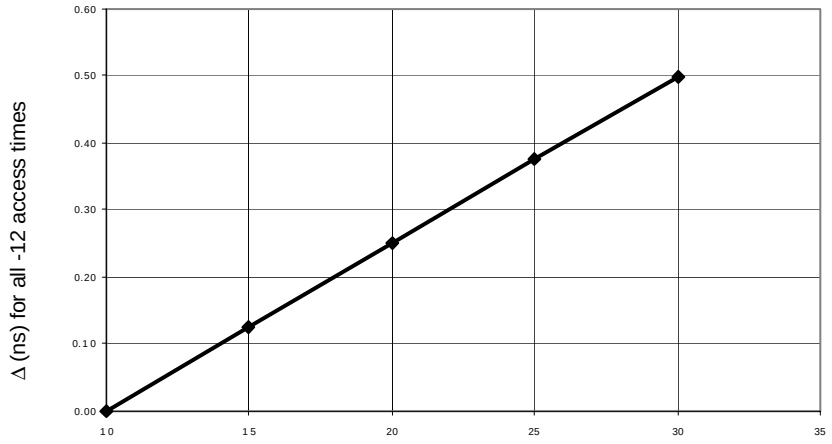
**(b) Thévenin Equivalent (Load 1)**

**(c) Three-State Delay (Load 2)**
(Used for $t_{CKLZ}$, $t_{OLZ}$, & $t_{OHZ}$ including scope and jig)

## AC Test Loads (Applicable to -6 only)[12]




**(a) Load 1 (-6 only)**




**(b) Load Derating Curve**

**Note:**
12. Test Conditions: C = 10 pF.

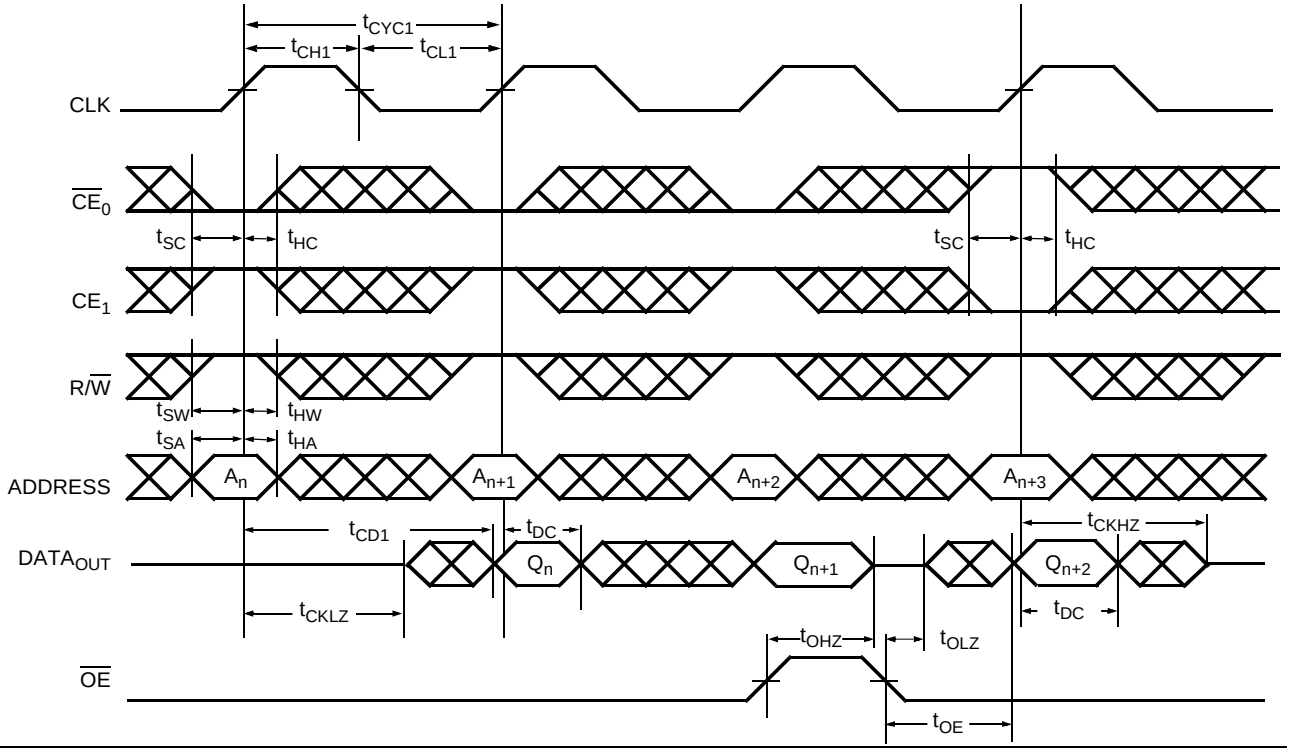
## Switching Characteristics Over the Operating Range

| Parameter | Description | CY7C09279/89 CY7C09379/89 | | | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | -6[1] | | -7 | | -9 | | -12 | | |
| | | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | |
| $f_{MAX1}$ | $f_{Max}$ Flow-Through | | 53 | | 45 | | 40 | | 33 | MHz |
| $f_{MAX2}$ | $f_{Max}$ Pipelined | | 100 | | 83 | | 67 | | 50 | MHz |
| $t_{CYC1}$ | Clock Cycle Time - Flow-Through | 19 | | 22 | | 25 | | 30 | | ns |
| $t_{CYC2}$ | Clock Cycle Time - Pipelined | 10 | | 12 | | 15 | | 20 | | ns |
| $t_{CH1}$ | Clock HIGH Time - Flow-Through | 6.5 | | 7.5 | | 12 | | 12 | | ns |
| $t_{CL1}$ | Clock LOW Time - Flow-Through | 6.5 | | 7.5 | | 12 | | 12 | | ns |
| $t_{CH2}$ | Clock HIGH Time - Pipelined | 4 | | 5 | | 6 | | 8 | | ns |
| $t_{CL2}$ | Clock LOW Time - Pipelined | 4 | | 5 | | 6 | | 8 | | ns |
| $t_R$ | Clock Rise Time | | 3 | | 3 | | 3 | | 3 | ns |
| $t_F$ | Clock Fall Time | | 3 | | 3 | | 3 | | 3 | ns |
| $t_{SA}$ | Address Set-Up Time | 3.5 | | 4 | | 4 | | 4 | | ns |
| $t_{HA}$ | Address Hold Time | 0 | | 0 | | 1 | | 1 | | ns |
| $t_{SC}$ | Chip Enable Set-Up Time | 3.5 | | 4 | | 4 | | 4 | | ns |
| $t_{HC}$ | Chip Enable Hold Time | 0 | | 0 | | 1 | | 1 | | ns |
| $t_{SW}$ | R/$\overline{W}$ Set-Up Time | 3.5 | | 4 | | 4 | | 4 | | ns |
| $t_{HW}$ | R/$\overline{W}$ Hold Time | 0 | | 0 | | 1 | | 1 | | ns |
| $t_{SD}$ | Input Data Set-Up Time | 3.5 | | 4 | | 4 | | 4 | | ns |
| $t_{HD}$ | Input Data Hold Time | 0 | | 0 | | 1 | | 1 | | ns |
| $t_{SAD}$ | $\overline{ADS}$ Set-Up Time | 3.5 | | 4 | | 4 | | 4 | | ns |
| $t_{HAD}$ | $\overline{ADS}$ Hold Time | 0 | | 0 | | 1 | | 1 | | ns |
| $t_{SCN}$ | $\overline{CNTEN}$ Set-Up Time | 3.5 | | 4 | | 4 | | 4 | | ns |
| $t_{HCN}$ | $\overline{CNTEN}$ Hold Time | 0 | | 0 | | 1 | | 1 | | ns |
| $t_{SRST}$ | $\overline{CNTRST}$ Set-Up Time | 3.5 | | 4 | | 4 | | 4 | | ns |
| $t_{HRST}$ | $\overline{CNTRST}$ Hold Time | 0 | | 0 | | 1 | | 1 | | ns |
| $t_{OE}$ | Output Enable to Data Valid | | 8 | | 9 | | 10 | | 12 | ns |
| $t_{OLZ}$[13, 14] | $\overline{OE}$ to Low Z | 2 | | 2 | | 2 | | 2 | | ns |
| $t_{OZ}$[13, 14] | $\overline{OE}$ to High Z | 1 | 7 | 1 | 7 | 1 | 7 | 1 | 7 | ns |
| $t_{CD1}$ | Clock to Data Valid - Flow-Through | | 15 | | 18 | | 20 | | 25 | ns |
| $t_{CD2}$ | Clock to Data Valid - Pipelined | | 6.5 | | 7.5 | | 9 | | 12 | ns |
| $t_{DC}$ | Data Output Hold After Clock HIGH | 2 | | 2 | | 2 | | 2 | | ns |
| $t_{CKHZ}$[13, 14] | Clock HIGH to Output High Z | 2 | 9 | 2 | 9 | 2 | 9 | 2 | 9 | ns |
| $t_{CKLZ}$[13, 14] | Clock HIGH to Output Low Z | 2 | | 2 | | 2 | | 2 | | ns |
| **Port to Port Delays** | | | | | | | | | | |
| $t_{CWDD}$ | Write Port Clock HIGH to Read Data Delay | | 30 | | 35 | | 40 | | 40 | ns |
| $t_{CCS}$ | Clock to Clock Set-Up Time | | 9 | | 10 | | 15 | | 15 | ns |

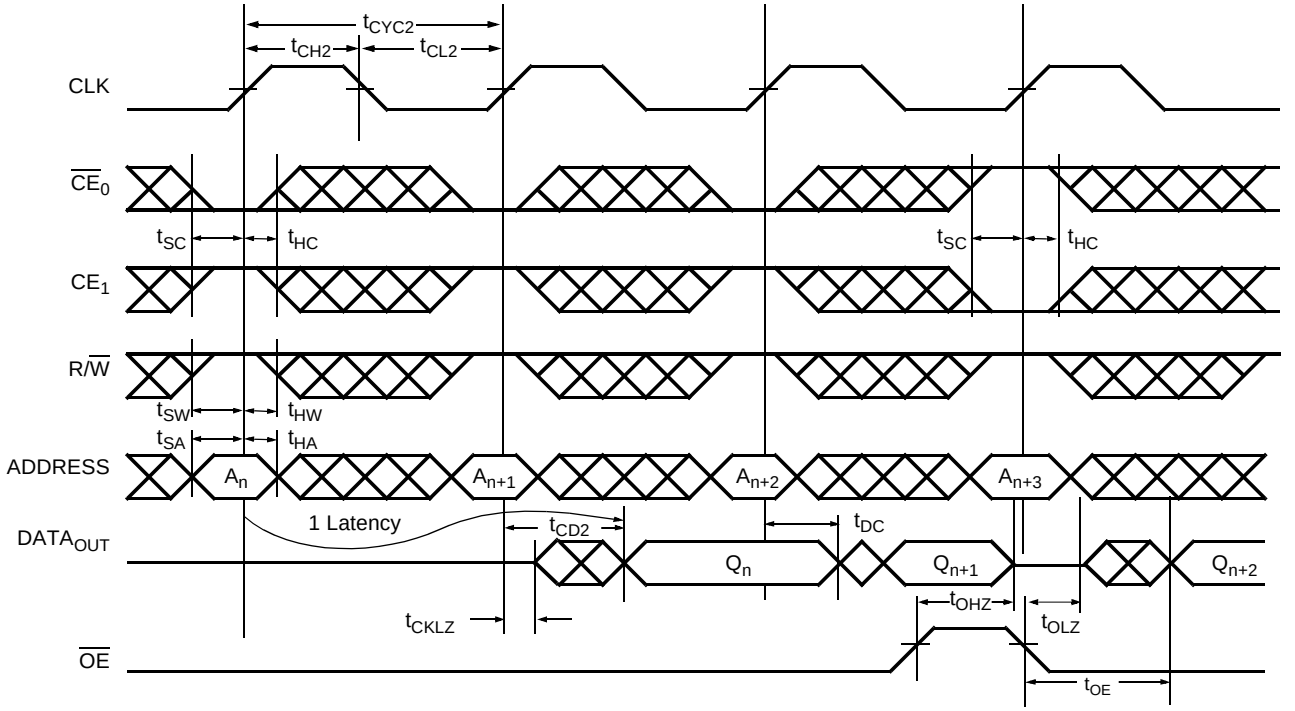
**Notes:**
13. Test conditions used are Load 2.
14. This parameter is guaranteed by design, but it is not production tested.

## Switching Waveforms

**Read Cycle for Flow-Through Output ($\overline{FT}$/PIPE = $V_{IL}$)**[15, 16, 17, 18]




**Read Cycle for Pipelined Operation ($\overline{FT}$/PIPE = $V_{IH}$)**[15, 16, 17, 18]

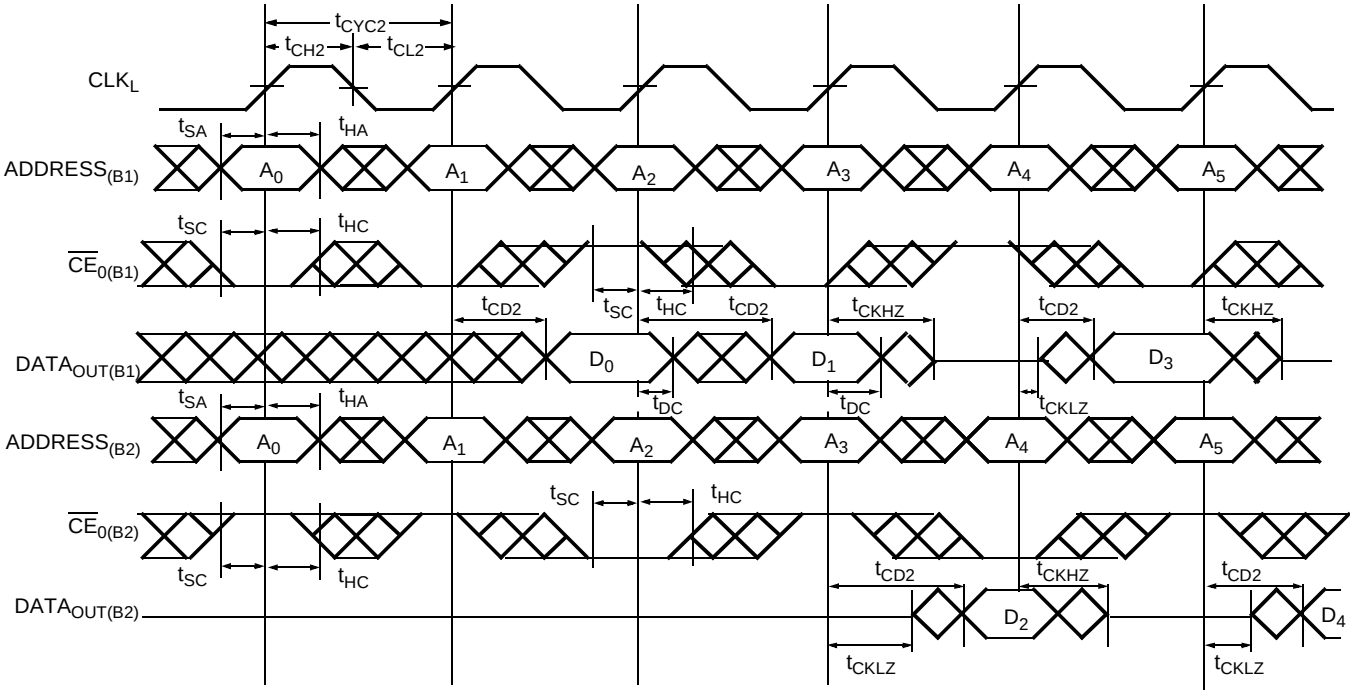



**Notes:**

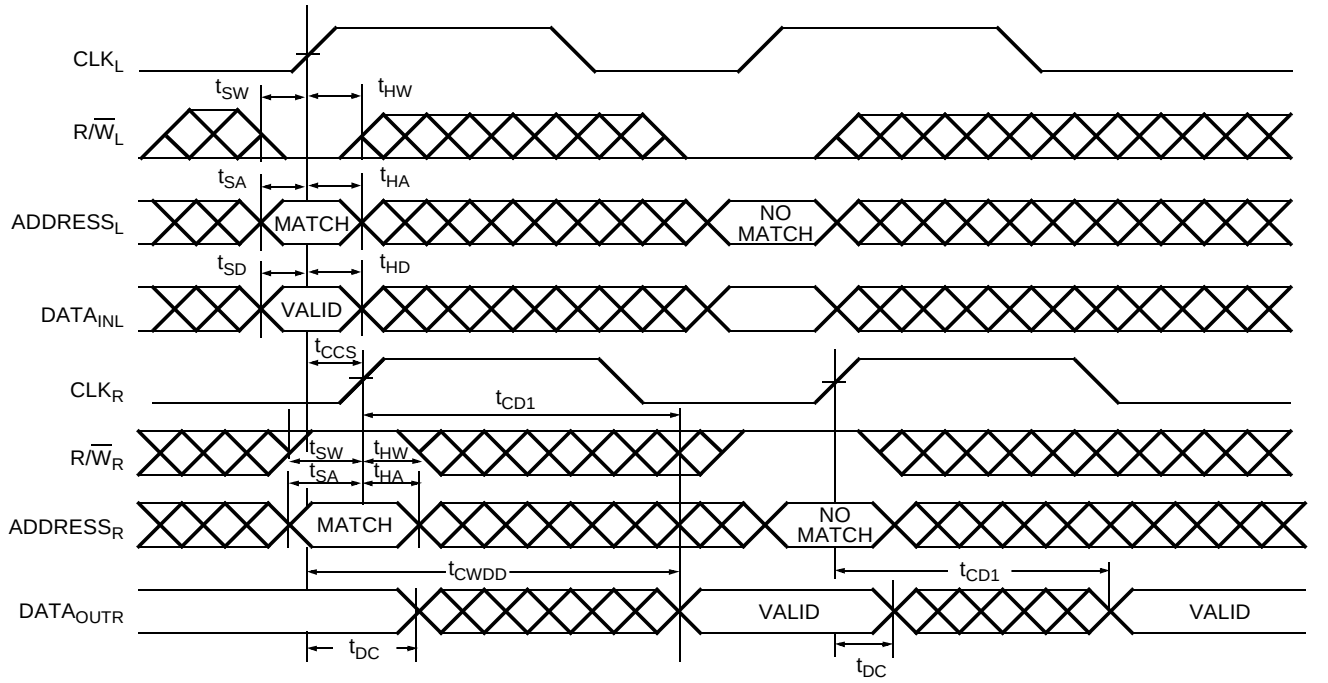
15. $\overline{OE}$ is asynchronously controlled; all other inputs are synchronous to the rising clock edge.
16. $\overline{ADS}$ = $V_{IL}$, CNTEN and $\overline{CNTRST}$ = $V_{IH}$.
17. The output is disabled (high-impedance state) by $\overline{CE}_0$=$V_{IH}$ or $CE_1$ = $V_{IL}$ following the next rising edge of the clock.
18. Addresses do not have to be accessed sequentially since $\overline{ADS}$ = $V_{IL}$ constantly loads the address on the rising edge of the CLK. Numbers are for reference only.

## Switching Waveforms (continued)

### Bank Select Pipelined Read[19, 20]




### Left Port Write to Flow-Through Right Port Read[21, 22, 23, 24]

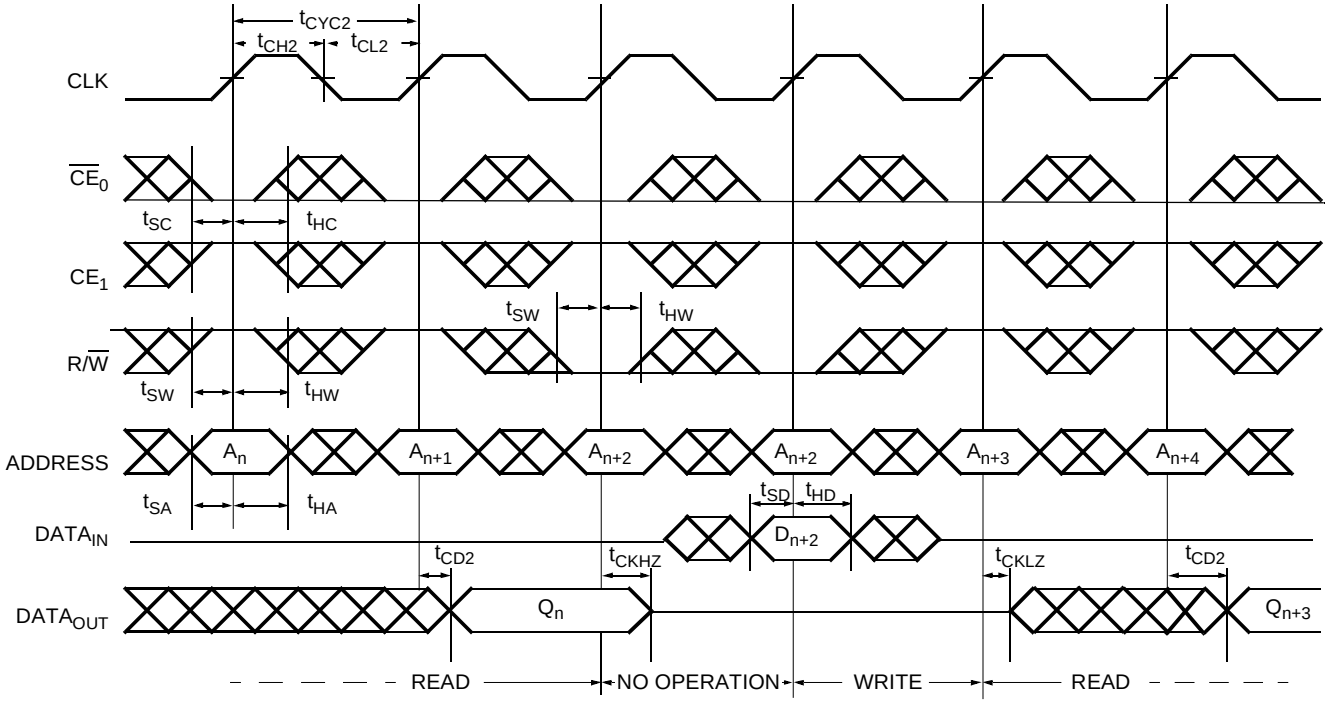



**Notes:**

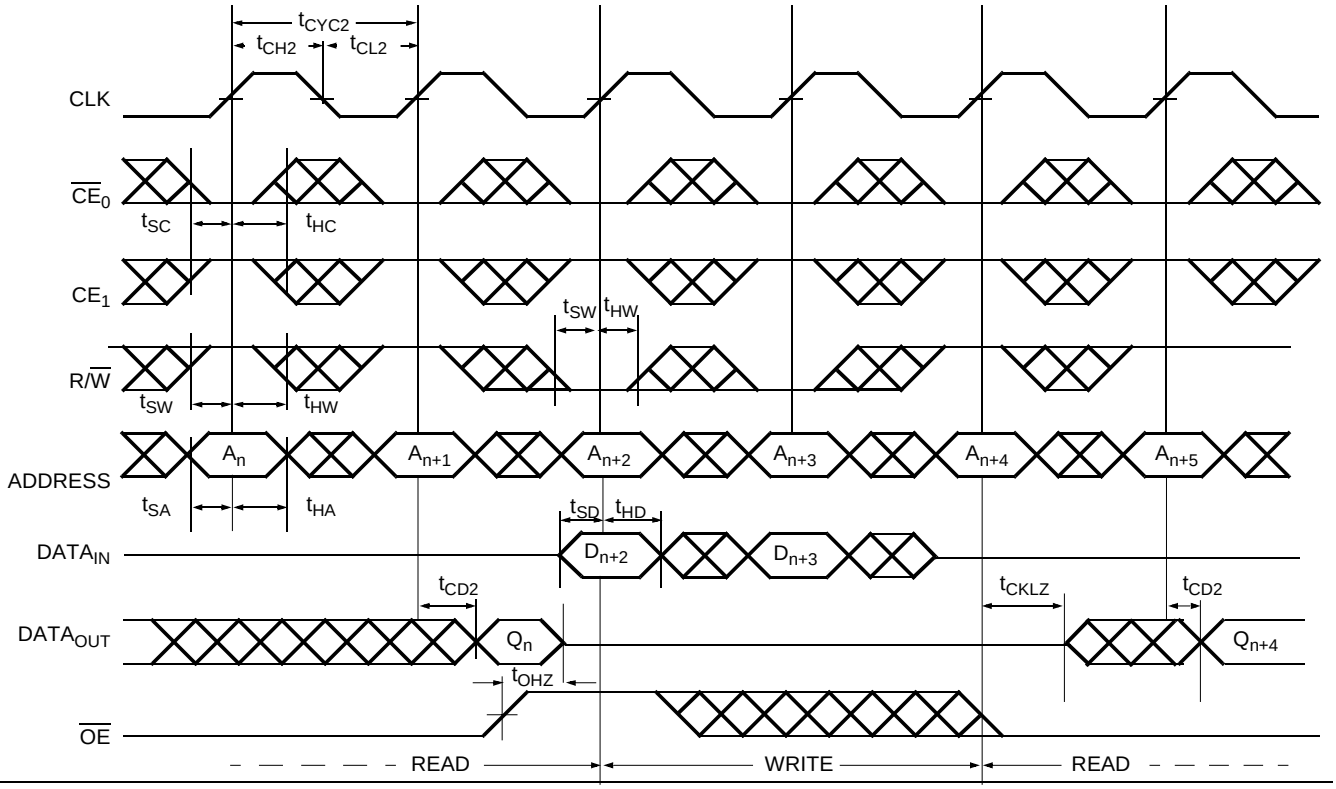
19. In this depth expansion example, B1 represents Bank #1 and B2 is Bank #2; each Bank consists of one Cypress dual-port device from this data sheet. $ADDRESS_{(B1)} = ADDRESS_{(B2)}$.
20. $\overline{UB}$, $\overline{LB}$, $\overline{OE}$ and $\overline{ADS} = V_{IL}$; $CE_{1(B1)}$, $CE_{1(B2)}$, $R/\overline{W}$, $\overline{CNTEN}$, and $\overline{CNTRST} = V_{IH}$.
21. The same waveforms apply for a right port write to flow-through left port read.
22. $\overline{CE}_0$, $\overline{UB}$, $\overline{LB}$, and $\overline{ADS} = V_{IL}$; $CE_1$, $\overline{CNTEN}$, and $\overline{CNTRST} = V_{IH}$.
23. $\overline{OE} = V_{IL}$ for the right port, which is being read from. $\overline{OE} = V_{IH}$ for the left port, which is being written to.
24. If $t_{CCS} \le$ maximum specified, then data from right port READ is not valid until the maximum specified for $t_{CWDD}$. If $t_{CCS}$>maximum specified, then data is not valid until $t_{CCS} + t_{CD1}$. $t_{CWDD}$ does not apply in this case.

## Switching Waveforms (continued)

**Pipelined Read-to-Write-to-Read ($\overline{OE}$ = $V_{IL}$)**[18, 25, 26, 27]




**Pipelined Read-to-Write-to-Read ($\overline{OE}$ Controlled)**[18, 25, 26, 27]

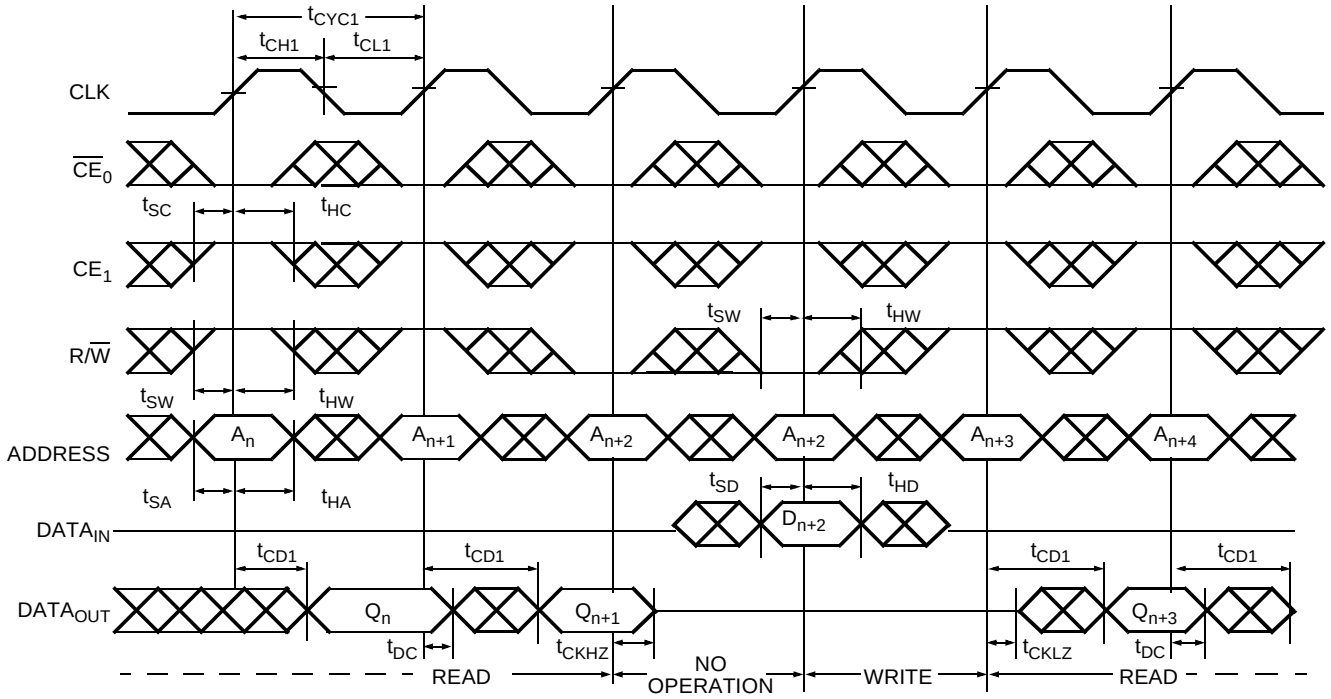



**Notes:**

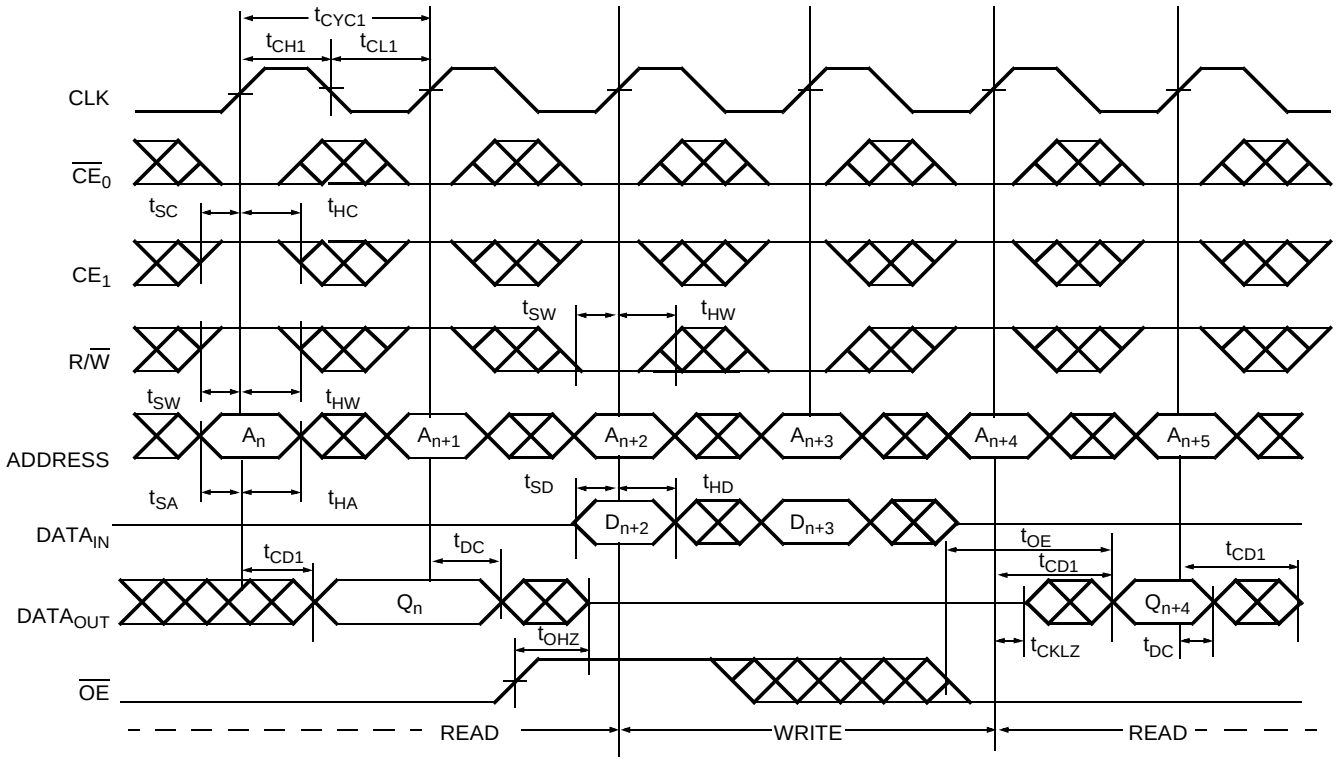
25. Output state (HIGH, LOW, or High-Impedance) is determined by the previous cycle control signals.
26. $\overline{CE_0}$ and ADS = $V_{IL}$; $CE_1$, CNTEN, and CNTRST = $V_{IH}$.
27. During "No Operation," data in memory at the selected address may be corrupted and should be rewritten to ensure data integrity.

## Switching Waveforms (continued)

**Flow-Through Read-to-Write-to-Read ($\overline{OE}$ = $V_{IL}$)**[16, 18, 25, 26]

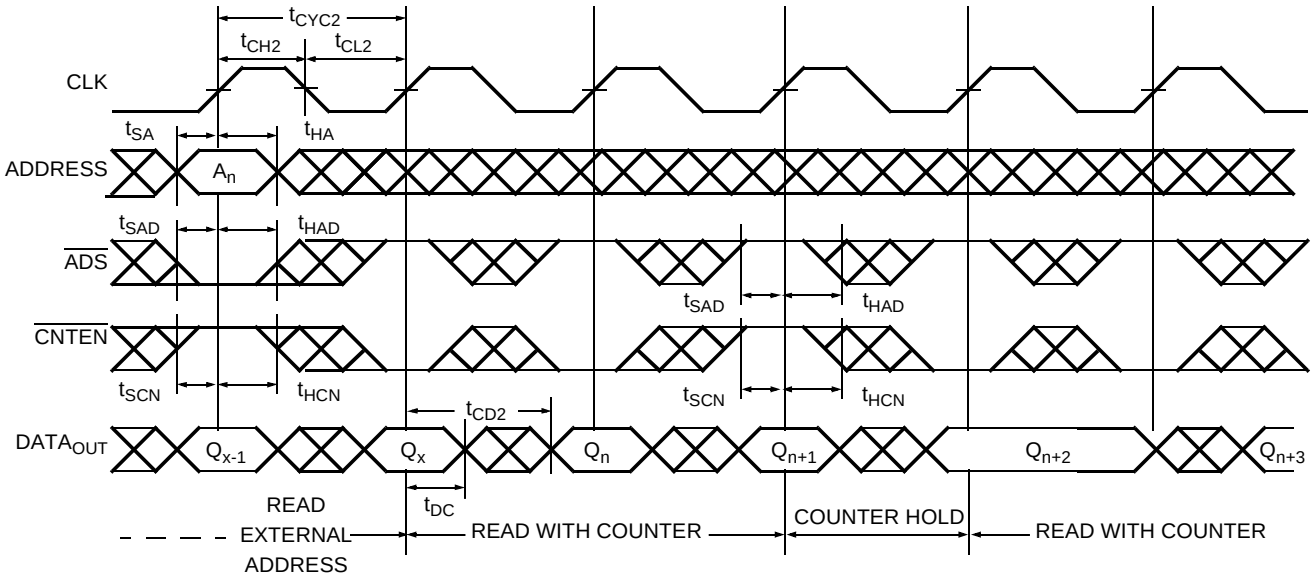



**Flow-Through Read-to-Write-to-Read ($\overline{OE}$ Controlled)**[16, 18, 25, 26]

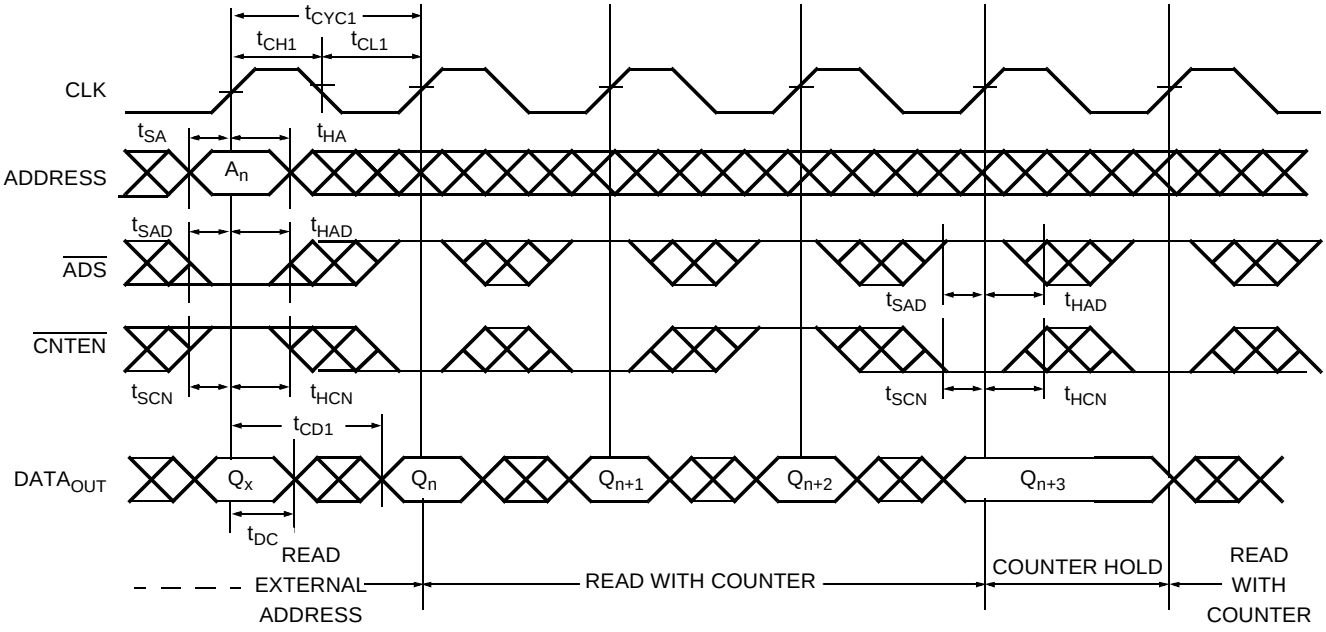


## Switching Waveforms (continued)

**Pipelined Read with Address Counter Advance**[28]




**Flow-Through Read with Address Counter Advance**[28]

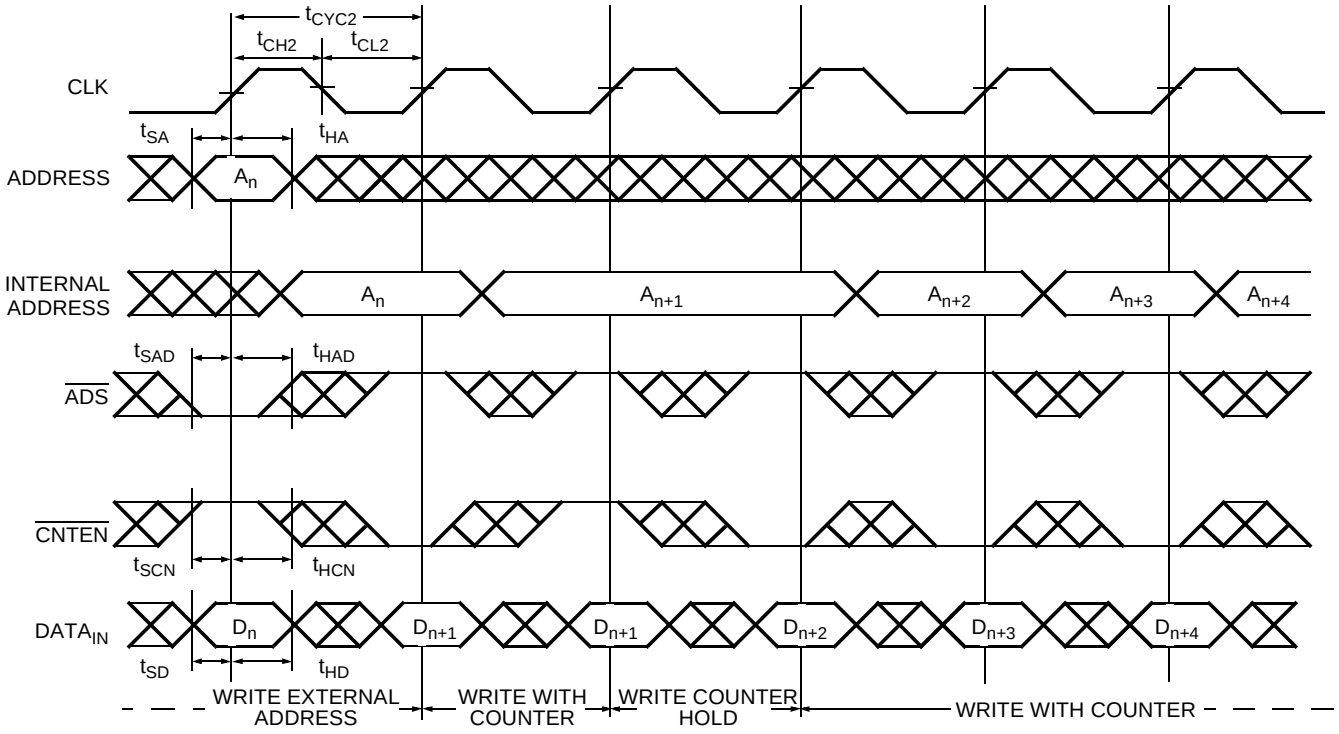



**Note:**

28. $\overline{CE_0}$ and $\overline{OE}$ = $V_{IL}$; $CE_1$, R/$\overline{W}$ and $\overline{CNTRST}$ = $V_{IH}$.

## Switching Waveforms (continued)

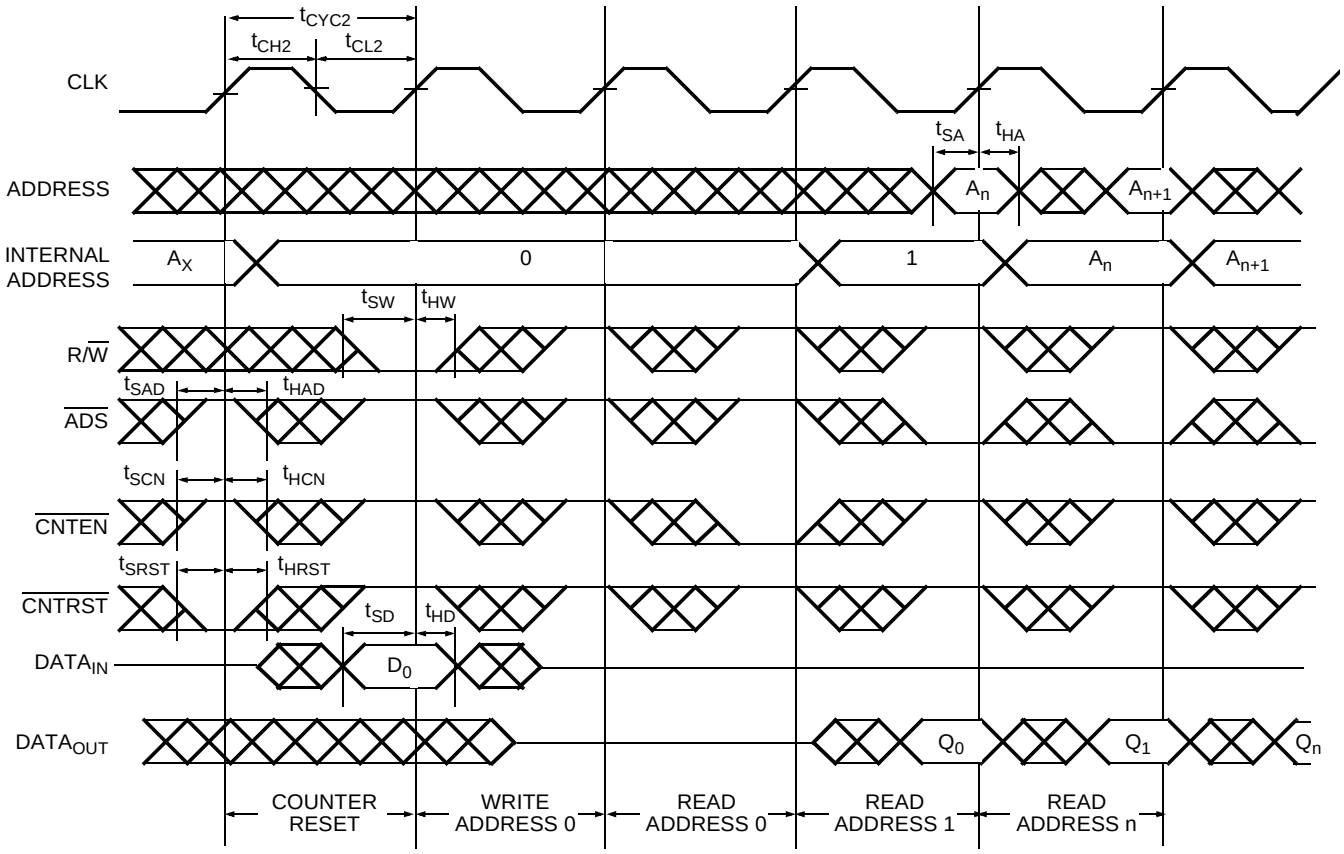
**Write with Address Counter Advance (Flow-Through or Pipelined Outputs)**[29, 30]




**Notes:**
29. $\overline{CE_0}$, $\overline{UB}$, $\overline{LB}$, and R/$\overline{W}$ = $V_{IL}$; $CE_1$ and $\overline{CNTRST}$ = $V_{IH}$.
30. The “Internal Address” is equal to the “External Address” when $\overline{ADS}$ = $V_{IL}$ and equals the counter output when $\overline{ADS}$ = $V_{IH}$.

## Switching Waveforms (continued)

**Counter Reset (Pipelined Outputs)**[18, 30, 31, 32]




**Notes:**

31. $\overline{CE_0}$, $\overline{UB}$, and $\overline{LB}$ = $V_{IL}$; $CE_1$ = $V_{IH}$.
32. No dead cycle exists during counter reset. A READ or WRITE cycle may be coincidental with the counter reset.

## Read/Write and Enable Operation[33, 34, 35]

| Inputs | | | | | Outputs | |
|---|---|---|---|---|---|---|
| $\overline{OE}$ | CLK | $\overline{CE_0}$ | $CE_1$ | R/$\overline{W}$ | $I/O_0$–$I/O_{17}$ | Operation |
| X | ⎍ | H | X | X | High-Z | Deselected[36] |
| X | ⎍ | X | L | X | High-Z | Deselected[36] |
| X | ⎍ | L | H | L | $D_{IN}$ | Write |
| L | ⎍ | L | H | H | $D_{OUT}$ | Read[34] |
| H | X | L | H | X | High-Z | Outputs Disabled |

## Address Counter Control Operation[33, 37, 38, 39]

| Address | Previous Address | CLK | $\overline{ADS}$ | $\overline{CNTEN}$ | $\overline{CNTRST}$ | I/O | Mode | Operation |
|---|---|---|---|---|---|---|---|---|
| X | X | ⎍ | X | X | L | $D_{out(0)}$ | Reset | Counter Reset to Address 0 |
| $A_n$ | X | ⎍ | L | X | H | $D_{out(n)}$ | Load | Address Load into Counter |
| X | $A_n$ | ⎍ | H | H | H | $D_{out(n)}$ | Hold | External Address Blocked—Counter Disabled |
| X | $A_n$ | ⎍ | H | L | H | $D_{out(n+1)}$ | Increment | Counter Enabled—Internal Address Generation |

**Notes:**
33. "X" = "Don't Care," "H" = $V_{IH}$, "L" = $V_{IL}$.
34. $\overline{ADS}$, $\overline{CNTEN}$, $\overline{CNTRST}$ = "Don't Care."
35. $\overline{OE}$ is an asynchronous input signal.
36. When $\overline{CE}$ changes state in the pipelined mode, deselection and read happen in the following clock cycle.
37. $\overline{CE_0}$ and $\overline{OE}$ = $V_{IL}$; $CE_1$ and R/$\overline{W}$ = $V_{IH}$.
38. Data shown for flow-through mode; pipelined mode output will be delayed by one cycle.
39. Counter operation is independent of $\overline{CE_0}$ and $CE_1$.

## Ordering Information

**32K x16 Synchronous Dual-Port SRAM**

| Speed (ns) | Ordering Code | Package Name | Package Type | Operating Range |
|---|---|---|---|---|
| 6.5[1] | CY7C09279-6AC | A100 | 100-Pin Thin Quad Flat Pack | Commercial |
| 7.5 | CY7C09279-7AC | A100 | 100-Pin Thin Quad Flat Pack | Commercial |
| 9 | CY7C09279-9AC | A100 | 100-Pin Thin Quad Flat Pack | Commercial |
| 12 | CY7C09279-12AC | A100 | 100-Pin Thin Quad Flat Pack | Commercial |

**64K x16 Synchronous Dual-Port SRAM**

| Speed (ns) | Ordering Code | Package Name | Package Type | Operating Range |
|---|---|---|---|---|
| 6.5[1] | CY7C09289-6AC | A100 | 100-Pin Thin Quad Flat Pack | Commercial |
| 7.5 | CY7C09289-7AC | A100 | 100-Pin Thin Quad Flat Pack | Commercial |
| 9 | CY7C09289-9AC | A100 | 100-Pin Thin Quad Flat Pack | Commercial |
| | CY7C09289-9AI | A100 | 100-Pin Thin Quad Flat Pack | Industrial |
| 12 | CY7C09289-12AC | A100 | 100-Pin Thin Quad Flat Pack | Commercial |

**32K x18 Synchronous Dual-Port SRAM**

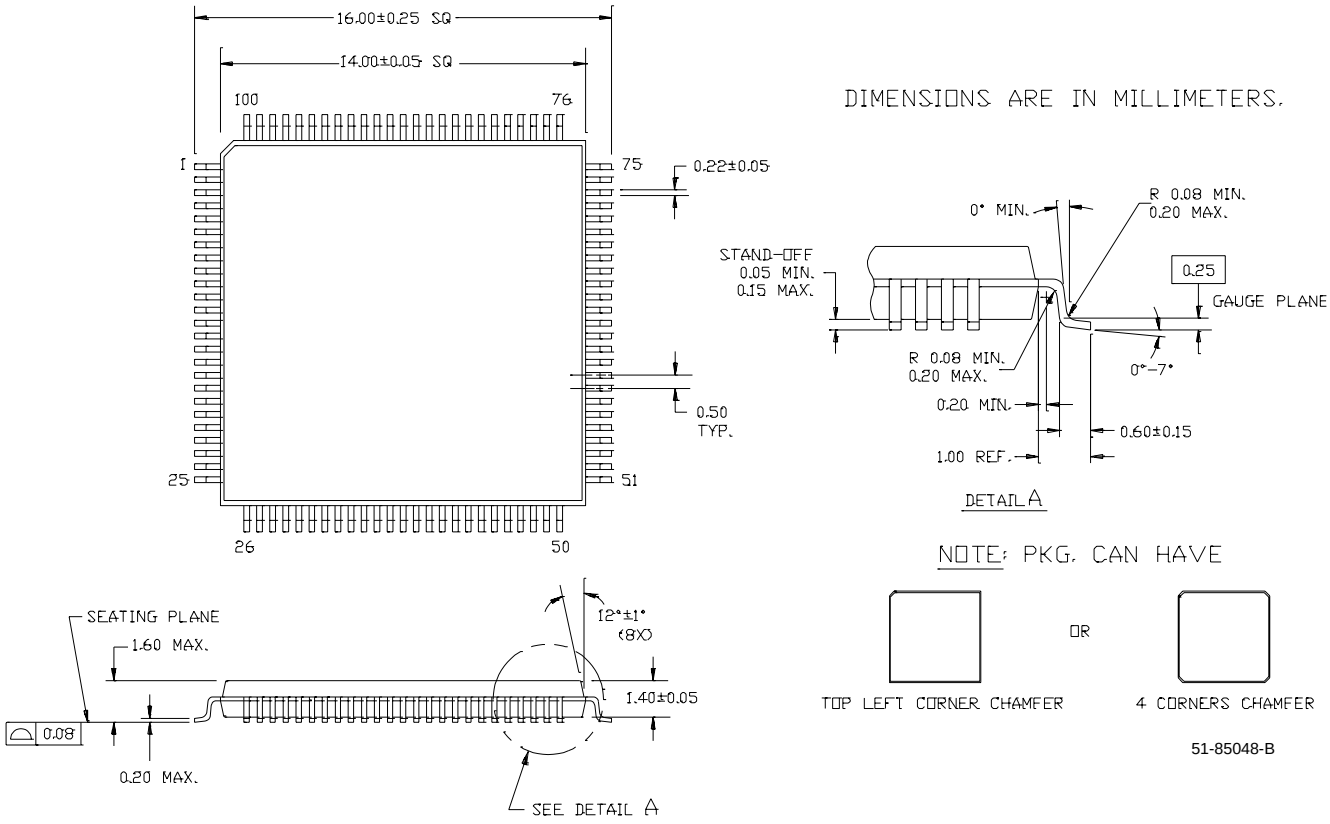
| Speed (ns) | Ordering Code | Package Name | Package Type | Operating Range |
|---|---|---|---|---|
| 6.5[1] | CY7C09379-6AC | A100 | 100-Pin Thin Quad Flat Pack | Commercial |
| 7.5 | CY7C09379-7AC | A100 | 100-Pin Thin Quad Flat Pack | Commercial |
| 9 | CY7C09379-9AC | A100 | 100-Pin Thin Quad Flat Pack | Commercial |
| 12 | CY7C09379-12AC | A100 | 100-Pin Thin Quad Flat Pack | Commercial |

**64K x18 Synchronous Dual-Port SRAM**

| Speed (ns) | Ordering Code | Package Name | Package Type | Operating Range |
|---|---|---|---|---|
| 6.5[1] | CY7C09389-6AC | A100 | 100-Pin Thin Quad Flat Pack | Commercial |
| 7.5 | CY7C09389-7AC | A100 | 100-Pin Thin Quad Flat Pack | Commercial |
| 9 | CY7C09389-9AC | A100 | 100-Pin Thin Quad Flat Pack | Commercial |
| | CY7C09389-9AI | A100 | 100-Pin Thin Quad Flat Pack | Industrial |
| 12 | CY7C09389-12AC | A100 | 100-Pin Thin Quad Flat Pack | Commercial |

## Package Diagram

**100-Pin Thin Plastic Quad Flat Pack (TQFP) A100**






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| Document Title: CY7C09279/89, CY7C09379/89 32K/64K X 16/18 Synchronous Dual Port Static RAM<br>Document Number: 38-06040 | | | | |
|---|---|---|---|---|
| **REV.** | **ECN NO.** | **Issue Date** | **Orig. of Change** | **Description of Change** |
| ** | 110188 | 09/29/01 | SZV | Change from Spec number: 38-00664 to 38-06040 |
| *A | 122290 | 12/27/02 | RBI | Power up requirements added to Maximum Ratings information |

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