DATA SHEET

For a complete data sheet, please also download:

- The IC06 74HC/HCT/HCU/HCMOS Logic Family Specifications
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Information
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Outlines

74HC/HCT7030

9-bit x 64-word FIFO register; 3-state

Product specification
File under Integrated Circuits, IC06

December 1990

Philips Semiconductors

PHILIPS

FEATURES

- Synchronous or asynchronous operation
- 3-state outputs
- Master-reset input to clear control functions
- 33 MHz (typ.) shift-in, shift-out rates with or without flags
- Very low power consumption
- Cascadable to 25 MHz (typ.)
- Readily expandable in word and bit dimensions
- Pinning arranged for easy board layout: input pins directly opposite output pins
- Output capability: standard
- I_{CC} category: LSI

GENERAL DESCRIPTION

The 74HC/HCT7030 are high-speed Si-gate CMOS devices specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT7030 is an expandable, First-In First-Out (FIFO) memory organized as 64 words by 9 bits. A 33 MHz data-rate makes it ideal for high-speed applications. Even at high frequencies, the I_{CC} dynamic is very low (f_{max} = 18 MHz; V_{CC} = 5 V produces a dynamic I_{CC} of 80 mA). If the device is not continuously operating at f_{max}, then I_{CC} will decrease proportionally.

With separate controls for shift-in (SI) and shift-out ($\overline{SO}$), reading and writing operations are completely independent, allowing synchronous and asynchronous data transfers. Additional controls include a master-reset input ($\overline{MR}$) and an output enable input ($\overline{OE}$). Flags for data-in-ready (DIR) and data-out-ready (DOR) indicate the status of the device.

Devices can be interconnected easily to expand word and bit dimensions. All output pins are directly opposite the corresponding input pins thus simplifying board layout in expanded applications.

INPUTS AND OUTPUTS

Data inputs (D_0 to D_8)

As there is no weighting of the inputs, any input can be assigned as the MSB. The size of the FIFO memory can be reduced from the 9×64 configuration, i.e. 8×64, 7×64, down to 1×64, by tying unused data input pins to V_{CC} or GND.

Data outputs (Q_0 to Q_8)

As there is no weighting of the outputs, any output can be assigned as the MSB. The size of the FIFO memory can be reduced from the 9×64 configuration as described for data inputs. In a reduced format, the unused data output pins must be left open circuit.

Master-reset ($\overline{MR}$)

When $\overline{MR}$ is LOW, the control functions within the FIFO are cleared, and data content is declared invalid. The data-in-ready (DIR) flag is set HIGH and the data-out-ready (DOR) flag is set LOW. The output stage remains in the state of the last word that was shifted out, or in the random state existing at power-up.

Status flag outputs (DIR, DOR)

Indication of the status of the FIFO is given by two status flags, data-in-ready (DIR) and data-out-ready (DOR):

DIR	=	HIGH indicates the input stage is empty and ready to accept valid data
DIR	=	LOW indicates that the FIFO is full or that a previous shift-in operation is not complete (busy)
DOR	=	HIGH assures valid data is present at the outputs Q_0 to Q_8 (does not indicate that new data is awaiting transfer into the output stage)
DOR	=	LOW indicates the output stage is busy or there is no valid data

Shift-in control (SI)

Data is loaded into the input stage on a LOW-to-HIGH transition of SI. A HIGH-to-LOW transition triggers an automatic data transfer process (ripple through). If SI is held HIGH during reset, data will be loaded at the rising edge of the $\overline{MR}$ signal.

Shift-out control ($\overline{SO}$)

A LOW-to-HIGH transition of $\overline{SO}$ causes the DOR flags to go LOW. A HIGH-to-LOW transition of $\overline{SO}$ causes upstream data to move into the output stage, and empty locations to move towards the input stage (bubble-up).

Output enable ($\overline{OE}$)

The outputs Q_0 to Q_8 are enabled when $\overline{OE}$ = LOW. When $\overline{OE}$ = HIGH the outputs are in the high impedance OFF-state.

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}/ t_{PLH}	propagation delay	C_L = 15 pF; V_{CC} = 5 V			
	$\overline{MR}$ to DIR and DOR		21	26	ns
	$\overline{SO}$ to Q_n		36	40	ns
f_{max}	maximum clock frequency SI and $\overline{SO}$		33	29	MHz
C_I	input capacitance		3.5	3.5	pF
C_P	power dissipation capacitance per package	notes 1 and 2	660	660	pF

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):

   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o)$ where:

   f_i = input frequency in MHz

   f_o = output frequency in MHz

   $\sum (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs

   C_L = output load capacitance in pF

   V_{CC} = supply voltage in V

2. For HC the condition is V_I = GND to V_{CC}
   For HCT the condition is V_I = GND to V_{CC} – 1.5 V

ORDERING INFORMATION

See *"74HC/HCT/HCU/HCMOS Logic Package Information"*.

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 2, 14	GND	ground (0 V)
3	DIR	data-in-ready output
4	SI	shift-in input (LOW-to-HIGH, edge-triggered)
5, 6, 7, 8, 9, 10, 11, 12, 13	D_0 to D_8	parallel data inputs
15	$\overline{OE}$	output enable input (active LOW)
24, 23, 22, 21, 20, 19, 18, 17, 16	Q_0 to Q_8	3-state parallel data outputs
25	DOR	data-out-ready output
26	$\overline{SO}$	shift-out input (HIGH-to-LOW, edge-triggered)
27	$\overline{MR}$	asynchronous master-reset input (active LOW)
28	V_{CC}	positive supply voltage

Note

1. Pin 14 must be connected to GND. Pins 1 and 2 can be left floating or connected to GND, however it is not allowed to let current flow in either direction between pins 1, 2 and 14.

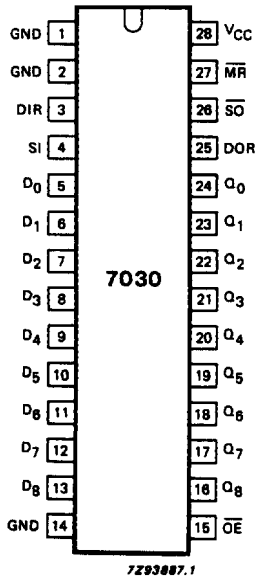


Fig.1 Pin configuration.

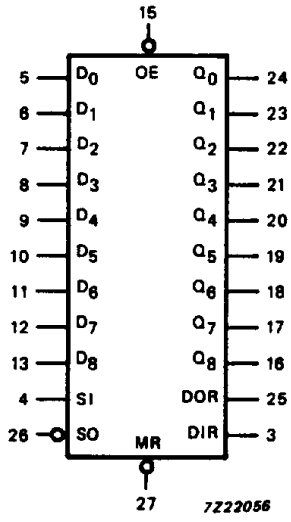


Fig.2 Logic symbol.

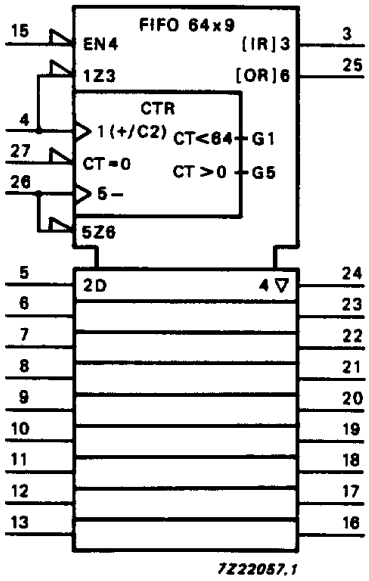


Fig.3 IEC logic symbol.

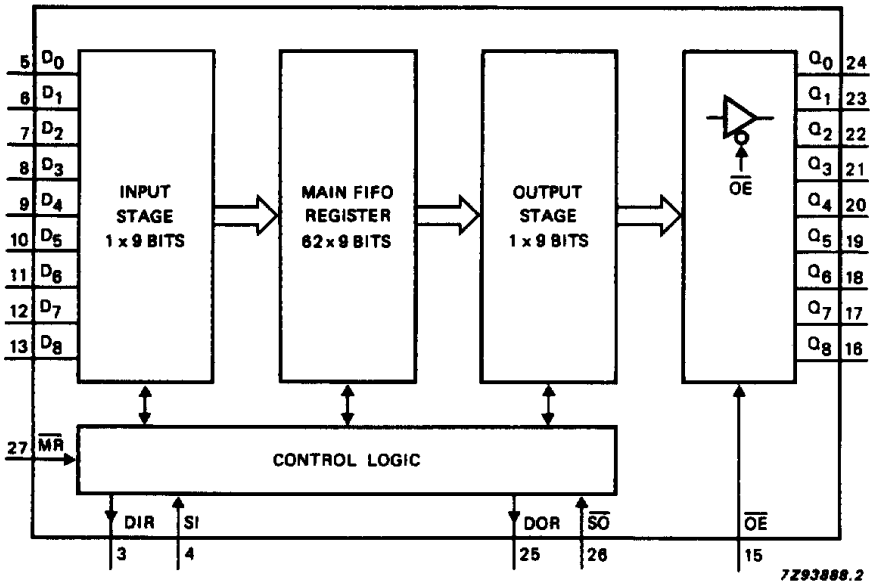


Fig.4 Functional diagram.

APPLICATIONS

- High-speed disc or tape controller
- Video timebase correction
- A/D output buffers
- Voice synthesis
- Input/output formatter for digital filters and FFTs
- Bit-rate smoothing

FUNCTIONAL DESCRIPTION

Data input

Following power-up, the master-reset ($\overline{MR}$) input is pulsed LOW to clear the FIFO memory (see Fig.8). The data-in-ready flag (DIR = HIGH) indicates that the FIFO input stage is empty and ready to receive data. When DIR is valid (HIGH), data present at D_0 to D_8 can be shifted-in using the SI control input. With SI = HIGH, data is shifted into the input stage and a busy indication is given by DIR going LOW.

The data remains at the first location in the FIFO until SI is set to LOW. With SI = LOW data moves through the FIFO to the output stage, or to the last empty location. If the FIFO is not full after the SI pulse, DIR again becomes valid (HIGH) to indicate that space is available in the FIFO. The DIR flag remains LOW if the FIFO is full (see Fig.6). The SI pulse must be made LOW in order to complete the shift-in process.

With the FIFO full, SI can be held HIGH until a shift-out ($\overline{SO}$) pulse occurs. Then, following a shift-out of data, an empty location appears at the FIFO input and DIR goes HIGH to allow the next data to be shifted-in. This remains at the first FIFO location until SI again goes LOW (see Fig.7).

Data transfer

After data has been transferred from the input stage of the FIFO following SI = LOW, data moves through the FIFO asynchronously and is stacked at the output end of the register. Empty locations appear at the input end of the FIFO as data moves through the device.

Data output

The data-out-ready flag (DOR = HIGH) indicates that there is valid data at the output (Q_0 to Q_8). The initial master-reset at power-on ($\overline{MR}$ = LOW) sets DOR to LOW (see Fig.8). After $\overline{MR}$ = HIGH, data shifted into the FIFO moves through to the output stage causing DOR to go HIGH. As the DOR flag goes HIGH, data can be shifted-out using the $\overline{SO}$ control input. With $\overline{SO}$ = HIGH, data in the output stage is shifted out and a busy indication is given by DOR going LOW. When $\overline{SO}$ is made LOW, data moves through the FIFO to fill the output stage and an empty location appears at the input stage. When the output stage is filled DOR goes HIGH, but if the last of the valid data has been shifted out leaving the FIFO empty the DOR flag remains LOW (see Fig.9). With the FIFO empty, the last word that was shifted-out is latched at the output Q_0 to Q_8.

With the FIFO empty, the $\overline{SO}$ input can be held HIGH until the SI control input is used. Following an SI pulse, data moves through the FIFO to the output stage, resulting in the DOR flag pulsing HIGH and a shift-out of data occurring. The $\overline{SO}$ control must be made LOW before additional data can be shifted out (see Fig.10).

High-speed burst mode

If it is assumed that the shift-in/shift-out pulses are not applied until the respective status flags are valid, it follows that the shift-in/shift-out rates are determined by the status flags. However, without the status flags a high-speed burst mode can be implemented. In this mode, the burst-in/burst-out rates are determined by the pulse widths of the shift-in/shift-out inputs and burst rates of 35 MHz can be obtained. Shift pulses can be applied without regard to the status flags but shift-in pulses that would overflow the storage capacity of the FIFO are not allowed (see Figs 11 and 12).

Expanded format

With the addition of a logic gate, the FIFO is easily expanded to increase word length (see Fig.17). The basic operation and timing are identical to a single FIFO, with the exception of an additional gate delay on the flag outputs. If during application, the following occurs:

- SI is held HIGH when the FIFO is empty, some additional logic is required to produce a composite DIR pulse (see Figs 7 and 18).
- $\overline{SO}$ is held HIGH when the FIFO is full, some additional logic is required to produce a composite DOR pulse (see Figs 10 and 18).

Due to the part-to-part spread of the ripple through time, the flag signals of $FIFO_A$ and $FIFO_B$ will not always coincide and the AND-gate will not produce a composite flag signal. The solution is given in Fig.18.

The “7030” is easily cascaded to increase the word capacity and no external components are needed. In the cascaded configuration, all necessary communications and timing are performed by the FIFOs. The intercommunication speed is determined by the minimum flag pulse widths and the flag delays. The data rate of cascaded devices is typically 25 MHz. Word-capacity can be expanded to and beyond 128-words $\times$ 9-bits (see Fig.19).

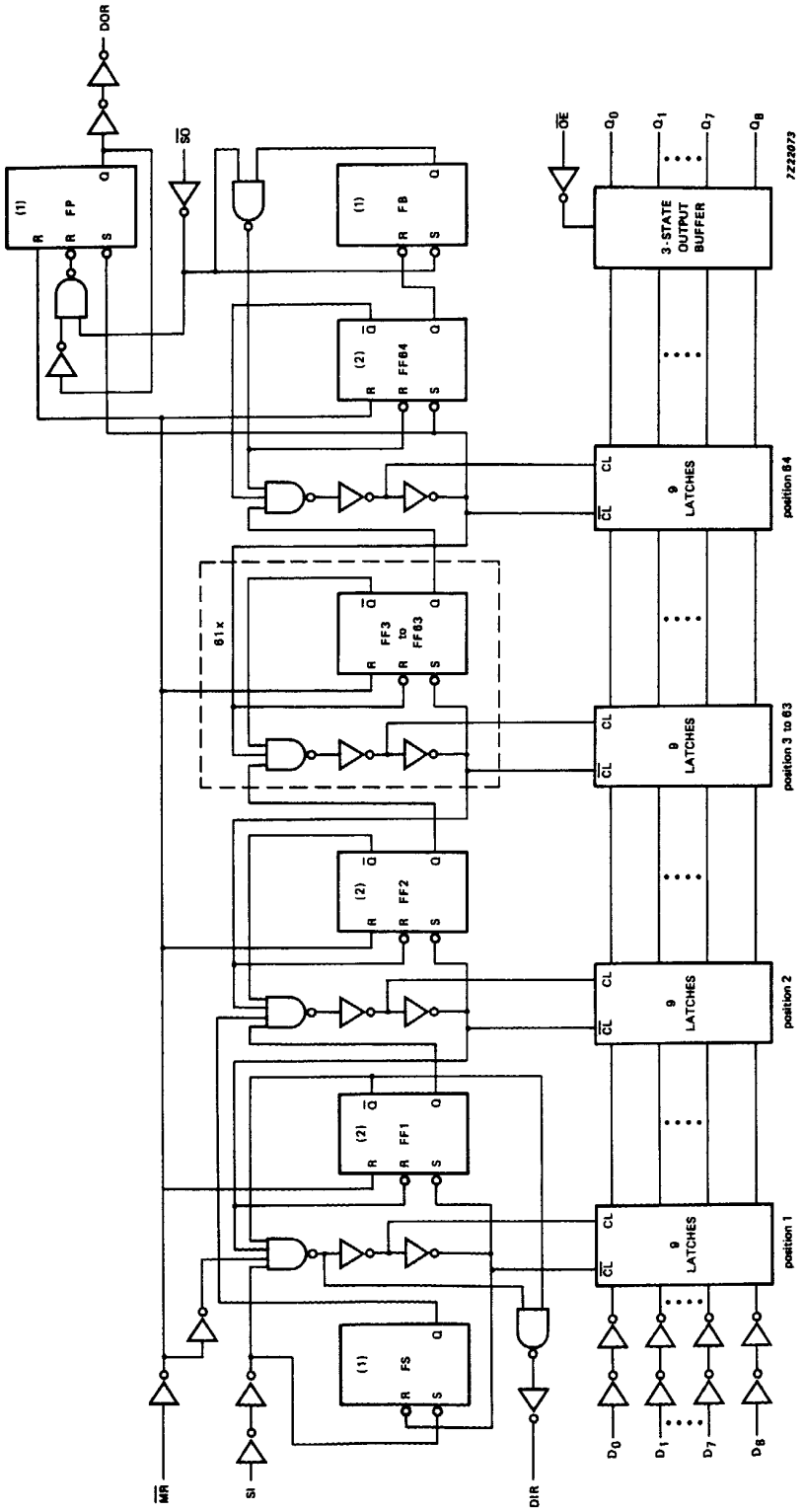


Fig.5 Logic diagram.

(see control flip-flops)

(1) LOW on $\overline{S}$ input of flip-flops FS, FB and FP will set Q output to HIGH independent of state on $\overline{R}$ input.

(2) LOW on $\overline{R}$ input to FF1 to FF64 will set Q output to LOW independent of state on $\overline{S}$ input.

DC CHARACTERISTICS FOR 74HC

For the DC characteristics see *"74HC/HCT/HCU/HCMOS Logic Family Specifications"*.

Output capability: standard
I_{CC} category: LSI

AC CHARACTERISTICS FOR 74HC

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HC								V_{CC} (V)	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/ t_{PLH}	propagation delay $\overline{MR}$ to DIR, DOR		69 25 20	210 42 36		265 53 45		315 63 54	ns	2.0 4.5 6.0	Fig.8
t_{PHL}/ t_{PLH}	propagation delay SI to DIR		77 28 22	235 47 40		295 59 50		355 71 60	ns	2.0 4.5 6.0	Fig.6
t_{PHL}/ t_{PLH}	propagation delay $\overline{SO}$ to DOR		102 37 30	315 63 54		395 79 67		475 95 81	ns	2.0 4.5 6.0	Fig.9
t_{PHL}/ t_{PLH}	propagation delay DOR to Q_n		11 4 3	35 7 6		45 9 8		55 11 9	ns	2.0 4.5 6.0	Fig.10
t_{PHL}/ t_{PLH}	propagation delay $\overline{SO}$ to Q_n		113 41 33	345 69 59		430 86 73		520 104 88	ns	2.0 4.5 6.0	Fig.14
t_{PLH}	propagation delay/ ripple through delay SI to DOR		2.5 0.9 0.7	8.0 1.6 1.3		10 2.0 1.6		12 2.4 1.9	µs	2.0 4.5 6.0	Fig.10
t_{PLH}	propagation delay/ bubble-up delay $\overline{SO}$ to DIR		3.3 1.2 1.0	10.0 2.0 1.6		12 2.5 2.0		15 3.0 2.4	µs	2.0 4.5 6.0	Fig.7
t_{PZH}/ t_{PZL}	3-state output enable $\overline{OE}$ to Q_n		52 19 15	175 35 30		220 44 37		265 53 45	ns	2.0 4.5 6.0	Fig.16
t_{PHZ}/ t_{PLZ}	3-state output disable $\overline{OE}$ to Q_n		50 18 14	150 30 26		190 38 33		225 45 38	ns	2.0 4.5 6.0	Fig.16
t_{THL}/ t_{TLH}	output transition time		19 7 6	75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Fig.14
t_W	SI pulse width HIGH or LOW	50 10 9	14 5 4		65 13 11		75 15 13		ns	2.0 4.5 6.0	Fig.6

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HC								V_{CC} (V)	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_W	$\overline{SO}$ pulse width HIGH or LOW	100 20 17	33 12 10		125 25 21		150 30 26		ns	2.0 4.5 6.0	Fig.9
t_W	DIR pulse width HIGH	10 5 4	47 17 14	145 29 25	8 4 3	180 36 31	8 4 3	220 44 38	ns	2.0 4.5 6.0	Fig.7
t_W	DOR pulse width HIGH	10 5 4	47 17 14	145 29 25	8 4 3	180 36 31	8 4 3	220 44 38	ns	2.0 4.5 6.0	Fig.10
t_W	$\overline{MR}$ pulse width LOW	70 14 12	22 8 6		90 18 15		105 21 18		ns	2.0 4.5 6.0	Fig.8
t_{rem}	removal time $\overline{MR}$ to SI	80 16 14	24 8 7		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig.15
t_{su}	set-up time D_n to SI	−35 −7 −6	−36 −13 −10		−45 −9 −8		−55 −11 −9		ns	2.0 4.5 6.0	Fig.13
t_h	hold time D_n to SI	135 27 23	44 16 13		170 34 29		205 41 35		ns	2.0 4.5 6.0	Fig.13
f_{max}	maximum clock pulse frequency SI, $\overline{SO}$ burst mode		9.9 30 36		2.8 14 16		2.4 12 14		MHz	2.0 4.5 6.0	Figs 11 and 12
f_{max}	maximum clock pulse frequency SI, $\overline{SO}$ using flags		9.9 30 36		2.8 14 16		2.4 12 14		MHz	2.0 4.5 6.0	Figs 6 and 9
f_{max}	maximum clock pulse frequency SI, $\overline{SO}$ cascaded		7.6 23 27		2.2 11 13		1.8 9.2 11		MHz	2.0 4.5 6.0	Figs 6 and 9

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see *"74HC/HCT/HCU/HCMOS Logic Family Specifications"*.

Output capability: standard
I_{CC} category: LSI

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications. To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
$\overline{OE}$	1.00
SI	1.50
D_n	0.75
$\overline{MR}$	1.50
$\overline{SO}$	1.50

AC CHARACTERISTICS FOR 74HCT

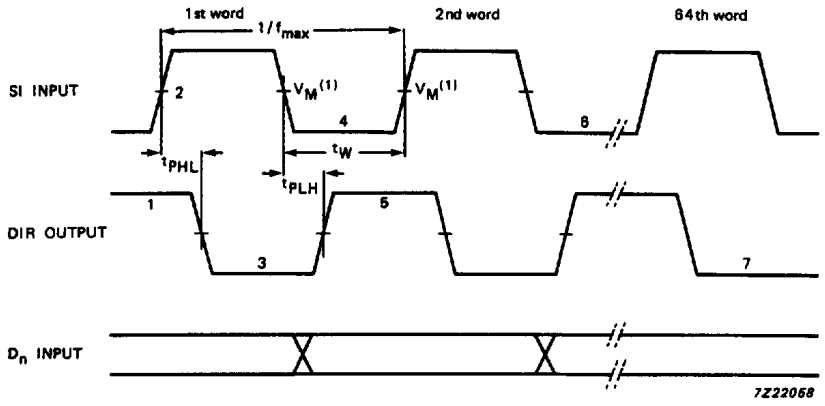
GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HCT								V_{CC} (V)	WAVEFORMS
		+25			–40 to +85		–40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/ t_{PLH}	propagation delay $\overline{MR}$ to DIR, DOR		30	51		53		63	ns	4.5	Fig.8
t_{PHL}/ t_{PLH}	propagation delay SI to DIR		29	49		61		74	ns	4.5	Fig.6
t_{PHL}/ t_{PLH}	propagation delay $\overline{SO}$ to DOR		39	67		84		101	ns	4.5	Fig.9
t_{PHL}/ t_{PLH}	propagation delay $\overline{SO}$ to Q_n		46	78		98		117	ns	4.5	Fig.14
t_{PHL}/ t_{PLH}	propagation delay DOR to Q_n		7	12		15		18	ns	4.5	Fig.10
t_{PLH}	propagation delay/ripple through delay SI to DOR		0.9	1.6		2.0		2.4	µs	4.5	Fig.10
t_{PLH}	propagation delay/ bubble-up delay $\overline{SO}$ to DIR		1.2	2.0		2.5		3.0	µs	4.5	Fig.7
t_{PZH}/ t_{PZL}	3-state output enable $\overline{OE}$ to Q_n		20	35		44		53	ns	4.5	Fig.16
t_{PHZ}/ t_{PLZ}	3-state output disable $\overline{OE}$ to Q_n		19	35		44		53	ns	4.5	Fig.16
t_{THL}/ t_{TLH}	output transition time		7	15		19		22	ns	4.5	Fig.14

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HCT								V_{CC} (V)	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_W	SI pulse width HIGH or LOW	12	6		15		18		ns	4.5	Fig.6
t_W	$\overline{SO}$ pulse width HIGH or LOW	15	9		19		22		ns	4.5	Fig.9
t_W	DIR pulse width HIGH	7	22	37	6	46	6	56	ns	4.5	Fig.7
t_W	DOR pulse width HIGH	6	20	35	5	44	5	53	ns	4.5	Fig.10
t_W	$\overline{MR}$ pulse width LOW	18	10		23		27		ns	4.5	Fig.8
t_{rem}	removal time $\overline{MR}$ to SI	18	10		23		27		ns	4.5	Fig.15
t_{su}	set-up time D_n to SI	−5	−16		−4		−4		ns	4.5	Fig.13
t_h	hold time D_n to SI	30	18		38		45		ns	4.5	Fig.13
f_{max}	maximum clock pulse frequency SI, $\overline{SO}$ burst mode	15	26		12		10		MHz	4.5	Figs 11 and 12
f_{max}	maximum clock pulse frequency SI, $\overline{SO}$ using flags	15	26		12		10		MHz	4.5	Figs 6 and 9
f_{max}	maximum clock pulse frequency SI, $\overline{SO}$ cascaded	13	22		10		8.6		MHz	4.5	Figs 6 and 9

AC WAVEFORMS

Shifting in sequence FIFO empty to FIFO full



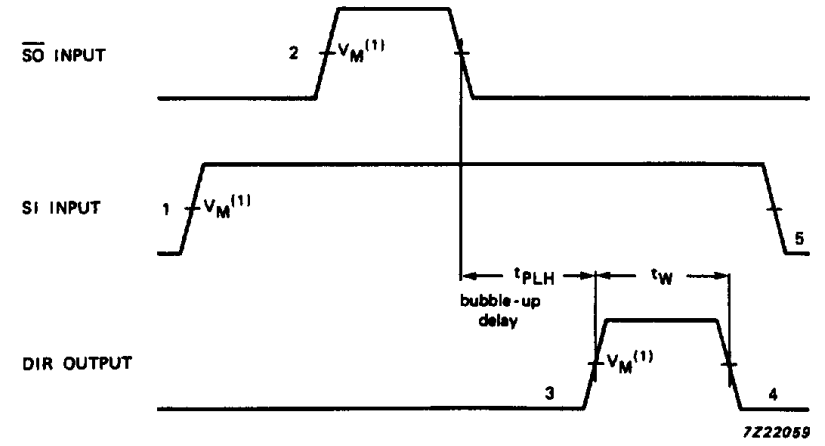
(1) HC : V_M = 50%; V_I = GND to V_{CC}.
HCT: V_M = 1.3 V; V_I = GND to 3 V.

Fig.6 Waveforms showing the SI input to DIR output propagation delay. The SI pulse width and SI maximum pulse frequency.

Notes to Fig.6

1. DIR initially HIGH; FIFO is prepared for valid data.
2. SI set HIGH; data loaded into input stage.
3. DIR drops LOW, input stage “busy”.
4. SI set LOW; data from first location “ripple through”.
5. DIR goes HIGH, status flag indicates FIFO prepared for additional data.
6. Repeat process to load 2nd word through to 64th word into FIFO.
7. DIR remains LOW; with attempt to shift into full FIFO, no data transfer occurs.

With FIFO full; SI held HIGH in anticipation of empty location



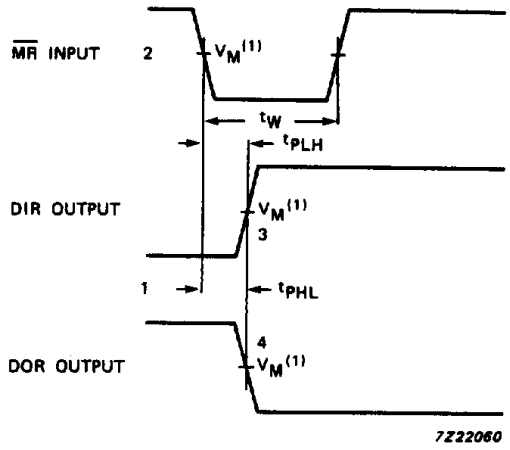
(1) HC : V_M = 50%; V_I = GND to V_{CC}.
HCT: V_M = 1.3 V; V_I = GND to 3 V.

Fig.7 Waveforms showing bubble-up delay, $\overline{SO}$ input to DIR output and DIR output pulse width.

Notes to Fig.7

1. FIFO is initially full, shift-in is held HIGH.
2. $\overline{SO}$ pulse; data in the output stage is unloaded, “bubble-up process of empty locations begins”.
3. DIR HIGH; when empty location reached input stage, flag indicates FIFO is prepared for data input.
4. DIR returns to LOW; FIFO is full again.
5. SI brought LOW; necessary to complete shift-in process, DIR remains LOW, because FIFO is full.

Master reset applied with FIFO full



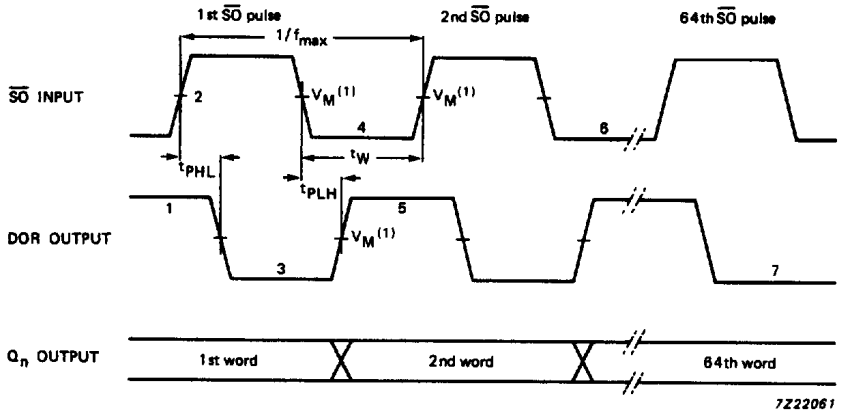
(1) HC : V_M = 50%; V_I = GND to V_{CC}.
HCT: V_M = 1.3 V; V_I = GND to 3 V.

Fig.8 Waveforms showing the $\overline{MR}$ input to DIR, DOR output propagation delays and the $\overline{MR}$ pulse width.

Notes to Fig.8

1. DIR LOW, output ready HIGH; assume FIFO is full.
2. $\overline{MR}$ pulse LOW; clears FIFO.
3. DIR goes HIGH; flag indicates input prepared for valid data.
4. DOR drops LOW; flag indicates FIFO empty.

Shifting out sequence; FIFO full to FIFO empty



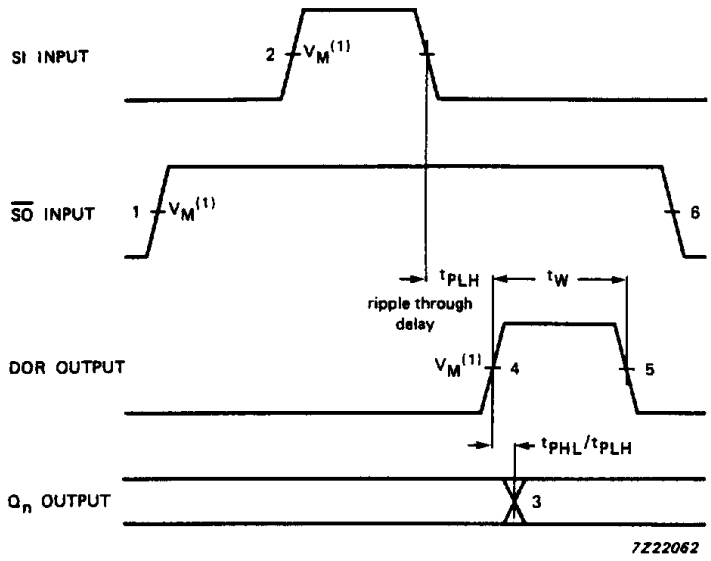
(1) HC : V_M = 50%; V_I = GND to V_{CC}.
HCT: V_M = 1.3 V; V_I = GND to 3 V.

Fig.9 Waveforms showing the $\overline{SO}$ input to DIR output propagation delay. The $\overline{SO}$ pulse width and $\overline{SO}$ maximum pulse frequency.

Notes to Fig.9

1. DOR HIGH; no data transfer in progress, valid data is present at output stage.
2. $\overline{SO}$ set HIGH; results in DOR going LOW.
3. DOR drops LOW; output stage “busy”.
4. $\overline{SO}$ is set LOW; data in the input stage is unloaded, and new data replaces it as empty location “bubbles-up” to input stage.
5. DOR goes HIGH; transfer process completed, valid data present at output after the specified propagation delay.
6. Repeat process to unload the 3rd through to the 64th word from FIFO.
7. DOR remains LOW; FIFO is empty.

With FIFO empty; $\overline{SO}$ is held HIGH in anticipation



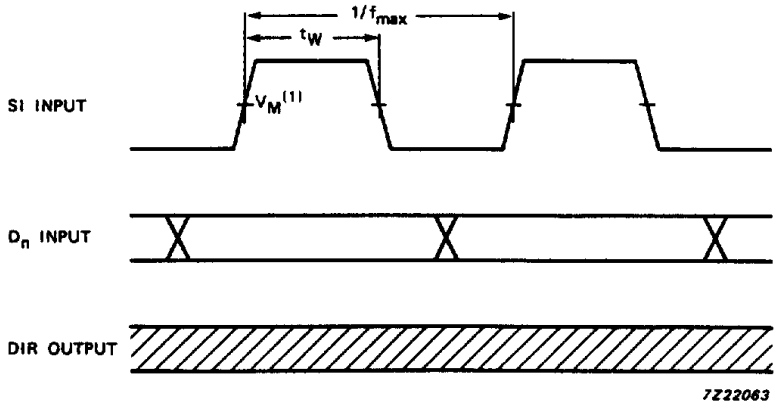
(1) HC : V_M = 50%; V_I = GND to V_{CC}.
HCT: V_M = 1.3 V; V_I = GND to 3 V.

Fig.10 Waveforms showing ripple through delay SI input to DOR output, DOR output pulse width and propagation delay from the DOR pulse to the Q_n output.

Notes to Fig.10

1. FIFO is initially empty, $\overline{SO}$ is held HIGH.
2. SI pulse; loads data into FIFO and initiates ripple through process.
3. DOR flag signals the arrival of valid data at the output stage.
4. Output transition; data arrives at output stage after the specified propagation delay between the rising edge of the DOR pulse to the Q_n output.
5. DOR goes LOW; FIFO is empty again.
6. SO set LOW; necessary to complete shift-out process. DOR remains LOW, because FIFO is empty.

Shift-in operation; high-speed burst mode

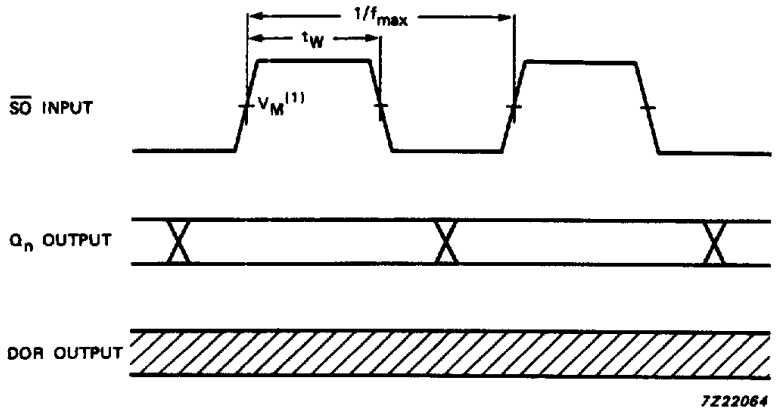


In the high-speed mode, the burst-in rate is determined by the minimum shift-in HIGH and shift-in LOW specifications. The DIR status flag is a don't care condition, and a shift-in pulse can be applied regardless of the flag. A SI pulse which would overflow the storage capacity of the FIFO is ignored.

(1) HC : V_M = 50%; V_I = GND to V_{CC}.
HCT: V_M = 1.3 V; V_I = GND to 3 V.

Fig.11 Waveforms showing SI minimum pulse width and SI maximum pulse frequency, in high-speed shift-in burst mode.

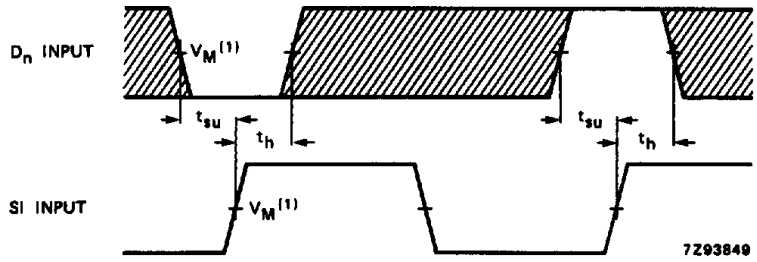
Shift-out operation; high-speed burst mode



In the high-speed mode, the burst-out rate is determined by the minimum shift-out HIGH and shift-out LOW specifications. The DOR flag is a don't care condition and a $\overline{SO}$ pulse can be applied without regard to the flag.

(1) HC : V_M = 50%; V_I = GND to V_{CC}.
HCT: V_M = 1.3 V; V_I = GND to 3 V.

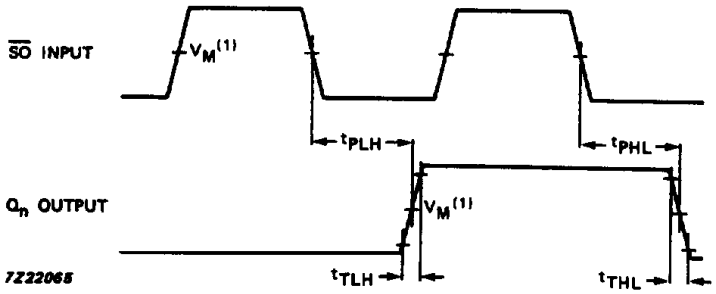
Fig.12 Waveforms showing $\overline{SO}$ minimum pulse width and maximum pulse frequency, in high-speed shift-out burst mode.



The shaded areas indicate when the input is permitted to change for predictable output performance.

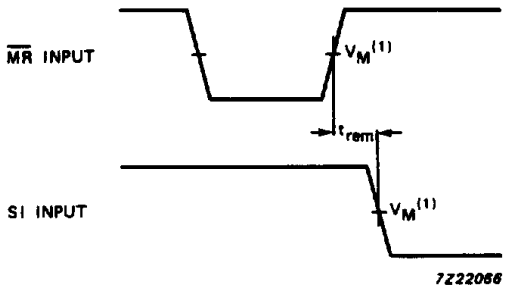
(1) HC : V_M = 50%; V_I = GND to V_{CC}.
HCT: V_M = 1.3 V; V_I = GND to 3 V.

Fig.13 Waveforms showing hold and set-up times for D_n input to SI input.



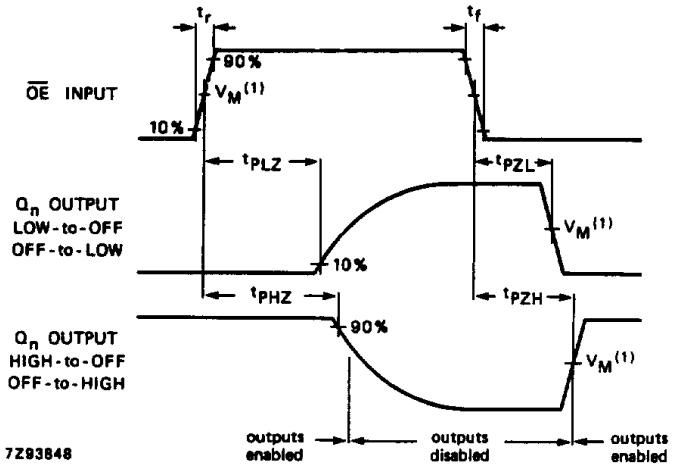
(1) HC : V_M = 50%; V_I = GND to V_{CC}.
HCT: V_M = 1.3 V; V_I = GND to 3 V.

Fig.14 Waveforms showing $\overline{SO}$ input to Q_n output propagation delays and output transition time.



(1) HC : V_M = 50%; V_I = GND to V_{CC}.
HCT: V_M = 1.3 V; V_I = GND to 3 V.

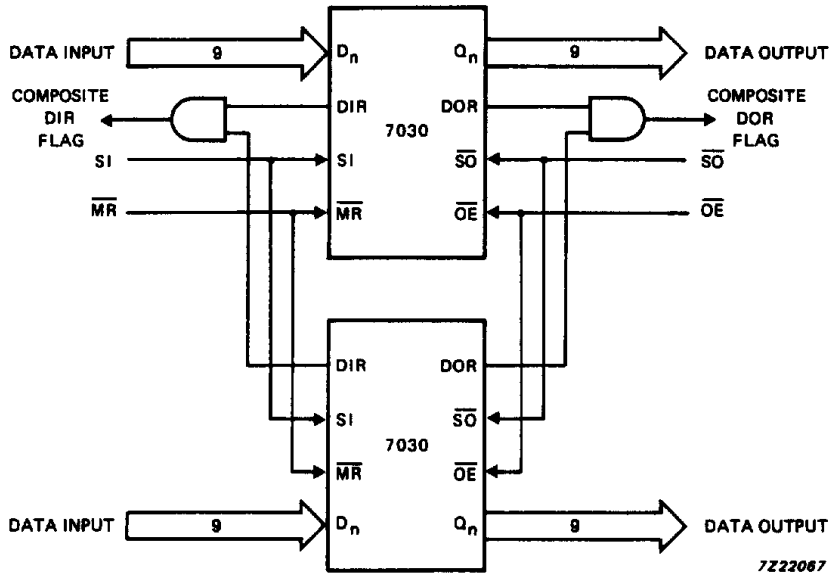
Fig.15 Waveforms showing the $\overline{MR}$ input to SI input removal time.



(1) HC : V_M = 50%; V_I = GND to V_{CC}.
HCT: V_M = 1.3 V; V_I = GND to 3 V.

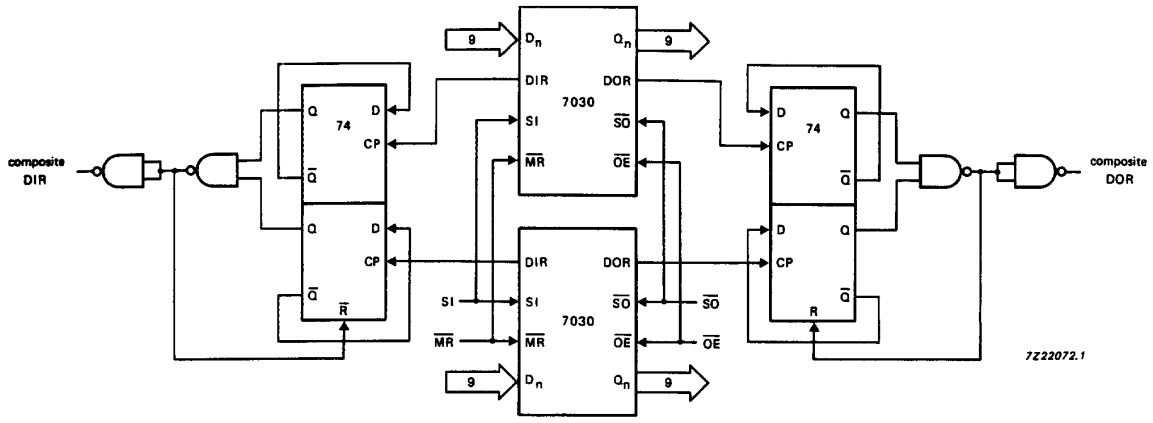
Fig.16 Waveforms showing the 3-state enable and disable times for input $\overline{OE}$.

APPLICATION INFORMATION



The PC74HC/HCT7030 is easily expanded to increase word length. Composite DIR and DOR flags are formed with the addition of an AND gate. The basic operation and timing are identical to a single FIFO, with the exception of an added gate delay on the flags.

Fig.17 Expanded FIFO for increased word length; 64 words $\times$ 18 bits.

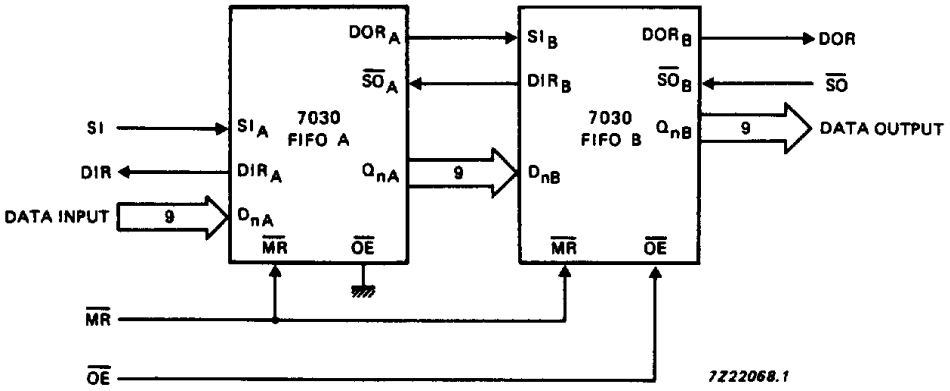


This circuit is only required if the SI input is constantly held HIGH, when the FIFO is empty and the automatic shift-in cycles are started or if $\overline{SO}$ output is constantly held HIGH, when the FIFO is full and the automatic shift-out cycles are started (see Figs 7 and 10).

Fig.18 Expanded FIFO for increased word length.

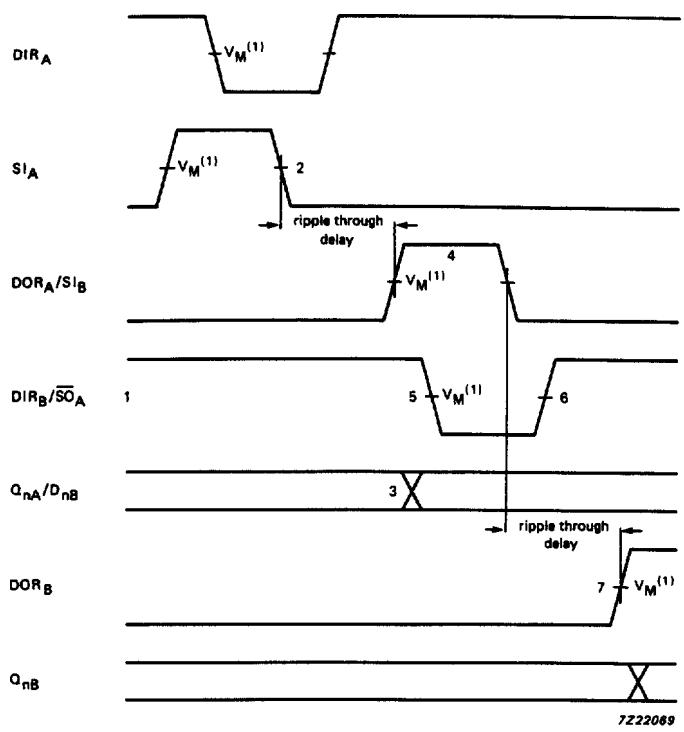
Expanded format

Fig.19 shows two cascaded FIFOs providing a capacity of 128 words × 9 bits.
Fig.20 shows the signals on the nodes of both FIFOs after the application of a SI pulse, when both FIFOs are initially empty. After a rippled through delay, data arrives at the output of $FIFO_A$. Due to $\overline{SO}_A$ being HIGH, a DOR pulse is generated. The requirements of SI_B and D_{nB} are satisfied by the DOR_A pulse width and the timing between the rising edge of DOR_A and Q_{nA}. After a second ripple through delay, data arrives at the output of $FIFO_B$.
Fig.21 shows the signals on the nodes of both FIFOs after the application of a $\overline{SO}_B$ pulse, when both FIFOs are initially full. After a bubble-up delay a DIR_B pulse is generated, which acts as a $\overline{SO}_A$ pulse for $FIFO_A$. One word is transferred from the output of $FIFO_A$ to the input of $FIFO_B$. The requirements of the $\overline{SO}_A$ pulse for $FIFO_A$ is satisfied by the pulse width of DOR_B. After a second bubble-up delay an empty space arrives at D_{nA}, at which time DIR_A goes HIGH.
Fig.22 shows the waveforms at all external nodes of both FIFOs during a complete shift-in and shift-out sequence.



The PC74HC/HCT7030 is easily cascaded to increase word capacity without any external circuitry. In cascaded format, all necessary communications are handled by the FIFOs. Figs 17 to 19 demonstrate the intercommunication timing between $FIFO_A$ and $FIFO_B$. Fig.22 gives an overview of pulses and timing of two cascaded FIFOs, when shifted full and shifted empty again.

Fig.19 Cascading for increased word capacity; 128 words × 9 bits.

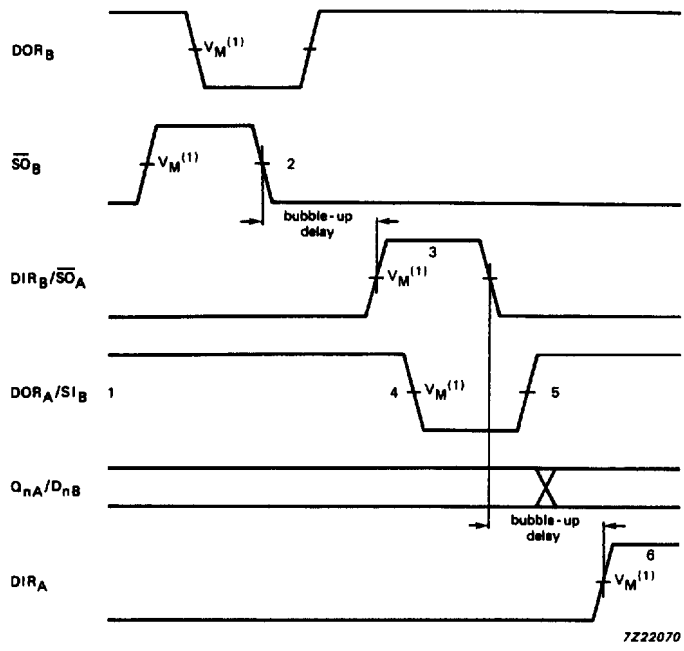


(1) HC : V_M = 50%; V_I = GND to V_{CC}.
HCT: V_M = 1.3 V; V_I = GND to 3 V.

Fig.20 FIFO to FIFO communication; input timing under empty condition.

Notes to Fig.20

1. $FIFO_A$ and $FIFO_B$ initially empty, $\overline{SO}_A$ held HIGH in anticipation of data.
2. Load one word into $FIFO_A$; SI pulse applied, results in DIR pulse.
3. Data out $_A$/data in $_B$ transition; valid data arrives at $FIFO_A$ output stage after a specified delay of the DOR flag, meeting data input set-up requirements of $FIFO_B$.
4. DOR_A and SI_B pulse HIGH; (ripple through delay after SI_A LOW) data is unloaded from $FIFO_A$ as a result of the data output ready pulse, data is shifted into $FIFO_B$.
5. DIR_B and $\overline{SO}_A$ go LOW; flag indicates input stage of $FIFO_B$ is busy, shift-out of $FIFO_A$ is complete.
6. DIR_B and $\overline{SO}_A$ go HIGH automatically; the input stage of $FIFO_B$ is again able to receive data, $\overline{SO}$ is held HIGH in anticipation of additional data.
7. DOR_B goes HIGH; (ripple through delay after SI_B LOW) valid data is present one propagation delay later at the $FIFO_B$ output stage.

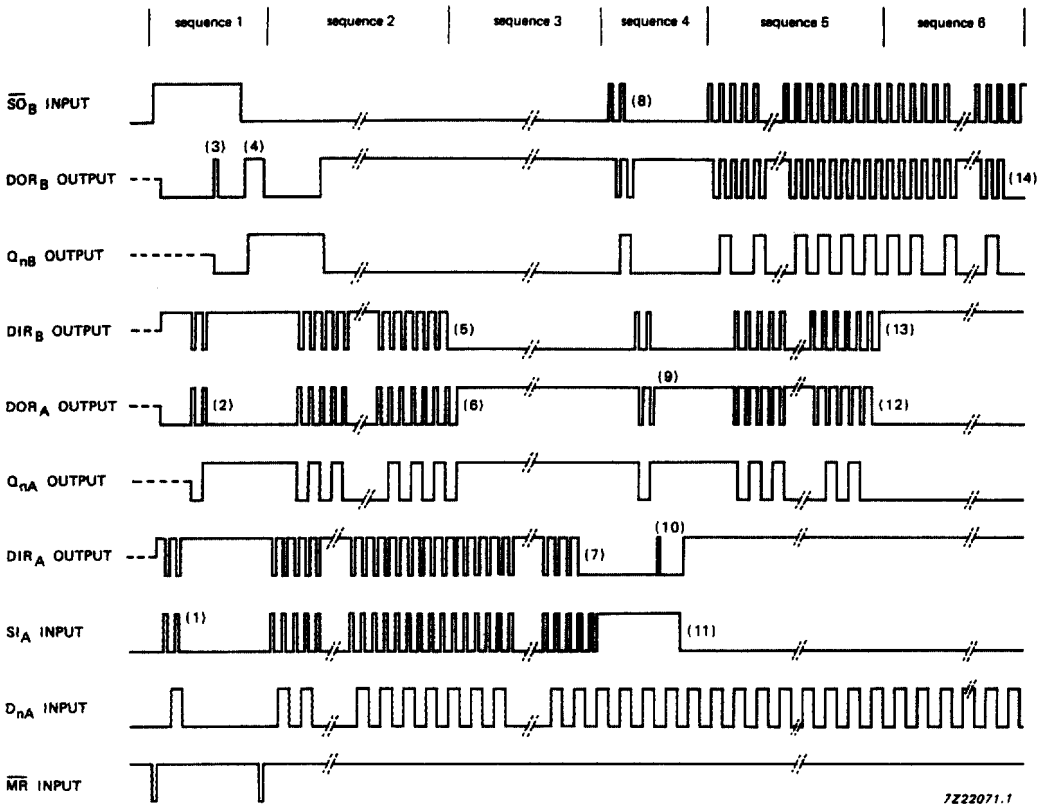


(1) HC : V_M = 50%; V_I = GND to V_{CC}.
HCT: V_M = 1.3 V; V_I = GND to 3 V.

Fig.21 FIFO to FIFO communication; output timing under full condition.

Notes to Fig.21

1. $FIFO_A$ and $FIFO_B$ initially full, SI_B held HIGH in anticipation of shifting in new data as empty location bubbles-up.
2. Unload one word from $FIFO_B$; $\overline{SO}$ pulse applied, results in DOR pulse.
3. DIR_B and $\overline{SO}_A$ pulse HIGH; (bubble-up delay after $\overline{SO}_B$ LOW) data is loaded into $FIFO_B$ as a result of the DIR pulse, data is shifted out of $FIFO_A$.
4. DOR_A and SI_B go LOW; flag indicates the output stage of $FIFO_A$ is busy, shift-in to $FIFO_B$ is complete.
5. DOR_A and SI_B go HIGH; flag indicates valid data is again available at $FIFO_A$ output stage, SI_B is held HIGH, awaiting bubble-up of empty location.
6. DIR_A goes HIGH; (bubble-up delay after $\overline{SO}_A$ LOW) an empty location is present at input stage of $FIFO_A$.



Sequence 1 (Both FIFOs empty, starting shift-in process):
After a $\overline{MR}$ pulse has been applied $FIFO_A$ and $FIFO_B$ are empty. The DOR flags of $FIFO_A$ and $FIFO_B$ go LOW due to no valid data being present at the outputs. The DIR flags are set HIGH due to the FIFOs being ready to accept data. $\overline{SO}_B$ is held HIGH and two SI_A pulses are applied (1). These pulses allow two data words to ripple through to the output stage of $FIFO_A$ and to the input stage of $FIFO_B$ (2). When data arrives at the output of $FIFO_B$, a DOR_B pulse is generated (3). When $\overline{SO}_B$ goes LOW, the first bit is shifted out and a second bit ripples through to the output after which DOR_B goes HIGH (4).

Sequence 2 ($FIFO_B$ runs full):
After the $\overline{MR}$ pulse, a series of 64 SI pulses are applied. When 64 words are shifted in, DIR_B remains LOW due to $FIFO_B$ being full (5). DOR_A goes LOW due to $FIFO_A$ being empty.

Sequence 3 ($FIFO_A$ runs full):
When 65 words are shifted in, DOR_A remains HIGH due to valid data remaining at the output of $FIFO_A$. Q_{nA} remains HIGH, being the polarity of the 65th data word (6). After the 128th SI pulse, DIR remains LOW and both FIFOs are full (7). Additional pulses have no effect.

Sequence 4 (Both FIFOs full, starting shift-out process):
SI_A is held HIGH and two $\overline{SO}_B$ pulses are applied (8). These pulses shift out two words and thus allow two empty locations to bubble-up to the input stage of $FIFO_B$, and proceed to $FIFO_A$ (9). When the first empty location arrives at the input of $FIFO_A$, a DIR_A pulse is generated (10) and a new word is shifted into $FIFO_A$. SI_A is made LOW and now the second empty location reaches the input stage of $FIFO_A$, after which DIR_A remains HIGH (11).

Sequence 5 ($FIFO_A$ runs empty):
At the start of sequence 5 $FIFO_A$ contains 63 valid words due to two words being shifted out and one word being shifted in in sequence 4. An additional series of $\overline{SO}_B$ pulses are applied. After 63 $\overline{SO}_B$ pulses, all words from $FIFO_A$ are shifted into $FIFO_B$. DOR_A remains LOW (12).

Sequence 6 ($FIFO_B$ runs empty):
After the next $\overline{SO}_B$ pulse, DIR_B remains HIGH due to the input stage of $FIFO_B$ being empty (13). After another 63 $\overline{SO}_B$ pulses, DOR_B remains LOW due to both FIFOs being empty (14). Additional $\overline{SO}_B$ pulses have no effect. The last word remains available at the output Q_n.

Fig.22 Waveforms showing the functionality and intercommunication between two FIFOs (refer to Fig.19).

PACKAGE OUTLINES

See *"74HC/HCT/HCU/HCMOS Logic Package Outlines"*.

TradeElectronics.ru

гарантия бесперебойности производства и качества выпускаемой продукции

О компании

ООО "ТрейдЭлектроникс" - это оперативные поставки широкого спектра электронных компонентов отечественного и импортного производства напрямую от производителей и с крупнейших мировых складов. Реализуемая нашей компанией продукция насчитывает более полумиллиона наименований.

Благодаря этому наша компания предлагает к поставке практически не ограниченный ассортимент компонентов как оптовыми, мелкооптовыми партиями, так и в розницу.

Наличие собственной эффективной системы логистики обеспечивает надежную поставку продукции по конкурентным ценам в точно указанные сроки.

Срок поставки со стоков в **Европе и Америке – от 3 до 14 дней.**

Срок поставки из **Азии – от 10 дней.**

Благодаря развитой сети поставщиков, помогаем в поиске и приобретении экзотичных или снятых с производства компонентов.

Предоставляем спец цены на элементы для создания инженерных сэмплов.

Упорный труд, качественный результат дают нам право быть уверенными в себе и надежными для наших клиентов.

Наша компания это:

- Гарантия качества поставляемой продукции
- Широкий ассортимент
- Минимальные сроки поставок
- Техническая поддержка
- Подбор комплектации
- Индивидуальный подход
- Гибкое ценообразование

Наша организация особенно сильна в поставках модулей, микросхем, пассивных компонентов, ксайленсах (XC), EPF, EPM и силовой электроники.

Большой выбор предлагаемой продукции, различные виды оплаты и доставки, позволят Вам сэкономить время и получить максимум выгоды от сотрудничества с нами!

Trade Electronics.ru

гарантия бесперебойности производства и качества выпускаемой продукции

Перечень производителей, продукцию которых мы поставляем на российский рынок

Trade Electronics.ru

гарантия бесперебойности производства и качества выпускаемой продукции

С удовольствием будем прорабатывать для Вас поставки всех необходимых компонентов по текущим запросам для скорейшего выявления групп элементов, по которым сотрудничество именно с нашей компанией будет для Вас максимально выгодным!

С уважением,

Менеджер отдела продаж ООО

«Трейд Электроникс»

Шишлаков Евгений

8 (495)668-30-28 доб 169

manager28@tradeelectronics.ru

http://www.tradeelectronics.ru/