

## TENTATIVE

## TOSHIBA MOS DIGITAL INTEGRATED CIRCUIT SILICON GATE CMOS

131,072-WORD BY 8-BIT STATIC RAM

## DESCRIPTION

The TC551001CPI/CFI/CFTI/CTRI/CSTI/CSRI is a 1,048,576-bit static random access memory (SRAM) organized as 131,072 words by 8 bits. Fabricated using Toshiba's CMOS Silicon gate process technology, this device operates from a single  $5\text{ V} \pm 10\%$  power supply. Advanced circuit technology provides both high speed and low power at an operating current of  $5\text{ mA/MHz}$  (typ) and a minimum cycle time of  $70\text{ ns}$ . It is automatically placed in low-power mode at  $1\text{ }\mu\text{A}$  standby current (typ) when chip enable (CE1) is asserted high or (CE2) is asserted low. There are three control inputs. CE1 and CE2 are used to select the device and for data retention control, and output enable (OE) provides fast memory access. This device is well suited to various microprocessor system applications where high speed, low power and battery backup are required. And, with a guaranteed operating range of  $-40^\circ$  to  $85^\circ\text{C}$ , the TC551001CPI/CFI/CFTI/CTRI/CSTI/CSRI can be used in environments exhibiting extreme temperature conditions. The TC551001CPI/CFI/CFTI/CTRI/CSTI/CSRI is available in a standard plastic 32-pin dual-in-line package (DIP), plastic 32-pin small-outline package (SOP) and normal and reverse pinout plastic 32-pin thin-small-outline package (TSOP).

## FEATURES

- Low-power dissipation  
Operating:  $27.5\text{ mW/MHz}$  (typical)
- Single power supply voltage of  $5\text{ V} \pm 10\%$
- Power down features using CE1 and CE2.
- Data retention supply voltage of 2 to 5.5 V
- Direct TTL compatibility for all inputs and outputs
- Wide operating temperature range of  $-40^\circ$  to  $85^\circ\text{C}$

- Standby Current (maximum) :

|      | TC551001CPI/CFI/CFTI/CTRI/CSTI/CSRI |                         |
|------|-------------------------------------|-------------------------|
|      | -70, -85                            | -70L, -85L              |
| 5.5V | $200\text{ }\mu\text{A}$            | $40\text{ }\mu\text{A}$ |
| 3.0V | $100\text{ }\mu\text{A}$            | $20\text{ }\mu\text{A}$ |

- Access Times (maximum):

|                 | TC551001CPI/CFI/CFTI/CTRI/CSTI/CSRI |                |
|-----------------|-------------------------------------|----------------|
|                 | -70, -70L                           | -85, -85L      |
| Access Time     | $70\text{ ns}$                      | $85\text{ ns}$ |
| CE1 Access Time | $70\text{ ns}$                      | $85\text{ ns}$ |
| CE2 Access Time | $70\text{ ns}$                      | $85\text{ ns}$ |
| OE Access Time  | $35\text{ ns}$                      | $45\text{ ns}$ |

- Packages:

|                               |                      |
|-------------------------------|----------------------|
| DIP32-P-600-2.54 (CPI)        | (Weight: 4.45 g typ) |
| SOP32-P-525-1.27 (CFI)        | (Weight: 1.04 g typ) |
| TSOP I 32-P-0820-0.50 (CFTI)  | (Weight: 0.34 g typ) |
| TSOP I 32-P-0820-0.50A (CTRI) | (Weight: 0.34 g typ) |
| TSOP I 32-P-0.50 (CSTI)       | (Weight: 0.24 g typ) |
| TSOP I 32-P-0.50A (CSRI)      | (Weight: 0.24 g typ) |

## PIN ASSIGNMENT (TOP VIEW)

## ○ 32 PIN DIP &amp; SOP

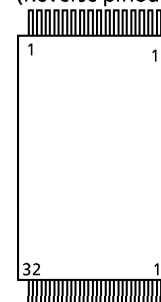
|      |    |    |                 |
|------|----|----|-----------------|
| NC   | 1  | 32 | V <sub>DD</sub> |
| A16  | 2  | 31 | A15             |
| A14  | 3  | 30 | CE2             |
| A12  | 4  | 29 | R/W             |
| A7   | 5  | 28 | A13             |
| A6   | 6  | 27 | A8              |
| A5   | 7  | 26 | A9              |
| A4   | 8  | 25 | A11             |
| A3   | 9  | 24 | OE              |
| A2   | 10 | 23 | A10             |
| A1   | 11 | 22 | CE1             |
| A0   | 12 | 21 | I/O8            |
| I/O1 | 13 | 20 | I/O7            |
| I/O2 | 14 | 19 | I/O6            |
| I/O3 | 15 | 18 | I/O5            |
| GND  | 16 | 17 | I/O4            |

## ○ 32 PIN TSOP

(Normal pinout)



(Reverse pinout)



## PIN NAMES

|                 |                    |
|-----------------|--------------------|
| A0 to A16       | Address Inputs     |
| R/W             | Read/Write Control |
| OE              | Output Enable      |
| CE1, CE2        | Chip Enable        |
| I/O1 to I/O8    | Data Input/Output  |
| V <sub>DD</sub> | Power (+ 5 V)      |
| GND             | Ground             |
| NC              | No Connection      |

|          |                 |                |                |                 |      |      |                 |                 |      |                 |                 |                 |                |                |                 |                |
|----------|-----------------|----------------|----------------|-----------------|------|------|-----------------|-----------------|------|-----------------|-----------------|-----------------|----------------|----------------|-----------------|----------------|
| Pin No.  | 1               | 2              | 3              | 4               | 5    | 6    | 7               | 8               | 9    | 10              | 11              | 12              | 13             | 14             | 15              | 16             |
| Pin Name | A <sub>11</sub> | A <sub>9</sub> | A <sub>8</sub> | A <sub>13</sub> | R/W  | CE2  | A <sub>15</sub> | V <sub>DD</sub> | NC   | A <sub>16</sub> | A <sub>14</sub> | A <sub>12</sub> | A <sub>7</sub> | A <sub>6</sub> | A <sub>5</sub>  | A <sub>4</sub> |
| Pin No.  | 17              | 18             | 19             | 20              | 21   | 22   | 23              | 24              | 25   | 26              | 27              | 28              | 29             | 30             | 31              | 32             |
| Pin Name | A <sub>3</sub>  | A <sub>2</sub> | A <sub>1</sub> | A <sub>0</sub>  | I/O1 | I/O2 | I/O3            | GND             | I/O4 | I/O5            | I/O6            | I/O7            | I/O8           | CE1            | A <sub>10</sub> | OE             |

961001EBA1

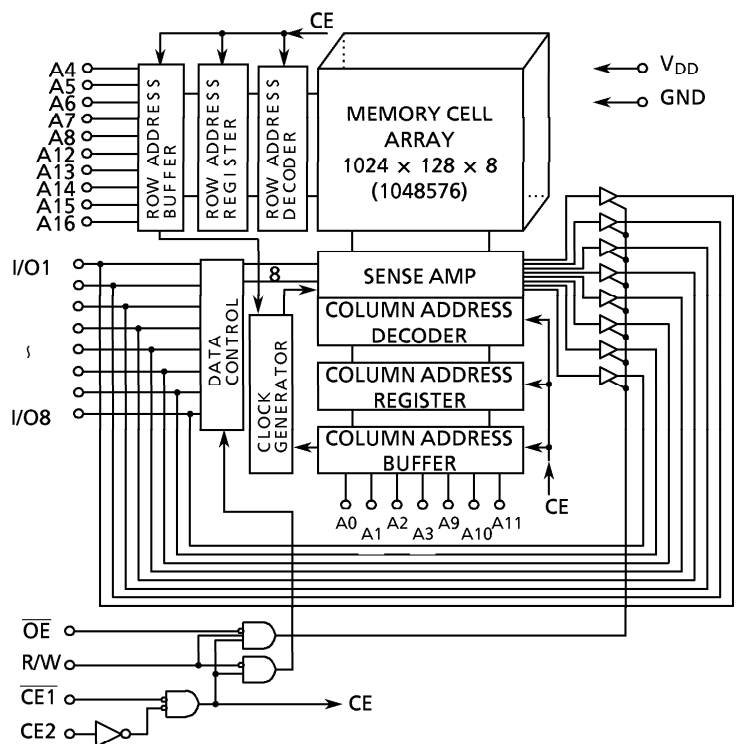
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# BLOCK DIAGRAM



# OPERATION MODE

| MODE             | CE1 | CE2 | OE | R/W | I/O1 to I/O8     | POWER            |
|------------------|-----|-----|----|-----|------------------|------------------|
| Read             | L   | H   | L  | H   | D <sub>OUT</sub> | I <sub>DDO</sub> |
| Write            | L   | H   | x  | L   | D <sub>IN</sub>  | I <sub>DDO</sub> |
| Outputs Disabled | L   | H   | H  | H   | High-Z           | I <sub>DDO</sub> |
| Standby          | H   | x   | x  | x   | High-Z           | I <sub>DDS</sub> |
|                  | x   | L   | x  | x   | High-Z           | I <sub>DDS</sub> |

Note: x = don't care. H = logic high. L = logic low.

# ABSOLUTE MAXIMUM RATINGS

| SYMBOL              | RATING                       | VALUE                          | UNIT |
|---------------------|------------------------------|--------------------------------|------|
| V <sub>DD</sub>     | Power Supply Voltage         | - 0.3 to 7.0                   | V    |
| V <sub>IN</sub>     | Input Voltage                | - 0.3* to 7.0                  | V    |
| V <sub>IO</sub>     | Input and Output Voltage     | - 0.5 to V <sub>DD</sub> + 0.5 | V    |
| P <sub>D</sub>      | Power Dissipation            | 1.0/0.6**                      | W    |
| T <sub>solder</sub> | Soldering Temperature (10 s) | 260                            | °C   |
| T <sub>strg.</sub>  | Storage Temperature          | - 55 to 150                    | °C   |
| T <sub>opr.</sub>   | Operating Temperature        | - 40 to 85                     | °C   |

\* - 3.0 V when measured at a pulse width of 50 ns

\*\* SOP

DC RECOMMENDED OPERATING CONDITIONS ( $T_a = -40^\circ$  to  $85^\circ\text{C}$ )

| SYMBOL   | PARAMETER                     | MIN      | TYP | MAX            | UNIT |
|----------|-------------------------------|----------|-----|----------------|------|
| $V_{DD}$ | Power Supply Voltage          | 4.5      | 5.0 | 5.5            | V    |
| $V_{IH}$ | Input High Voltage            | 2.4      | –   | $V_{DD} + 0.3$ |      |
| $V_{IL}$ | Input Low Voltage             | $-0.3^*$ | –   | 0.6            |      |
| $V_{DH}$ | Data Retention Supply Voltage | 2.0      | –   | 5.5            |      |

\*  $-3.0\text{ V}$  when measured at a pulse width of 50 nsDC CHARACTERISTICS ( $T_a = -40^\circ$  to  $85^\circ\text{C}$ ,  $V_{DD} = 5\text{ V} \pm 10\%$ )

| SYMBOL                      | PARAMETER              | TEST CONDITION                                                                                                                                                                 |                   |                   | MIN   | TYP | MAX   | UNIT |    |
|-----------------------------|------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------------------|-------------------|-------|-----|-------|------|----|
| I <sub>IL</sub>             | Input Leakage Current  | V <sub>IN</sub> = 0 V to V <sub>DD</sub>                                                                                                                                       |                   |                   | –     | –   | ± 1.0 | μA   |    |
| I <sub>OH</sub>             | Output High Current    | V <sub>OH</sub> = 2.4 V                                                                                                                                                        |                   |                   | – 1.0 | –   | –     | mA   |    |
| I <sub>OL</sub>             | Output Low Current     | V <sub>OL</sub> = 0.4 V                                                                                                                                                        |                   |                   | 4.0   | –   | –     | mA   |    |
| I <sub>LO</sub>             | Output Leakage Current | $\overline{CE1} = V_{IH}$ or CE2 = V <sub>IL</sub> or R/W = V <sub>IL</sub> or<br>$\overline{OE} = V_{IH}$ , V <sub>OUT</sub> = 0 V to V <sub>DD</sub>                         |                   |                   | –     | –   | ± 1.0 | μA   |    |
| I <sub>DDO1</sub>           | Operating Current      | $\overline{CE1} = V_{IL}$ and CE2 = V <sub>IH</sub><br>and R/W = V <sub>IH</sub> ,<br>I <sub>OUT</sub> = 0 mA<br>Other Inputs = V <sub>IH</sub> /V <sub>IL</sub>               |                   | Tcycle            | min   | –   | –     | 70   | mA |
| 1 μs                        |                        |                                                                                                                                                                                |                   |                   | –     | –   | 20    |      |    |
| I <sub>DDO2</sub>           |                        | $\overline{CE1} = 0.2\text{ V}$ and CE2 = V <sub>DD</sub> – 0.2 V<br>R/W = V <sub>DD</sub> – 0.2 V,<br>I <sub>OUT</sub> = 0 mA<br>Other Inputs = V <sub>DD</sub> – 0.2 V/0.2 V |                   | Tcycle            | min   | –   | –     | 60   | mA |
| 1 μs                        |                        |                                                                                                                                                                                |                   |                   | –     | –   | 10    |      |    |
| I <sub>DDS1</sub>           | Standby Current        | $\overline{CE1} = V_{IH}$ or CE2 = V <sub>IL</sub>                                                                                                                             |                   |                   | –     | –   | 3     | mA   |    |
| I <sub>DDS2</sub><br>(Note) |                        | $\overline{CE1} = V_{DD} - 0.2\text{ V}$<br>or CE2 = 0.2 V<br>V <sub>DD</sub> = 2.0 to 5.5 V                                                                                   | -70, -85          | Ta = 25°C         |       | –   | 1     | –    | μA |
|                             |                        |                                                                                                                                                                                |                   | Ta = –40° to 85°C |       | –   | –     | 200  |    |
|                             |                        | -70L, -85L                                                                                                                                                                     | Ta = 25°C         |                   | –     | 1   | 2     |      |    |
|                             |                        |                                                                                                                                                                                | Ta = –40° to 85°C |                   | –     | –   | 40    |      |    |

Note: In standby mode with  $\overline{CE1} \geq V_{DD} - 0.2\text{ V}$ , these limits are assured for the condition  $CE2 \geq V_{DD} - 0.2\text{ V}$  or  $CE2 \leq 0.2\text{ V}$ .CAPACITANCE ( $T_a = 25^\circ\text{C}$ ,  $f = 1\text{ MHz}$ )

| SYMBOL    | PARAMETER          | TEST CONDITION         | MAX | UNIT |
|-----------|--------------------|------------------------|-----|------|
| $C_{IN}$  | Input Capacitance  | $V_{IN} = \text{GND}$  | 10  | pF   |
| $C_{OUT}$ | Output Capacitance | $V_{OUT} = \text{GND}$ | 10  |      |

Note: This parameter is periodically sampled and is not 100% tested.

**AC CHARACTERISTICS AND OPERATING CONDITIONS** ( $T_a = -40^\circ$  to  $85^\circ\text{C}$ ,  $V_{DD} = 5\text{ V} \pm 10\%$ )

**READ CYCLE**

| SYMBOL           | PARAMETER                           | TC551001CPI/CFI/CFTI/CTRI/CSTI/CSRI |     |           |     | UNIT |
|------------------|-------------------------------------|-------------------------------------|-----|-----------|-----|------|
|                  |                                     | -70, -70L                           |     | -85, -85L |     |      |
|                  |                                     | MIN                                 | MAX | MIN       | MAX |      |
| t <sub>RC</sub>  | Read Cycle Time                     | 70                                  | –   | 85        | –   | ns   |
| t <sub>ACC</sub> | Address Access Time                 | –                                   | 70  | –         | 85  |      |
| t <sub>CO1</sub> | Chip Enable (CE1) Access Time       | –                                   | 70  | –         | 85  |      |
| t <sub>CO2</sub> | Chip Enable (CE2) Access Time       | –                                   | 70  | –         | 85  |      |
| t <sub>OE</sub>  | Output Enable Access Time           | –                                   | 35  | –         | 45  |      |
| t <sub>COE</sub> | Chip Enable Low to Output Active    | 5                                   | –   | 5         | –   |      |
| t <sub>OEE</sub> | Output Enable Low to Output Active  | 0                                   | –   | 0         | –   |      |
| t <sub>OD</sub>  | Chip Enable High to Output High-Z   | –                                   | 30  | –         | 35  |      |
| t <sub>ODO</sub> | Output Enable High to Output High-Z | –                                   | 30  | –         | 35  |      |
| t <sub>OH</sub>  | Output Data Hold Time               | 10                                  | –   | 10        | –   |      |

**WRITE CYCLE**

| SYMBOL           | PARAMETER                   | TC551001CPI/CFI/CFTI/CTRI/CSTI/CSRI |     |           |     | UNIT |
|------------------|-----------------------------|-------------------------------------|-----|-----------|-----|------|
|                  |                             | -70, -70L                           |     | -85, -85L |     |      |
|                  |                             | MIN                                 | MAX | MIN       | MAX |      |
| t <sub>WC</sub>  | Write Cycle Time            | 70                                  | –   | 85        | –   | ns   |
| t <sub>WP</sub>  | Write Pulse Width           | 50                                  | –   | 60        | –   |      |
| t <sub>CW</sub>  | Chip Enable to End of Write | 60                                  | –   | 75        | –   |      |
| t <sub>AS</sub>  | Address Setup Time          | 0                                   | –   | 0         | –   |      |
| t <sub>WR</sub>  | Write Recovery Time         | 0                                   | –   | 0         | –   |      |
| t <sub>ODW</sub> | R/W Low to Output High-Z    | –                                   | 30  | –         | 35  |      |
| t <sub>OEW</sub> | R/W High to Output Active   | 0                                   | –   | 0         | –   |      |
| t <sub>DS</sub>  | Data Setup Time             | 30                                  | –   | 35        | –   |      |
| t <sub>DH</sub>  | Data Hold Time              | 0                                   | –   | 0         | –   |      |

**AC TEST CONDITIONS**

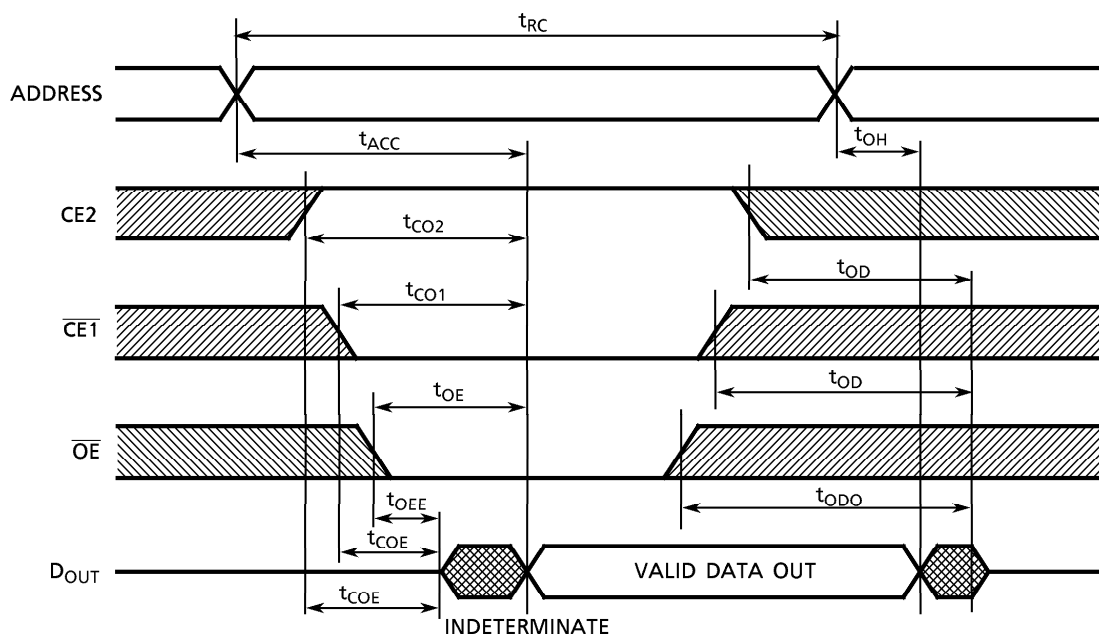
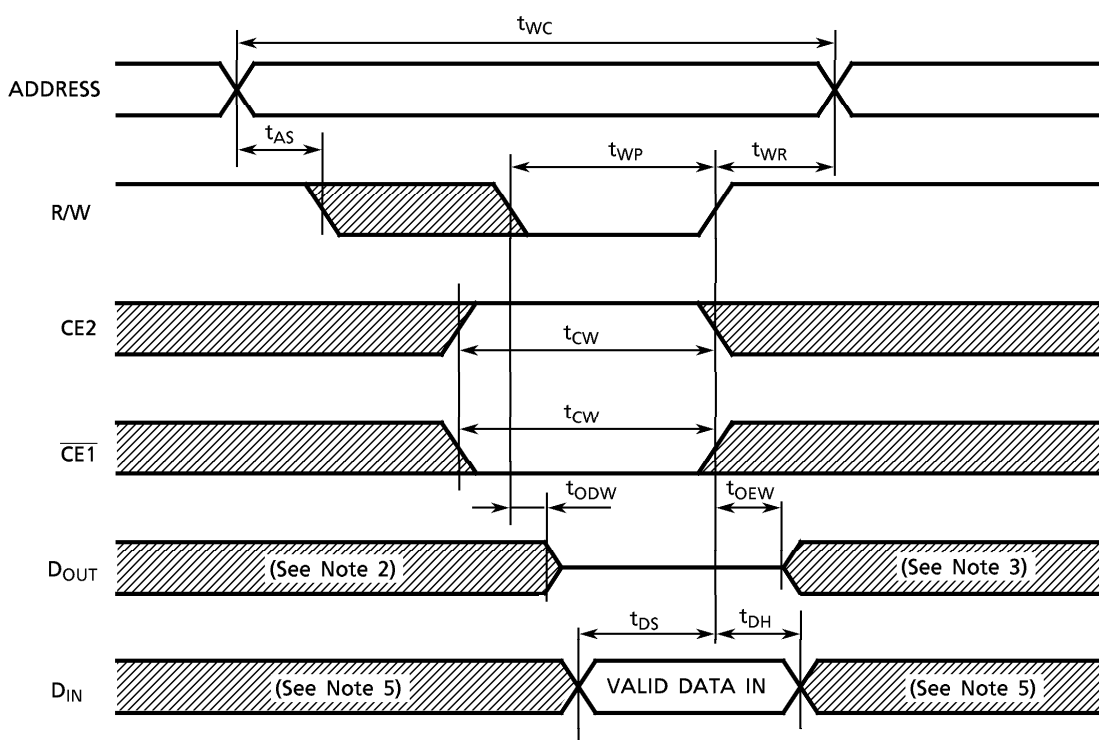
Output load: 100 pF + one TTL gate

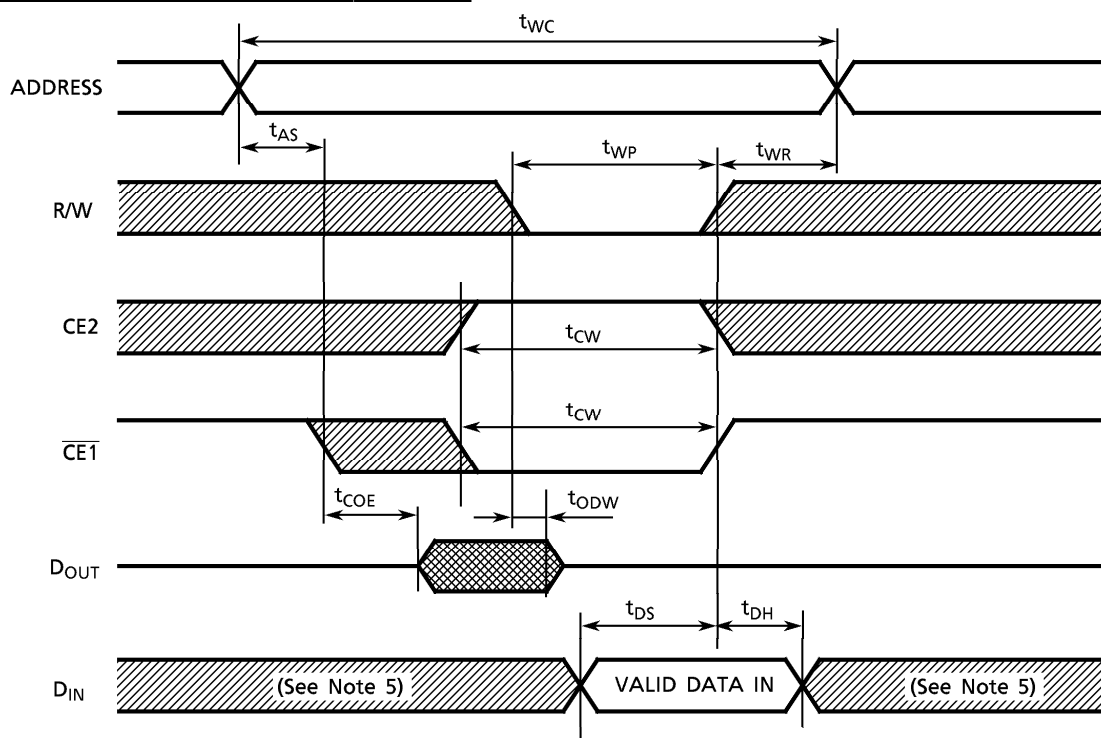
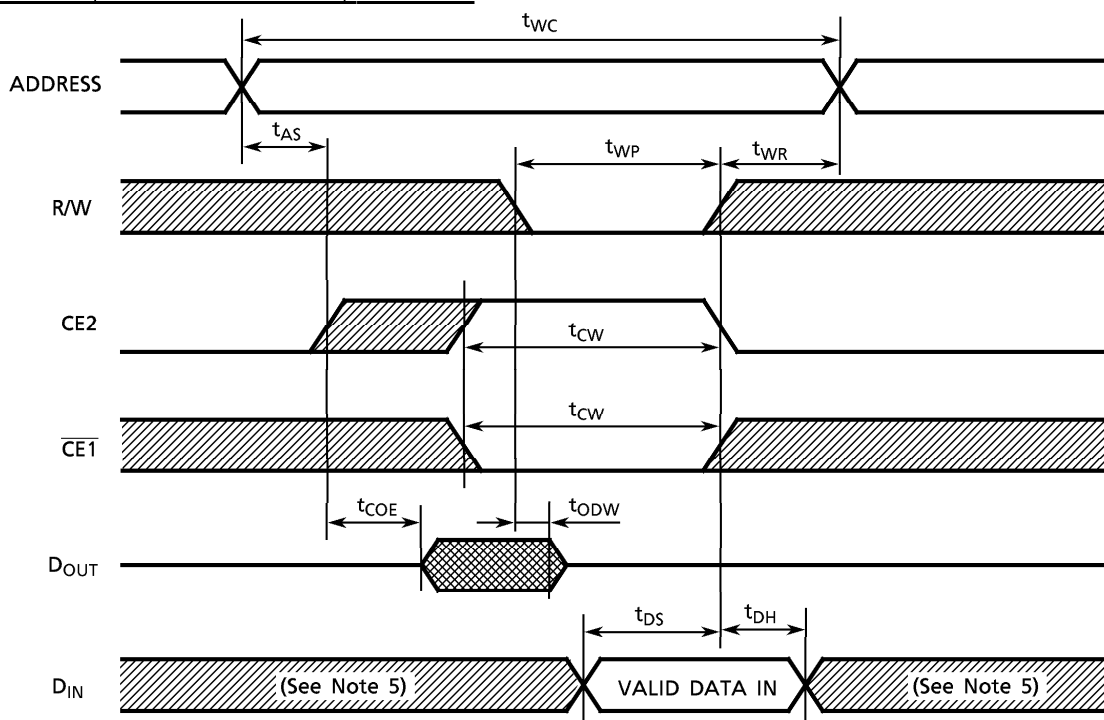
Input pulse level: 0.4 V, 2.6 V

Timing measurements: 1.5 V

Reference level: 1.5 V

$t_R$ ,  $t_F$ : 5 ns

**TIMING DIAGRAMS**
**READ CYCLE (See Note 1)**

**WRITE CYCLE 1 (R/W CONTROLLED) (See Note 4)**


**WRITE CYCLE 2 ( $\overline{\text{CE1}}$  CONTROLLED) (See Note 4)**

**WRITE CYCLE 3 (CE2 CONTROLLED) (See Note 4)**


Note: (1) R/W remains HIGH for the read cycle.

(2) If  $\overline{\text{CE1}}$  goes LOW (or CE2 goes HIGH) coincident with or after R/W goes LOW, the outputs will remain at high impedance.

(3) If  $\overline{\text{CE1}}$  goes HIGH (or CE2 goes LOW) coincident with or before R/W goes HIGH, the outputs will remain at high impedance.

(4) If  $\overline{\text{OE}}$  is HIGH during the write cycle, the outputs will remain at high impedance.

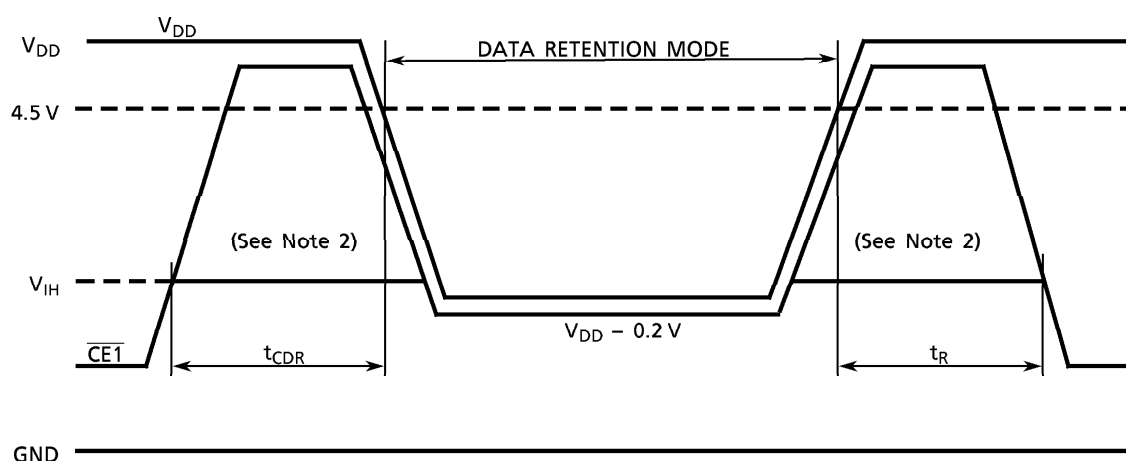
(5) Because I/O signals may be in the output state at this time, input signals of reverse polarity must not be applied.

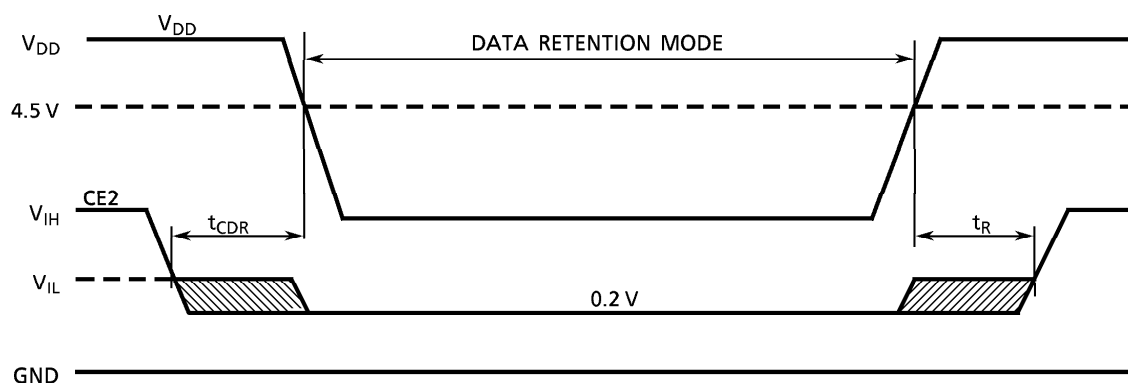
### DATA RETENTION CHARACTERISTICS (Ta = - 40° to 85°C)

| SYMBOL            | PARAMETER                                 |            |                         | MIN | TYP | MAX | UNIT |
|-------------------|-------------------------------------------|------------|-------------------------|-----|-----|-----|------|
| V <sub>DH</sub>   | Data Retention Supply Voltage             |            |                         | 2.0 | –   | 5.5 | V    |
| I <sub>DD52</sub> | Standby Current                           | -70, -85   | V <sub>DH</sub> = 3.0 V | –   | –   | 100 | μA   |
|                   |                                           |            | V <sub>DH</sub> = 5.5 V | –   | –   | 200 |      |
|                   |                                           | -70L, -85L | V <sub>DH</sub> = 3.0 V | –   | –   | 20* |      |
|                   |                                           |            | V <sub>DH</sub> = 5.5 V | –   | –   | 40  |      |
| t <sub>CDR</sub>  | Chip Deselect to Data Retention Mode Time |            |                         | 0   | –   | –   | nS   |
| t <sub>R</sub>    | Recovery Time                             |            |                         | 5   | –   | –   | mS   |

\* 2 μA (max) at Ta = - 40° to 40°C

### $\overline{\text{CE1}}$ CONTROLLED DATA RETENTION MODE (See Note 1)



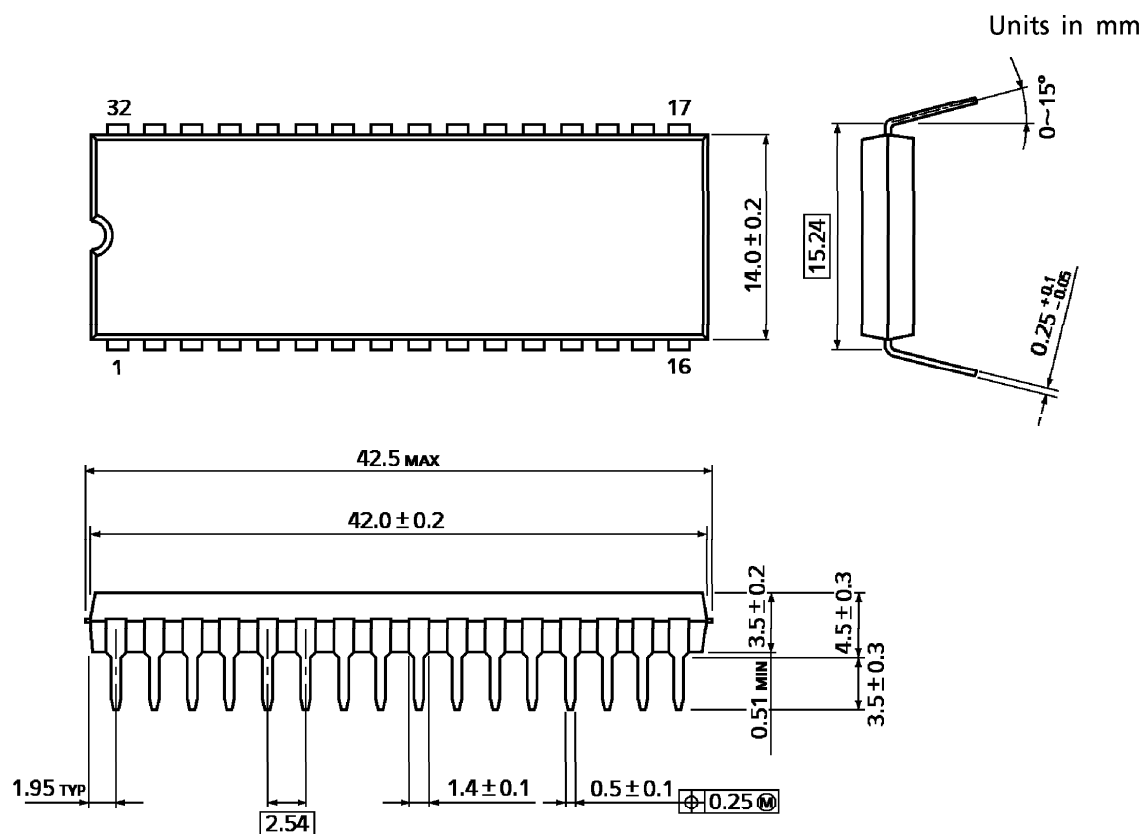
CE2 CONTROLLED DATA RETENTION MODE (See Note 3)

Note: (1) In  $\overline{CE1}$  controlled data retention mode, minimum standby current mode is entered when

$$\overline{CE2} \leq 0.2 \text{ V or } \overline{CE2} \geq V_{DD} - 0.2 \text{ V.}$$

(2) When  $\overline{CE1}$  is operating at the  $V_{IH}$  level (2.4 V), the operation current is given by  $I_{DDSI}$  during the transition of  $V_{DD}$  from 4.5 to 2.6 V.

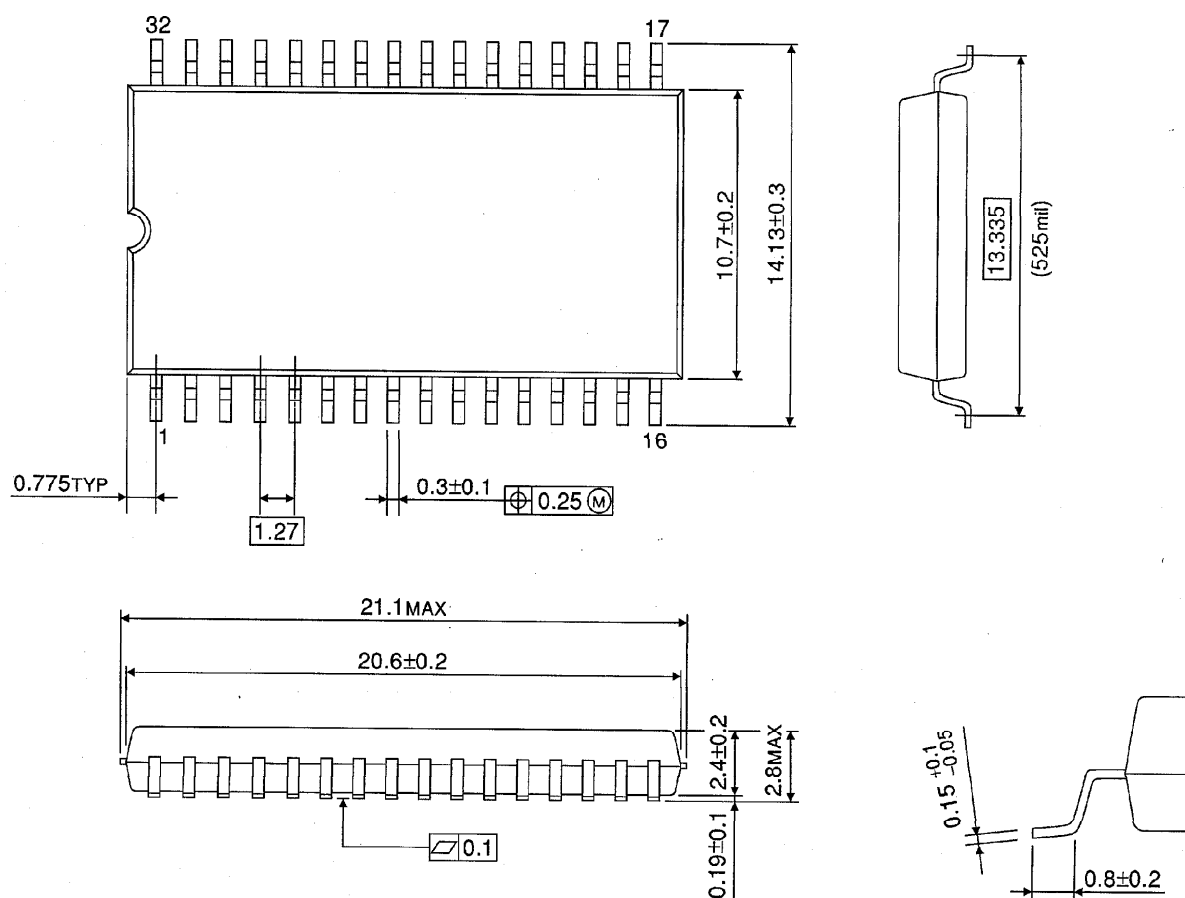
(3) In CE2 controlled data retention mode, minimum standby current mode is entered when  $\overline{CE2} \leq 0.2 \text{ V}$ .

**PACKAGE DIMENSIONS (DIP32-P-600-2.54)**


Weight: 4.45 g (typ)

**PACKAGE DIMENSIONS (SOP32-P-525-1.27)**

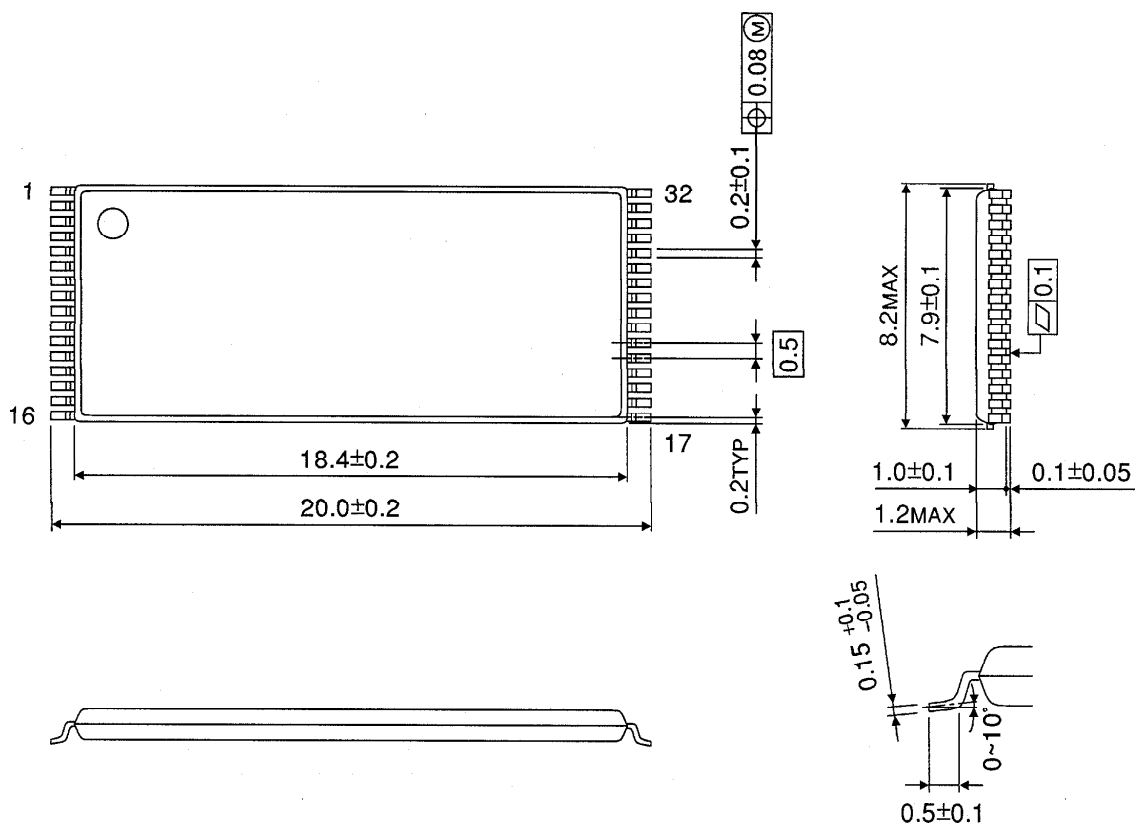
Units in mm



Weight: 1.04 g (typ)

**PACKAGE DIMENSIONS (TSOP I 32-P-0820-0.50)**

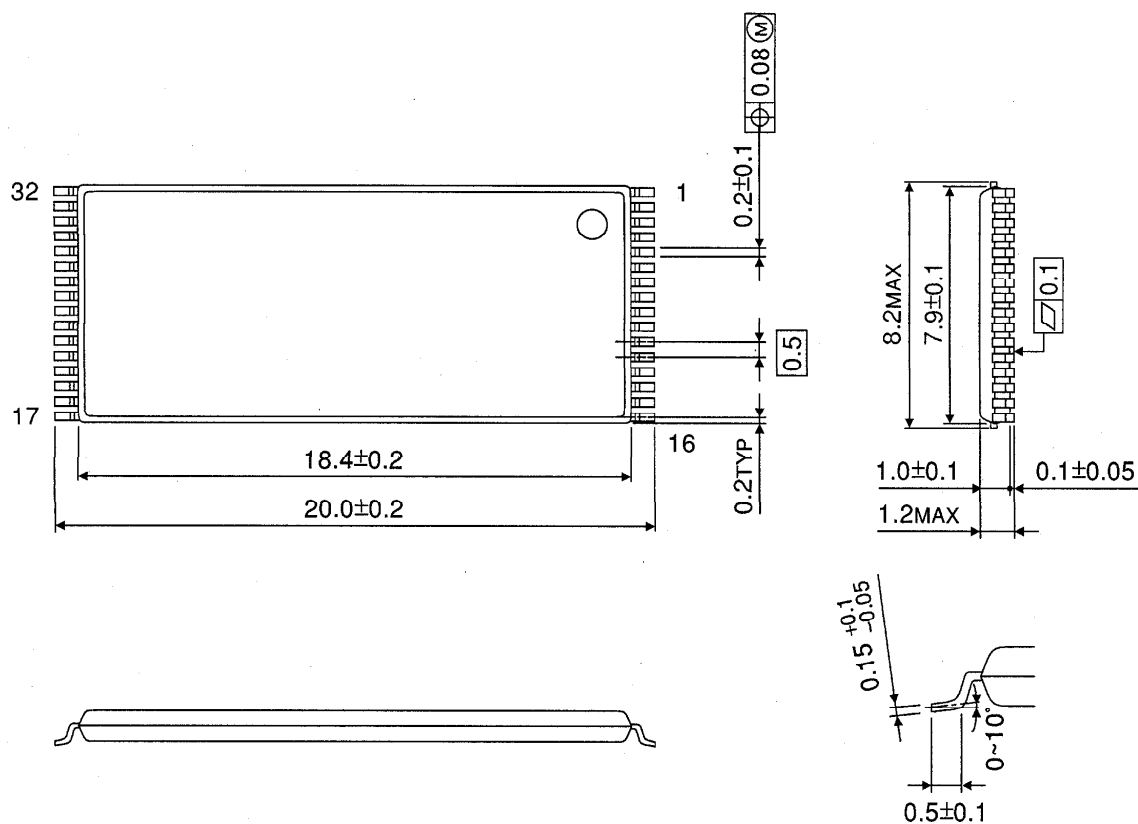
Units in mm



Weight: 0.34 g (typ)

**PACKAGE DIMENSIONS (TSOP I 32-P-0820-0.50A)**

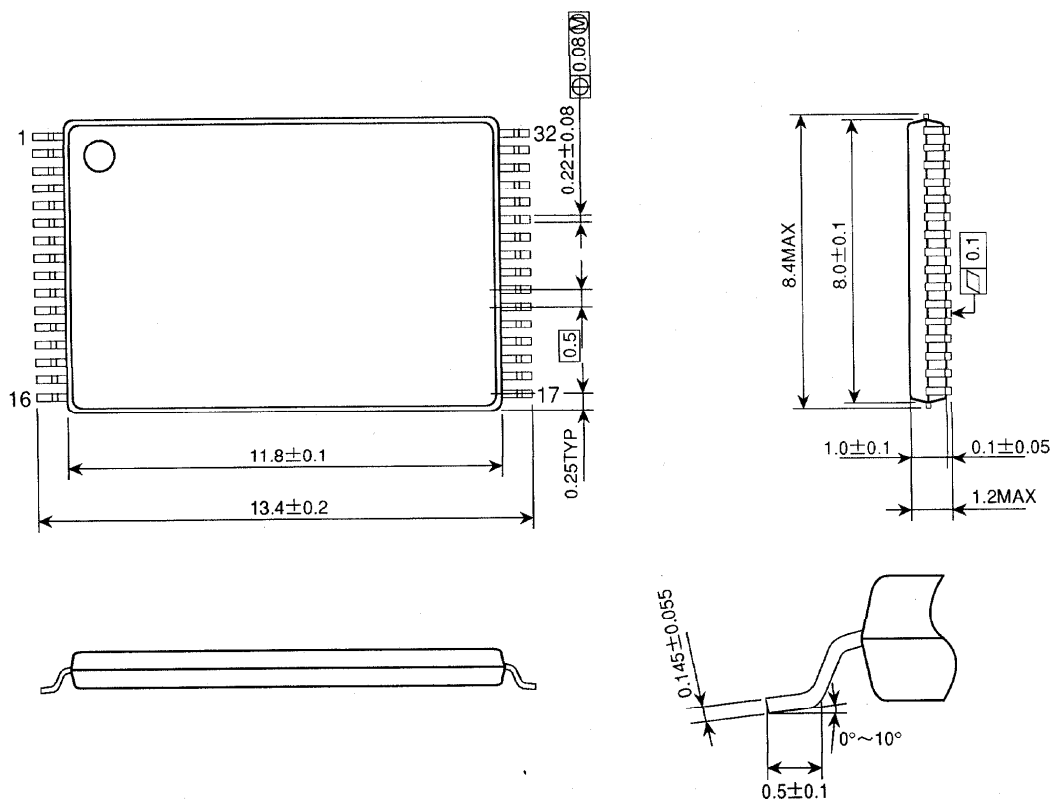
Units in mm



Weight: 0.34 g (typ)

**PACKAGE DIMENSIONS (TSOP I 32-P-0.50)**

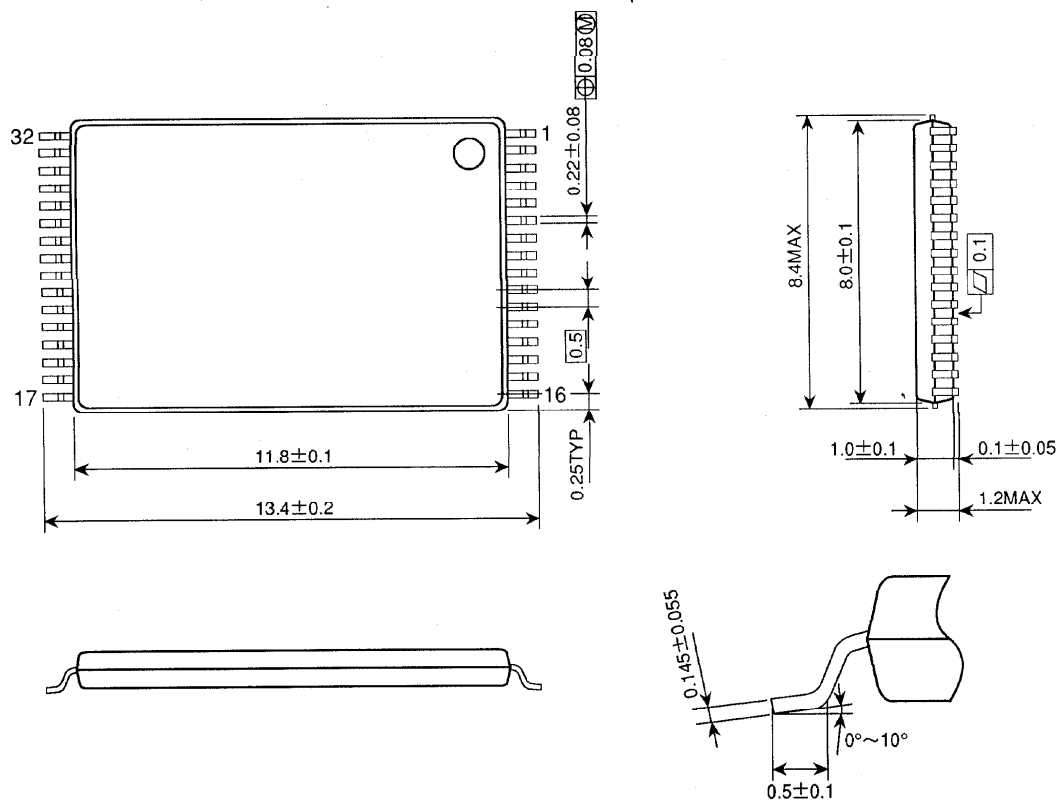
Units in mm



Weight: 0.24 g (typ)

**PACKAGE DIMENSIONS (TSOP I 32-P-0.50A)**

Units in mm



Weight: 0.24 g (typ)



## О компании

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Срок поставки из **Азии – от 10 дней.**

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- Минимальные сроки поставок
- Техническая поддержка
- Подбор комплектации
- Индивидуальный подход
- Гибкое ценообразование

Наша организация особенно сильна в поставках модулей, микросхем, пассивных компонентов, ксайленсах (XC), EPF, EPM и силовой электроники.

Большой выбор предлагаемой продукции, различные виды оплаты и доставки, позволят Вам сэкономить время и получить максимум выгоды от сотрудничества с нами!

## Перечень производителей, продукцию которых мы поставляем на российский рынок





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С уважением,

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