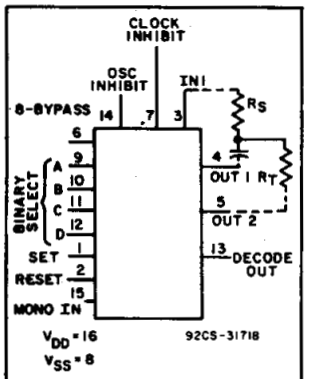
TEXAS INSTRUMENTS
Data sheet acquired from Harris Semiconductor
SCHS083B – Revised March 2003

# CD4536B Types

## CMOS Programmable Timer

High-Voltage Types (20-Volt Rating)



FUNCTIONAL DIAGRAM

■ CD4536B is a programmable timer consisting of 24 ripple-binary counter stages. The salient feature of this device is its flexibility. The device can count from 1 to $2^{24}$ or the first 8 stages can be bypassed to allow an output, selectable by a 4-bit code, from any one of the remaining 16 stages. It can be driven by an external clock or an RC oscillator that can be constructed using on-chip components. Input IN1 serves as either the external clock input or the input to the on-chip RC oscillator. OUT1 and OUT2 are connection terminals for the external RC components. In addition, an on-chip monostable circuit is provided to allow a variable pulse width output. Various timing functions can be achieved using combinations of these capabilities.

A logic 1 on the 8-BYPASS input enables a bypass of the first 8 stages and makes stage 9 the first counter stage of the last 16 stages. Selection of 1 of 16 outputs is accomplished by the decoder and the BCD inputs A, B, C and D. MONO IN is the timing input for the on-chip monostable oscillator. Grounding of the MONO IN terminal through a resistor of 10K ohms or higher, disables the one-shot circuit and connects the decoder directly to the DECODE OUT terminal. A resistor to $V_{DD}$ and a capacitor to ground from the MONO IN terminal enables the one-shot circuit and controls its pulse width.

A fast test mode is enabled by a logic 1 on 8-BYPASS, SET, and RESET. This mode divides the 24-stage counter into three 8-stage sections to facilitate a fast test sequence.

The CD4536B types are supplied in 16-lead hermetic dual-in-line ceramic packages (F3A suffix), 16-lead dual-in-line plastic packages (E suffix), 16-lead small-outline packages (DW, DWR, and NSR suffixes), and 16-lead thin shrink small-outline packages (PW and PWR suffixes).

*Features:*

- **24 flip-flop stages — counts from $2^0$ to $2^{24}$**
- **Last 16 stages selectable by BCD select code**
- **Bypass input allows bypassing first 8 stages**
- **On-chip RC oscillator provision**
- **Clock inhibit input**
- **Schmitt-trigger in clock line permits operation with very long rise and fall times**
- **On-chip monostable output provision**
- **Typical $f_{CL}$ = 3 MHz at $V_{DD}$ = 10 V**
- **Test mode allows fast test sequence**
- **Set and reset inputs**
- **Capable of driving two low power TTL loads, one lower-power Schottky load, or two HTL loads over the rated temperature range**
- **Standardized, symmetrical output characteristics**
- **100% tested for quiescent current at 20 V**
- **5-V, 10-V, and 15-V parametric ratings**
- **Meets all requirements of JEDEC Tentative Standard No. 13B, "Standard Specifications for Description of 'B' Series CMOS Devices"**

**RECOMMENDED OPERATING CONDITIONS**

**For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:**

| CHARACTERISTIC | LIMITS | | UNITS |
|---|---|---|---|
| | Min. | Max. | |
| Supply-Voltage Range (For $T_A$ = Full Package Temperature Range) | 3 | 18 | V |

**DECODE OUT SELECTION TABLE**

| D | C | B | A | NUMBER OF STAGES IN DIVIDER CHAIN | |
|---|---|---|---|---|---|
| | | | | 8-BYPASS = 0 | 8-BYPASS = 1 |
| 0 | 0 | 0 | 0 | 9 | 1 |
| 0 | 0 | 0 | 1 | 10 | 2 |
| 0 | 0 | 1 | 0 | 11 | 3 |
| 0 | 0 | 1 | 1 | 12 | 4 |
| 0 | 1 | 0 | 0 | 13 | 5 |
| 0 | 1 | 0 | 1 | 14 | 6 |
| 0 | 1 | 1 | 0 | 15 | 7 |
| 0 | 1 | 1 | 1 | 16 | 8 |
| 1 | 0 | 0 | 0 | 17 | 9 |
| 1 | 0 | 0 | 1 | 18 | 10 |
| 1 | 0 | 1 | 0 | 19 | 11 |
| 1 | 0 | 1 | 1 | 20 | 12 |
| 1 | 1 | 0 | 0 | 21 | 13 |
| 1 | 1 | 0 | 1 | 22 | 14 |
| 1 | 1 | 1 | 0 | 23 | 15 |
| 1 | 1 | 1 | 1 | 24 | 16 |

**0 = Low Level 1 = High Level**

**MAXIMUM RATINGS,** *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, ($V_{DD}$)
Voltages referenced to $V_{SS}$ Terminal) ..... -0.5V to +20V
INPUT VOLTAGE RANGE, ALL INPUTS ..... -0.5V to $V_{DD}$ +0.5V
DC INPUT CURRENT, ANY ONE INPUT ..... ±10mA
POWER DISSIPATION PER PACKAGE ($P_D$):
For $T_A$ = -55°C to +100°C ..... 500mW
For $T_A$ = +100°C to +125°C ..... Derate Linearity at 12mW/°C to 200mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR
FOR $T_A$ = FULL PACKAGE-TEMPERATURE RANGE (All Package Types)..... 100mW
OPERATING-TEMPERATURE RANGE ($T_A$) ..... -55°C to +125°C
STORAGE TEMPERATURE RANGE ($T_{stg}$) ..... -65°C to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79mm) from case for 10s max ..... +265°C



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## STATIC ELECTRICAL CHARACTERISTICS

| CHARACTERISTIC | CONDITIONS | | | LIMITS AT INDICATED TEMPERATURES (°C) | | | | | | | UNITS |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | $V_O$ (V) | $V_{IN}$ (V) | $V_{DD}$ (V) | −55 | −40 | +85 | +125 | +25 Min. | +25 Typ. | +25 Max. | |
| Quiescent Device Current, $I_{DD}$ Max. | – | 0,5 | 5 | 5 | 5 | 150 | 150 | – | 0.04 | 5 | μA |
| | – | 0,10 | 10 | 10 | 10 | 300 | 300 | – | 0.04 | 10 | |
| | – | 0,15 | 15 | 20 | 20 | 600 | 600 | – | 0.04 | 20 | |
| | – | 0,20 | 20 | 100 | 100 | 3000 | 3000 | – | 0.08 | 100 | |
| Output Low (Sink) Current $I_{OL}$ Min. | 0.4 | 0,5 | 5 | 0.64 | 0.61 | 0.42 | 0.36 | 0.51 | 1 | – | mA |
| | 0.5 | 0,10 | 10 | 1.6 | 1.5 | 1.1 | 0.9 | 1.3 | 2.6 | – | |
| | 1.5 | 0,15 | 15 | 4.2 | 4 | 2.8 | 2.4 | 3.4 | 6.8 | – | |
| Output High (Source) Current, $I_{OH}$ Min. | 4.6 | 0,5 | 5 | −0.64 | −0.61 | −0.42 | −0.36 | −0.51 | −1 | – | |
| | 2.5 | 0,5 | 5 | −2 | −1.8 | −1.3 | −1.15 | −1.6 | −3.2 | – | |
| | 9.5 | 0,10 | 10 | −1.6 | −1.5 | −1.1 | −0.9 | −1.3 | −2.6 | – | |
| | 13.5 | 0,15 | 15 | −4.2 | −4 | −2.8 | −2.4 | −3.4 | −6.8 | – | |
| Output Voltage: Low-Level, $V_{OL}$ Max. | – | 0,5 | 5 | 0.05 | | | | – | 0 | 0.05 | V |
| | – | 0,10 | 10 | 0.05 | | | | – | 0 | 0.05 | |
| | – | 0,15 | 15 | 0.05 | | | | – | 0 | 0.05 | |
| Output Voltage: High-Level, $V_{OH}$ Min. | – | 0,5 | 5 | 4.95 | | | | 4.95 | 5 | – | |
| | – | 0,10 | 10 | 9.95 | | | | 9.95 | 10 | – | |
| | – | 0,15 | 15 | 14.95 | | | | 14.95 | 15 | – | |
| Input Low Voltage $V_{IL}$ Max. | 0.5,4.5 | – | 5 | 1.5 | | | | – | – | 1.5 | V |
| | 1,9 | – | 10 | 3 | | | | – | – | 3 | |
| | 1.5,13.5 | – | 15 | 4 | | | | – | – | 4 | |
| Input High Voltage, $V_{IH}$ Min. | 0.5,4.5 | – | 5 | 3.5 | | | | 3.5 | – | – | |
| | 1,9 | – | 10 | 7 | | | | 7 | – | – | |
| | 1.5,13.5 | – | 15 | 11 | | | | 11 | – | – | |
| Input Current $I_{IN}$ Max. | – | 0,18 | 18 | ±0.1 | ±0.1 | ±1 | ±1 | – | $\pm 10^{-5}$ | ±0.1 | μA |

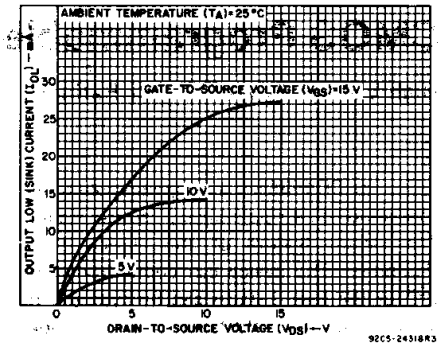



*Fig. 2—Typical output low (sink) current characteristics.*

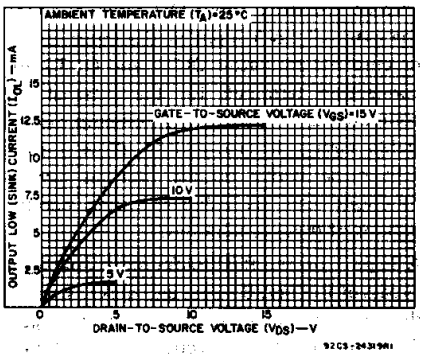



*Fig. 3—Minimum output low (sink) current characteristics.*

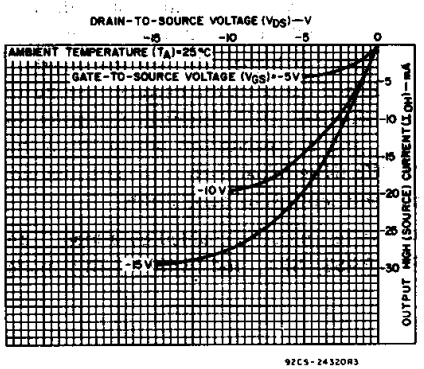



*Fig. 4—Typical output high (source) current characteristics.*

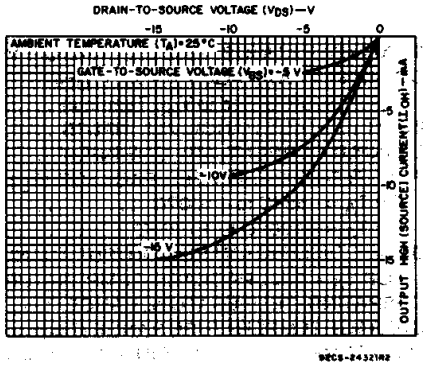



*Fig. 5—Minimum output high (source) current characteristics.*

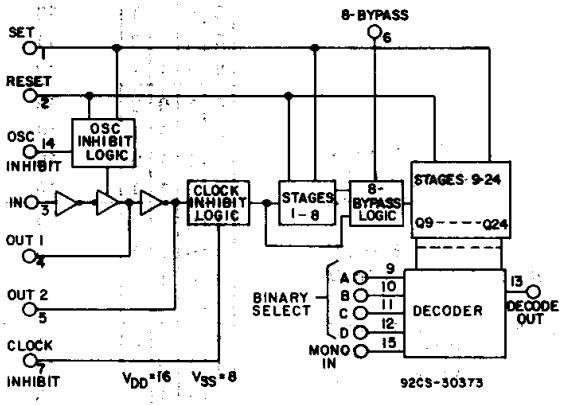



*Fig. 1 — Functional block diagram.*

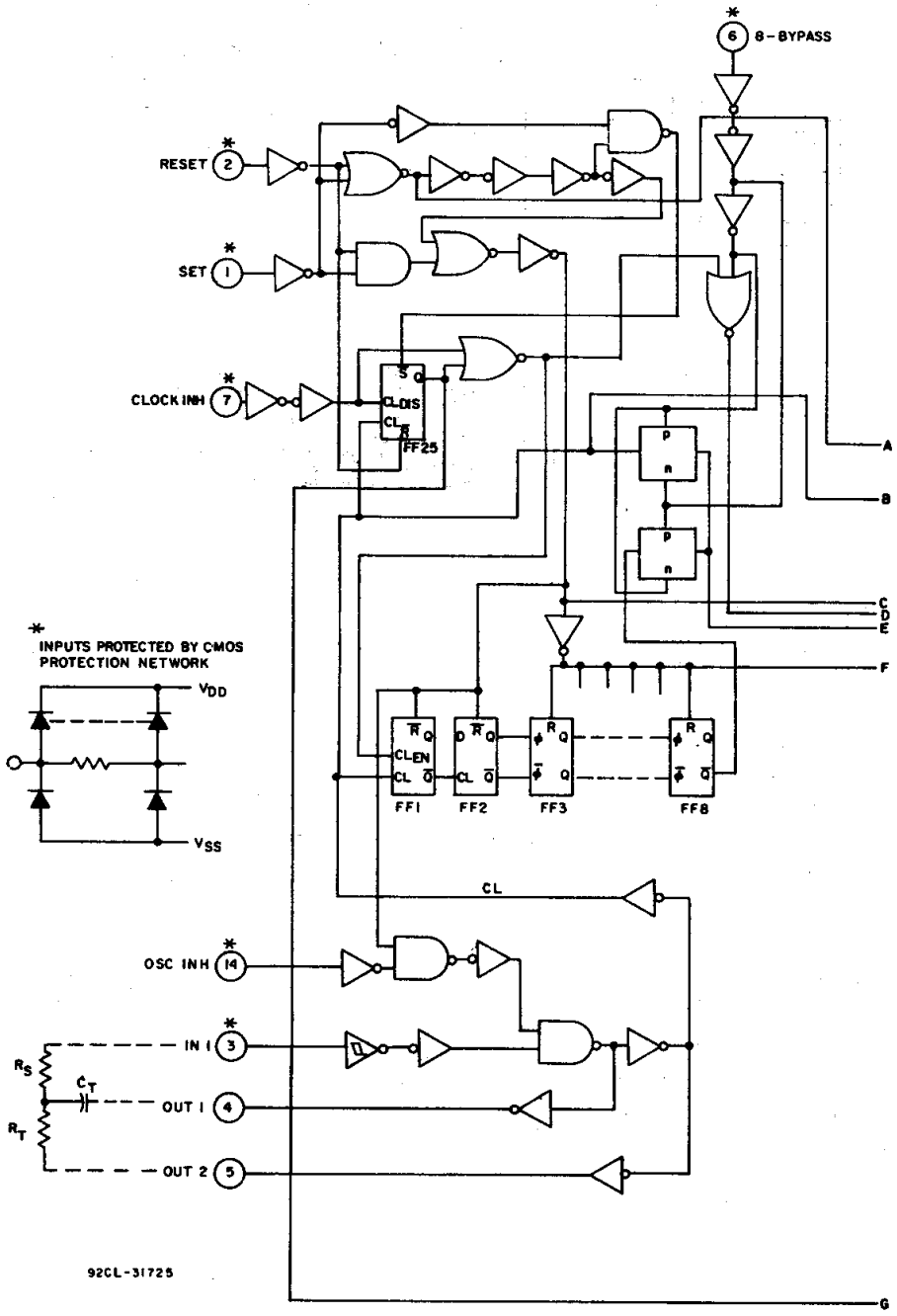



*Fig.6 - Logic diagram for CD4536B* [*continued on next page*].

NOTE: $f \approx \frac{1}{3R_T C_T}$, $R_S \approx (5 \rightarrow 10) \times R_T$

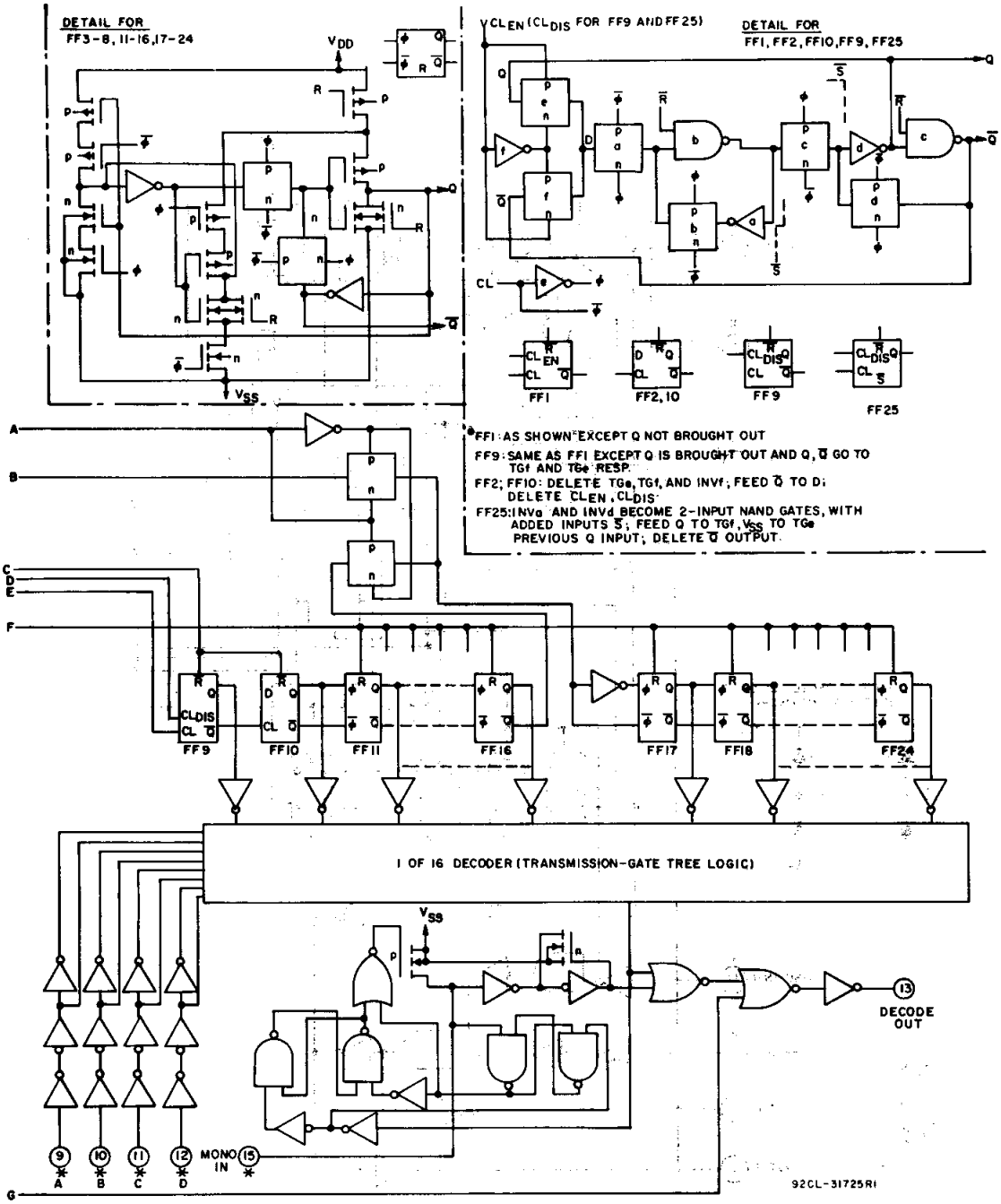
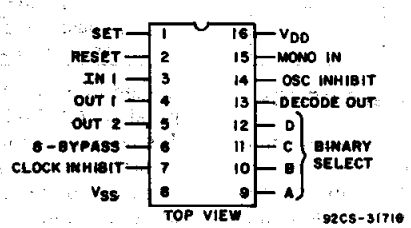



*Fig.6 - Logic diagram for CD4536B [continued from previous page].*

**DYNAMIC ELECTRICAL CHARACTERISTICS,** *at $T_A = 25°C$, Input $t_r$, $t_f = 20$ ns, $C_L = 50$ pF, $R_L = 200$ kΩ*

| CHARACTERISTIC | $V_{DD}$ (V) | LIMITS Min. | Typ. | Max. | UNITS |
|---|---|---|---|---|---|
| Propagation Delay Times: Clock to Q1, 8-Bypass High $t_{PHL}$, $t_{PLH}$ | 5 | — | 1 | 2 | μs |
| | 10 | — | 0.5 | 1 | |
| | 15 | — | 0.35 | 0.7 | |
| Clock to Q1, 8-Bypass Low $t_{PHL}$, $t_{PLH}$ | 5 | — | 2.5 | 5 | μs |
| | 10 | — | 0.8 | 1.6 | |
| | 15 | — | 0.6 | 1.2 | |
| Clock to Q16, $T_{PHL}$ $t_{PLH}$ | 5 | — | 4 | 8 | μs |
| | 10 | — | 1.5 | 3 | |
| | 15 | — | 1 | 2 | |
| $Q_n$ to $Q_{n+1}$, $t_{PHL}$, $t_{PLH}$ | 5 | — | 150 | 300 | ns |
| | 10 | — | 75 | 150 | |
| | 15 | — | 50 | 100 | |
| Set to $Q_n$, $t_{PLH}$ | 5 | — | 300 | 600 | ns |
| | 10 | — | 125 | 250 | |
| | 15 | — | 80 | 160 | |
| Reset to $Q_n$, $t_{PHL}$ | 5 | — | 3 | 6 | μs |
| | 10 | — | 1 | 2 | |
| | 15 | — | 0.75 | 1.5 | |
| Transition Time, $t_{THL}$, $t_{TLH}$ | 5 | — | 100 | 200 | ns |
| | 10 | — | 50 | 100 | |
| | 15 | — | 40 | 80 | |
| Minimum Pulse Widths: Clock | 5 | — | 200 | 400 | ns |
| | 10 | — | 75 | 150 | |
| | 15 | — | 50 | 100 | |
| Set | 5 | — | 200 | 400 | ns |
| | 10 | — | 100 | 200 | |
| | 15 | — | 60 | 120 | |
| Reset | 5 | — | 3 | 6 | μs |
| | 10 | — | 1 | 2 | |
| | 15 | — | 0.75 | 1.5 | |
| Minimum Set Recovery Time, | 5 | — | 2.5 | 5 | μs |
| | 10 | — | 1 | 2 | |
| | 15 | — | 0.6 | 1.6 | |
| Minimum Reset Recovery Time, | 5 | — | 3.5 | 7 | μs |
| | 10 | — | 1.5 | 3 | |
| | 15 | — | 1 | 2 | |
| Maximum Clock Pulse Input Frequency, $f_{CL}$ | 5 | 0.5 | 1 | — | MHz |
| | 10 | 1.5 | 3 | — | |
| | 15 | 2.5 | 5 | — | |
| Maximum Clock Pulse Input Rise or Fall Time, $t_r$, $t_f$ | 5,10,15 | Unlimited | | | μs |




**Terminal Assignment**

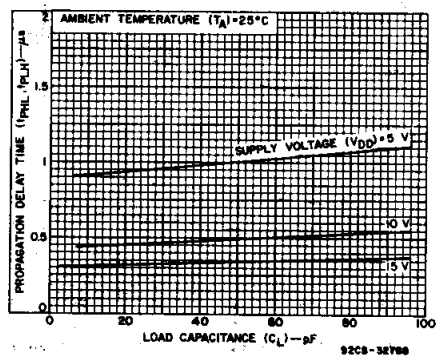



*Fig. 7—Typical propagation delay time as a function of load capacitance (CLOCK to $Q_1$, 8-BYPASS high).*

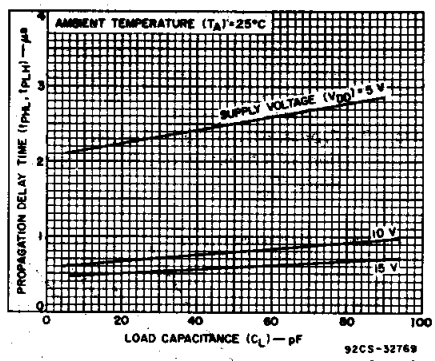



*Fig. 8—Typical propagation delay time as a function of load capacitance (CLOCK to $Q_1$, 8-BYPASS low).*

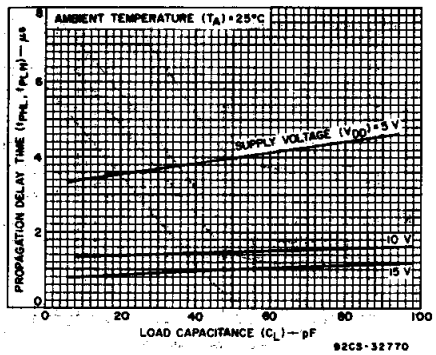



*Fig. 9—Typical propagation delay time as a function of load capacitance (CLOCK to $Q_{16}$, 8-BYPASS high).*

3

COMMERCIAL CMOS HIGH VOLTAGE ICs

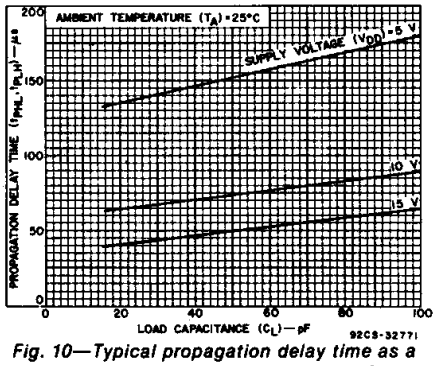



*Fig. 10—Typical propagation delay time as a function of load capacitance ($Q_N$ to $Q_{N+1}$).*

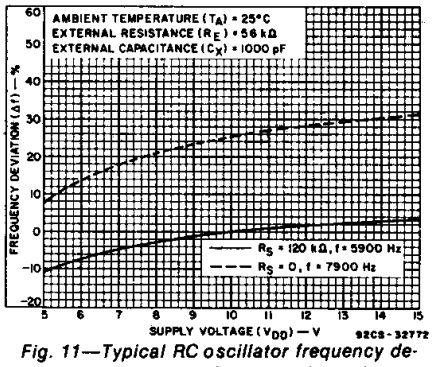



*Fig. 11—Typical RC oscillator frequency deviation as a function of supply voltage.*

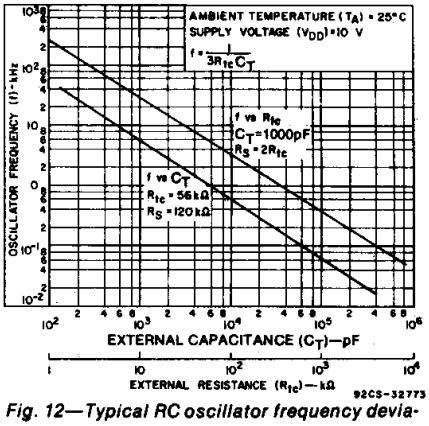



*Fig. 12—Typical RC oscillator frequency deviation as a function of time constant resistance and capacitance.*

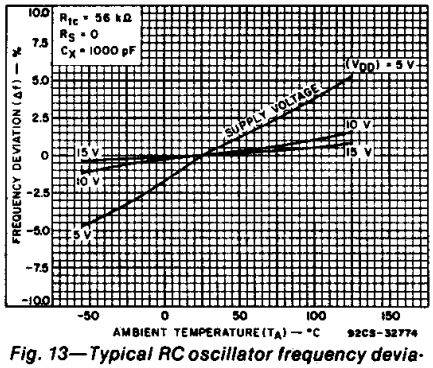



*Fig. 13—Typical RC oscillator frequency deviation as a function of ambient temperature ($R_S$ = 0).*

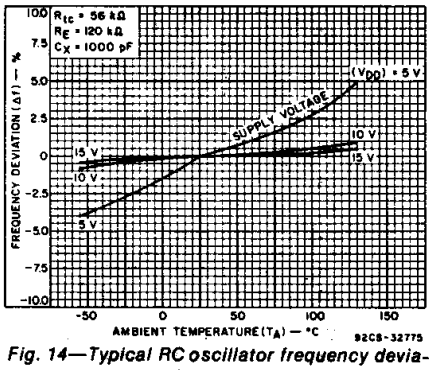



*Fig. 14—Typical RC oscillator frequency deviation as a function of ambient temperature ($R_S$ = 120 kΩ).*

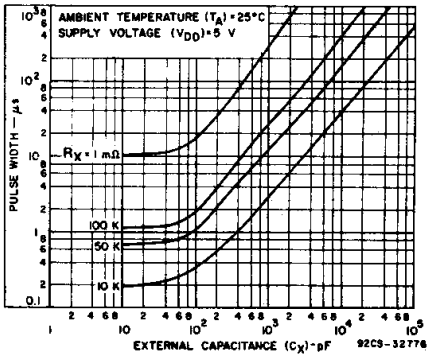



*Fig. 15—Typical pulse width as a function of external capacitance ($V_{DD}$ = 5 V).*

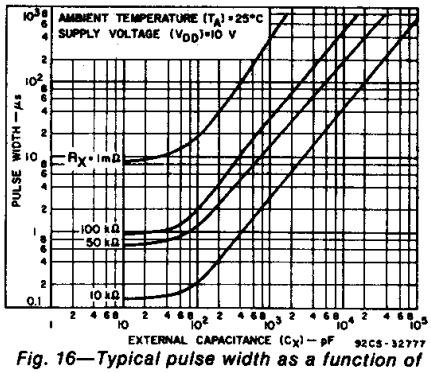



*Fig. 16—Typical pulse width as a function of external capacitance ($V_{DD}$ = 10 V).*

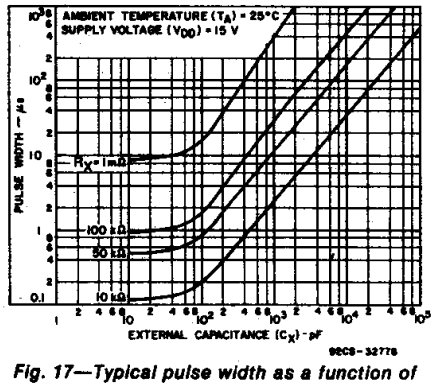



*Fig. 17—Typical pulse width as a function of external capacitance ($V_{DD}$ = 15 V).*

| Functional Test Sequence | | | | | |
|---|---|---|---|---|---|
| Inputs | | | | Outputs | Comments |
| $In_1$ | Set | Reset | 8-Bypass | Decode Out Q1 thru Q24 | All 24 steps are in Reset mode |
| 1 | 0 | 1 | 1 | 0 | |
| 1 | 1 | 1 | 1 | 0 | Counter is in three 8-stage section in parallel mode |
| 0 | 1 | 1 | 1 | 0 | First "1" to "0" transition of clock |
| 1<br>0<br>—<br>—<br>— | 1 | 1 | 1 | | 255 "1" to "0" transitions are clocked in the counter |
| 0 | 1 | 1 | 1 | 1 | The 255 "1" to "0" transition |
| 0 | 0 | 0 | 0 | 1 | Counter converted back to 24 stages in series mode<br>Set and Reset must be connected together and simultaneously go from "1" to "0" |
| 1 | 0 | 0 | 0 | 1 | $In_1$ Switches to a "1" |
| 0 | 0 | 0 | 0 | 0 | Counter Ripples from an all "1" state to an all "0" state |

## FUNCTIONAL TEST SEQUENCE

Test Function (Figure 23) has been included for the reduction of test time required to exercise all 24 counter stages. This test function divides the counter into three 8-stage sections and 255 counts are loaded in each of the 8-stage sections in parallel. All flip-flops are now at a "1". The counter is now returned to the normal 24-steps in series configuration. One more pulse is entered into $In_1$ which will cause the counter to ripple from an all "1" state to an all "0" state.

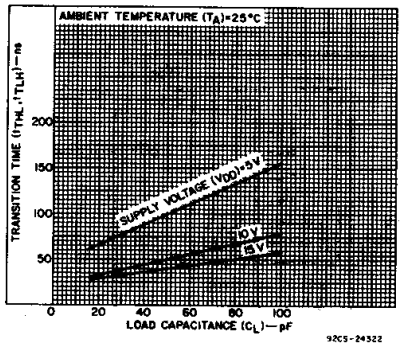



*Fig. 18—Typical transition time as a function of load capacitance.*

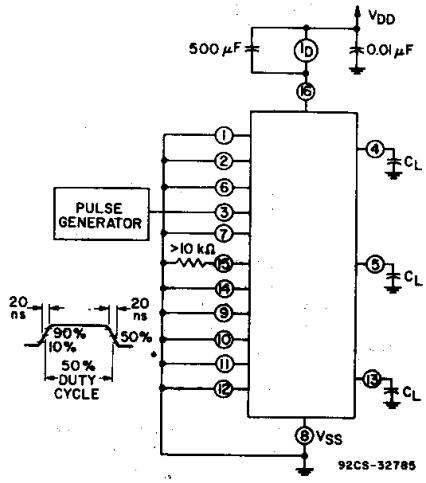



*Fig. 20—Dynamic power dissipation test circuit and waveform.*

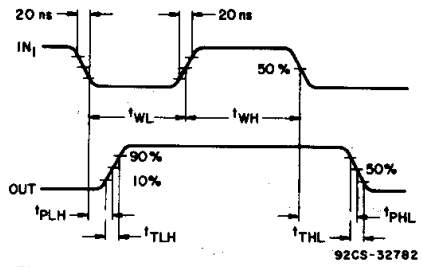



*Fig. 22—Input waveforms for switching-time test circuit.*

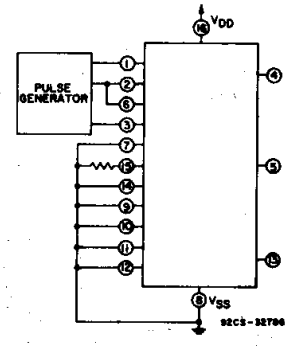
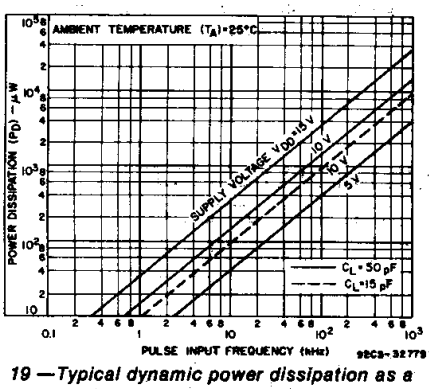



*Fig. 23—Functional test circuit.*




*19 —Typical dynamic power dissipation as a function of input pulse frequency.*

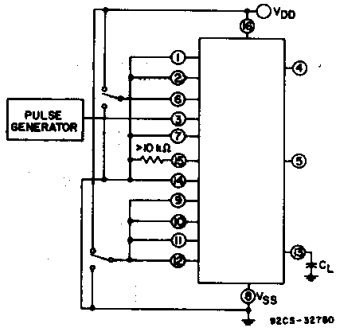



*Fig. 21—Switching time test circuit.*

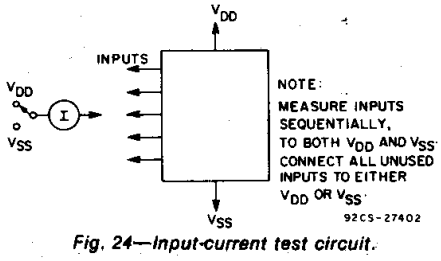



*Fig. 24—Input-current test circuit.*

TRUTH TABLE

| IN1 | SET | RESET | CLOCK INH | OSC INH | OUT1 | OUT2 | DECODE OUT |
|---|---|---|---|---|---|---|---|
| ↗ | 0 | 0 | 0 | 0 | ↗ | ↘ | No Change |
| ↘ | 0 | 0 | 0 | 0 | ↘ | ↗ | Advance to Next State |
| X | 1 | 0 | 0 | 0 | 0 | 1 | 1 |
| X | 0 | 1 | 0 | 0 | 0 | 1 | 0 |
| X | 0 | 0 | 1 | 0 | | | No Change |
| 0 | 0 | 0 | 0 | X | 0 | 1 | No Change |
| 1 | 0 | 0 | 0 | ↗ | ↘ | ↗ | Advance to Next State |

0 = Low Level  1 = High Level  X = Don't Care

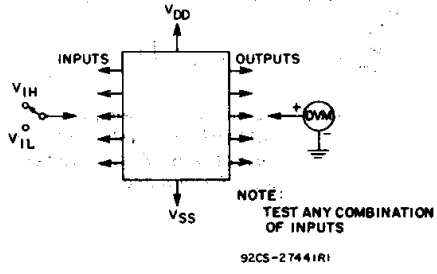



*Fig. 25—Input-voltage test circuit.*

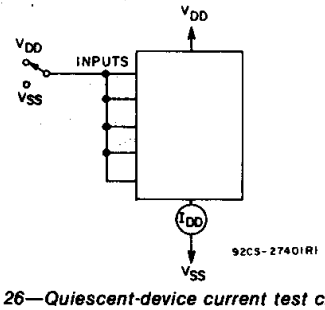



*Fig. 26—Quiescent-device current test circuit.*

## APPLICATIONS

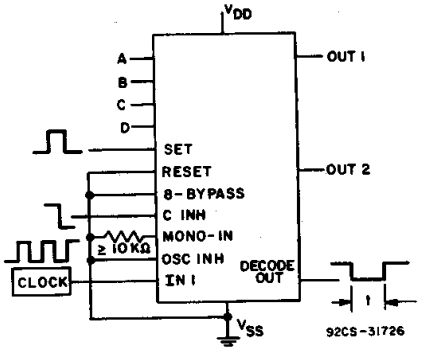



*Fig. 27—Time interval configuration using external clock; set and clock inhibit functions.*

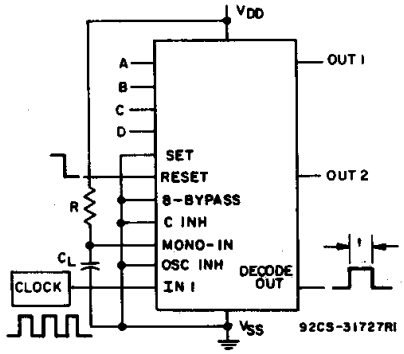



*Fig. 28—Time interval configuration using external clock; reset and output monostable to achieve a pulse output.*

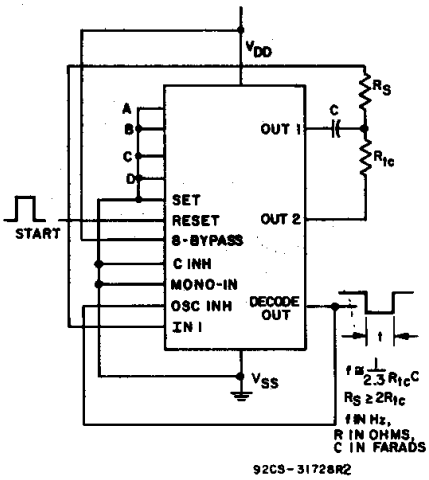



*Fig. 29—Time interval configuration using on-chip RC oscillator and reset input to initiate time interval.*

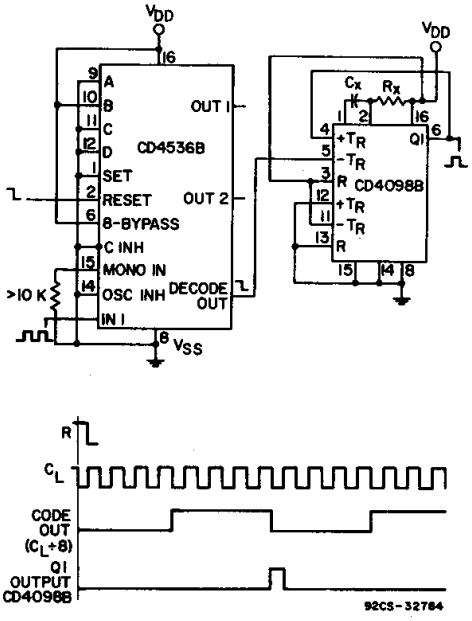



*Fig.30 – Application showing use of CD4098B and CD4536B to get decode pulse 8 clock pulses after Reset pulse.*

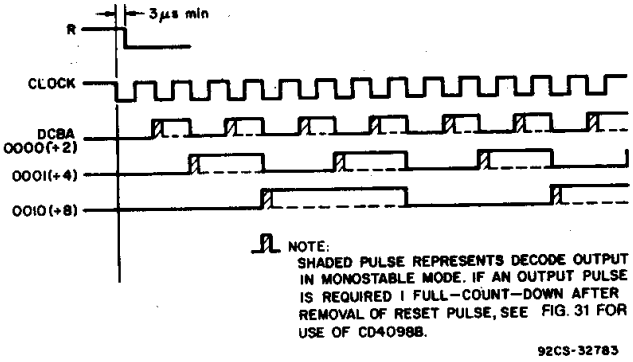
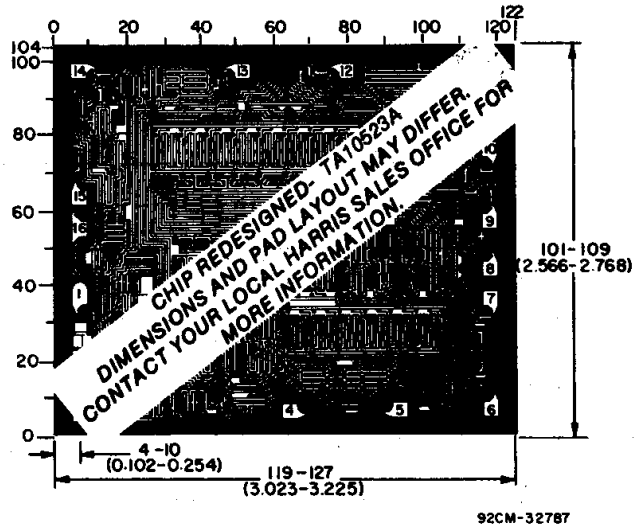



*Fig.31 – CD4536B Timing Diagram.*

*Dimensions and pad layout for CD4536BH.*

*Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils ($10^{-3}$ inch).*



## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish | MSL Peak Temp (3) | Op Temp (°C) | Top-Side Markings (4) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| CD4536BDW | ACTIVE | SOIC | DW | 16 | 40 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -55 to 125 | CD4536BM | Samples |
| CD4536BDWE4 | ACTIVE | SOIC | DW | 16 | 40 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -55 to 125 | CD4536BM | Samples |
| CD4536BDWG4 | ACTIVE | SOIC | DW | 16 | 40 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -55 to 125 | CD4536BM | Samples |
| CD4536BDWR | ACTIVE | SOIC | DW | 16 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -55 to 125 | CD4536BM | Samples |
| CD4536BDWRE4 | ACTIVE | SOIC | DW | 16 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -55 to 125 | CD4536BM | Samples |
| CD4536BDWRG4 | ACTIVE | SOIC | DW | 16 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -55 to 125 | CD4536BM | Samples |
| CD4536BE | ACTIVE | PDIP | N | 16 | 25 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type | -55 to 125 | CD4536BE | Samples |
| CD4536BEE4 | ACTIVE | PDIP | N | 16 | 25 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type | -55 to 125 | CD4536BE | Samples |
| CD4536BF3A | ACTIVE | CDIP | J | 16 | 1 | TBD | A42 | N / A for Pkg Type | -55 to 125 | CD4536BF3A | Samples |
| CD4536BNSR | ACTIVE | SO | NS | 16 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -55 to 125 | CD4536B | Samples |
| CD4536BNSRE4 | ACTIVE | SO | NS | 16 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -55 to 125 | CD4536B | Samples |
| CD4536BNSRG4 | ACTIVE | SO | NS | 16 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -55 to 125 | CD4536B | Samples |
| CD4536BPW | ACTIVE | TSSOP | PW | 16 | 90 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -55 to 125 | CM536B | Samples |
| CD4536BPWE4 | ACTIVE | TSSOP | PW | 16 | 90 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -55 to 125 | CM536B | Samples |
| CD4536BPWG4 | ACTIVE | TSSOP | PW | 16 | 90 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -55 to 125 | CM536B | Samples |
| CD4536BPWR | ACTIVE | TSSOP | PW | 16 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -55 to 125 | CM536B | Samples |
| CD4536BPWRE4 | ACTIVE | TSSOP | PW | 16 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -55 to 125 | CM536B | Samples |

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish | MSL Peak Temp (3) | Op Temp (°C) | Top-Side Markings (4) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| CD4536BPWRG4 | ACTIVE | TSSOP | PW | 16 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -55 to 125 | CM536B | Samples |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
**TBD:** The Pb-Free/Green conversion plan has not been defined.
**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**OTHER QUALIFIED VERSIONS OF CD4536B, CD4536B-MIL :**

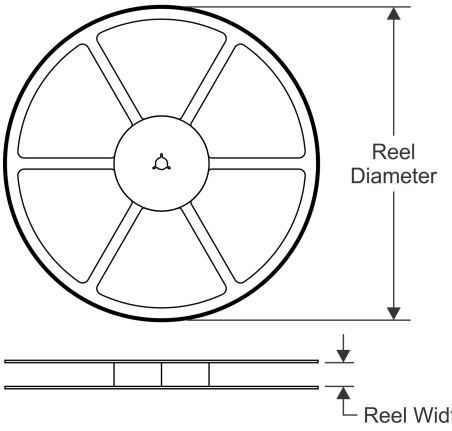
- Catalog: CD4536B
- Military: CD4536B-MIL

NOTE: Qualified Version Definitions:

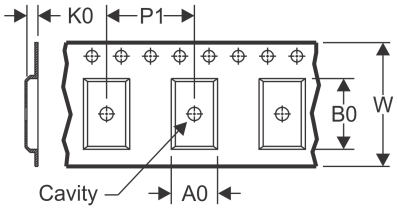
- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

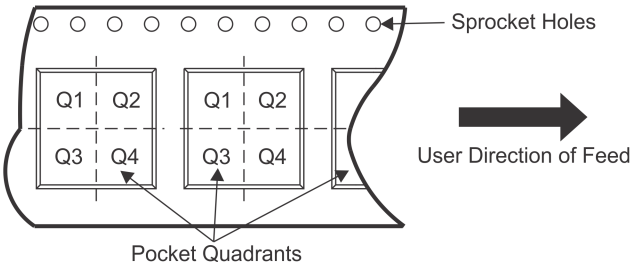



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

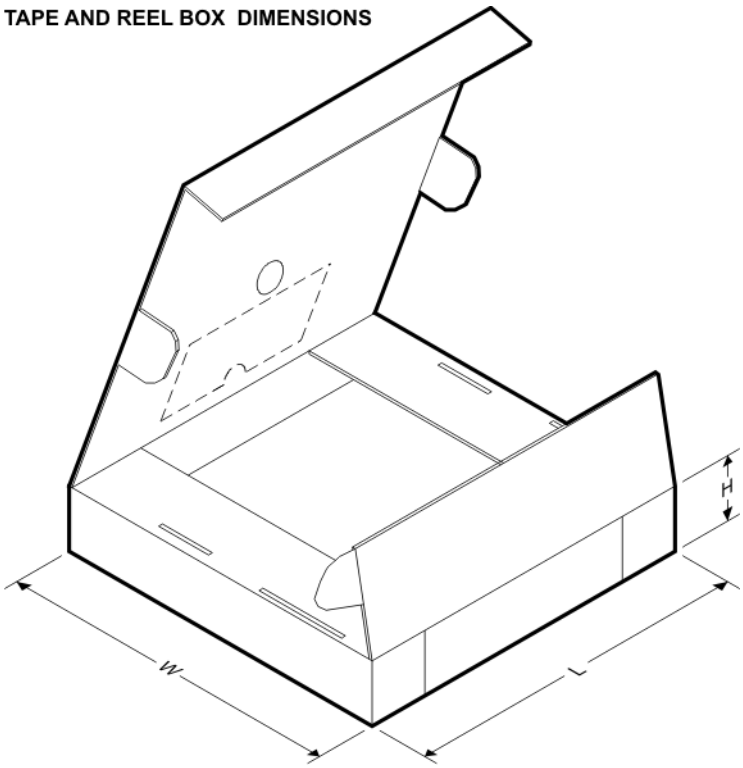
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| CD4536BDWR | SOIC | DW | 16 | 2000 | 330.0 | 16.4 | 10.75 | 10.7 | 2.7 | 12.0 | 16.0 | Q1 |
| CD4536BNSR | SO | NS | 16 | 2000 | 330.0 | 16.4 | 8.2 | 10.5 | 2.5 | 12.0 | 16.0 | Q1 |
| CD4536BPWR | TSSOP | PW | 16 | 2000 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS

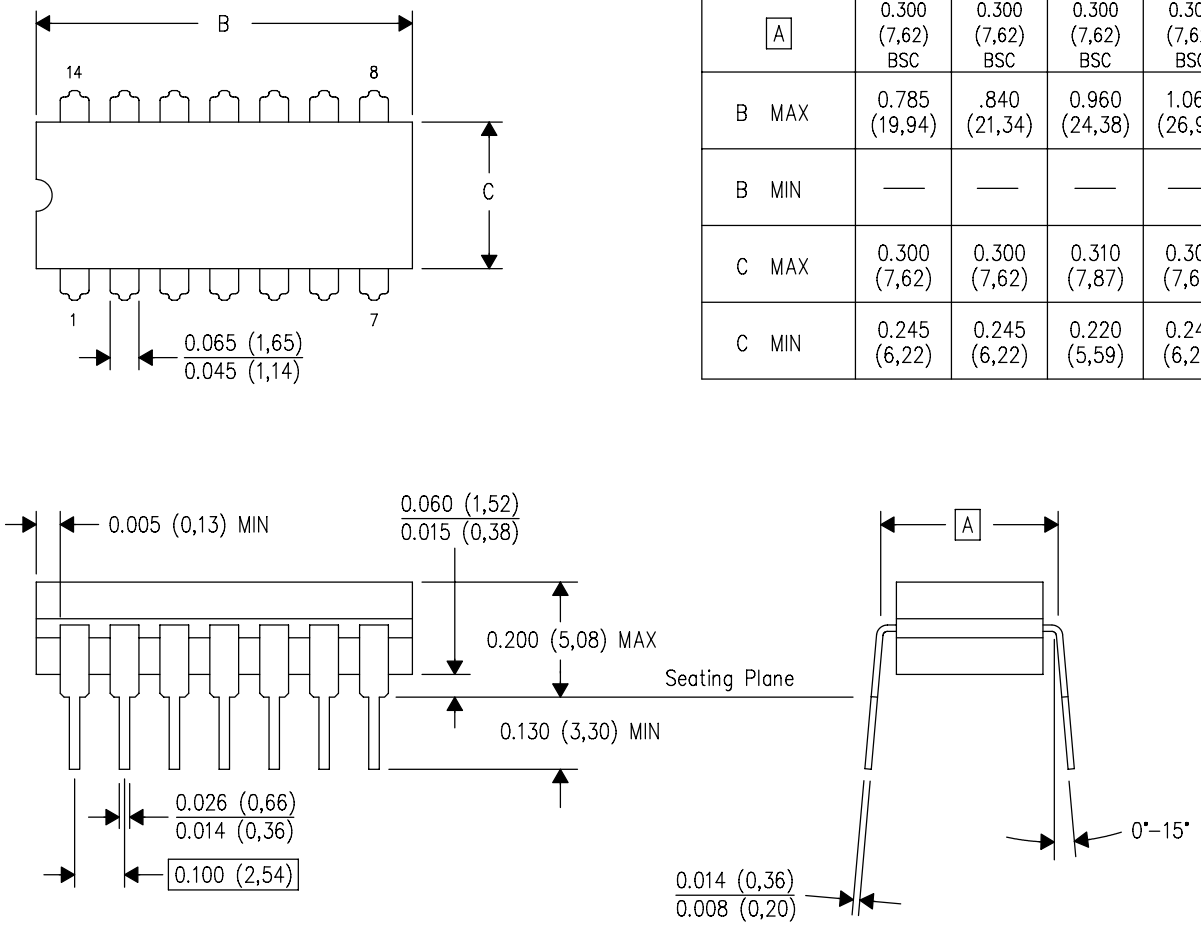



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| CD4536BDWR | SOIC | DW | 16 | 2000 | 367.0 | 367.0 | 38.0 |
| CD4536BNSR | SO | NS | 16 | 2000 | 367.0 | 367.0 | 38.0 |
| CD4536BPWR | TSSOP | PW | 16 | 2000 | 367.0 | 367.0 | 35.0 |

J (R–GDIP–T**) CERAMIC DUAL IN–LINE PACKAGE

14 LEADS SHOWN



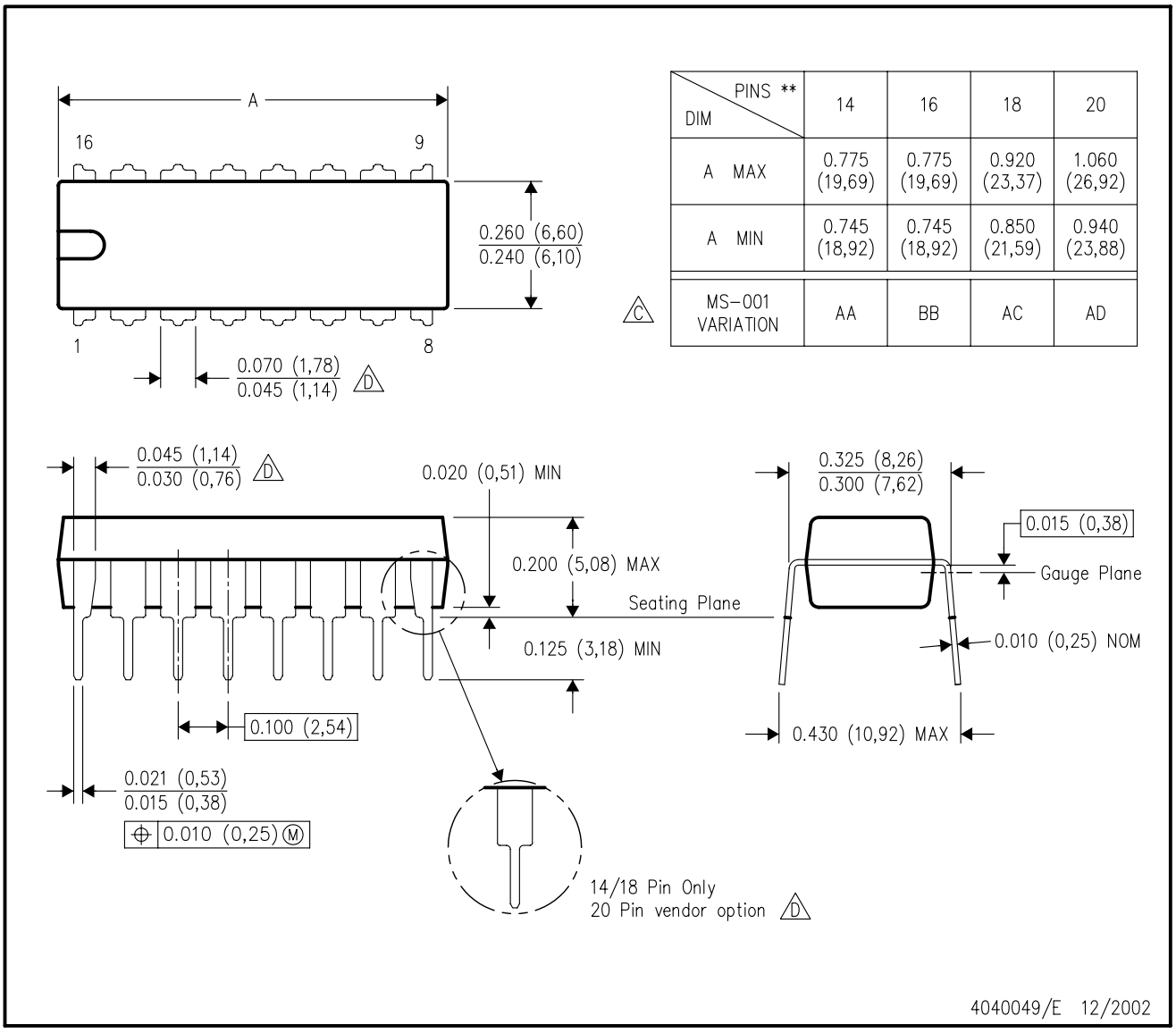

| DIM \ PINS ** | 14 | 16 | 18 | 20 |
|---|---|---|---|---|
| A | 0.300 (7,62) BSC | 0.300 (7,62) BSC | 0.300 (7,62) BSC | 0.300 (7,62) BSC |
| B MAX | 0.785 (19,94) | .840 (21,34) | 0.960 (24,38) | 1.060 (26,92) |
| B MIN | — | — | — | — |
| C MAX | 0.300 (7,62) | 0.300 (7,62) | 0.310 (7,87) | 0.300 (7,62) |
| C MIN | 0.245 (6,22) | 0.245 (6,22) | 0.220 (5,59) | 0.245 (6,22) |

4040083/F 03/03

NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package is hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
- E. Falls within MIL STD 1835 GDIP1–T14, GDIP1–T16, GDIP1–T18 and GDIP1–T20.

## N (R–PDIP–T**) PLASTIC DUAL–IN–LINE PACKAGE

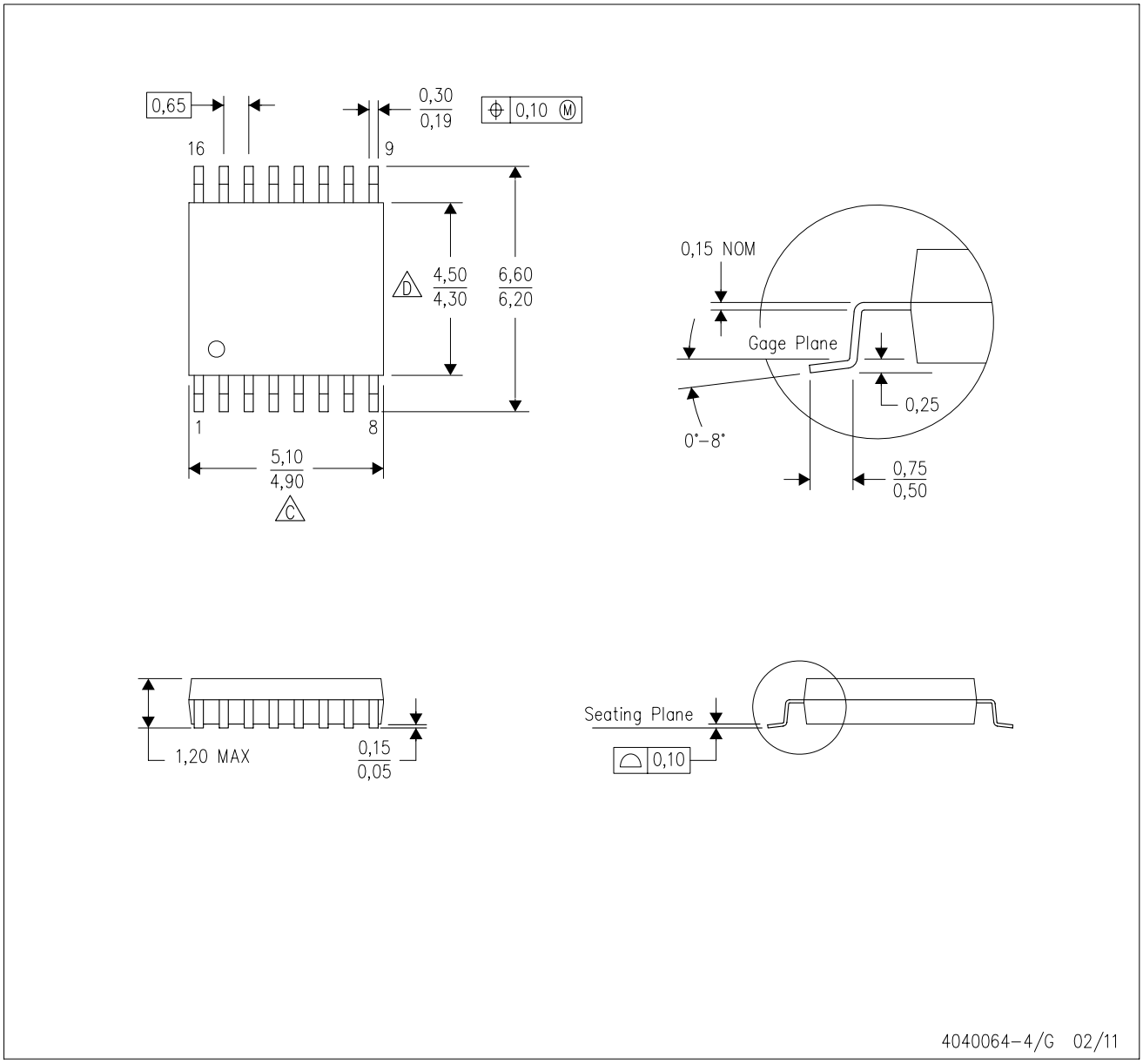
16 PINS SHOWN




| DIM \ PINS ** | 14 | 16 | 18 | 20 |
|---|---|---|---|---|
| A MAX | 0.775 (19,69) | 0.775 (19,69) | 0.920 (23,37) | 1.060 (26,92) |
| A MIN | 0.745 (18,92) | 0.745 (18,92) | 0.850 (21,59) | 0.940 (23,88) |
| MS–001 VARIATION (C) | AA | BB | AC | AD |

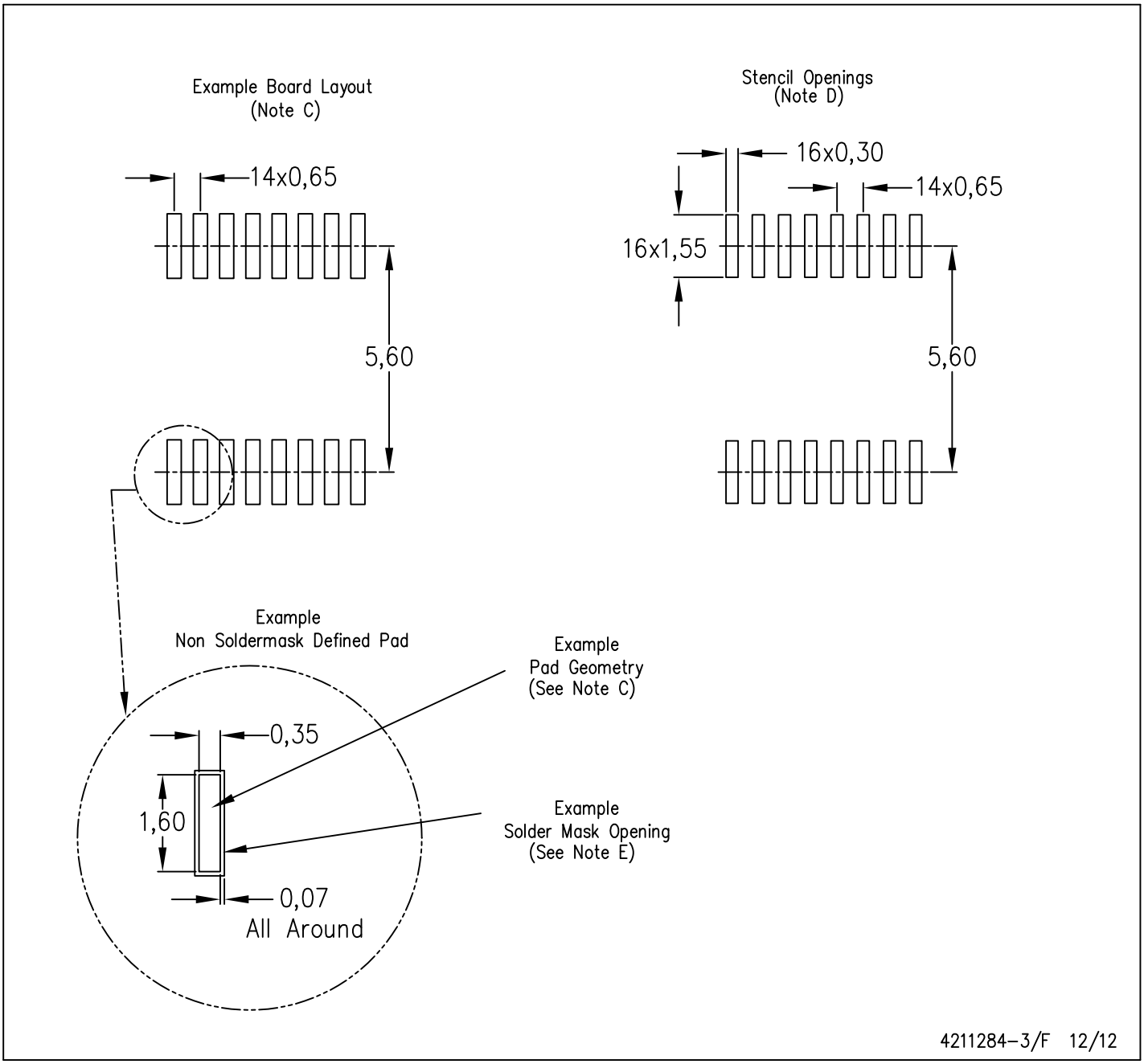
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

PW (R–PDSO–G16) PLASTIC SMALL OUTLINE



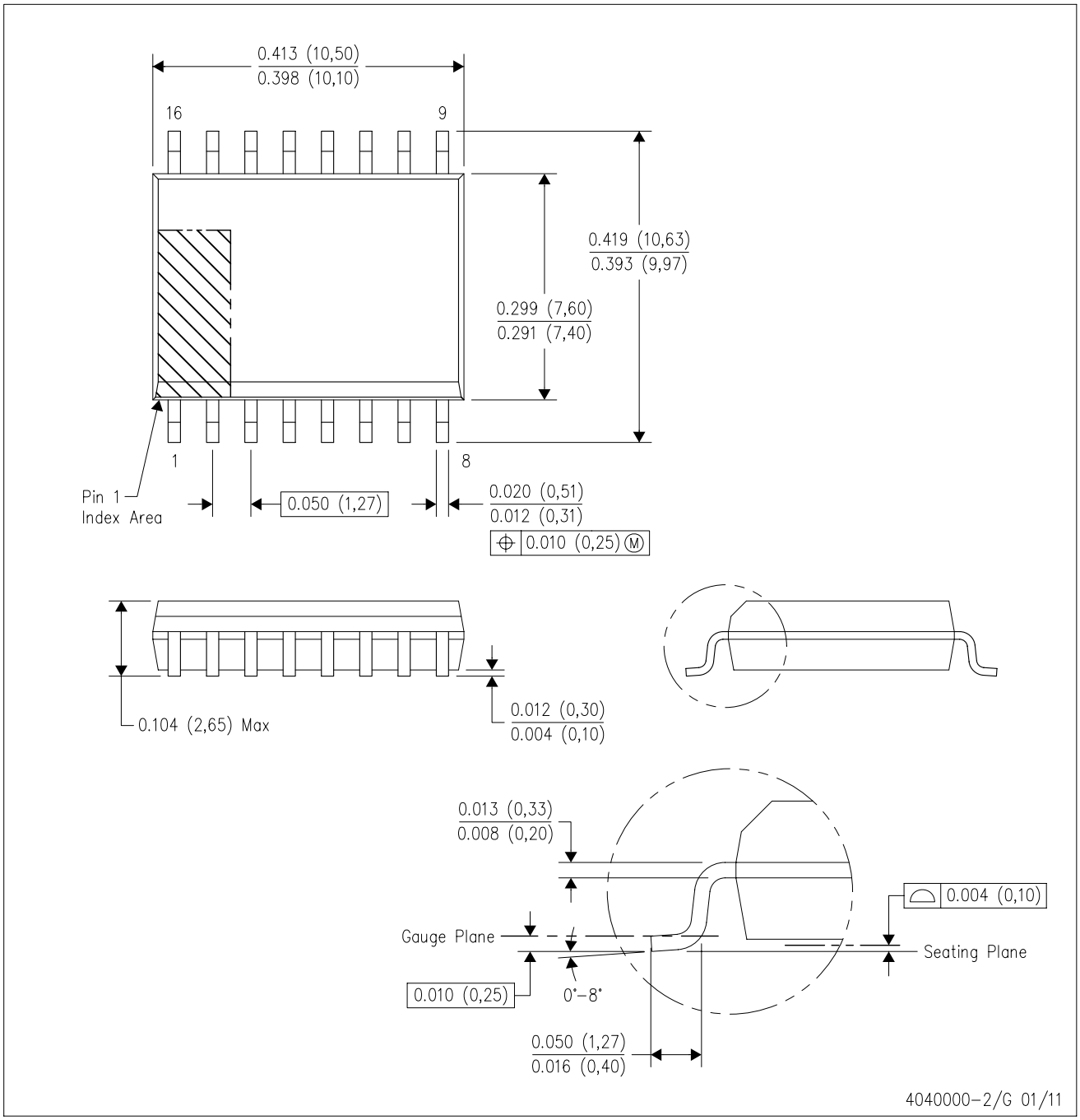

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO–153

PW (R–PDSO–G16) PLASTIC SMALL OUTLINE



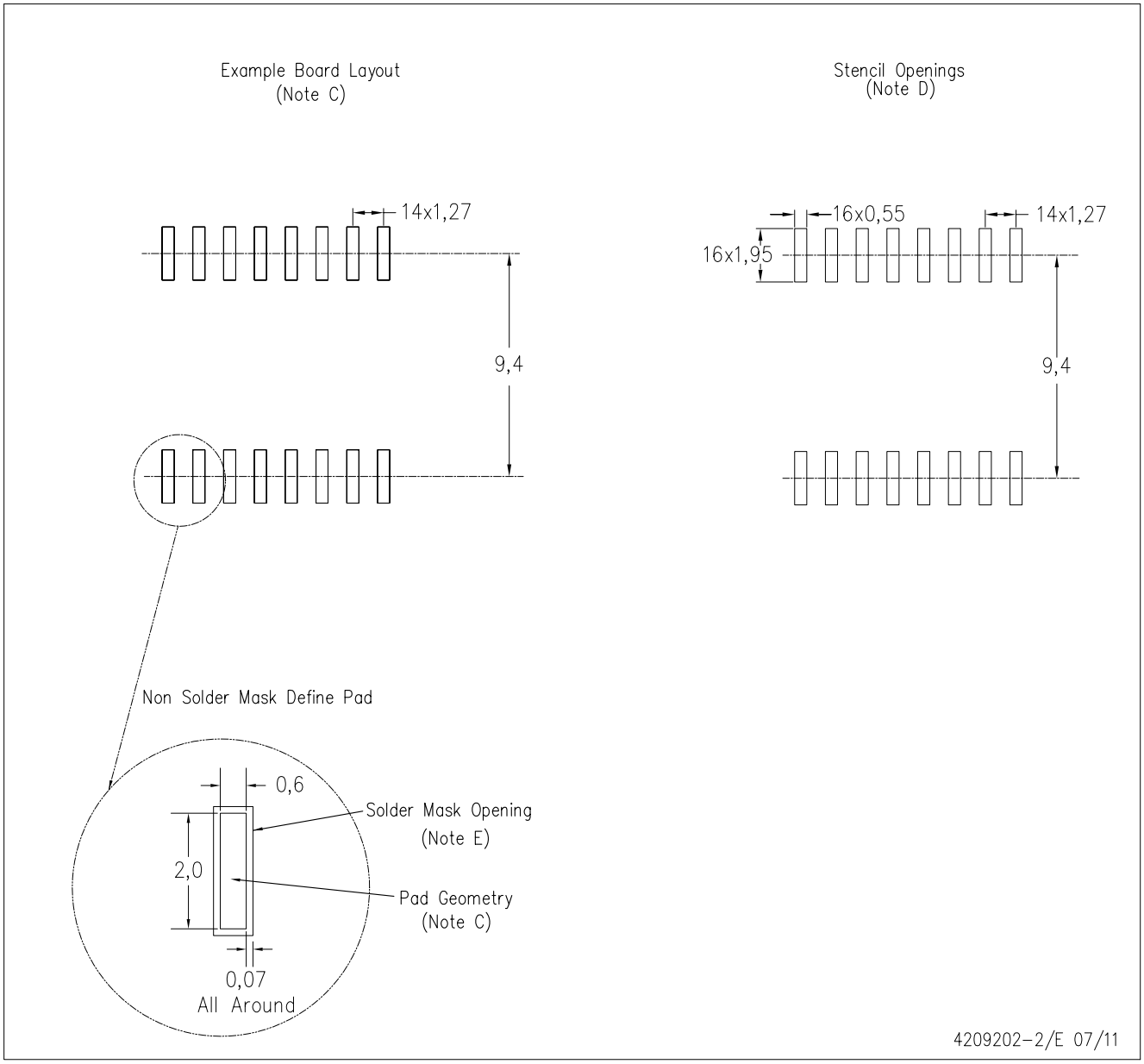

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

DW (R–PDSO–G16) PLASTIC SMALL OUTLINE




NOTES:
A. All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MS–013 variation AA.

DW (R–PDSO–G16) PLASTIC SMALL OUTLINE

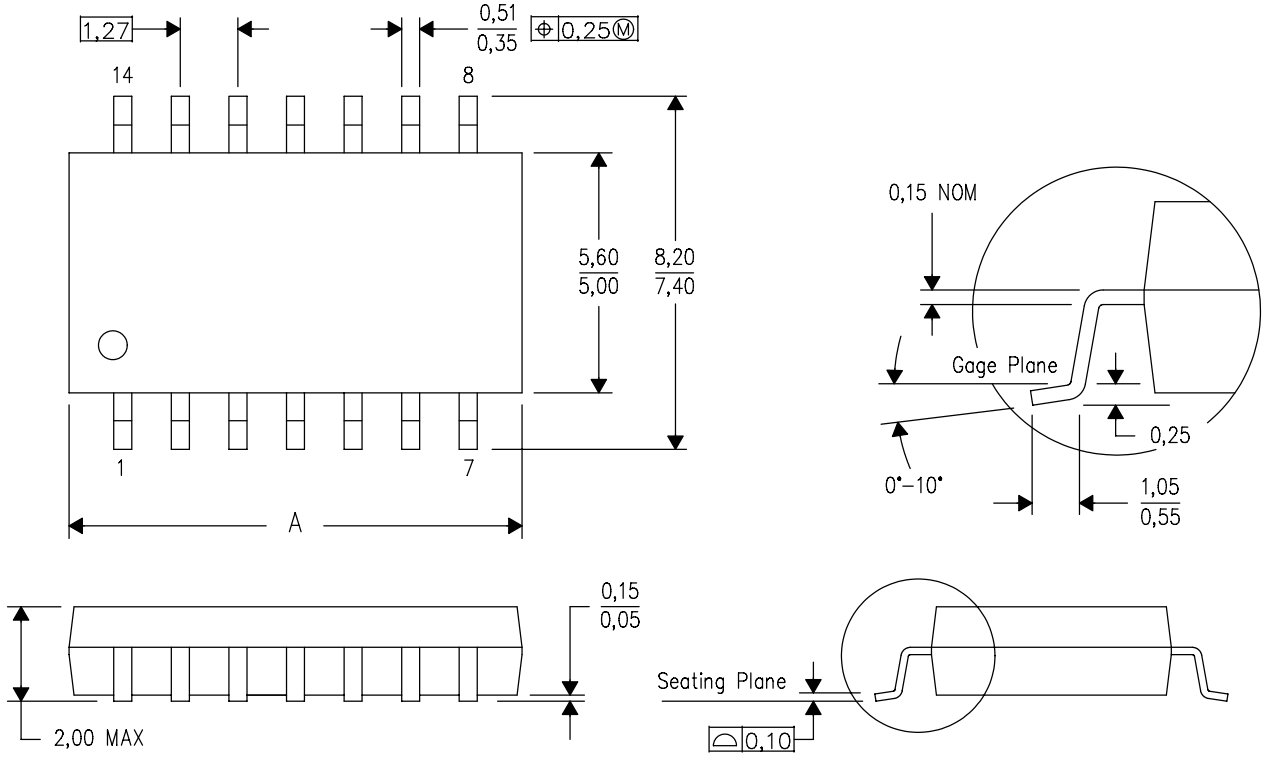



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Refer to IPC7351 for alternate board design.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

## MECHANICAL DATA

**NS (R-PDSO-G**)** **PLASTIC SMALL-OUTLINE PACKAGE**

**14-PINS SHOWN**




| DIM \ PINS ** | 14 | 16 | 20 | 24 |
|---|---|---|---|---|
| A MAX | 10,50 | 10,50 | 12,90 | 15,30 |
| A MIN | 9,90 | 9,90 | 12,30 | 14,70 |

4040062/C 03/03

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

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Предоставляем спец цены на элементы для создания инженерных сэмплов.

**Упорный труд, качественный результат дают нам право быть уверенными в себе и надежными для наших клиентов.**

## Наша компания это:

- Гарантия качества поставляемой продукции
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- Индивидуальный подход
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Наша организация особенно сильна в поставках модулей, микросхем, пассивных компонентов, ксайленсах (XC), EPF, EPM и силовой электроники.

Большой выбор предлагаемой продукции, различные виды оплаты и доставки, позволят Вам сэкономить время и получить максимум выгоды от сотрудничества с нами!

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