

128K x 16 Static RAM

Features

- **High Speed**
 - 55ns and 70ns speed availability
- **Low Voltage range:**
 - 2.7V-3.3V
- **Ultra-low active power**
 - Typical active current: 1.5 mA @ $f = 1\text{MHz}$
 - Typical active current: 7 mA @ $f = f_{\text{max}}$
- **Low standby power**
- **Easy memory expansion with $\overline{\text{CE}}$ and $\overline{\text{OE}}$ features**
- **Automatic power-down when deselected**
- **CMOS for optimum speed/power**

Functional Description

The WCMA2016U4B is a high-performance CMOS static RAMs organized as 128K words by 16 bits. These devices feature advanced circuit design to provide ultra-low active current. This device is ideal for portable applications such as cellular telephones. The devices also have an automatic power-down feature that significantly reduces power consumption by 80% when addresses are not toggling. The device can also

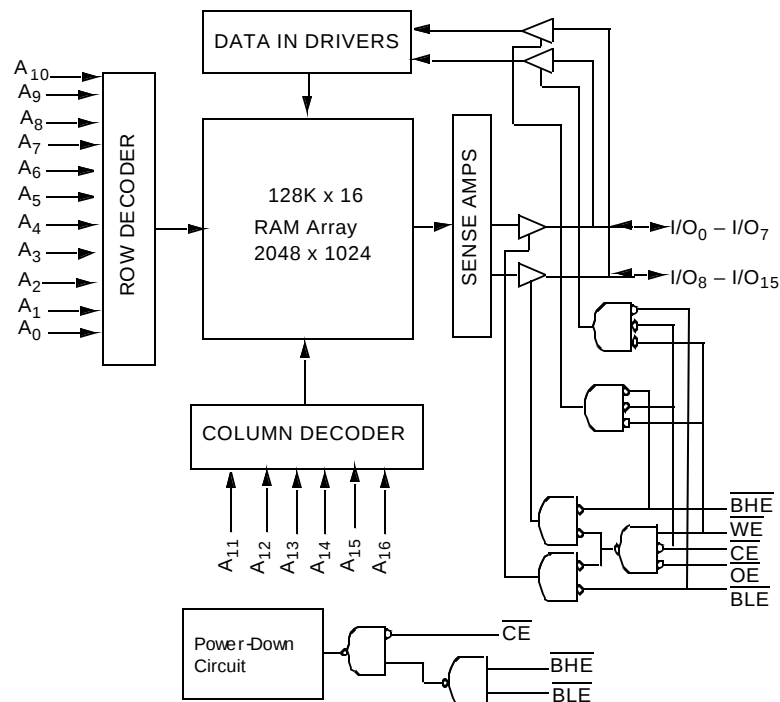
be put into standby mode reducing power consumption by more than 99% when deselected ($\overline{\text{CE}}$ HIGH or both BLE and BHE are HIGH). The input/output pins (I/O_0 through I/O_{15}) are placed in a high-impedance state when: deselected $\overline{\text{CE}}$ HIGH, outputs are disabled ($\overline{\text{OE}}$ HIGH), both Byte High Enable and Byte Low Enable are disabled ($\overline{\text{BHE}}$, BLE HIGH), or during a write operation ($\overline{\text{CE}}$ LOW, and $\overline{\text{WE}}$ LOW).

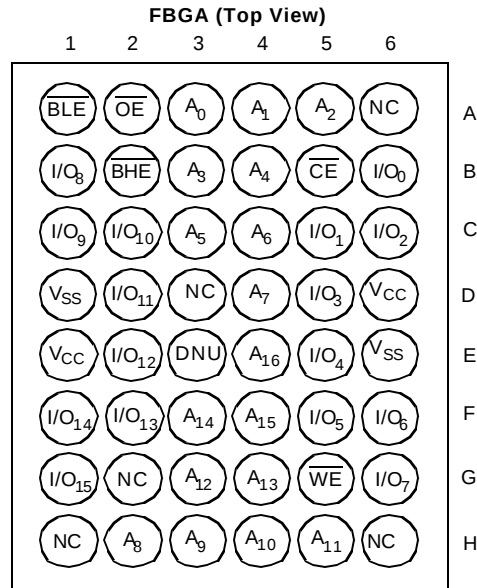
Writing to the device is accomplished by taking Chip Enable ($\overline{\text{CE}}$) and Write Enable ($\overline{\text{WE}}$) inputs LOW. If Byte Low Enable (BLE) is LOW, then data from I/O pins (I/O_0 through I/O_7), is written into the location specified on the address pins (A_0 through A_{16}). If Byte High Enable ($\overline{\text{BHE}}$) is LOW, then data from I/O pins (I/O_8 through I/O_{15}) is written into the location specified on the address pins (A_0 through A_{16}).

Reading from the device is accomplished by taking Chip Enable ($\overline{\text{CE}}$) and Output Enable ($\overline{\text{OE}}$) LOW while forcing the Write Enable ($\overline{\text{WE}}$) HIGH. If Byte Low Enable (BLE) is LOW, then data from the memory location specified by the address pins will appear on I/O_0 to I/O_7 . If Byte High Enable ($\overline{\text{BHE}}$) is LOW, then data from memory will appear on I/O_8 to I/O_{15} . See the truth table at the back of this data sheet for a complete description of read and write modes.

The WCMA2016U4B is available in a 48-ball FBGA package.

Logic Block Diagram



Pin Configuration^[1, 2]

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature -65°C to +150°C

Ambient Temperature with

Power Applied -55°C to +125°C

Supply Voltage to Ground Potential ... -0.5V to V_{CCmax} + 0.5V

DC Voltage Applied to Outputs

in High Z State^[3] -0.5V to V_{CC} + 0.5V

DC Input Voltage^[3] -0.5V to V_{CC} + 0.5V

Output Current into Outputs (LOW)..... 20 mA

Static Discharge Voltage >2001V
(per MIL-STD-883, Method 3015)

Latch-Up Current >200 mA

Operating Range

Device	Range	Ambient Temperature	V _{CC}
WCMA2016U4B	Industrial	-40°C to +85°C	2.7V to 3.3V

Product Portfolio

Product	V _{CC} Range(V)			Speed (ns)	Power Dissipation (Industrial)					
					Operating, I _{CC} (mA)				Standby, I _{SB2} (mA)	
					f = 1 MHz		f = f _{max}			
	V _{CC(min.)}	V _{CC(typ.)} ^[4]	V _{CC(max.)}		Typ. ^[4]	Max.	Typ. ^[4]	Max.	Typ. ^[4]	Max.
WCMA2016U4B	2.7	3.0	3.3	70	1.5	2	7	15	2	10
				55						

Notes:

1. NC pins are not connected to the die.
2. E3 (DNU) can be left as NC or V_{SS} to ensure proper application.
3. V_{L(min.)} = -2.0V for pulse durations less than 20 ns.
4. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at V_{CC} = V_{CC(typ.)}, T_A = 25°C.

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions		WCMA2016U4B-55			WCMA2016U4B-70			Unit
				Min.	Typ. ^[4]	Max.	Min.	Typ. ^[4]	Max.	
V _{OH}	Output HIGH Voltage	I _{OH} = −1.0 mA	V _{CC} = 2.7V	2.4			2.4			V
V _{OL}	Output LOW Voltage	I _{OL} = 2.1mA	V _{CC} = 2.7V			0.4			0.4	V
V _{IH}	Input HIGH Voltage			2.2		V _{CC} + 0.5V	2.2		V _{CC} + 0.5V	V
V _{IL}	Input LOW Voltage			−0.3		0.8	−0.3		0.8	V
I _{IX}	Input Leakage Current	GND ≤ V _I ≤ V _{CC}		−1		+1	−1		+1	μA
I _{OZ}	Output Leakage Current	GND ≤ V _O ≤ V _{CC} , Output Disabled		−1		+1	−1		+1	μA
I _{CC}	V _{CC} Operating Supply Current	f = f _{MAX} = 1/t _{RC}	V _{CC} = 3.3V I _{OUT} = 0 mA CMOS Levels		7	15		7	15	mA
		f = 1 MHz			1.5	3		1.5	3	
I _{SB1}	Automatic CE Power-Down Current— CMOS Inputs	CE ≥ V _{CC} − 0.2V V _{IN} ≥ V _{CC} − 0.2V or V _{IN} ≤ 0.2V, f = f _{max} (Address and Data Only), f=0 (OE,WE,BHE and BLE)			2	10		2	10	μA
I _{SB2}	Automatic CE Power-Down Current— CMOS Inputs	CE ≥ V _{CC} − 0.2V V _{IN} ≥ V _{CC} − 0.2V or V _{IN} ≤ 0.2V, f = 0, Vcc=3.3V								

Capacitance^[5]

Parameter	Description	Test Conditions	Max.	Unit
C _{IN}	Input Capacitance	T _A = 25°C, f = 1 MHz, V _{CC} = V _{CC} (typ.)	6	pF
C _{OUT}	Output Capacitance		8	pF

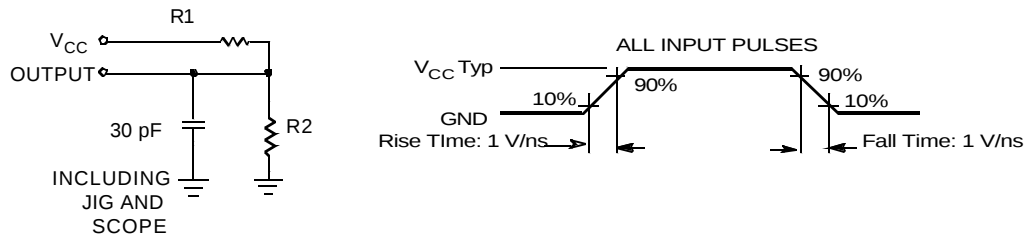
Thermal Resistance

Description	Test Conditions	Symbol	BGA	Units
Thermal Resistance (Junction to Ambient) ^[5]	Still Air, soldered on a 4.25 x 1.125 inch, 4-layer printed circuit board	Θ _{JA}	55	°C/W
Thermal Resistance (Junction to Case) ^[5]		Θ _{JC}	16	°C/W

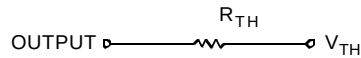
Note:

5. Tested initially and after any design or process changes that may affect these parameters.

AC Test Loads and Waveforms



Equivalent to: THÉVENIN EQUIVALENT

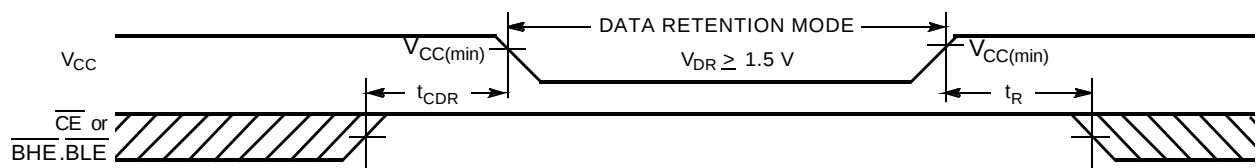


Parameters	3.0V	Unit
R1	1.105	KOhms
R2	1.550	KOhms
R_{TH}	0.645	KOhms
V_{TH}	1.75	Volts

Data Retention Characteristics (Over the Operating Range)

Parameter	Description	Conditions	Min.	Typ. ^[4]	Max.	Unit
V_{DR}	V_{CC} for Data Retention		1.5		$V_{CC\text{ max}}$	V
I_{CCDR}	Data Retention Current	$V_{CC} = 1.5\text{V}$ $CE \geq V_{CC} - 0.2\text{V}$, $V_{IN} \geq V_{CC} - 0.2\text{V}$ or $V_{IN} \leq 0.2\text{V}$		0.5	7.5	μA
$t_{CDR}^{[5]}$	Chip Deselect to Data Retention Time		0			ns
$t_R^{[6]}$	Operation Recovery Time		70			ns

Data Retention Waveform^[7]



Note:

- Full Device AC operation requires linear V_{CC} ramp from V_{DR} to $V_{CC(\text{min})} > 100\text{ }\mu\text{s}$ or stable at $V_{CC(\text{min})} > 100\text{ }\mu\text{s}$.
- $\overline{BHE}.\overline{BLE}$ is the AND of both $\overline{BHE}$ and $\overline{BLE}$. Chip can be deselected by either disabling the chip enable signals or by disabling both $\overline{BHE}$ and $\overline{BLE}$.

Switching Characteristics Over the Operating Range^[8]

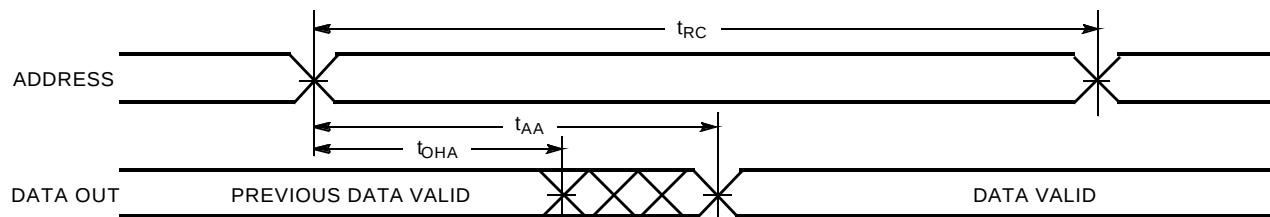
Parameter	Description	55ns		70 ns		Unit
		Min	Max	Min	Max	
READ CYCLE						
t _{RC}	Read Cycle Time	55		70		ns
t _{AA}	Address to Data Valid		55		70	ns
t _{OHA}	Data Hold from Address Change	10		10		ns
t _{ACE}	$\overline{\text{CE}}$ LOW to Data Valid		55		70	ns
t _{DOE}	$\overline{\text{OE}}$ LOW to Data Valid		25		35	ns
t _{LZOE}	$\overline{\text{OE}}$ LOW to Low Z ^[9]	5		5		ns
t _{HZOE}	$\overline{\text{OE}}$ HIGH to High Z ^[9, 11]		25		25	ns
t _{LZCE}	$\overline{\text{CE}}$ LOW to Low Z ^[9]	10		10		ns
t _{HZCE}	$\overline{\text{CE}}$ HIGH to High Z ^[9, 11]		25		25	ns
t _{PU}	$\overline{\text{CE}}$ LOW to Power-Up	0		0		ns
t _{PD}	$\overline{\text{CE}}$ HIGH to Power-Down		55		70	ns
t _{DBE}	$\overline{\text{BHE}} / \overline{\text{BLE}}$ LOW to Data Valid		55		70	ns
t _{LZBE} ^[10]	$\overline{\text{BHE}} / \overline{\text{BLE}}$ LOW to Low Z ^[9]	5		5		ns
t _{HZBE}	$\overline{\text{BHE}} / \overline{\text{BLE}}$ HIGH to High Z ^[9, 11]		25		25	ns
WRITE CYCLE ^[12]						
t _{WC}	Write Cycle Time	55		70		ns
t _{SCE}	$\overline{\text{CE}}$ LOW to Write End	45		60		ns
t _{AW}	Address Set-Up to Write End	45		60		ns
t _{HA}	Address Hold from Write End	0		0		ns
t _{SA}	Address Set-Up to Write Start	0		0		ns
t _{PWE}	$\overline{\text{WE}}$ Pulse Width	40		50		ns
t _{BW}	$\overline{\text{BHE}} / \overline{\text{BLE}}$ Pulse Width	50		60		ns
t _{SD}	Data Set-Up to Write End	25		30		ns
t _{HD}	Data Hold from Write End	0		0		ns
t _{HZWE}	$\overline{\text{WE}}$ LOW to High Z ^[9, 11]		20		25	ns
t _{LZWE}	$\overline{\text{WE}}$ HIGH to Low Z ^[9]	5		10		ns

Notes:

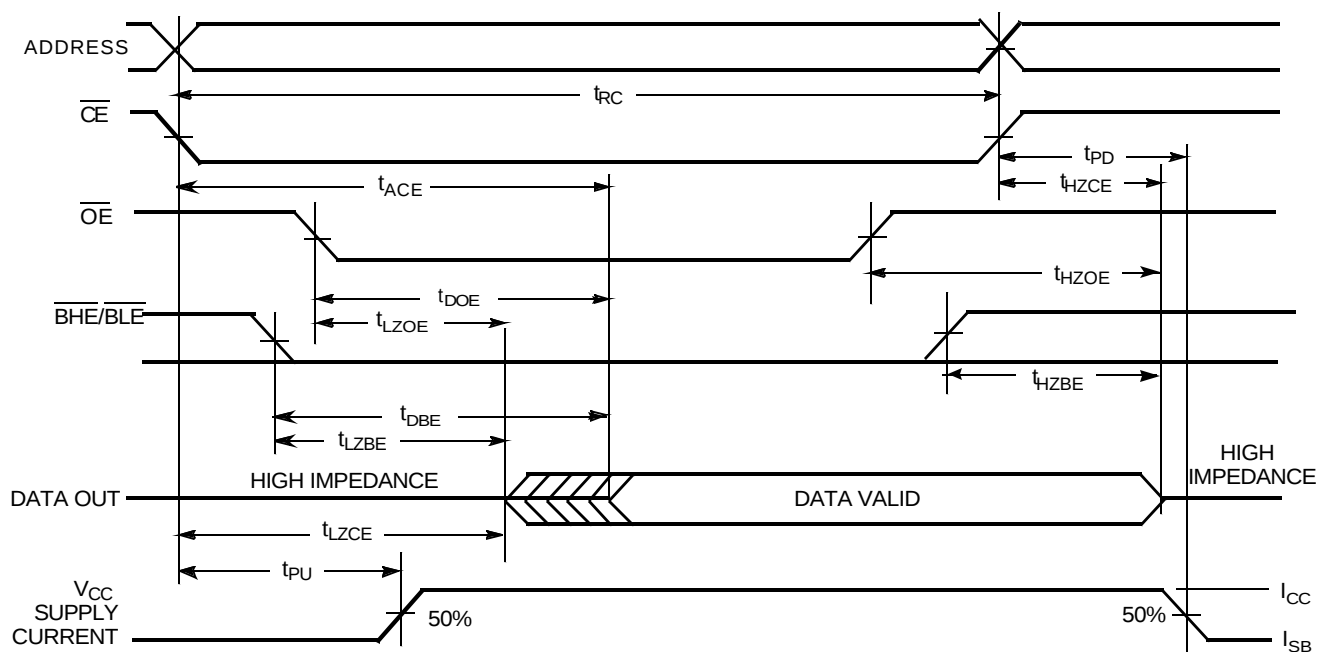
8. Test conditions assume signal transition time of 5 ns or less, timing reference levels of $V_{CC(typ.)}/2$, input pulse levels of 0 to $V_{CC(typ.)}$, and output loading of the specified I_{OL}/I_{OH} and 30 pF load capacitance.
9. At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE} , t_{HZBE} is less than t_{LZBE} , t_{HZOE} is less than t_{LZOE} , and t_{HZWE} is less than t_{LZWE} for any given device.
10. If both byte enables are toggled together this value is 10ns
11. t_{HZOE} , t_{HZCE} , t_{HZBE} , and t_{HZWE} transitions are measured when the outputs enter a high impedance state.
12. The internal write time of the memory is defined by the overlap of $\overline{WE}$, $\overline{CE} = V_{IL}$, $\overline{BHE}$ and/or $\overline{BLE} = V_{IL}$. All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input set-up and hold timing should be referenced to the edge of the signal that terminates the write..

Switching Waveforms

Read Cycle No. 1 (Address Transition Controlled) ^[13, 14]

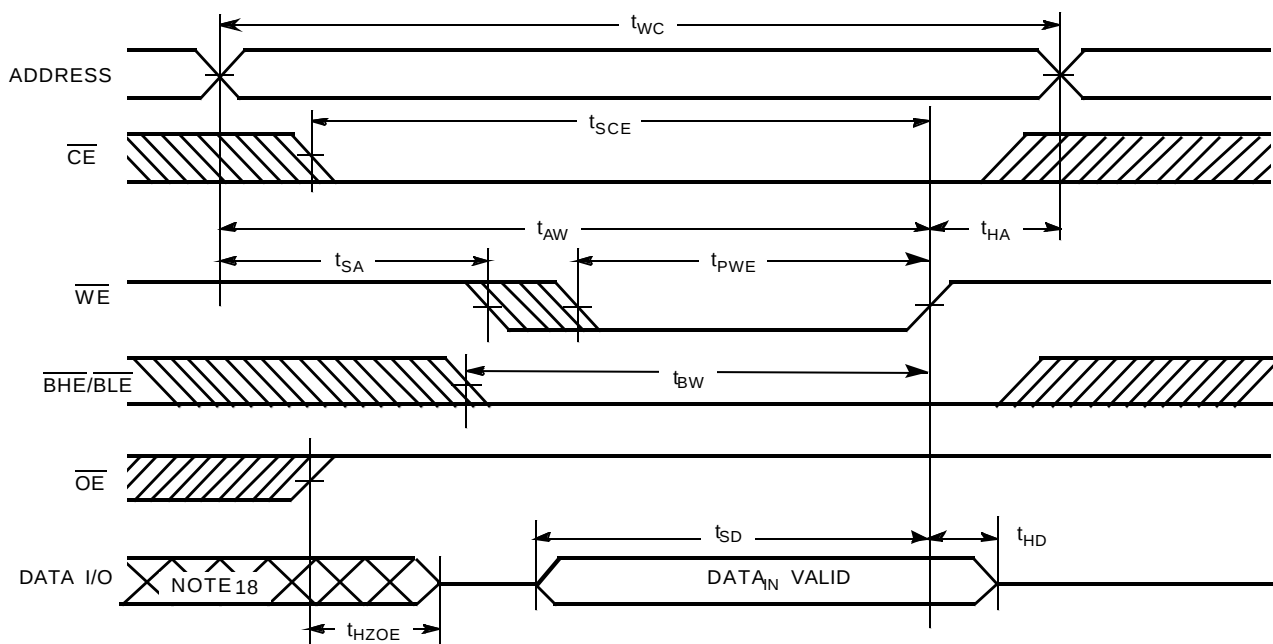
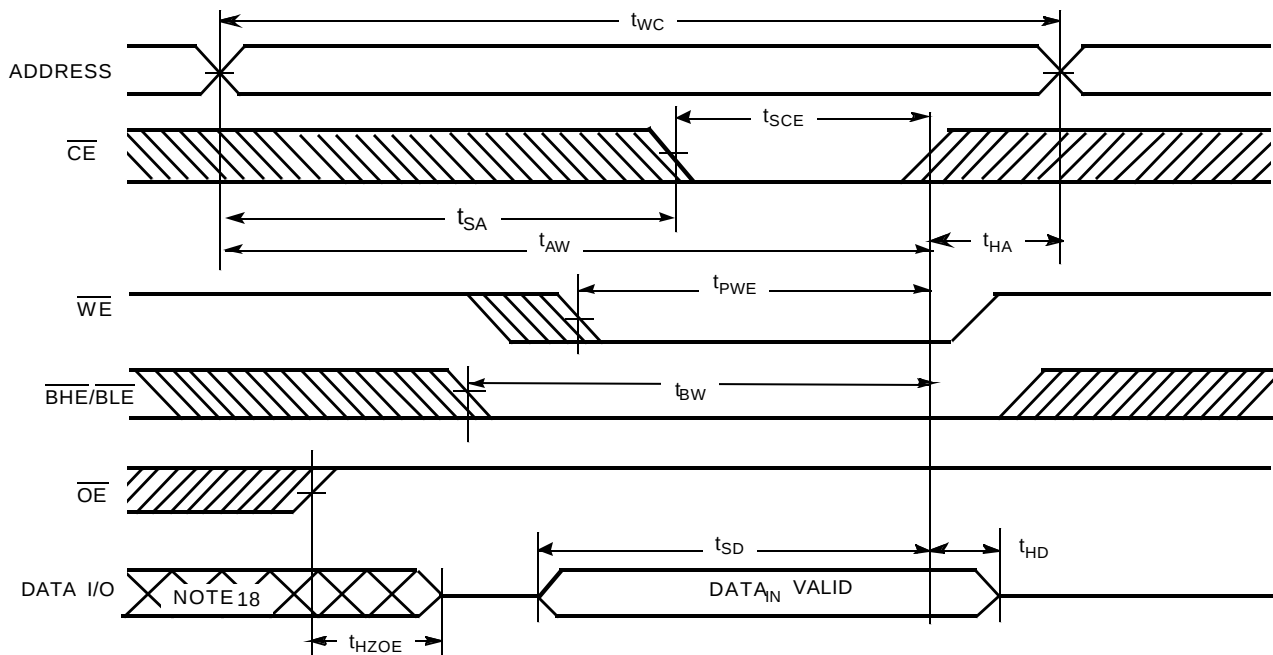


Read Cycle No. 2 ($\overline{\text{OE}}$ Controlled) ^[14, 15]

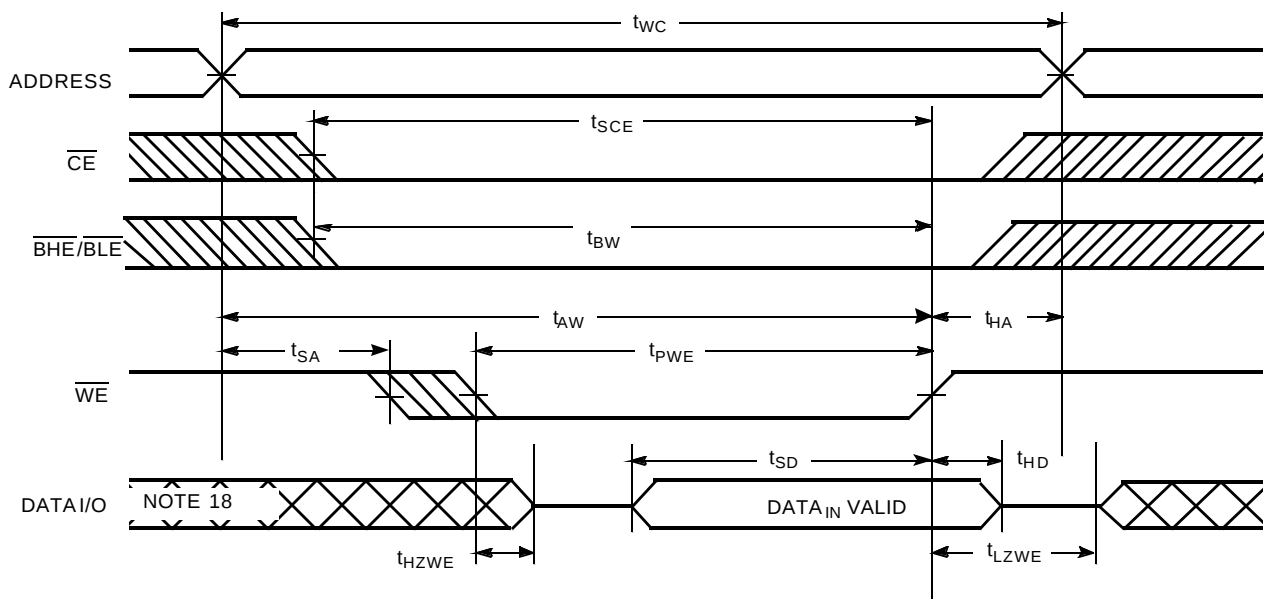
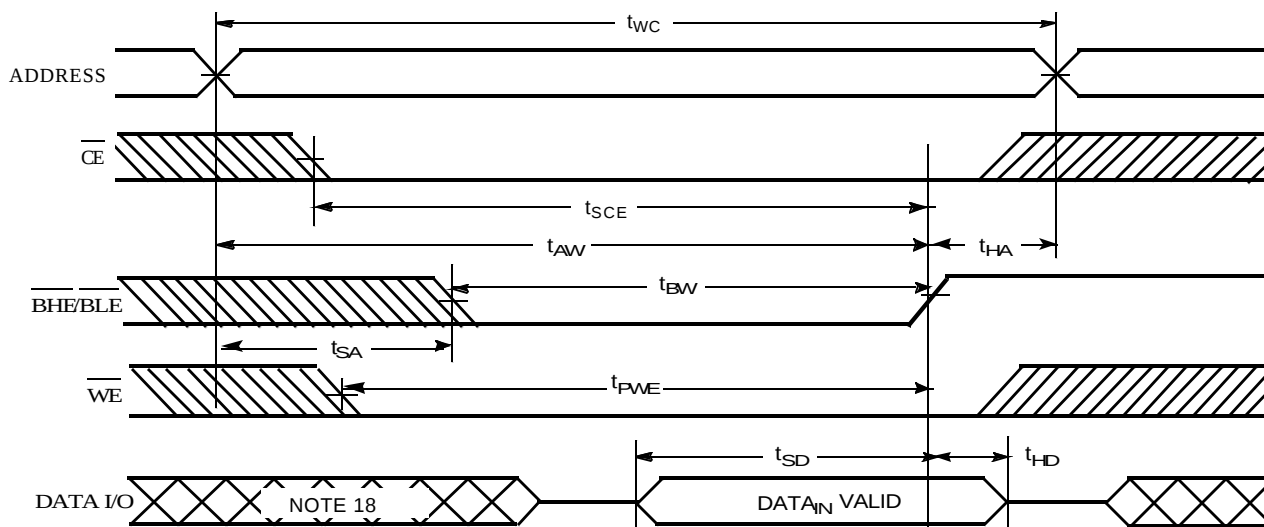


Notes:

13. Device is continuously selected. $\overline{\text{OE}}, \overline{\text{CE}} = V_{\text{IL}}, \overline{\text{BHE}}, \overline{\text{BLE}} = V_{\text{IL}}$.
14. $\overline{\text{WE}}$ is HIGH for read cycle.
15. Address valid prior to or coincident with $\overline{\text{CE}}, \overline{\text{BHE}}, \overline{\text{BLE}}$ transition LOW.

Switching Waveforms (continued)
Write Cycle No. 1 ($\overline{WE}$ Controlled) ^[12, 16, 17]

Write Cycle No. 2 ($\overline{CE}$ Controlled) ^[12, 16, 17]

Notes:

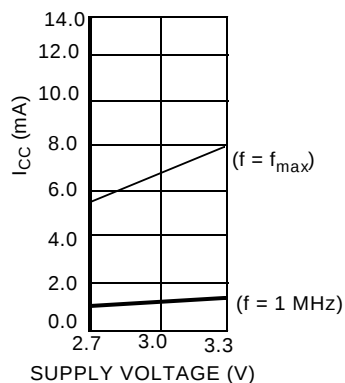
16. Data I/O is high-impedance if $\overline{OE} = V_{IH}$.
17. If $\overline{CE}$ goes HIGH simultaneously with $\overline{WE}$ HIGH, the output remains in a high-impedance state.
18. During this period, the I/Os are in output state and input signals should not be applied.

Switching Waveforms (continued)
Write Cycle No. 3 ($\overline{\text{WE}}$ Controlled, $\overline{\text{OE}}$ LOW)^[17]

Write Cycle No. 4 ($\overline{\text{BHE/BLER}}$ Controlled, $\overline{\text{OE}}$ LOW)^[17]


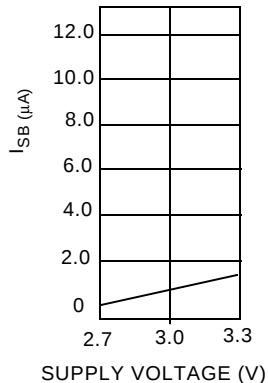
Typical DC and AC Parameters

(Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at $V_{CC} = V_{CC(yp.)}$, $T_A = 25^\circ\text{C}$)

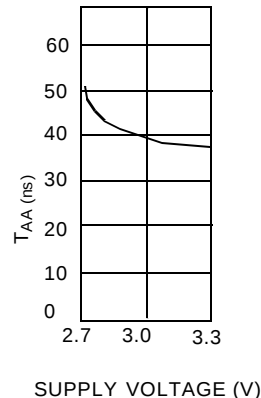
Operating Current vs. Supply Voltage



Standby Current vs. Supply Voltage



Access Time vs. Supply Voltage



Truth Table

CE	WE	OE	BHE	BLE	Inputs/Outputs	Mode	Power
H	X	X	X	X	High Z	Deselect/Power-Down	Standby (I_{SB})
X	X	X	H	H	High Z	Deselect/Power-Down	Standby (I_{SB})
L	H	L	L	L	Data Out (I/O_0 – I/O_{15})	Read	Active (I_{CC})
L	H	L	H	L	Data Out (I/O_0 – I/O_7); I/O_8 – I/O_{15} in High Z	Read	Active (I_{CC})
L	H	L	L	H	Data Out (I/O_8 – I/O_{15}); I/O_0 – I/O_7 in High Z	Read	Active (I_{CC})
L	H	H	L	L	High Z	Output Disabled	Active (I_{CC})
L	H	H	H	L	High Z	Output Disabled	Active (I_{CC})
L	H	H	L	H	High Z	Output Disabled	Active (I_{CC})
L	L	X	L	L	Data In (I/O_0 – I/O_{15})	Write	Active (I_{CC})
L	L	X	H	L	Data In (I/O_0 – I/O_7); I/O_8 – I/O_{15} in High Z	Write	Active (I_{CC})
L	L	X	L	H	Data In (I/O_8 – I/O_{15}); I/O_0 – I/O_7 in High Z	Write	Active (I_{CC})



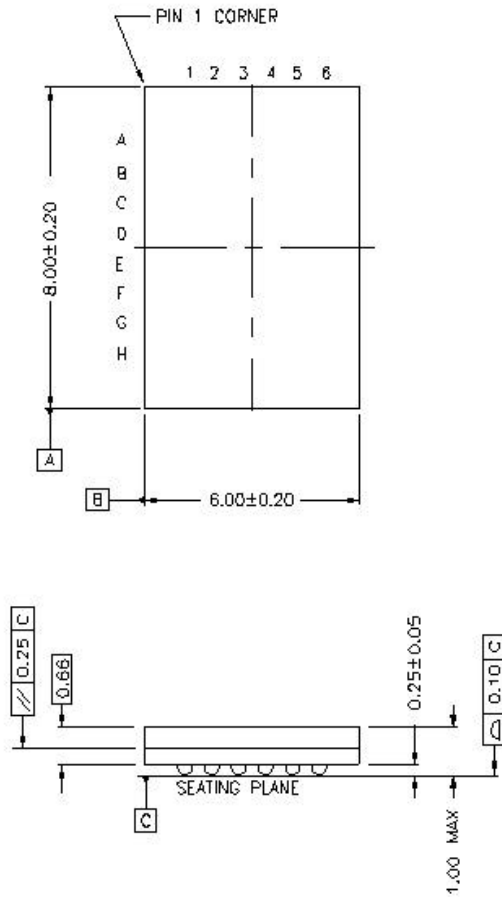
Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
70	WCMA2016U4B-FF70	FB48A	48-Ball Fine Pitch BGA	Industrial
55	WCMA2016U4B-FF55			

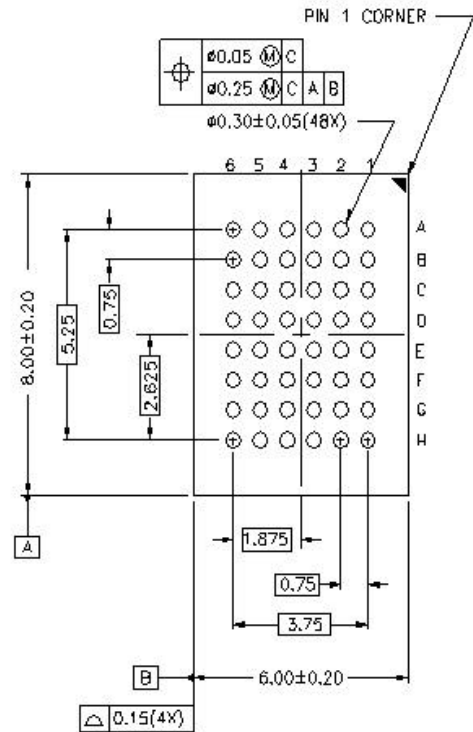
Package Diagrams

48-Ball (6.0 mm x 8.0 mm x 1.0 mm) Fine Pitch BGA, FB48A

Top View



Bottom View





Document Title: WCMA2016U4B, 128K x 16 STATIC RAM					
REV.	Spec #	ECN #	Issue Date	Orig. of Change	Description of Change
**	38-05320	117494	7/19/02	CBD	New Datasheet



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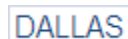
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- Гибкое ценообразование

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