CS-5143

Brushless DC Motor Driver/Controller (with back-emf sensing)

Description

The CS-5143 is a back emf sensing, brushless DC Motor Driver/ Controller IC. An onboard transconductance amplifier and tach circuitry control motor speed. Back emf induced by the motor in its windings determines rotor position and insures efficient commutation.

With its full wave drive capability, the CS-5143 fits in both star-connected and delta-connected motors. The commutation algorithm allows output phase switching at the optimum time to minimize torque ripple independent of motor type or motor load.

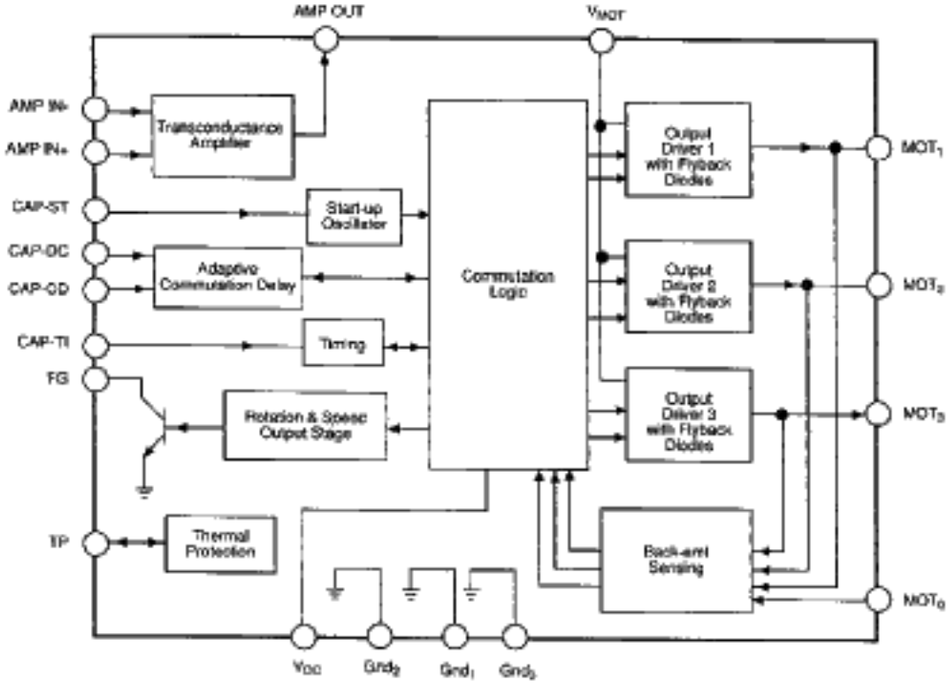
The output drive stages are protected from short circuit conditions and excessive power dissipation by on board thermal shutdown and current limiting circuitry.

The CS-5143 is used in sensorless hard disk drive motor control systems but it is equally well suited for brushless DC motors where improved motor performance and reduced discrete component count are needed.

Features

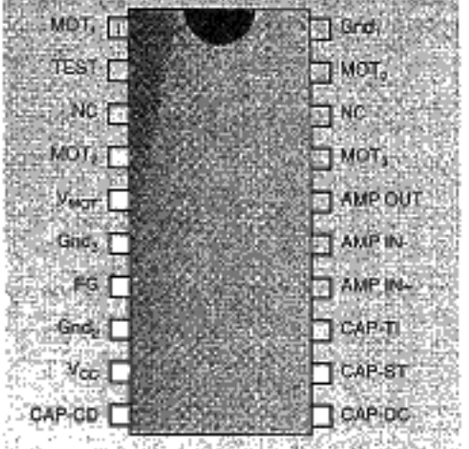
- Full Wave Commutation without Discrete Position Sensors
- Built in Start Up Circuitry
- Three Push-pull Output Drivers
  - 0.8A Output Current
  - Low Driver Saturation Current
  - Internal Flyback Diodes
- Tach Output Requires no Sensor Input
- Position Pulse for Phase Lock Loop Control
- Output Protection Circuitry
  - Built in Current Limit (0.8A typ)
  - Thermal Shutdown
- Tolerant to Variation in External Components
- Sleepmode Option

Block Diagram



Package Options

20 Lead SO Wide



Cherry Semiconductor

Cherry Semiconductor Corporation
2000 South County Trail
East Greenwich, Rhode Island 02818-1530
Tel: (401)885-3600 Fax (401)885-5786

Absolute Maximum Ratings

Supply Voltage Range 18V
Input voltage range (except V_{MOT}) ..... -0.3 to Vcc + 0.5V
V_{MOT} input range ..... -0.4 to 17V
Input voltages, all CAPs 2.5V
Electrostatic Discharge (Human Body Model) 4kV
Operating Temperature Range ..... 0° to 70°C
Junction Temperature Range ..... -55° to 150°C
Storage Temperature Range ..... -55° to 150°C
Lead Temperature Soldering: Reflow (SMD styles only) ..... 60 sec. max above 183°C, 230°C peak

Electrical Characteristics: V_{CC} = 14.5V; T_A = 25°C

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
■ Supply					
Supply Voltage Range	Note 1	4		18	V
Input Current Range	Note 2		5.5	8.0	mA
Output Driver Supply Voltage		3		16	V
■ Thermal Protection					
Shutdown Temp. (at the sensor)		130	140	150	°C
Temp. Drop Before Turn-on	After Shut Down Occurs		T_{SD}-30		°C
■ MOT_x					
Input Voltage Range		-0.5		V_{VMOT}	V
Input Bias Current	$0.5<V_x<V_{MOT}$-1.5V	-10			µA
Comparator Switching Level	Note 3	20	30	40	mV
Switch Level Variation		-3	0	3	mV
Comparator Hysteresis			75		µV
■ MOT_y, MOT_y and MOT_z					
Driver Output Voltage Range	I_{OUT}=100mA	0.4		V_{VMOT}-1.2	V
Dropout Voltage	I_{OUT}=500mA		2.1		V
Lower Transistor V_{SAT} Variation	I_{OUT}=100mA			180	mV
Upper Transistor V_{SAT} Variation	I_{OUT}=100mA			180	mV
Current Limit	Lower trans. V_{CE}=6V	600	800	1000	mA
Output Slew Rate	V_{VMOT}=12V, V_{CC}=13.2	0.279		2.520	V/µs
Upper Diode Forward Voltage	I_{OUT}=-500mA, Notes 4&5			1.8	V
Lower Diode Forward Voltage	I_{OUT}=500mA, Notes 4&5	-1.5			V
Peak Diode Current	Note 5			1	A
■ V_{MOT}					
Input Voltage Range		3		16	V
■ +AMP IN, -AMP IN and AMP OUT					
Input Voltage Range		-0.3		V_{CC}-1.7	V
Differential Input Voltage	No Latchup			V_{CC}	V

Electrical Characteristics: Continued

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
■ +AMP IN, -AMP IN and AMP OUT (Continued)					
Input Bias Current				650	nA
Input Capacitance			4		pF
Input Offset Voltage				10	mV
Output Sink Current		40			mA
Saturation Voltage	I_{IN}=40mA		1.5	2.1	V
Maximum Output Voltage		18			V
Slew Rate	R_L=330Ω, C_L=50pF		60		mA/µs
Transfer Gain		0.3			S
■ FG					
Output Voltage Low	I_{OUT}=1.6mA			0.4	V
Maximum Output Voltage		V_{CC}			V
Transition Time High-to-Low	R_L=10kΩ,C_L=50pF		0.5		µs
FG Frequency to Commutation Frequency Ratio			1:2		
FG Duty Factor			50		%
■ CAP-ST					
Output Sink Current		1.0	2.0	3.0	µA
Output Source Current		-3.0	-2.0	-1.0	µA
Lower Switch Level			0.2		V
Upper Switch Level			2.20		V
■ CAP-TI					
Output Sink Current			28		µA
Output Source Current HIGH			-57		µA
Output Source Current LOW			-5		µA
Lower Switch Level			50		mV
Middle Switch Level			300		mV
Upper Switch Level			2.20		V
■ CAP-CD					
Output Sink Current		10.6	16.2	22.0	µA
Output Source Current		-5.3	-8.1	-11.0	µA
Sink to Source Current Ratio		1.85	2.05	2.25	
Input Voltage Level Low		800	875	950	mV
Input Voltage Level High		2.2	2.4	2.6	V
■ CAP-DC					
Output Sink Current		10.1	15.5	20.9	µA
Output Source Current		-20.9	-15.5	-10.1	µA
Sink to Source Current Ratio		0.900	1.025	1.150	

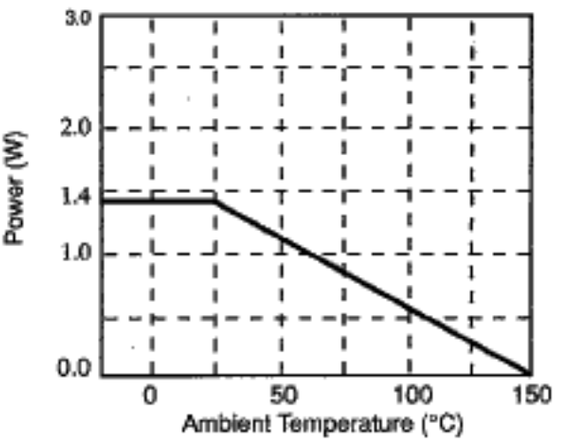
NOTES:
1. An unstabilized supply can be used.
2. V_{+AMP}=V_{CC}, all other inputs at 0V, all outputs at V_{CC} and I_{OUT}=0mA.
3. Switch levels are determined with respect to MOT_x, MOT_y, and MOT_z.
4. Drivers are in high impedance OFF state.
5. Short-circuit protection is afforded by limiting the driver output current and the IC temperature.

Package Pin Description

PACKAGE PIN #	PIN SYMBOL	FUNCTION
20L SO wide		
1	MOT_1	Driver Output 1
2	TEST	Disables outputs when 600µA nominal is input to this pin
3	NC	Not Connected
4	MOT_2	Driver Output 2
5	V_{MOT}	Output Driver Supply
6	Gnd_2	TACHO circuit ground
7	FG	Frequency Generator; open collector output; negative going edge valid
8	Gnd_1	Analog ground
9	V_{CC}	Voltage supply for logic circuitry
10	CAP-CD	Connection for external adaptive commutation timing delay capacitor 1
11	CAP-DC	Connection for external adaptive commutation timing delay capacitor 2
12	CAP-ST	Connection for start-up oscillator capacitor
13	CAP-TI	Connection for timing capacitor
14	AMP IN+	Non-inverting input for transconductance amplifier
15	AMP IN-	Inverting input for transconductance amplifier
16	AMP OUT	Output for transconductance amplifier (open collector)
17	MOT_3	Driver Output 3
18	NC	Not Connected
19	MOT_0	Motor center tap connection
20	Gnd_2	Output Power ground

Typical Performance Characteristics

Power Derating Curve



Definition of Terms

Adaptive Commutation Delay: an algorithm used during motor startup, it insures that the motor comes to its correct speed quickly. During the motor's steady state, it insures that the motor's rotation rate remains constant.

Back-emf: induced voltage in the unenergized coil in a brushless motor. The magnitude of the voltage is proportional to rotor speed and air gap between coil and magnet as well as coil and magnet properties.

Commutation Logic: on chip logic that controls the sequence, timing, and direction of current through the motor windings.

Flyback Pulse: the voltage generated in a coil when the current through it is changed abruptly.

Tachometer Signal: output signal generated by the motor control IC that is proportional to the motor's rotation rate.

Three Phase Motor: a motor with three coils; each coil is unenergized one third of the time.

Tristated: an output transistor placed in a high impedance mode.

Zero Crossing: The point at which the generated emf voltage crosses the motor's center tap voltage. The point occurs approximately half way between output commutations regardless of motor speed or loading.

Circuit Description

Output Stages - Performance and Protection

Three push-pull output stages are used to drive a sensorless three- phase motor in full-wave mode. Each output is capable of sourcing and sinking 600mA. The three outputs (MOT_1, MOT_2, MOT_3) occur in six different combinations or states (Table 1). In each state, two outputs are active; i.e. one is sourcing and the other is sinking current; the third is tristated.

TABLE 1. Output State Sequence for 1 Rotation of Motor

State	MOT_1	MOT_2	MOT_3
0	HI	LO	Hi Z
1	HI	Hi Z	LO
2	Hi Z	HI	LO
3	LO	HI	Hi Z
4	LO	Hi Z	HI
5	Hi Z	LO	HI

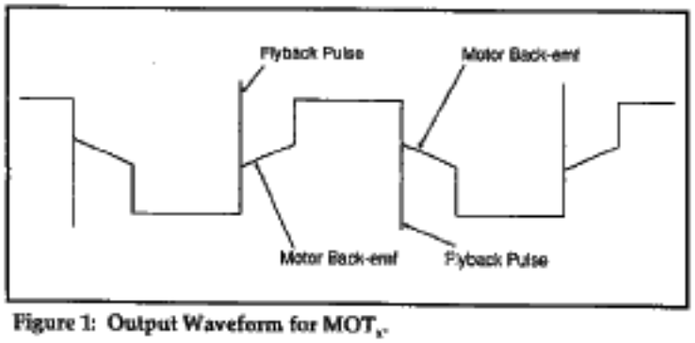


Figure 1: Output Waveform for MOT_x

The tristated output stage presents a high impedance to the motor and an internal comparator, associated with that output, measures the back-emf induced by the passing magnet in the unexcited coil. (Figure 1)

Each output stage is protected from damaging voltage transients, overheating and short circuit conditions. If a fault occurs on one output, all outputs are immediately tristated. On chip flyback diodes in each output stage absorb flyback voltages induced in the coils when their currents abruptly change. Thermal shutdown circuitry prevents die junction temperatures from exceeding 150°C (max) and built in hysteresis insures that the output stages do not reactivate before junction temperatures drop 30°C (typ). Short circuit protection limits output current to 1A max.

Commutation Logic

Commutation logic controls the timing and sequence of motor coil excitations. During startup, when no back emf signal is present, on chip timing signals are required to start the rotor spinning. Once the motor is rotating, different timing circuitry is used to keep the motor's rotation rate constant.

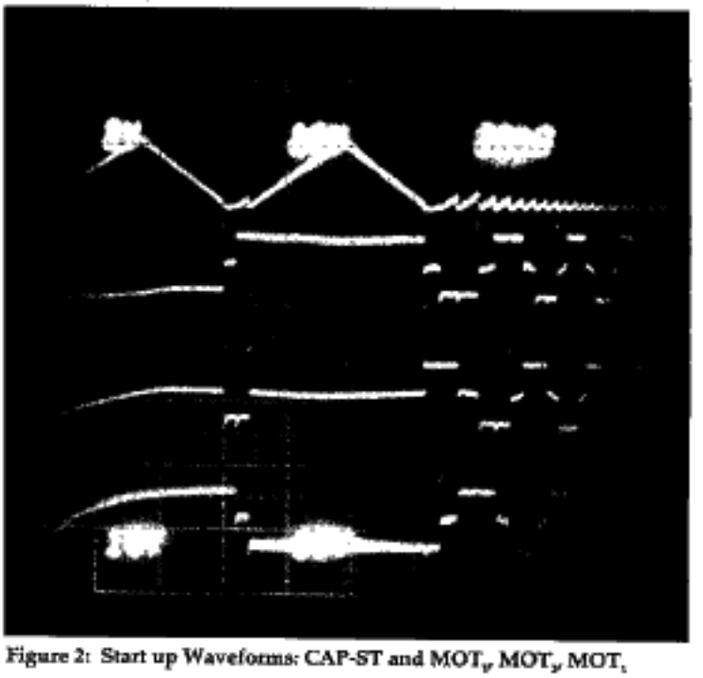


Figure 2: Start up Waveforms: CAP-ST and MOT_1, MOT_2, MOT_3

Circuit Description: continued

Motor Start Up

During startup, when the back-emf signal is absent, a start up oscillator generates commutation pulses (Figure 2). Oscillation frequency is determined by the equation:

$$T_{START} = 2 \times \text{CAP-ST or } f_{START} = \frac{1}{T_{START}}$$

where t is in seconds and CAP-ST is in μF. The startup oscillator is reset by each commutation pulse and therefore is only active during motor startup. The oscillator pulse causes the outputs to switch to their next state. This action continues until the motor is rotating fast enough to generate a back emf voltage that the IC can use in its commutation logic.

During startup, as the oscillator steps the motor through its sequential states, the motor will oscillate around each step. This oscillation must be damped sufficiently before the next step to insure that the motor does not rotate in reverse. Motor oscillation can be calculated from the equation:

$$f_{OSC} = \frac{1}{2\pi} \times \left(K_t \times I \times \frac{P}{J} \right)^{\frac{1}{2}}$$

where K_t = torque constant (Nm/ A)
I = current (A)
P = number of magnetic pole pairs
J = rotor inertia (kg/m2)

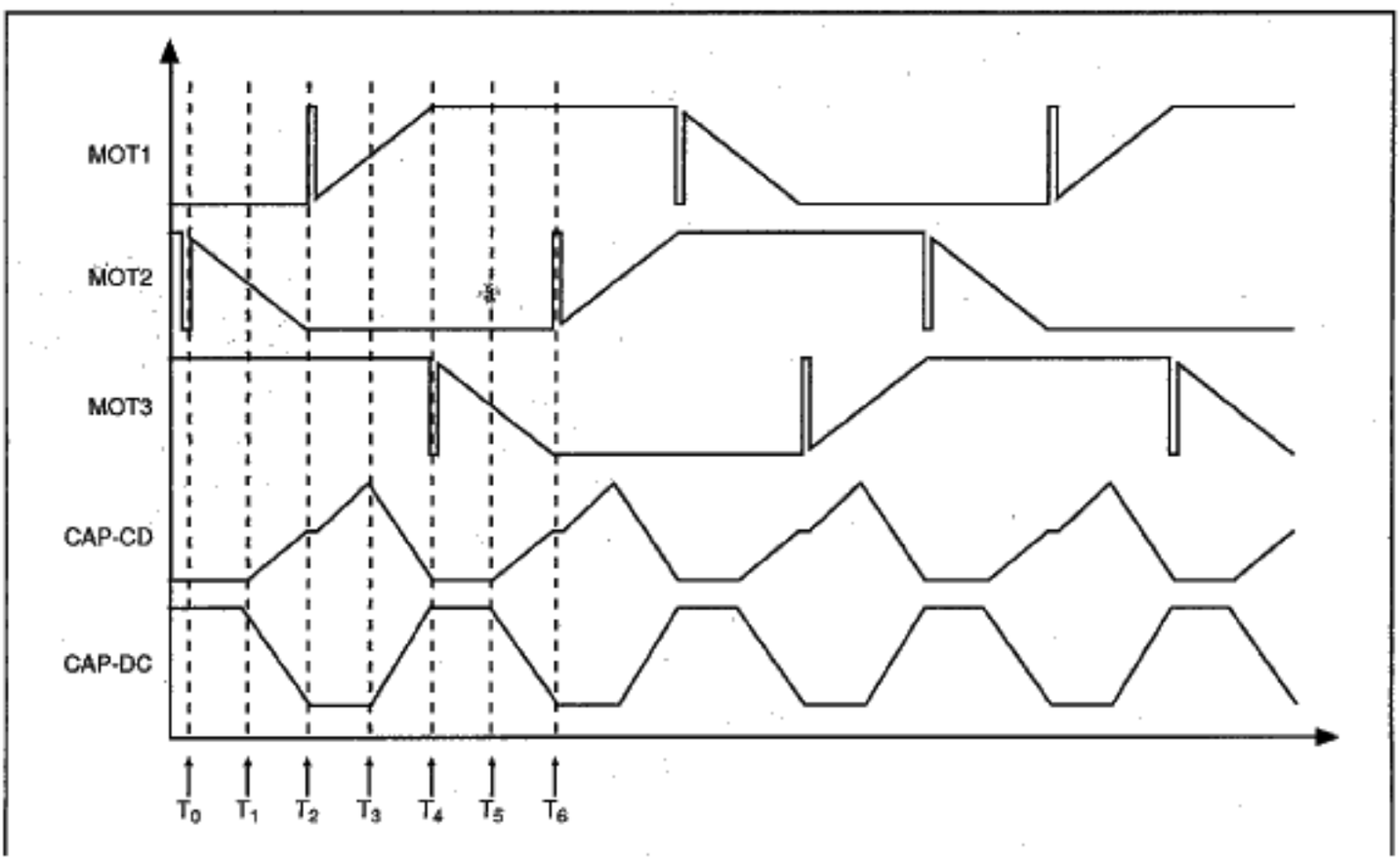
Once f_{OSC} is known, f_{START} is picked to be approximately one half the value of f_{OSC}, and the value of CAP-ST can be determined.

Adaptive Delay Commutation

Adaptive commutation begins during startup once the back emf signal is large enough and continues during the motor's steady state condition. Adaptive delay commutation circuitry controls the time that elapses between the zero crossing of the back-emf signal and commutation (the change of output states) (Figure 3).

As the motor approaches its intended speed, the back emf zero crossings occur more frequently and the switching time between output states (commutation), which occurs roughly half way between zero crossings, should decrease accordingly.

Commutation timing is controlled by two external capacitors, CAP-CD and CAP-DC. CAP-CD measures and divides the interval between zero crossings. CAP-DC stores the delay between the zero crossing and the commutation signal. Figure 3 shows the output voltage waveforms for all three motor drive phases and the two capacitors. At t_0, the delay time has been stored on CAP-DC. At t_1, a zero crossing occurs on output MOT_2. CAP-DC begins discharging towards its trigger threshold while CAP-CD begins charging. When CAP-DC reaches its threshold (t_2), commutation occurs and a flyback pulse appears at MOT_1. CAP-CD's charging is suspending during the flyback pulse to protect the commutation logic and prevent false triggering. After the flyback pulse, charging of CAP-CD resumes until a second zero crossing is detected on MOT_1 (t_3). CAP-CD now holds a voltage proportional to the time between zero crossings. It begins discharging at twice the rate it charged. When it reaches its preset threshold, a commutation signal is sent (t_4).



Adaptive Delay Commutation

During this time CAP-DC has been charging, in effect, storing the time delay between zero crossing and commutation. At t_4 it stops charging and holds its voltage until the next zero crossing (t_5). At t_5 CAP-DC begins discharging. When it reaches its threshold the next commutation signal is sent and the entire sequence (t_0 - t_5) is repeated.

CAP-DC and CAP-CD can be the same size. Their values are selected using the formula:

$$t_{delay} = C\left(\frac{1.3}{16.2\times10^6}\right) = 0.080C$$

where t_{delay} is given in ms and C in nF.

For adaptive commutation to work properly, the voltages in CAP-DC and CAP-CD must remain within the threshold voltage ranges.

The capacitor value also determines the lowest commutation frequency.

$$C = \frac{8.1\times10^6}{1.3f1} = \frac{6231}{f1}$$

where f_1 is the lowest commutation frequency in Hz and C is the capacitor value in nF.

Capacitor size and leakage current become important considerations under low frequency conditions. The capacitors must be large enough to ensure that, during low commutation frequency, the pin voltages remain below the level fixed by the current sources of the CAP-CD and CAP-CD pins. For the CS-5143 the pin voltage level is 2.3V typ. If capacitors are too leaky, their stored voltage will drop during the inactive phase of the commutation cycle and subsequent commutation will be distorted.

The Watchdog Timer

The watchdog timer is part of the circuitry used to prevent reverse motor rotation and motor oscillations that may occur during a blocked condition. The timer becomes active when an expected timing event does not occur during motor rotation; i.e. when the motor EMF does not recover from a negative going or positive going flyback pulse. Normally the flyback pulse only lasts tens of microseconds. But if the motor is stalled or in reverse, the timing is extended.

The watchdog timer frequency must be chosen carefully. If it is too high, eddy currents in the motor windings may trigger the circuit. If it is too low, the motor may run in reverse.

Watch dog timing depends on the value of capacitor CAP-TI. Within a commutation period, watchdog time is the time it takes to charge capacitor CAP-TI from 300mV to 2.2V with a 5µ A current. The size of the capacitor is

$$C = 2.63\times t$$

where t is in ms and the capacitor value is in nF.

External RC Network

Flyback pulses on the motor windings cause high frequency interference and acoustic noise. These pulses can be damped and acoustic noise attenuated by placing RC networks in parallel with the motor windings (Figure 4).

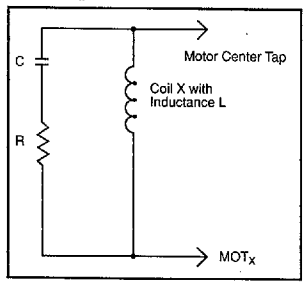


Figure 4: RC Network

However, the added RC network increases overall system power consumption and interferes with back emf sensing. Therefore the network components must be carefully chosen.

The values of R and C are related to coil inductance, motor rotation rate and the voltage needed to damp the coil after it is de-energized. The damping voltage and motor rotation are related by the equation

$$V_{DAMP} = e^{-w_O t}, \text{ or } W_O = \frac{\ln(V_{DAMP})}{t}$$

where w_o is the motor speed in rad/sec.

The value of the capacitor follows from the relationship

$$(W_O)^2 = \frac{1}{LC}$$

where L is the inductance of the coil. Solving for the capacitance gives

$$C = \frac{1}{(W_O)^2 L}$$

The value of R follows from

$$R = 2\left(\frac{L}{C}\right)^{\frac{1}{2}}$$

where the value of C was calculated in the previous equation.

The Tachometer Signal

The tachometer output signal is proportional to the total number of back-emf zero crossings per motor revolution. There are 6 pulses per IC output cycles in a 3 phase system.

$$f_G = \frac{(\text{no. of motor poles})\left(\frac{\text{rev}}{\text{sec}}\right)\left(\frac{6\text{ pulses}}{\text{pole}}\right)}{2}$$

The negative going edges of the tachometer signal generate interrupts at the system microprocessor. The accuracy of the signal is primarily dependent on the symmetry of motor construction.

The electrical accuracy of the tachometer signal is optimized by giving it its own ground pin.

Circuit Description: continued

Motor Control

Operational Transconductance Amplifier

A separate externally compensated transconductance amplifier is included on chip. It can be used as a control amplifier or a level shifter in conjunction with a switching power supply.

When used as an analog control amplifier, the OTA drives an external analog power transistor. When used with a switching power supply, the output drives a switching power transistor (Figure 5.)

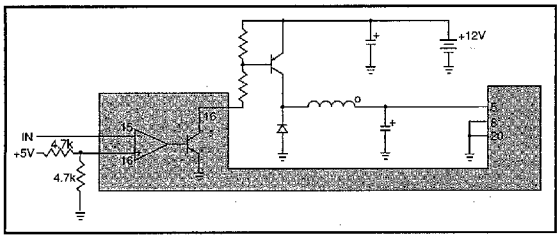


Figure 5: PWM Speed Control with OTA used as a Level Converter

Motor Control

The OTA can be used in either a voltage control or a current control application. In the voltage control application, the output impedance is increased for a particular frequency (commutation frequency). In the current control application, a resistor placed between Gnd2 and Gnd 1 is required. Both grounds are supply returns. Gnd 2 has a small constant current with respect to Gnd 1.

Motor Braking

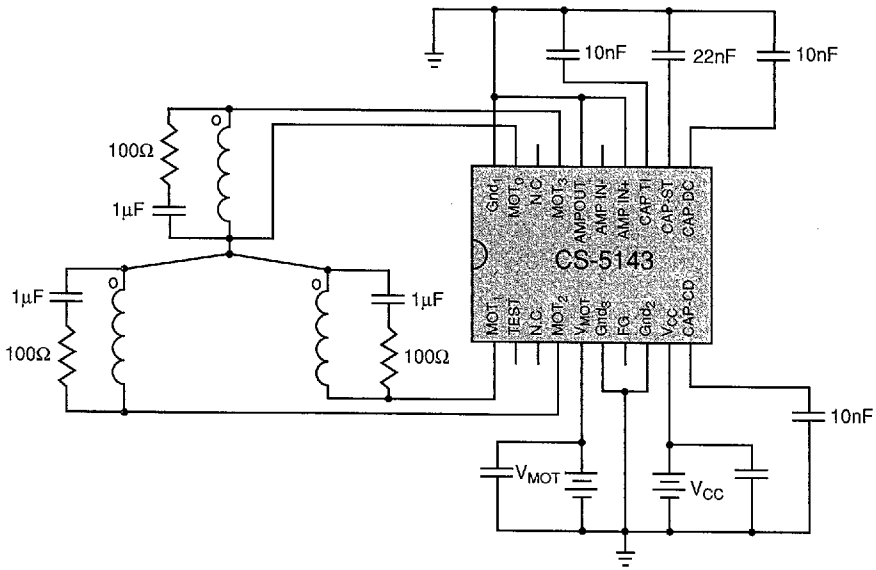
The CS-5143 does not have a built-in braking feature. However the motor acts as a voltage generator as it spins to rest following power disruption. The internal flyback diodes rectify the voltage. If a current drain is placed on pin V_{MOT}, a braking torque proportional to the drain current is exerted on the motor.

Additional Features

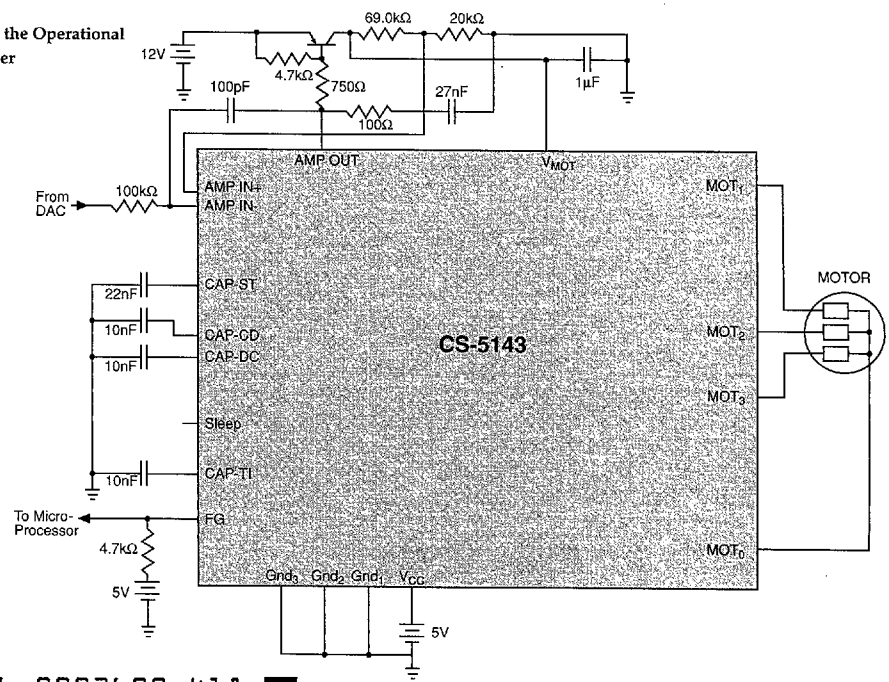
"Sleep" Mode=input of 600µA (nominal) to the TEST pin disables the output drivers and startup circuitry. IC current consumption is then less than 8mA in the V_{CC} line. Note that this pin should float if current is not being input. Grounding this pin will disable the over temperature shut down circuitry.

"Output Preset"=prior to operation, pulling the -AMPIN pin up to a Vbe above V_{CC} (current limited to 200µA) sets the output state such that MOT_3 sources to MOT_2 with MOT_1 tristated.

CS-5143 with RC Damping Network



CS-5143 Application using the Operational Transconductance Amplifier



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Package Specification

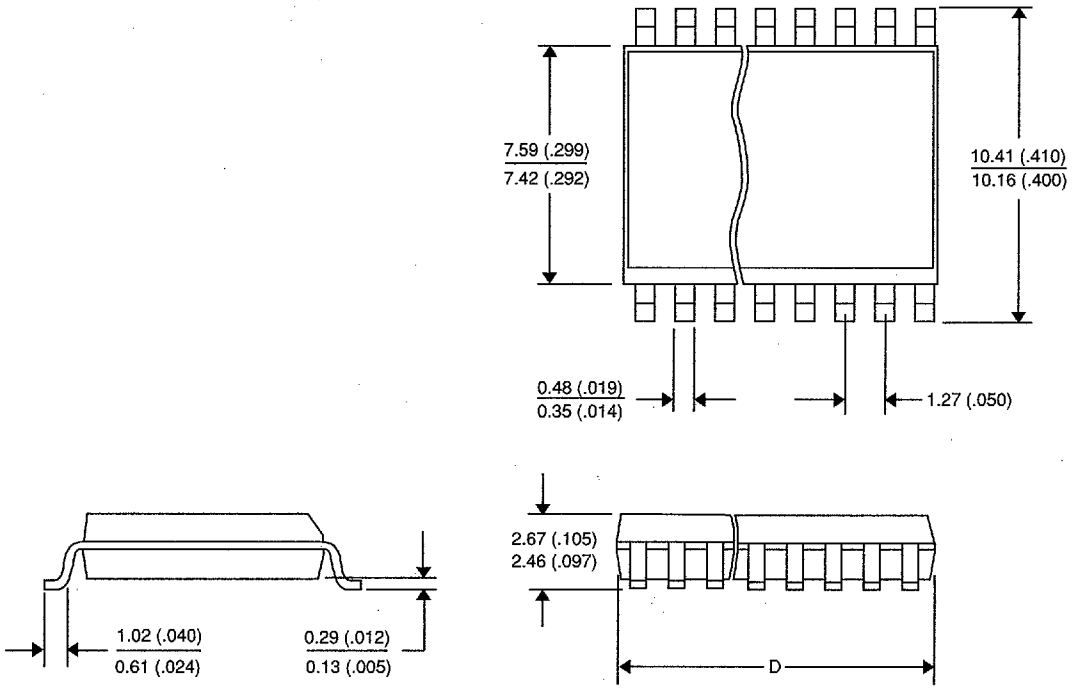
PACKAGE DIMENSIONS IN mm (INCHES)

Lead Count	D			
	Metric		English	
	Max	Min	Max	Min
20L SO WIDE	12.95	12.70	.510	.500

PACKAGE THERMAL DATA

Thermal Data		20L SO Wide	
$R_{\theta JC}$	typ	17	°C/W
$R_{\theta JA}$	typ	90	°C/W

SO Wide



Ordering Information

Part Number	Description
CS-5143DW20	20L SO Wide

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