DS1677
Portable System Controller

www.maxim-ic.com

GENERAL DESCRIPTION

The DS1677 portable system controller is a circuit that incorporates many of the functions necessary for low-power portable products integrated into one chip. The device provides a real-time clock (RTC), NV RAM controller, microprocessor monitor, power-fail warning, and a 3-channel, 8-bit analog-to-digital converter (ADC). Communication with the DS1677 is established through a simple 3-wire interface.

The RTC provides seconds, minutes, hours, day, date, month, and year information with leap year compensation. The RTC also provides an alarm interrupt. This interrupt works when the DS1677 is powered by the system power supply or when in battery-backup operation so the alarm can be used to wake up a system that is powered down.

Automatic backup and write protection of an external SRAM is provided through the V_{CCO} and $\overline{CEO}$ pins. The backup energy source used to power the RTC is also used to retain RAM data in the absence of V_{CC} through the V_{CCO} pin. $\overline{CEO}$, the chip-enable output to SRAM, is controlled during power transients to prevent data corruption.

ORDERING INFORMATION

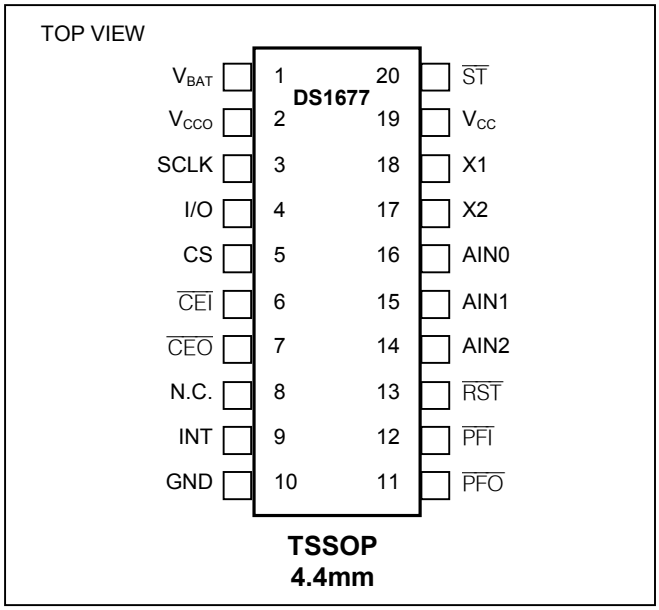
PART*	VOLTAGE (V)	PIN-PACKAGE	TOP MARK†
DS1677E	5.0	20 TSSOP	DS1677-5
DS1677E+	5.0	20 TSSOP	DS1677-5

** All devices are specified over the 0°C to +70°C operating range.*
† A "+" anywhere on the top mark denotes a lead-free device.
+ Denotes a lead-free/RoHS-compliant device.

FEATURES

- **Provides Real-Time Clock**
  Counts Seconds, Minutes, Hours, Date of the Month, Month, Day of the Week, and Year with Leap Year Compensation Valid Up to 2100
  Power Control Circuitry Supports System Power-On from Day/Time Alarm
- **Microprocessor Monitor**
  Halts Microprocessor During Power-Fail
  Automatically Restarts Microprocessor After Power Failure
  Monitors Pushbutton for External Override
  Halts and Resets an Out-of-Control Microprocessor
- **NV RAM Control**
  Automatic Battery Backup and Write Protection to External SRAM
- **3-Channel, 8-Bit ADC**
- **Simple 3-Wire Interface**
- **+5.0V Operation**
- **1.25V Threshold Detector for Power-Fail Warning**
- **UL Recognized**

PIN CONFIGURATION



DETAILED DESCRIPTION

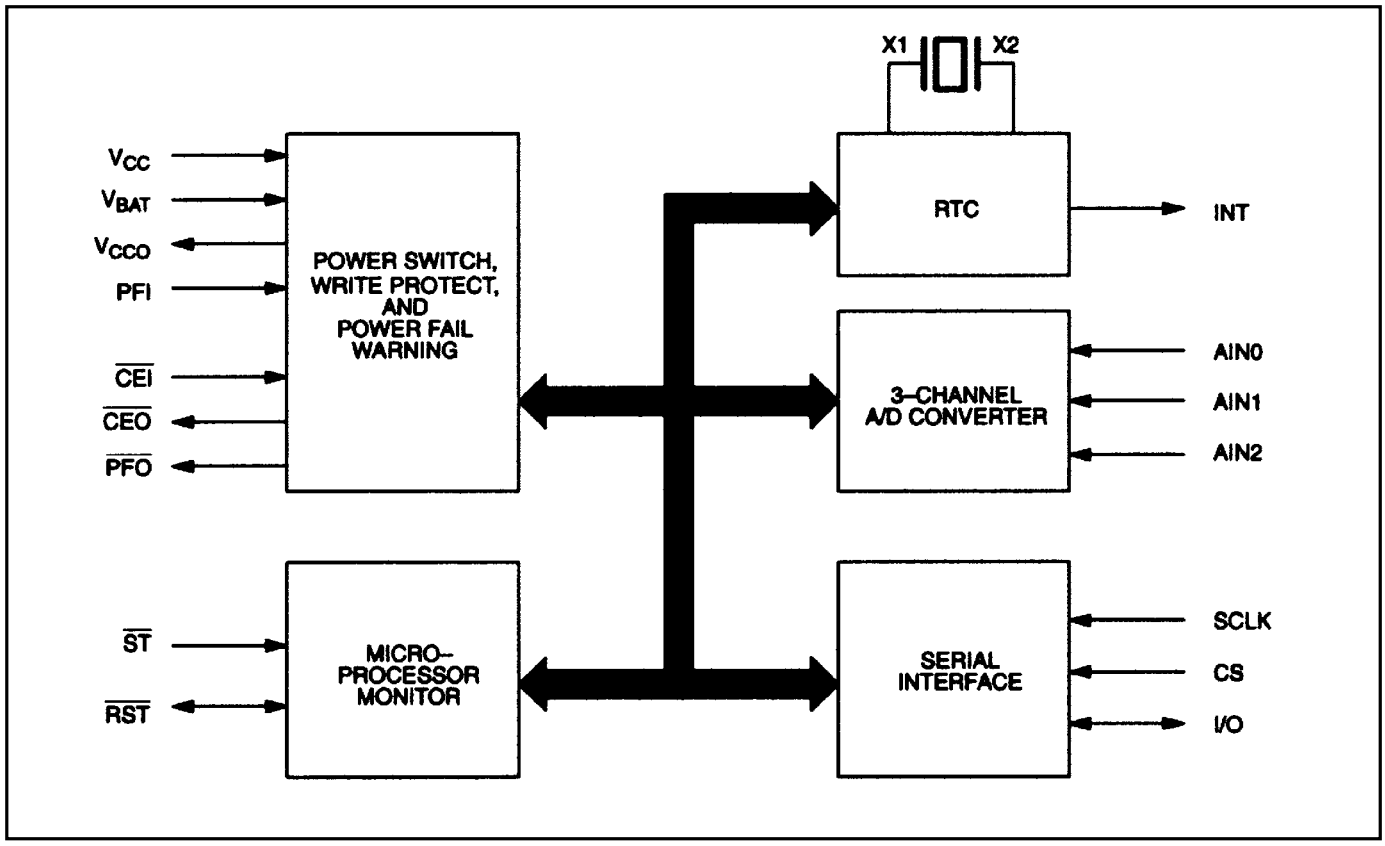
The microprocessor monitor circuitry of the DS1677 provides three basic functions. First, a precision temperature-compensated reference and comparator circuit monitors the status of V_{CC}. When an out-of-tolerance condition occurs, an internal power-fail signal is generated which forces the to $\overline{RST}$ the active state. When V_{CC} returns to an in-tolerance condition, the $\overline{RST}$ signal is kept in the active state for 250ms to allow the power supply and processor to stabilize. The DS1677 debounces a pushbutton input and guarantees an active $\overline{RST}$ pulse width of 250ms. The third function is a watchdog timer. The DS1677 has an internal timer that forces the $\overline{RST}$ signal to the active state if the strobe input is not driven low prior to watchdog timeout.

The DS1677 also provides a 3-channel 8-bit successive approximation ADC. The converter has an internal 2.55V (typical) reference voltage generated by an on-board band-gap circuit. The ADC is monotonic (no missing codes) and has an internal analog filter to reduce high-frequency noise.

OPERATION

The block diagram in Figure 1 shows the main elements of the DS1677. The following paragraphs describe the function of each pin.

DS1677 BLOCK DIAGRAM Figure 1



PIN DESCRIPTION

PIN	NAME	FUNCTION
1	V_{BAT}	Battery Input for Standard 3V Lithium Cell or Other Energy Source. UL recognized to ensure against reverse charging when used with a lithium battery. Go to www.maxim-ic.com/qa/info/ul/.
2	V_{CCO}	External SRAM Power Supply Output. This pin is internally connected to V_{CC} when V_{CC} is within nominal limits. However, during power-fail V_{CCO} is internally connected to the V_{BAT} pin. Switchover occurs when V_{CC} drops below the lower of V_{BAT} or 2.7V.
3	SCLK	Serial Clock Input. Used to synchronize data movement on the serial interface.
4	I/O	Data Input/Output. This pin is the bidirectional data pin for the 3-wire interface.
5	CS	Chip Select. Must be asserted high during a read or a write for communication over the 3-wire serial interface. CS has an internal 40kΩ pulldown resistor.
6	$\overline{CEI}$	RAM Chip-Enable In. Must be driven low to enable the external RAM.
7	$\overline{CEO}$	RAM Chip-Enable Out Low. Active-low chip-enable output for low-order SRAM byte.
8	N.C.	No Connection
9	INT	Interrupt Output. This pin is an active-high output that can be used as an interrupt input to a microprocessor. The INT output remains high as long as the status bit causing the interrupt is present and the corresponding interrupt-enable bit is set. The INT pin operates when the DS1677 is powered by V_{CC} or V_{BAT}.
10	GND	Ground. DC power is provided to the device on this pin.
11	$\overline{PFO}$	Active-Low Power-Fail Output. This pin goes low and sinks current when PFI is less than 1.25V; otherwise this pin remains high.
12	$\overline{PFI}$	Active-Low Power-Fail Input. When PFI is less than 1.25V, $\overline{PFO}$ goes low; otherwise $\overline{PFO}$ remains high. Connect PFI to GND or V_{CC} when not used.
13	$\overline{RST}$	Active-Low Reset. The $\overline{RST}$ pin functions as a microprocessor reset signal. This pin is driven low 1) when V_{CC} is outside of nominal limits; 2) when the watchdog timer has timed out; 3) during the power up reset period; and 4) in response to a pushbutton reset. The $\overline{RST}$ pin also functions as a pushbutton reset input. When the $\overline{RST}$ pin is driven low, the signal is debounced and timed such that a $\overline{RST}$ signal of at least 250ms is generated. This pin has an open-drain output with an internal 47kΩ pullup resistor.
14, 15, 16	AIN2, AIN1, AIN0	Analog Inputs. These pins are the three analog inputs for the 3-channel ADC.
17, 18	X2, X1	Connections for Standard 32.768kHz Quartz Crystal. For greatest accuracy, the DS1670 must be used with a crystal that has a specified load capacitance of 6pF. There is no need for external capacitors or resistors. Note: X1 and X2 are very high-impedance nodes. It is recommended that they and the crystal be guard-ringed with ground and that high frequency signals be kept away from the crystal area. For more information on crystal selection and crystal layout considerations, refer to *Application Note 58: Crystal Considerations with Dallas Real Time Clocks*. The DS1677 does not function without a crystal.
19	V_{CC}	+5.0V Input DC Power
20	$\overline{ST}$	Active-Low Strobe Input. The strobe input pin is used with the watchdog timer. If the $\overline{ST}$ pin is not driven low within the watchdog time period, the $\overline{RST}$ pin is driven low.

POWER-UP/POWER-DOWN CONSIDERATIONS

When V_{CC} is applied to the DS1677 and reaches a level greater than V_{CCTP} (power-fail trip point), the device becomes fully accessible after t_{RPU} (250ms typical). Before t_{RPU} elapses, all inputs are disabled. When V_{CC} drops below V_{CCSW}, the device is switched over to the V_{BAT} supply.

During power-up, when V_{CC} returns to an in-tolerance condition, the $\overline{RST}$ pin is kept in the active state for 250ms (typical) to allow the power supply and microprocessor to stabilize.

ADDRESS/COMMAND BYTE

The command byte for the DS1677 is shown in Figure 2. Each data transfer is initiated by a command byte. Bits 0 through 6 specify the address of the registers to be accessed. The MSB (bit 7) is the Read/Write bit. This bit specifies whether the accessed byte will be read or written. A read operation is selected if bit 7 is a zero and a write operation is selected if bit 7 is a one. The address map for the DS1677 is shown in Figure 3.

ADDRESS/COMMAND BYTE Figure 2

7	6	5	4	3	2	1	0
$\overline{RD}$ / WR	A6	A5	A4	A3	A2	A1	A0

DS1677 ADDRESS MAP Figure 3

	BIT7							BIT0
00	0	10 SECONDS			SECONDS			
01	0	10 MINUTES			MINUTES			
02	0	12/24	10 HR A/P	10 HR	HOURS			
03	0	0	0	0	0	DAY		
04	0	0	10 DATE		DATE			
05	0	0	0	10 MO.	MONTH			
06	10 YEAR				YEAR			
07	M	10 SEC ALARM			SECONDS ALARM			
08	M	10 MIN ALARM			MINUTES ALARM			
09	M	12/24	10 HR A/P	10 HR	HOUR ALARM			
0A	M	0	0	0	DAY ALARM			
0B	CONTROL REGISTER							
0C	STATUS REGISTER							
0D	WATCHDOG REGISTER							
0E	ADC REGISTER							
0F–7F	RESERVED							

CLOCK, CALENDAR, AND ALARM

The time and calendar information is accessed by reading/writing the appropriate register bytes. Note that some bits are set to zero. These bits will always read zero regardless of how they are written. Also note that registers 0Fh to 7Fh are reserved. These registers will always read zero regardless of how they are written. The contents of the time, calendar, and alarm registers are in the binary-coded decimal (BCD) format.

The DS1677 can run in either 12-hour or 24-hour mode. Bit 6 of the hours register is defined as the 12- or 24-hour mode select bit. When high, the 12-hour mode is selected. In the 12-hour mode, bit 5 is the AM/PM bit with logic one being PM. In the 24-hour mode, bit 5 is the second 10-hour bit (20–23 hours).

The DS1677 also contains a time of day alarm. The alarm registers are located in registers 07h to 0Ah. Bit 7 of each of the alarm registers are mask bits (see Table 1). When all of the mask bits are logic 0, an alarm will occur once per week when the values stored in timekeeping registers 00h to 03h match the values stored in the time of day alarm registers. An alarm will be generated every day when mask bit of the day alarm register is set to one. An alarm will be generated every hour when the day and hour alarm mask bits are set to one. Similarly, an alarm will be generated every minute when the day, hour, and minute alarm mask bits are set to one. When day, hour, minute, and seconds alarm mask bits are set to one, an alarm will occur every second.

TIME OF DAY ALARM BITS Table 1

ALARM REGISTER MASK BITS (BIT 7)				DESCRIPTION
SECONDS	MINUTES	HOURS	DAYS	
1	1	1	1	Alarm once per second.
0	1	1	1	Alarm when seconds match.
0	0	1	1	Alarm when minutes and seconds match.
0	0	0	1	Alarm when hours, minutes and seconds match.
0	0	0	0	Alarm when day, hours, minutes and seconds match.

SPECIAL PURPOSE REGISTERS

The DS1677 has two additional registers (control register and status register) that control the RTC and interrupts.

CONTROL REGISTER

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
$\overline{\text{EOSC}}$	WP	AIS1	AIS0	0	0	0	AIE

$\overline{\text{EOSC}}$ (Enable Oscillator). This bit, when set to logic 0 will start the oscillator. When this bit is set to a logic 1, the oscillator is stopped and the DS1677 is placed into a low-power standby mode with a current drain of less than 200nA when in battery-backup mode. When the DS1677 is powered by V_{CC}, the oscillator is always on regardless of the status of the $\overline{\text{EOSC}}$ bit; however, the RTC is incremented only when $\overline{\text{EOSC}}$ is a logic 0.

WP (Write Protect). Before any write operation to the real time clock or any other registers, this bit must be logic 0. When high, the write protect bit prevents a write operation to any register.

AIS0–AIS1 (Analog Input Select). These two bits are used to determine the analog input for the analog-to-digital conversion. Table 2 lists the specific analog input that is selected by these 2 bits.

AIE (Alarm Interrupt Enable). When set to a logic 1, this bit permits the Interrupt Request Flag (IRQF) bit in the status register to assert INT. When the AIE bit is set to logic 0, the IRQF bit does not initiate the INT signal.

ANALOG INPUT SELECTION Table 2

AIS1	AIS0	ANALOG INPUT
0	0	NONE
0	1	AIN0
1	0	AIN1
1	1	AIN2

STATUS REGISTER

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
CU	LOBAT	0	0	0	0	0	IRQF

CU (Conversion Update In Progress). When this bit is a one, an update to the ADC Register (register 0Eh) will occur within 488 µs. When this bit is a zero, an update to the ADC Register will not occur for at least 244 µs.

LOBAT (Low Battery Flag). This bit reflects the status of the backup power source connected to the V_{BAT} pin. When V_{BAT} is greater than 2.5V, LOBAT is set to a logic 0. When V_{BAT} is less than 2.3V, LOBAT is set to a logic 1.

IRQF (Interrupt Request Flag). A logic 1 in the Interrupt Request Flag bit indicates that the current time has matched the time of day Alarm registers. If the AIE bit is also a logic 1, the INT pin will go high. IRQF is cleared by reading or writing to any of the alarm registers.

POWER-UP DEFAULT STATES

These bits are set to a one upon initial power-up: $\overline{EOSC}$, TD0 and TD1. These bits are cleared upon initial power-up: WP, AIS1, and AIS0.

NONVOLATILE SRAM CONTROLLER

The DS1677 provides automatic backup and write protection for an external SRAM. This function is provided by gating the chip enable signal and by providing a constant power supply through the V_{CCO} pin.

The DS1677 nonvolatizes the external SRAM by write protecting the SRAM and by providing a back–up power supply in the absence of V_{CC}. When V_{CC} falls below V_{PF}, access to the external SRAM is prohibited by forcing $\overline{CE0}$ high regardless of the level of $\overline{CEI}$. Upon power-up, access is prohibited until the end of t_{RPU}.

POWER-FAIL COMPARATOR

The PFI input is connected to an internal reference. If PFI is less than 1.25V, $\overline{PFO}$ goes low. The power-fail comparator can be used as an undervoltage detector to signal an impending power supply failure. $\overline{PFO}$ can be used as a µP interrupt input to prepare for power-down. For battery conservation, the comparator is turned off and $\overline{PFO}$ is held low when in battery-backed mode

ADDING HYSTERESIS TO THE POWER-FAIL COMPARATOR

Hysteresis adds a noise margin to the power-fail comparator and prevents $\overline{PFO}$ from oscillating when V_{IN} is near the power-fail comparator trip point. Figure 8 shows how to add hysteresis to the power-fail comparator. Select the ratio of R1 and R2 such that PFI sees 1.25V when V_{IN} falls to the desired trip point (V_{TRIP}). Resistors R2 and R3 add hysteresis. R3 will typically be an order of magnitude greater than R1 or R2. R3 should be chosen in manner to prevent it from loading down the $\overline{PFO}$ pin. Capacitor C1 adds noise filtering and has a value of typically 1.0µF. See Figure 8 for a schematic diagram and equations.

MICROPROCESSOR MONITOR

The DS1677 monitors three vital conditions for a microprocessor: power supply, software execution, and external override.

First, a precision temperature-compensated reference and comparator circuit monitors the status of V_{CC}. When an out-of-tolerance condition occurs, an internal power-fail signal is generated which forces the $\overline{RST}$ pin to the active state thus warning a processor-based system of impending power failure. When V_{CC} returns to an in-tolerance condition upon power-up, the reset signal is kept in the active state for 250ms (typical) to allow the power supply and microprocessor to stabilize. Note however that if the $\overline{EOSC}$ bit is set to a logic 1 (to disable the oscillator during battery-backup mode), the $\overline{RST}$ signal will be kept in an active state for 250ms plus the startup time of the oscillator.

The second monitoring function is push-button reset control. The DS1677 provides for a push–button switch to be connected to the $\overline{RST}$ output pin. When the DS1677 is not in a reset cycle, it continuously monitors the $\overline{RST}$ signal for a low going edge. If an edge is detected, the DS1677 will debounce the switch by pulling the $\overline{RST}$ line low. After the internal 250ms timer has expired, the DS1677 will continue to monitor the $\overline{RST}$ line. If the line is still low, the DS1677 will continue to monitor the line looking for a rising edge. Upon detecting release, the DS1677 will force the $\overline{RST}$ line low and hold it low for 250ms.

The third microprocessor monitoring function provided by the DS1677 is a watchdog timer. The watchdog timer function forces $\overline{RST}$ to the active state when the $\overline{ST}$ input is not stimulated within the predetermined time period. The time period is set by the Time Delay (TD) bits in the Watchdog Register. The time delay can be set to 250ms, 500ms, or 1000ms (see Figure 4). If TD0 and TD1 are both set to zero, the watchdog timer is disabled. When enabled, the watchdog timer starts timing out from the set time period as soon as $\overline{RST}$ is inactive. The default setting is for the watchdog timer to be enabled with 1000 ms time delay. If a high-to-low transition occurs on the $\overline{ST}$ input pin prior to time out, the watchdog timer is reset and begins to time out again. If the watchdog timer is allowed to time out, then the $\overline{RST}$ signal is driven to the active state for 250ms (typical). The $\overline{ST}$ input can be derived from microprocessor address signals, data signals, and/or control signals. To guarantee that the watchdog timer does not time out, a high-to-low transition must occur at or less than the minimum period.

WATCHDOG TIMEOUT CONTROL Figure 4

WATCHDOG REGISTER

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
0	0	0	0	0	0	TD1	TD0

WATCHDOG REGISTER

TD1	TD0	WATCHDOG TIMEOUT
0	0	WATCHDOG DISABLED
0	1	250ms
1	0	500ms
1	1	1000ms

ANALOG-TO-DIGITAL CONVERTER

The DS1677 provides a 3-channel 8-bit analog-to-digital converter. The A/D reference voltage (2.55V typical) is derived from an on-chip band-gap circuit. Three multiplexed analog inputs are provided through the AIN0, AIN1, and AIN2 pins. The ADC is monotonic (no missing codes) and uses a successive approximation technique to convert the analog signal into a digital code.

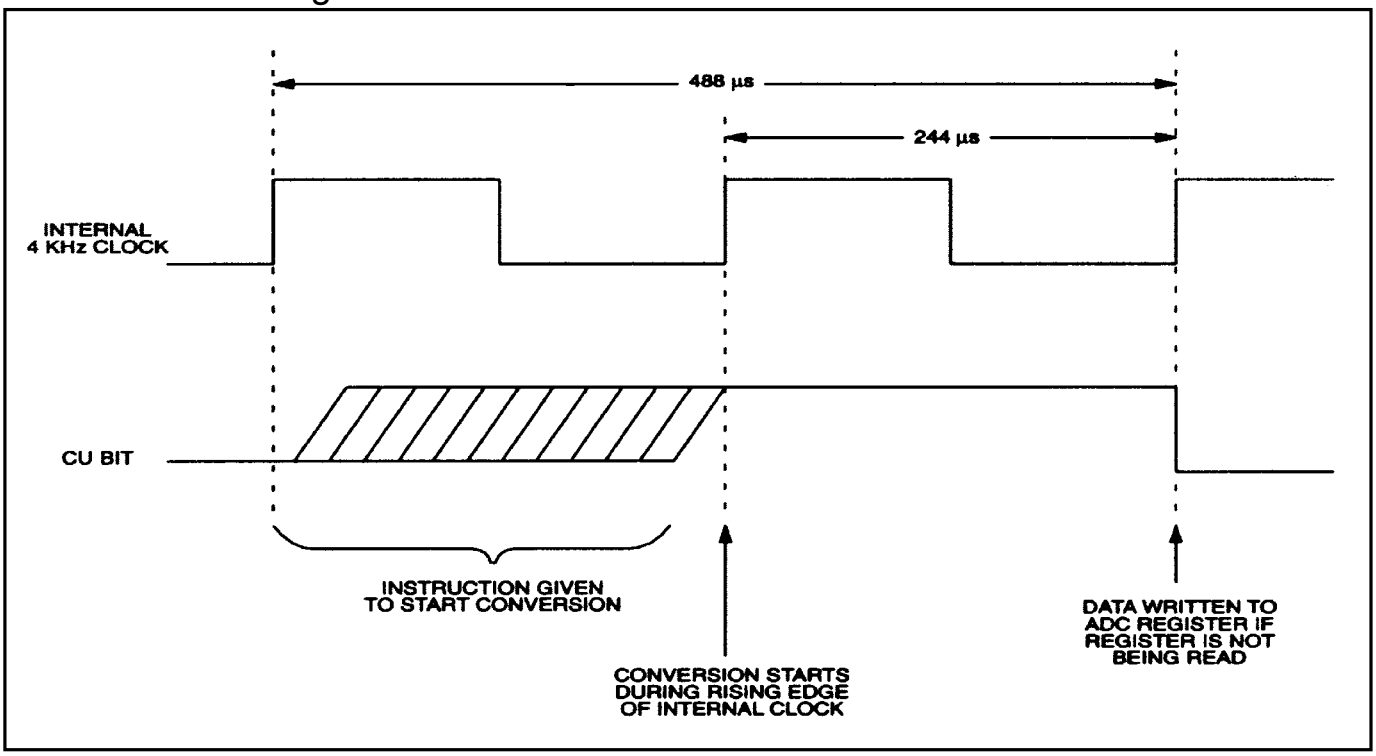
An A/D conversion is the process of assigning a digital code to an analog input voltage. This code represents the input value as a fraction of the full-scale voltage (FSV) range. Thus, the FSV range is then divided by the ADC into 256 codes (8 bits). The FSV range is bounded by an upper limit equal to the reference voltage and the lower limit, which is ground. The DS1677 has a FSV of 2.55V (typical) that provides a resolution of 10mV. An input voltage equal to the reference voltage converts to FFh while an input voltage equal to ground converts to 00h. The relative linearity of the ADC is ±0.5 LSB.

The ADC selects from one of three different analog inputs (AIN0–AIN2). The input that is selected is determined by the Analog Input Select (AIS) bits in the Control Register. Table 2 lists the specific analog input that is selected by these 2 bits. Note also that the converter can be turned off by these bits to reduce power. When the ADC is turned on by setting AIS0 and AIS1 to any value other than 0,0 the analog input voltage is converted and written to the ADC Register within 488µs. An internal analog filter at the input reduces high frequency noise. Subsequent updates occur approximately every 10ms. If AIS0 and/or AIS1 are changed, updates will occur at the next 10ms conversion time.

The Conversion Update In Progress (CU) bit in the Status Register indicates when the ADC Register can be read. When this bit is a one, an update to the ADC Register will occur within 488µs maximum. However, when this bit is zero an update will not occur for at least 244µs. The CU bit should be polled before reading the ADC Register to insure that the contents are stable during a read cycle. Once a read cycle to the ADC Register has been started, the DS1677 will not update that register until the read cycle has been completed. It should also be mentioned that taking CS low will abort the read cycle and will allow the ADC Register to be updated.

Figure 5 illustrates the timing of the CU bit relative to an instruction to begin conversion and the completion of that conversion.

CU BIT TIMING Figure 5



3-WIRE SERIAL INTERFACE

Communication with the DS1677 is accomplished through a simple 3-wire interface consisting of the Chip Select (CS), Serial Clock (SCLK) and Input/Output (I/O) pins.

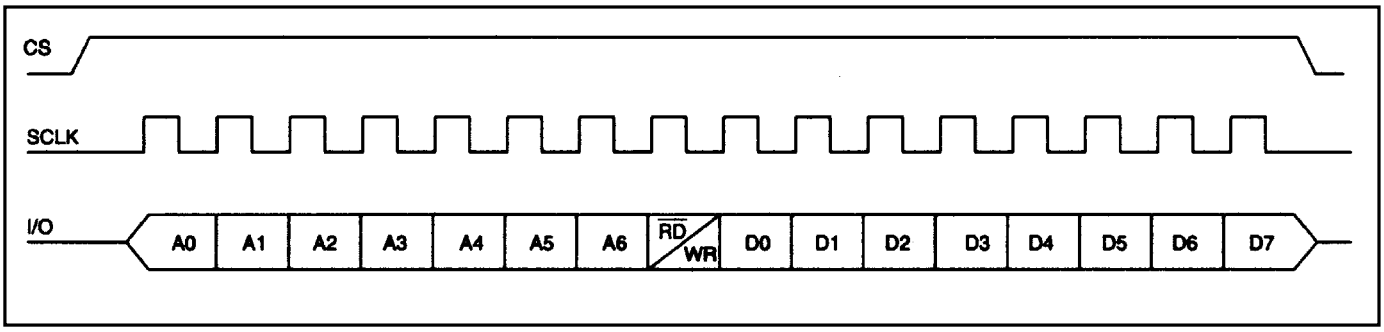
All data transfers are initiated by driving the CS input high. The CS input serves two functions. First, CS turns on the control logic, which allows access to the shift register for the address/command sequence. Second, the CS signal provides a method of terminating either single byte or multiple byte (burst) data transfer. A clock cycle is a sequence of a rising edge followed by a falling edge. For data input, data must be valid during the rising edge of the clock and data bits are output on the falling edge of the clock. If the CS input goes low, all data transfer terminates and the I/O pin goes to a high impedance state.

Address and data bytes are always shifted LSB first into the I/O pin. Any transaction requires the address/command byte to specify a read or write to a specific register followed by one or more bytes of data. The address byte is always the first byte entered after CS is driven high. The most significant bit ($\overline{RD}$/WR) of this byte determines if a read or write will take place. If this bit is 0, one or more read cycles will occur. If this bit is 1, one or more write cycles will occur.

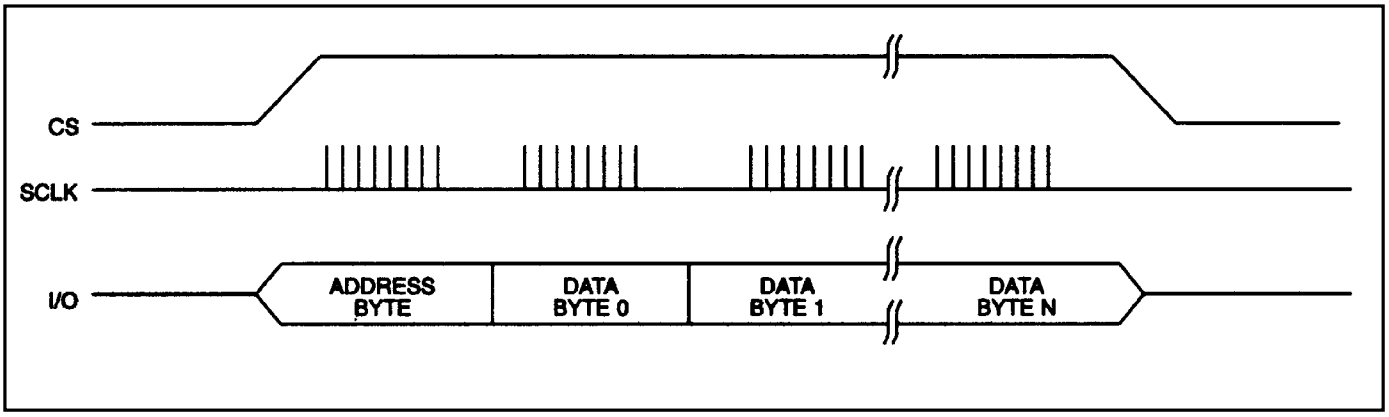
Data transfers can occur one byte at a time or in multiple byte burst mode. After CS is driven high an address is written to the DS1677. After the address, one or more data bytes can be read or written. For a single byte transfer one byte is read or written and then CS is driven low. For a multiple byte transfer, multiple bytes can be read or written to the DS1677 after the address has been written. Each read or write cycle causes the register address to automatically increment. Incrementing continues until the device is disabled. After accessing register 0Eh, the address wraps to 00h.

Data transfer for single byte transfer and multiple byte burst transfer is illustrated in Figures 6 and 7.

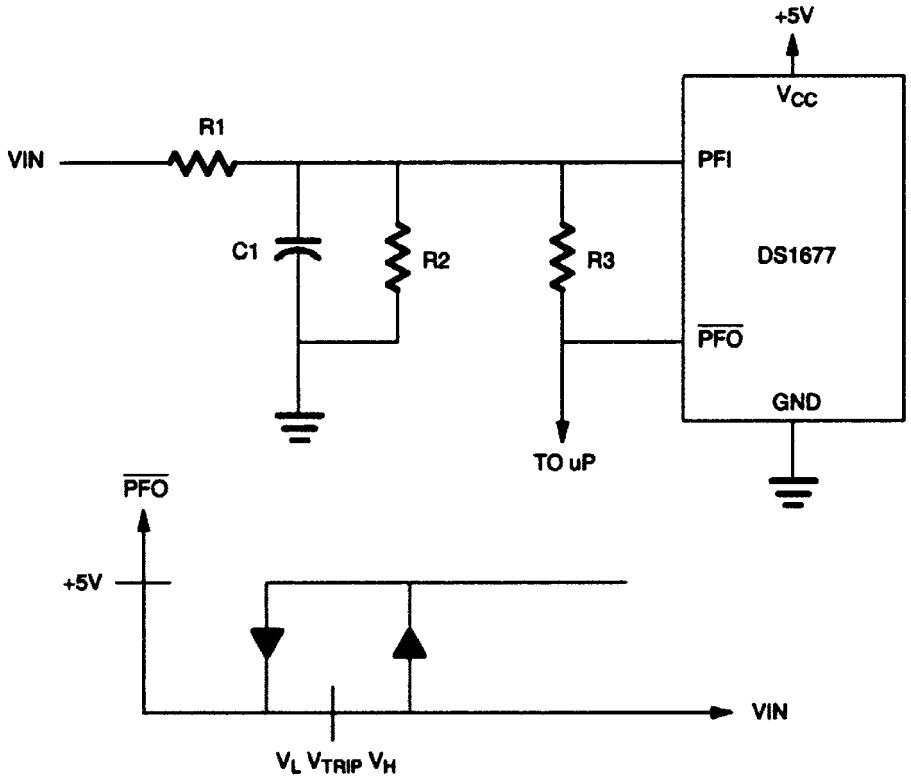
SINGLE BYTE DATA TRANSFER Figure 6



MULTIPLE BYTE BURST TRANSFER Figure 7



POWER-FAIL COMPARATOR Figure 8



$$V_{TRIP} = 1.25\left(\frac{R1 + R2}{R2}\right) \qquad V_H = 1.25/\left(\frac{R2 \| R3}{R1 + R2 \| R3}\right)$$

$$\frac{VL - 1.25}{R1} + \frac{5 - 1.25}{R3} = \frac{1.25}{R2}$$

ABSOLUTE MAXIMUM RATINGS

Voltage Range on Any Pin Relative to Ground……..-0.3V to +7.0V
Operating Temperature Range……..0°C to +70°C
Storage Temperature Range……-55°C to +125°C
Soldering Temperature…….See IPC/JEDEC J-STD-020 Specification

This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect device reliability.

RECOMMENDED DC OPERATING CONDITIONS (T_A = 0°C to +70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Power Supply Voltage	V_{CC}	4.5	5.0	5.5	V	1
Input Logic 1	V_{IH}	2.0		V_{CC} + 0.3	V	1
Input Logic 0	V_{IL}	-0.3		+0.8	V	1
Battery Voltage	V_{BAT}	2.5		3.7	V	1

DC ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0V ±10%, T_A = 0°C to +70°C.)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Leakage	I_{LI}	-1		+1	µA	
CS Leakage	I_{LO}			150	µA	7
Logic 1 Output (I_{OUT} = -0.4mA)	V_{OH}	2.4			V	1
Logic 0 Output (I_{OUT} = 1.5mA)	V_{OL}			0.4	V	1
Active Supply Current (CS = V_{CC} - 0.2)	I_{CCA}		1.5	2.0	mA	2
ADC Current	I_{ADC}			500	µA	3
Standby Current (CS = V_{IL})	I_{CCS}			300	µA	4
Battery Current (Oscillator On)	I_{BAT}		300	500	nA	
Battery Current (Oscillator Off)	I_{BAT}			200	nA	
Internal $\overline{RST}$ Pullup Resistor	R_P	35	47	60	kΩ	
V_{CC} Trip Point	V_{CCTP}	4.25	4.35	4.50	V	
V_{CC} Switchover	V_{CCSW}	2.60	2.70	2.80	V	10
A/D Reference Voltage	V_{ADC}	2.47	2.55	2.63	V	
Pushbutton Detect	PB_{DV}	0.8		2.0	V	
Pushbutton Release	PB_{RD}		0.3	0.8	V	
Output Voltage	V_{CCO}	V_{CC} - 0.3			V	9
PFI Input Threshold	V_{PFI}	1.20	1.25	1.30	V	
PFI Input Current	I_{PFI}	0.25	0.01	25	nA	
$\overline{PFO}$ Output Voltage (I_{OH} = -1µA)	V_{OH}	V_{CC} - 1.5			V	
$\overline{PFO}$ Output voltage (I_{OL} = 3.2µA)	V_{OL}			0.4	V	
V_{CCO} Output Current (Source = V_{CC})	I_{CCO1}			150	mA	11
V_{CCO} Output Current (Source = V_{BAT})	I_{CCO2}			150	µA	12

CAPACITANCE

(T_A = +25°C)

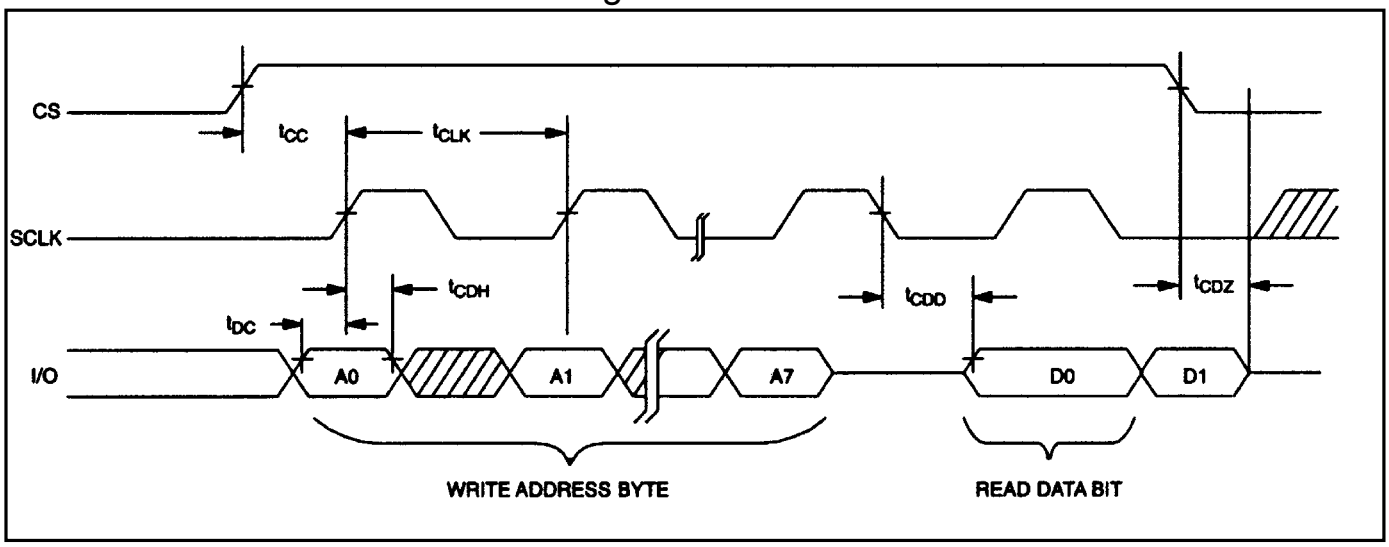
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C_I		10		pF	
I/O Capacitance	$C_{I/O}$		15		pF	
Crystal Capacitance	C_X		6		pF	

AC ELECTRICAL CHARACTERISTICS

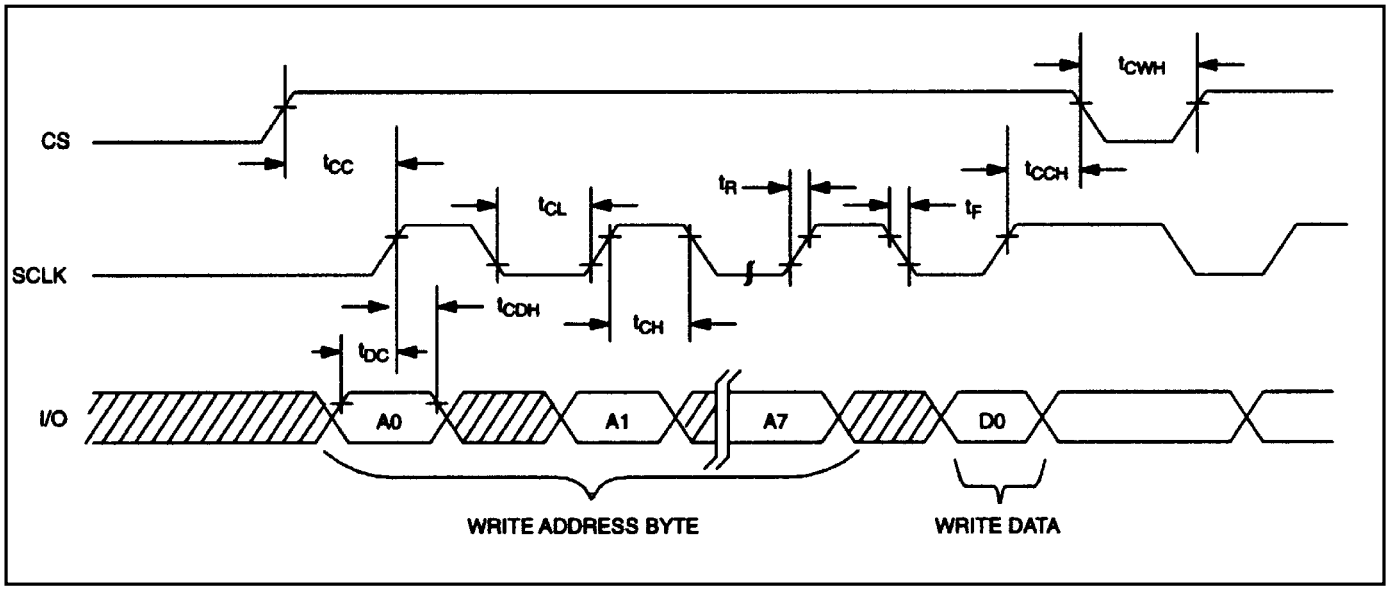
(0°C to 70°C; V_{CC}=5.0V±10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Data to Clock Setup	t_{DC}	50			ns	6
CLK to Data Hold	t_{CDH}	70			ns	6
CLK to Data Delay	t_{CDD}			200	ns	6,7,8
CLK to Low Time	t_{CL}	250			ns	6
CLK to High Time	t_{CH}	250			ns	6
CLK Frequency	t_{CLK}			2.0	MHz	6
CLK Rise and Fall	t_R, t_F			500	ns	
CS to CLK Setup	t_{CC}	1			µs	6
CLK to CS Hold	t_{CCH}	60			ns	6
CS Inactive Time	t_{CWH}	1			µs	6
CS to I/O High-Z	t_{CDZ}			70	ns	6
V_{CC} Slew Rate (4.5V to 2.3V)	t_F	1			ms	
V_{CC} Slew Rate (2.3V to 4.5V)	t_R	0			ns	
V_{CC} Detect to $\overline{RST}$ (V_{CC} Falling)	t_{RPD}			100	ns	
Reset Active Time	t_{RST}		250		ms	13
Pushbutton Debounce	PB_{DB}		250		ms	13
V_{CC} Detect to $\overline{RST}$ (V_{CC} Rising)	t_{RPU}		250		ms	13, 14
$\overline{ST}$ Pulse Width	t_{ST}	20			ns	
Chip Enable Propagation Delay to External SRAM	t_{CED}		8	15	ns	
Nominal Voltage to V_{CC} Switchover Fall Time	t_{FB}	200			µs	
PFI Low to $\overline{PFO}$ Low	t_{PFD}		2		µs	
PFI High to $\overline{PFO}$ High	t_{PFU}		2		µs	

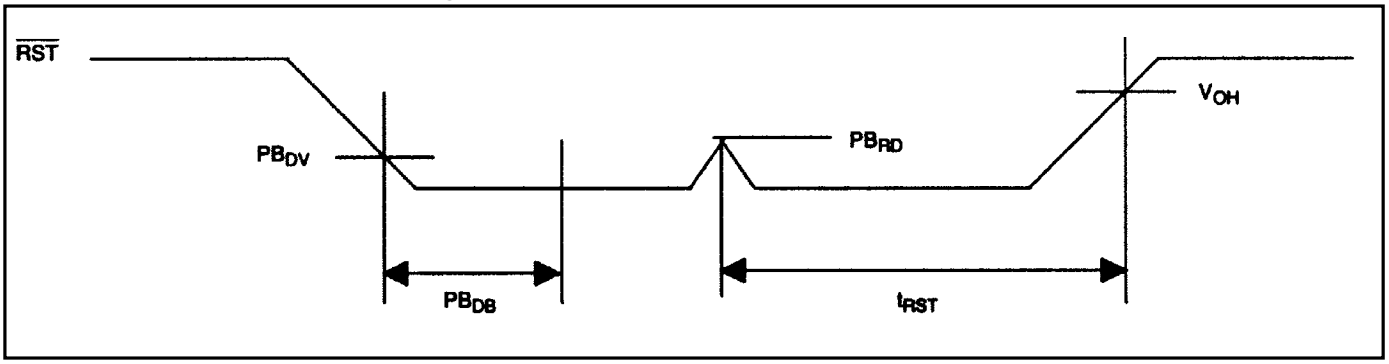
TIMING DIAGRAM: READ DATA Figure 9



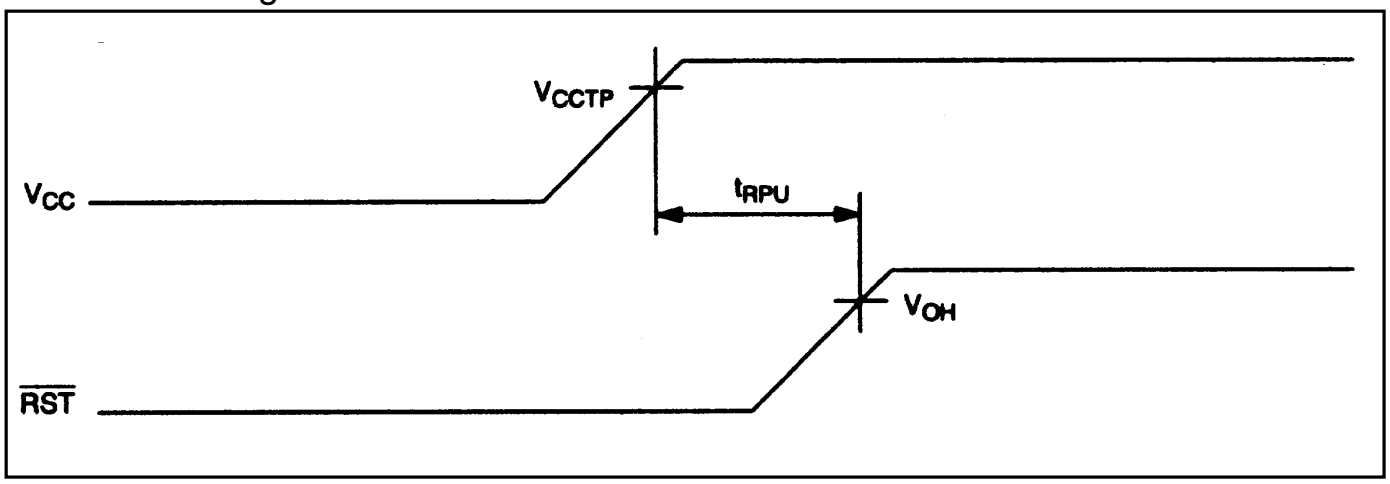
TIMING DIAGRAM: WRITE DATA Figure 10



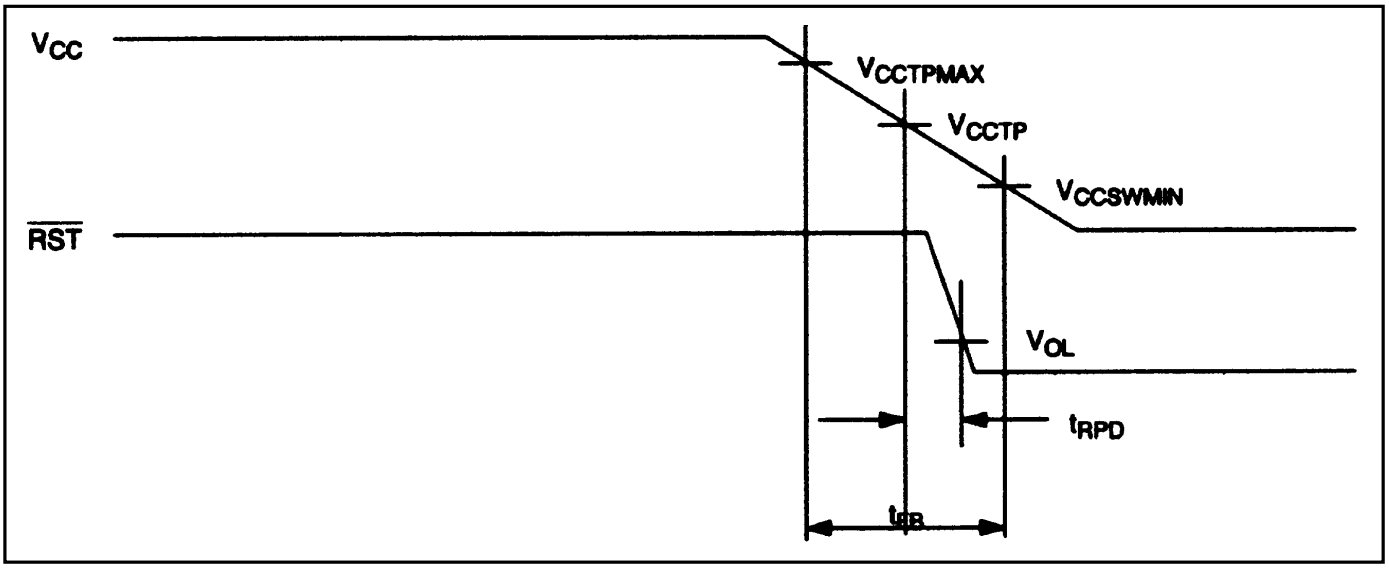
PUSHBUTTON RESET Figure 11



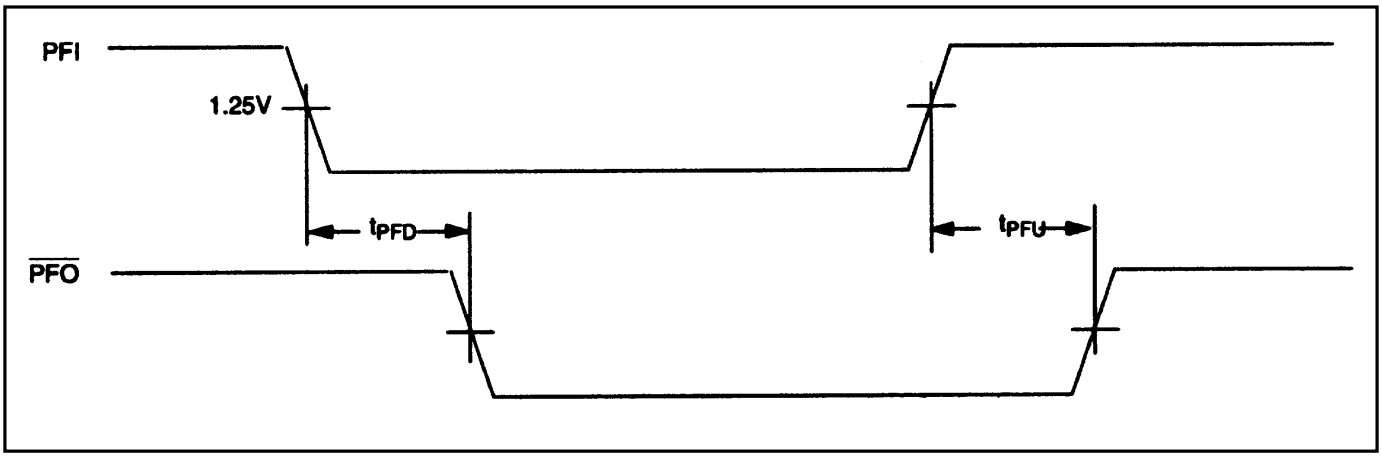
POWER-UP Figure 12



POWER-DOWN Figure 13



POWER-FAIL WARNING Figure 14

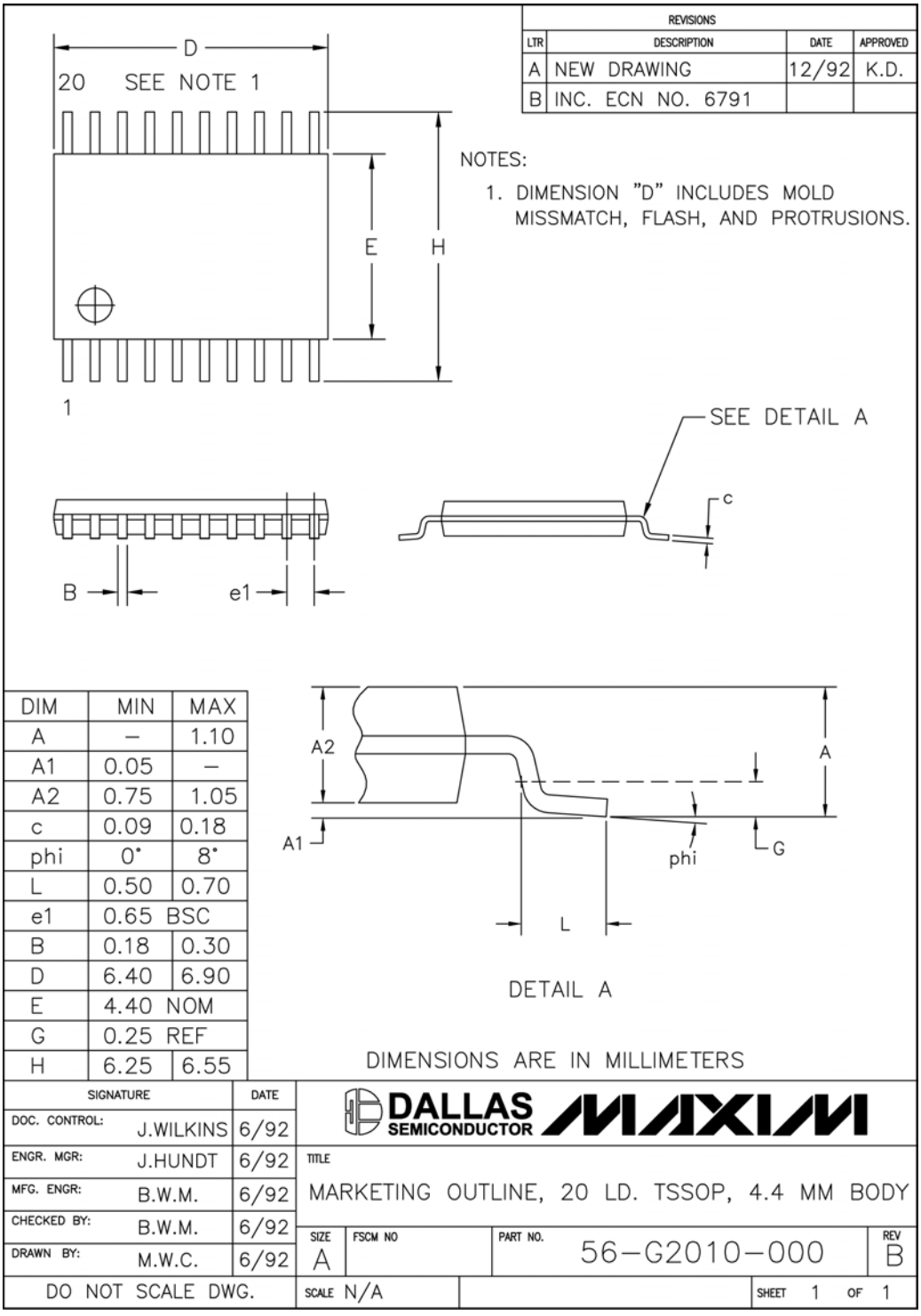


NOTES:

1. All voltages are referenced to ground.
2. I_{CCA} is specified with outputs open, CS set to a logic 1, SCLK = 500kHz, oscillator enabled, and ADC enabled.
3. I_{ADC} is specified with CS, V_{CCO} open and I/O, SCLK at logic 0. ADC is enabled.
4. I_{CCS} is specified with CS, V_{CCO} open and I/O, SCLK at logic 0. ADC is disabled.
5. CS has a 40kΩ pulldown resistor to ground.
6. Measured at V_{IH} = 2.0V or V_{IL} = 0.8V and 10ns maximum rise and fall time.
7. Measured at V_{OH} = 2.4V or V_{OL} = 0.4V.
8. Load capacitance = 25pF.
9. I_{CCO} = 100mA, $V_{CC} > V_{CCTP}$.
10. V_{CCO} switchover from V_{CC} to V_{BAT} occurs when V_{CC} drops below the lower of V_{CCSW} and V_{BAT}.
11. Current from V_{CC} input pin to V_{CCO} output pin.
12. Current from V_{BAT} input pin to V_{CCO} output pin.
13. Time base is generated by very accurate crystal oscillator. Accuracy of this time period is based on the crystal that is used. A typical crystal with a specified load capacitance of 6pF will provide an accuracy within ±100ppm over the 0°C to +70°C temperature range. For greater accuracy, refer to the DS32kHz data sheet.
14. If the $\overline{EOSC}$ bit in the Control Register is set to a logic 1, t_{RPU} is equal to 250ms plus the startup time of the crystal oscillator.

PACKAGE INFORMATION

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/DallasPackInfo**.)



DIM	MIN	MAX
A	–	1.10
A1	0.05	–
A2	0.75	1.05
c	0.09	0.18
phi	0°	8°
L	0.50	0.70
e1	0.65 BSC	
B	0.18	0.30
D	6.40	6.90
E	4.40 NOM	
G	0.25 REF	
H	6.25	6.55

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