



512K x 8 Static RAM

Features

- **Voltage Range**
 - 4.5V–5.5V
- **Low active power**
 - Typical active current: 2.5 mA @ $f = 1$ MHz
 - Typical active current: 12.5 mA @ $f = f_{\max}$
- **Low standby current**
- **Automatic power-down when deselected**
- **TTL-compatible inputs and outputs**
- **Easy memory expansion with CE and OE features**
- **CMOS for optimum speed/power**

Functional Description

The WCMA4008C1X is a high-performance CMOS static RAM organized as 512K words by 8 bits. Easy memory expansion is provided by an active LOW Chip Enable ($\overline{CE}$), an active

LOW Output Enable ($\overline{OE}$), and three-state drivers. This device has an automatic power-down feature that reduces power consumption by more than 99% when deselected.

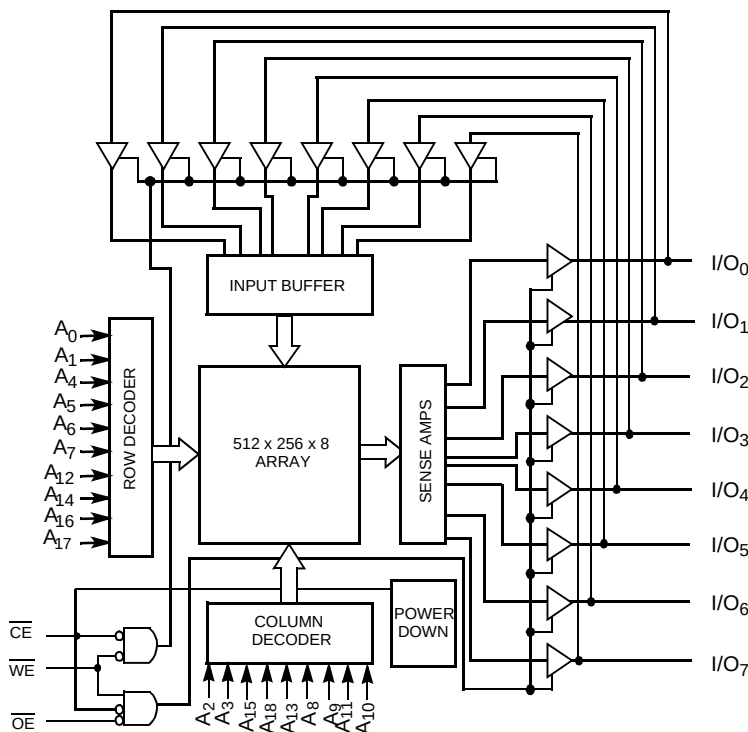
Writing to the device is accomplished by taking Chip Enable ($\overline{CE}$) and Write Enable ($\overline{WE}$) inputs LOW. Data on the eight I/O pins (I/O_0 through I/O_7) is then written into the location specified on the address pins (A_0 through A_{18}).

Reading from the device is accomplished by taking Chip Enable ($\overline{CE}$) and Output Enable ($\overline{OE}$) LOW while forcing Write Enable ($\overline{WE}$) HIGH for read. Under these conditions, the contents of the memory location specified by the address pins will appear on the I/O pins.

The eight input/output pins (I/O_0 through I/O_7) are placed in a high-impedance state when the device is deselected ($\overline{CE}$ HIGH), the outputs are disabled ($\overline{OE}$ HIGH), or during a write operation ($\overline{CE}$ LOW, and $\overline{WE}$ LOW).

The WCMA4008C1X is available in a standard 32-pin 450-mil-wide body width SOIC.

Logic Block Diagram



Pin Configuration

Top View SOIC			
A_{17}	1	32	V_{CC}
A_{16}	2	31	A_{15}
A_{14}	3	30	A_{18}
A_{12}	4	29	$\overline{WE}$
A_7	5	28	A_{13}
A_6	6	27	A_8
A_5	7	26	A_9
A_4	8	25	A_{11}
A_3	9	24	$\overline{OE}$
A_2	10	23	A_{10}
A_1	11	22	$\overline{CE}$
A_0	12	21	I/O_7
I/O_0	13	20	I/O_6
I/O_1	14	19	I/O_5
I/O_2	15	18	I/O_4
GND	16	17	I/O_3

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature -65°C to +150°C

Ambient Temperature with
Power Applied -55°C to +125°C

Supply Voltage on V_{CC} to Relative GND -0.5V to +7.0V

DC Voltage Applied to Outputs
in High Z State^[1] -0.5V to $V_{CC} + 0.5V$

DC Input Voltage^[1] -0.5V to $V_{CC} + 0.5V$

Current into Outputs (LOW) 20 mA

Static Discharge Voltage 2001V
(per MIL-STD-883, Method 3015)

Latch-Up Current >200 mA

Product Portfolio

Product	V_{CC} Range			Speed	Temp.	Power Dissipation			
						Operating, I_{CC}		Standby (I_{SB2})	
						$f = f_{max}$		Typ. ^[2]	Max.
	Min.	Typ.	Max.			Typ. ^[3]	Max.		
WCMA4008C1X	4.5 V	5.0V	5.5V	70 ns	Ind'l	12.5 mA	20 mA	4 μ A	20 μ A

Operating Range

Range	Ambient Temperature	V_{CC}
Industrial	-40°C to +85°C	4.5V–5.5V

Notes:

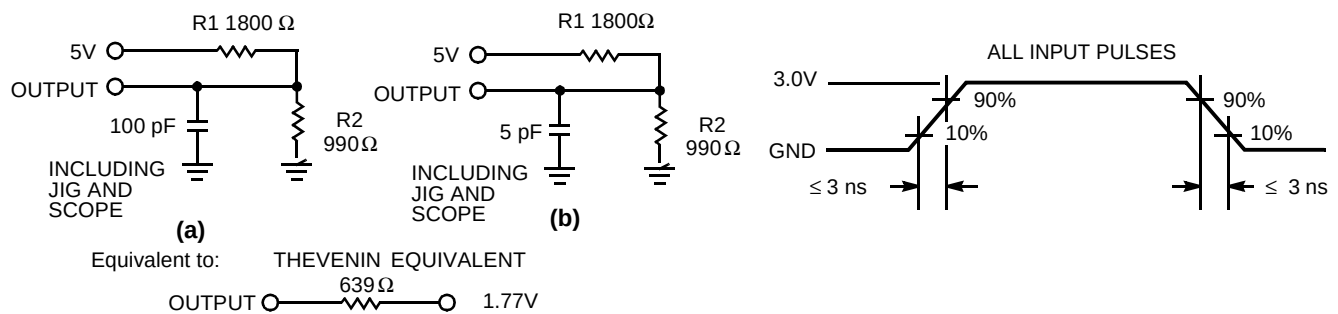
- V_{IL} (min.) = -2.0V for pulse durations of less than 20 ns.
- Typical values are measured at $V_{CC} = 5V$, $T_A = 25^\circ C$, and are included for reference only and are not tested or guaranteed.

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions	WCMA4008C1X			Unit
			Min.	Typ. ^[2]	Max.	
V_{OH}	Output HIGH Voltage	$V_{CC} = \text{Min.}, I_{OH} = -1 \text{ mA}$	2.4			V
V_{OL}	Output LOW Voltage	$V_{CC} = \text{Min.}, I_{OL} = 2.1 \text{ mA}$			0.4	V
V_{IH}	Input HIGH Voltage		2.2		$V_{CC} + 0.3$	V
V_{IL}	Input LOW Voltage		-0.3		0.8	V
I_{IX}	Input Leakage Current	$GND \leq V_I \leq V_{CC}$	-1		+1	μA
I_{OZ}	Output Leakage Current	$GND \leq V_I \leq V_{CC}$, Output Disabled	-1		+1	μA
I_{CC}	V_{CC} Operating Supply Current	$f = f_{MAX} = 1/t_{RC}$		12.5	20	mA
		$f = 1 \text{ MHz}$		2.5		mA
I_{SB1}	Automatic CE Power-Down Current —TTL Inputs	Max. $V_{CC}, \overline{CE} \geq V_{IH}$ $V_{IN} \geq V_{IH}$ or $V_{IN} \leq V_{IL}$, $f = f_{MAX}$			1.5	mA
I_{SB2}	Automatic CE Power-Down Current —CMOS Inputs	Max. $V_{CC}, \overline{CE} \geq V_{CC} - 0.3V$, $V_{IN} \geq V_{CC} - 0.3V$, or $V_{IN} \leq 0.3V$, $f = 0$		4	20	μA

Capacitance^[3]

Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	$T_A = 25^\circ\text{C}$, $f = 1 \text{ MHz}$, $V_{CC} = 5.0V$	6	pF
C_{OUT}	Output Capacitance		8	pF

AC Test Loads and Waveforms

Note:

- Tested initially and after any design or process changes that may affect these parameters.

Switching Characteristics^[4] Over the Operating Range

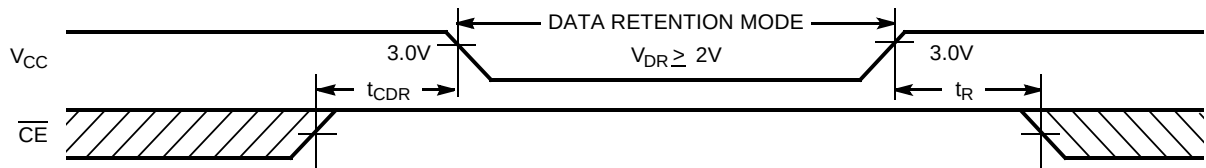
Parameter	Description	WCMA4008C1X		Unit
		Min.	Max.	
READ CYCLE				
t _{RC}	Read Cycle Time	70		ns
t _{AA}	Address to Data Valid		70	ns
t _{OHA}	Data Hold from Address Change	10		ns
t _{ACE}	$\overline{CE}$ LOW to Data Valid		70	ns
t _{DOE}	$\overline{OE}$ LOW to Data Valid		35	ns
t _{LZOE}	$\overline{OE}$ LOW to Low Z ^[5]	5		ns
t _{HZOE}	$\overline{OE}$ HIGH to High Z ^[5, 6]		25	ns
t _{LZCE}	$\overline{CE}$ LOW to Low Z ^[5]	10		ns
t _{HZCE}	$\overline{CE}$ HIGH to High Z ^[5, 6]		25	ns
t _{PU}	$\overline{CE}$ LOW to Power-Up	0		ns
t _{PD}	$\overline{CE}$ HIGH to Power-Down		70	ns
WRITE CYCLE ^[7]				
t _{WC}	Write Cycle Time	70		ns
t _{SCE}	$\overline{CE}$ LOW to Write End	60		ns
t _{AW}	Address Set-Up to Write End	60		ns
t _{HA}	Address Hold from Write End	0		ns
t _{SA}	Address Set-Up to Write Start	0		ns
t _{PWE}	$\overline{WE}$ Pulse Width	55		ns
t _{SD}	Data Set-Up to Write End	30		ns
t _{HD}	Data Hold from Write End	0		ns
t _{LZWE}	$\overline{WE}$ HIGH to Low Z ^[5]	5		ns
t _{HZWE}	$\overline{WE}$ LOW to High Z ^[5, 6]		25	ns

Notes:

- Test conditions assume signal transition time of 5 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I_{OL}/I_{OH} and 100-pF load capacitance.
- At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE} , t_{HZOE} is less than t_{LZOE} , and t_{HZWE} is less than t_{LZWE} for any given device.
- t_{HZOE} , t_{HZCE} , and t_{HZWE} are specified with a load capacitance of 5 pF as in part (b) of AC Test Loads. Transition is measured ± 500 mV from steady-state voltage.
- The internal write time of the memory is defined by the overlap of $\overline{CE}$ LOW, and $\overline{WE}$ LOW. $\overline{CE}$ and $\overline{WE}$ must be LOW to initiate a write, and the transition of any of these signals can terminate the write. The input data set-up and hold timing should be referenced to the leading edge of the signal that terminates the write.

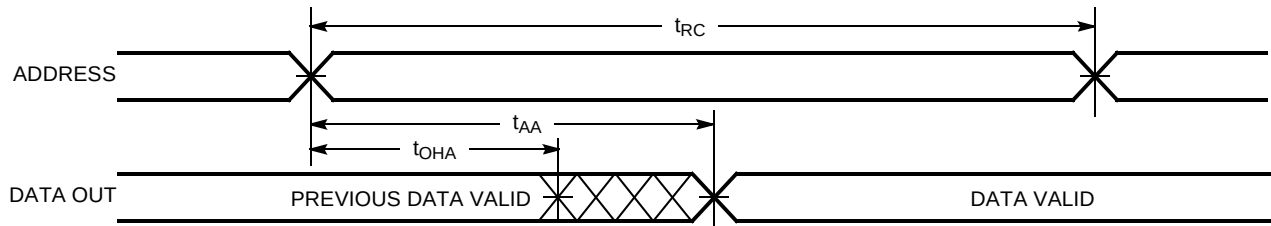
Data Retention Characteristics (Over the Operating Range)

Parameter	Description	Conditions	Min.	Typ. ^[2]	Max.	Unit
V_{DR}	V_{CC} for Data Retention		2.0			V
I_{CCDR}	Data Retention Current	No input may exceed $V_{CC} + 0.3V$ $V_{CC} = V_{DR} = 3.0V$ $CE > V_{CC} - 0.3V$ $V_{IN} > V_{CC} - 0.3V$ or $V_{IN} < 0.3V$			20	μA
$t_{CDR}^{[3]}$	Chip Deselect to Data Retention Time		0			ns
$t_R^{[8]}$	Operation Recovery Time		t_{RC}			ns

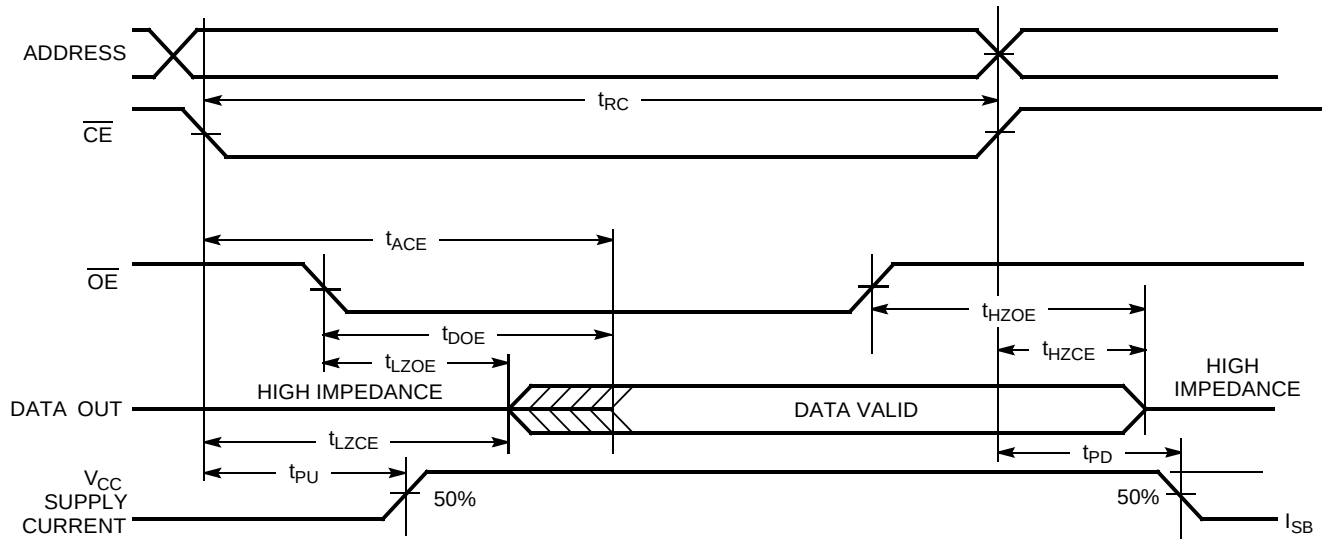
Data Retention Waveform


Switching Waveforms

Read Cycle No.1^[9, 10]

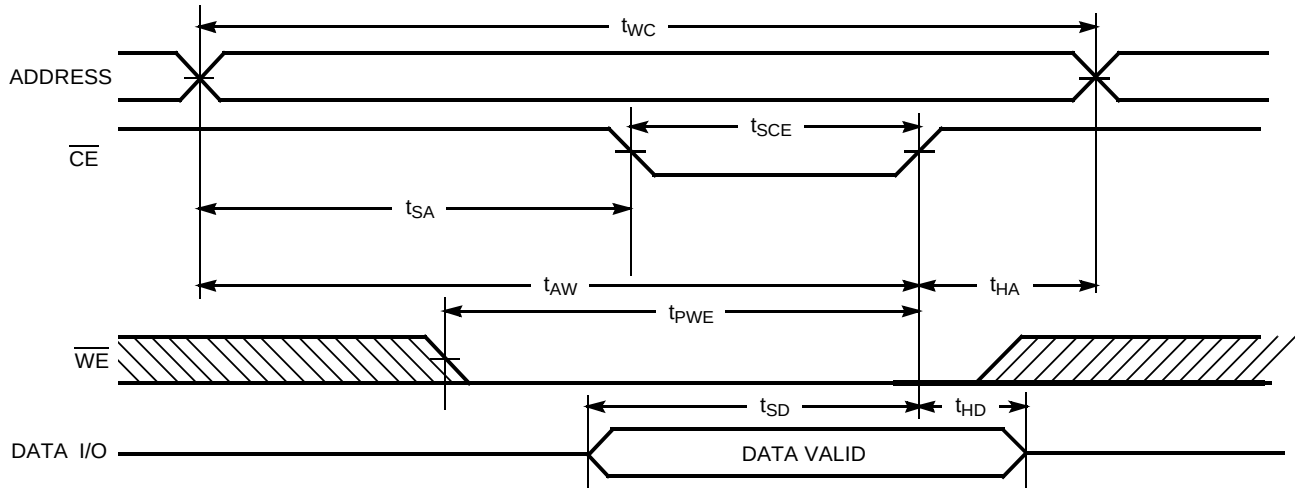
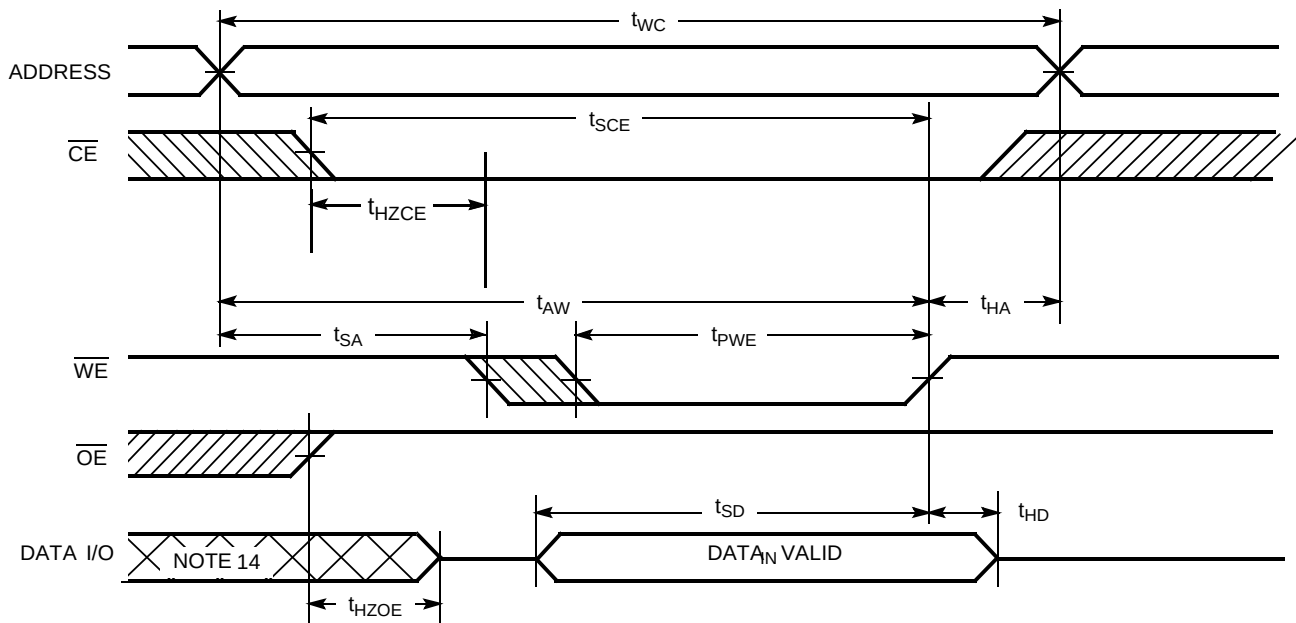


Read Cycle No. 2 ($\overline{OE}$ Controlled)^[10, 11]

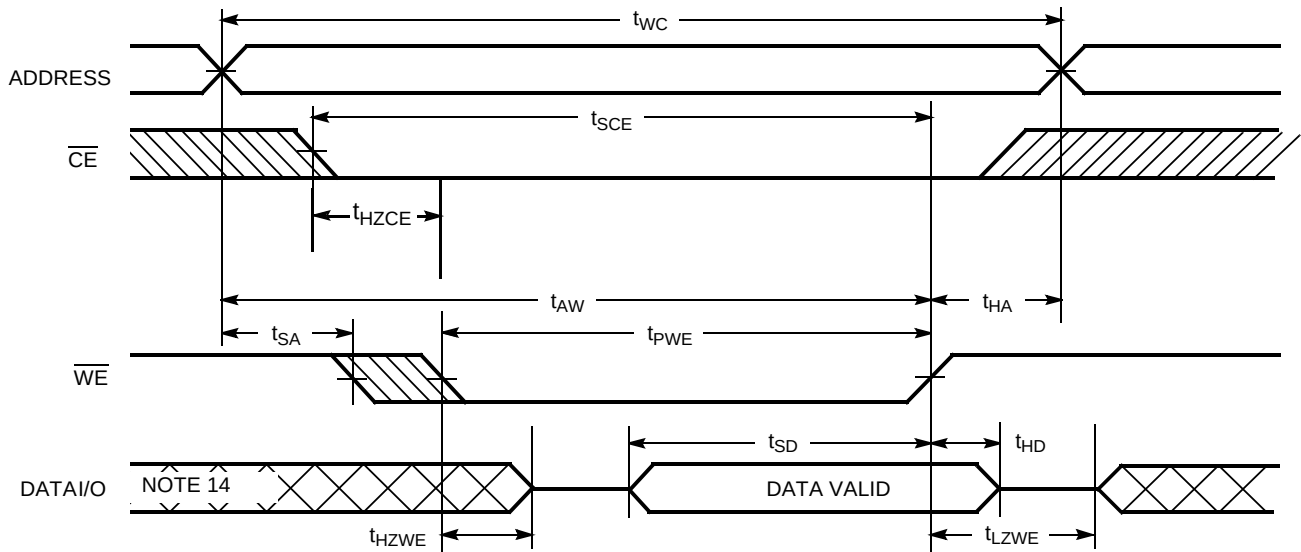


Notes:

8. Full Device operation requires linear V_{CC} ramp from V_{DR} to $V_{CC(min)} \geq 100 \mu s$ or stable at $V_{CC(min)} \geq 100 \mu s$.
9. Device is continuously selected. $\overline{OE}$, $\overline{CE} = V_{IL}$.
10. $\overline{WE}$ is HIGH for read cycle.
11. Address valid prior to or coincident with $\overline{CE}$ transition LOW.

Switching Waveforms (continued)
Write Cycle No. 1 ($\overline{\text{CE}}$ Controlled)^[12]

Write Cycle No. 2 ($\overline{\text{WE}}$ Controlled, $\overline{\text{OE}}$ HIGH During Write)^[12, 13]

Notes:

12. If $\overline{\text{CE}}$ goes HIGH simultaneously with $\overline{\text{WE}}$ going HIGH, the output remains in a high-impedance state.
13. Data I/O is high-impedance if $\overline{\text{OE}} = V_{IH}$.
14. During this period the I/Os are in the output state and input signals should not be applied.

Switching Waveforms (continued)
Write Cycle No.3 ($\overline{WE}$ Controlled, $\overline{OE}$ LOW)^[12, 13]

Truth Table

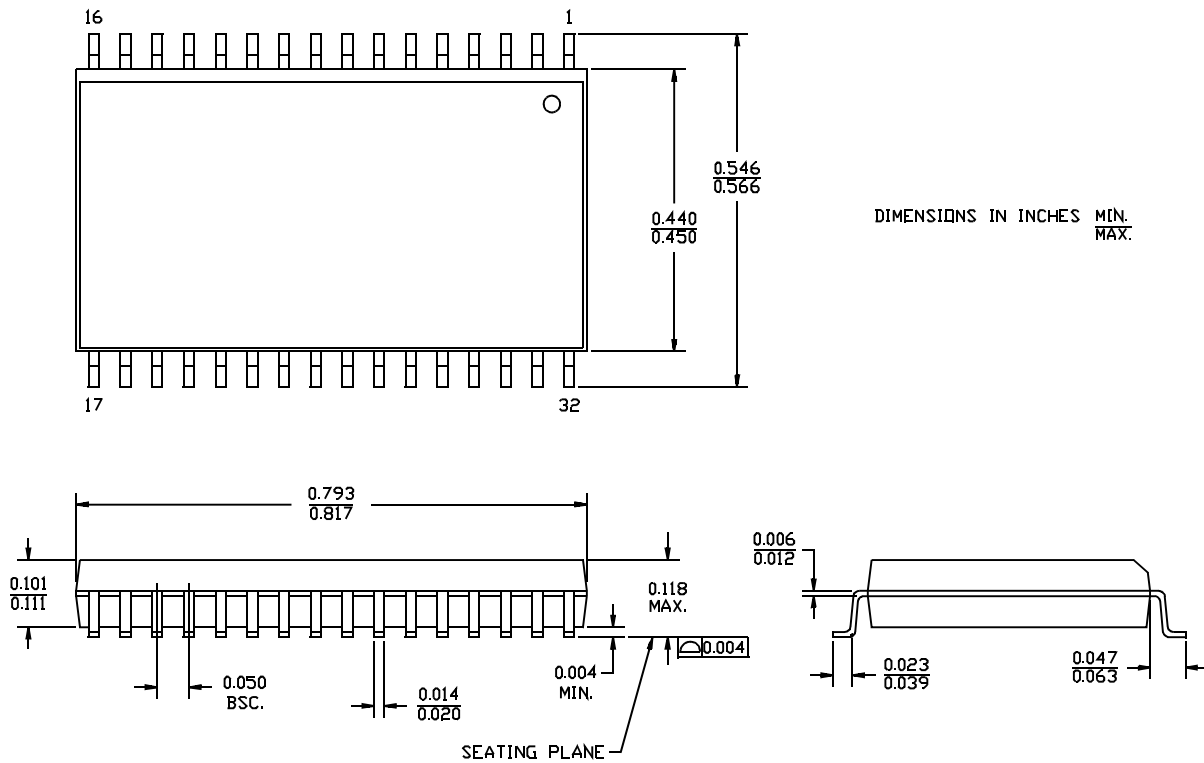
$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	I/O ₀ – I/O ₇	Mode	Power
H	X	X	High Z	Power-Down	Standby (I_{SB})
L	L	H	Data Out	Read	Active (I_{CC})
L	X	L	Data In	Write	Active (I_{CC})
L	H	H	High Z	Selected, Outputs Disabled	Active (I_{CC})

Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
70	WCMA4008C1X-GF70	G32	32-Lead (450-Mil) Molded SOIC	Industrial

Package Diagrams

32-Lead (450 MIL) Molded SOIC, G32



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